LUPA1300-2: High Speed CMOS Image Sensor

NOIL2SM1300A

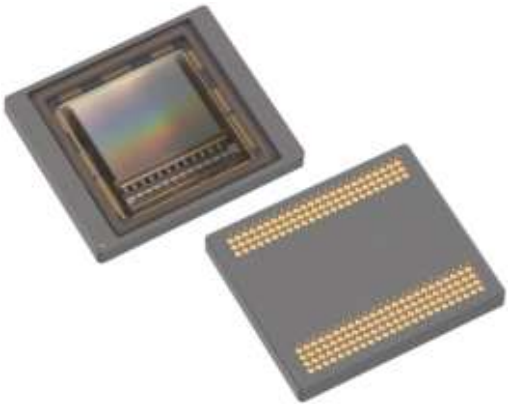


Figure 1. LUPA1300−2 Die Photo

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 2.

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Description

The LUPA1300-2 is an integrated SXGA high speed, high sensitivity CMOS image sensor. This sensor targets high speed machine vision and industrial monitoring applications. The LUPA1300-2 sensor runs at 500 fps and has triggered and pipelined shutter modes. It packs 24 parallel 10-bit A/D converters with an aggregate conversion rate of 740 MSPS. On-chip digital column FPN correction enables the sensor to output ready to use image data for most applications. To enable simple and reliable system integration, the 12 channels, 1 sync channel, 8 Gbps, and LVDS serial link protocol supports skew correction and serial link integrity monitoring.

The peak responsivity of the 14 µm x 14 µm 6T pixel is 63 DN/nJ/cm^2. Dynamic range is measured at 57 dB. In full frame video mode, the sensor consumes 1350 mW from the 2.5 V and 3.3 V power supplies. The sensors integrate A/D conversion, on-chip timing for a wide range of operating modes, and has an LVDS interface for easy system integration.

By removing the visually disturbing column patterned noise, this sensor enables building a camera without any offline correction or the need for memory. In addition, the on-chip column FPN correction is more reliable than an offline correction, because it compensates for supply and temperature variations. The sensor requires one master clock for operations up to 500 fps.

The LUPA1300-2 is housed in a 168 pin µPGA package and is available in a monochrome version and Bayer (RGB) patterned color filter array. The monochrome version is also available without glass. Contact your local **onsemi** office.

Features

- 1280 x 1024 Active Pixels
- 14 µm X 14 µm Square Pixels
- 1.4” Optical Format
- Monochrome or Color Digital Output
- 500 fps Frame Rate
- On-Chip 10-Bit ADCs
- 12 LVDS Serial Outputs
- Random Programmable ROI Readout
- Pipelined and Triggered Global Shutter
- On-Chip Column FPN Correction
- Serial Peripheral Interface (SPI)
- Limited Supplies: Nominal 2.5 V and 3.3 V
- −50 °C to +85 °C Operational Temperature Range
- 168-Pin µPGA Package
- Power Dissipation: 1350 mW
- These Devices are Pb-Free and are RoHS Compliant

Applications

- High Speed Machine Vision
- Motion Analysis
- Medical Imaging
- Intelligent Traffic System
- Industrial Imaging

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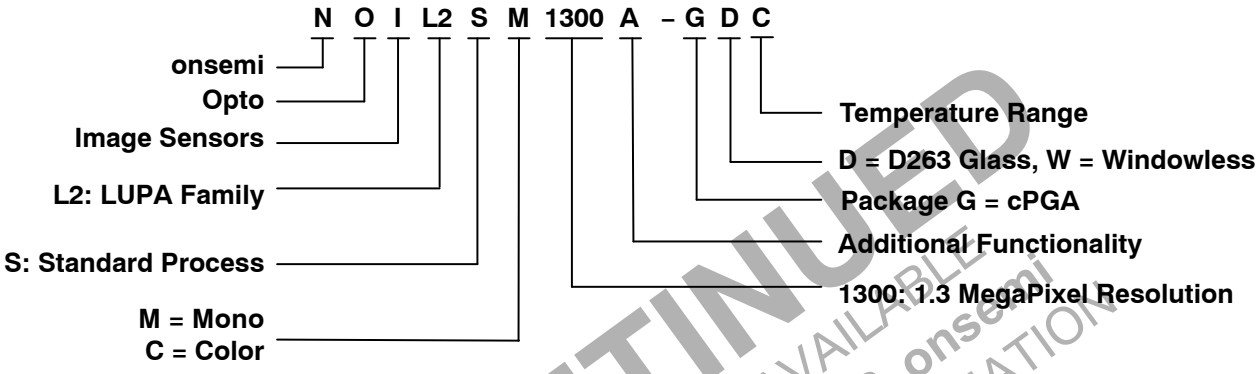
Marketing Part Number	Description	Package
NOIL2SM1300A-GDC	Mono with Glass	168 pin μPGA

DISCONTINUED (Note 1)

NOIL2SM1300A-GWC	Mono without Glass	168 pin μPGA
NOIL2SC1300A-GDC	Color with Glass	168 pin μPGA

1. **DISCONTINUED:** These devices are not available. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.

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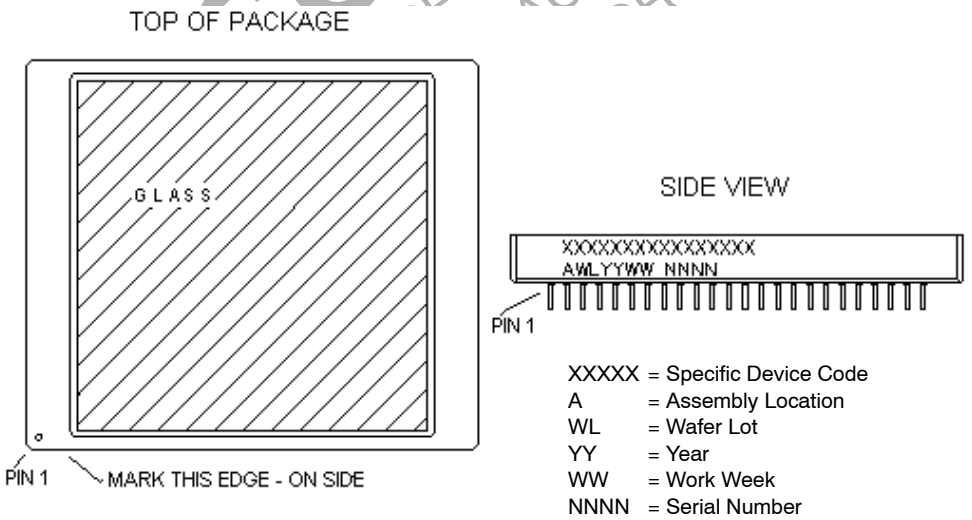


Figure 2. Marking Diagram

Line 1: NOIL2S**x**1300A-G**y**C where **x** denotes M = mono and C = color; **y** denotes D = D263 glass and W = windowless.
Line 2: **AWLYYWW** where AWL is PRODUCTION lot traceability, YYWW is the 4-digit date code

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SPECIFICATIONS

Key Specifications

Table 1. GENERAL SPECIFICATIONS

Parameter	Specifications
Active Pixels	1280 (H) x 1024 (V)
Pixel Size	14 μm x 14 μm
Pixel Type	6T pixel architecture
Pixel Rate	630 Mbps per channel (12 serial LVDS outputs)
Shutter Type	Pipelined and Triggered Global Shutter
Frame Rate	500 fps at 1.3 Mpixel (boosted by subsampling and windowing)
Master Clock	315 MHz for 500 fps
Windowing (ROI)	Randomly programmable ROI read out up to four multiple windows
Read Out	Windowed, flipped, mirrored, and subsampled readout possible
ADC Resolution	10-bit, on-chip
Extended Dynamic Range	Multiple slope (up to 90 dB optical dynamic range)

Table 2. ELECTRO-OPTICAL SPECIFICATIONS

Parameter	Value
Conversion Gain	0.0325 LSB10/e^-
Full Well Charge	30 ke^-
Responsivity	63 LSB10/nJ/cm^2 at 550 nm
Fill factor	40%
Parasitic Light Sensitivity	< 1/10,000
Dark Noise	1.2025 LSB10
QE x FF	35% at 550 nm
FPN	2% RMS of the output swing
PRNU	< 1% RMS of the output signal
Dark signal	162 LSB10/s, 5000 e^-/s
Power dissipation	1350 mW

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Absolute Maximum Ratings

Table 3. ABSOLUTE MAXIMUM RATINGS (Note 2)

Symbol	Description	Min	Max	Unit
ABS (2.5 V supply group)	ABS rating for 2.5 V supply group	−0.5	3.0	V
ABS (3.3 V supply group)	ABS rating for 3.3 V supply group	−0.5	4.3	V
ABS (3.5 V supply group)	ABS rating for 3.5 V supply group	−0.5	4.3	V
ESD (Note 4)	HBM	2000		V
	CDM	500		V
LU	Latchup	200		mA
T_S (Notes 5 and 6)	ABS Storage temperature range	−40	+150	°C
	ABS Storage humidity range at 85 °C		85	%RH

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING RATINGS

T_J (Notes 3 and 6)	Operating temperature range	−50	+85	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

2. Absolute maximum ratings are limits beyond which damage may occur.
3. Operating ratings are conditions at which operation of the device is intended to be functional.
4. **onsemi** recommends that our customers become familiar with, and follow the procedures in JEDEC Standard JESD625-A. Refer to Application Note AN52561. Long term exposure toward the maximum storage temperature will accelerate color filter degradation.
5. Caution needs to be taken to avoid dried stains on the underside of the glass due to condensation. The glass lid glue is permeable and can absorb moisture if the sensor is placed in a high % RH environment.
6. HTS – High Temperature Storage was successfully completed on LUPA 1300-2 color devices at +150 °C for 500 hours. Temperature Cycling was successfully completed from −40 °C to +125 °C up to 1000 cycles. No reliability stress has been performed at −50 °C.

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Electrical Specifications

Table 4. POWER SUPPLY RATINGS (Notes 1, 2 and 3)
Boldface limits apply for $T_J = T_{MIN}$ to T_{MAX}, all other limits T_J = +30 °C. Clock = 315 MHz

Symbol	Power Supply	Parameter	Condition	Min	Typ	Max	Unit
V_{ANA}, GND_{ANA}	Analog Supply	Operating Voltage		**-5%**	2.5	**+5%**	V
		Dynamic Current	Clock enabled, lux = 0		7	20	mA
		Peak Current	Clock enabled, lux = 0		16		mA
		Standby Current	Shutdown mode, lux = 0		1		mA
V_{DIG}, GND_{DIG}	Digital Supply	Operating Voltage		**-5%**	2.5	**+5%**	V
		Dynamic Current	Clock enabled, lux = 0		80	120	mA
		Peak Current	Clock enabled, lux = 0		130		
		Standby Current	Shutdown mode, lux = 0		52		mA
V_{PIX}, GND_{PIX}	Pixel Supply	Operating Voltage		**-5%**	2.5	**+5%**	V
		Dynamic Current	Clock enabled, lux = 0		6	50	mA
		Peak Current during FOT	Clock enabled, lux = 0, transient duration = 9 μs		1.4		A
		Peak Current during ROT	Clock enabled, lux = 0, transient duration = 2.5 μs		35		mA
		Standby Current	Shutdown mode, lux = 0		1		mA
V_{LVDS}, GND_{LVDS}	LVDS Supply	Operating Voltage		**-5%**	2.5	**+5%**	V
		Dynamic Current	Clock enabled, lux = 0		220	275	mA
		Peak Current	Clock enabled, lux = 0		280		mA
		Standby Current	Shutdown mode, lux = 0		100		mA
V_{ADC}, GND_{ADC}	ADC Supply	Operating Voltage		**-5%**	2.5	**+5%**	V
		Dynamic Current	Clock enabled, lux = 0		210	275	mA
		Peak Current	Clock enabled, lux = 0		260		mA
		Standby Current	Shutdown mode, lux = 0		3		mA
V_{BUF}, GND_{BUF}	Buffer Supply	Operating Voltage		**-5%**	2.5	**+5%**	V
		Dynamic Current	Clock enabled, lux = 0		30	50	mA
		Peak Current	Clock enabled, lux = 0		85		mA
		Standby Current	shutdown mode, lux = 0		0.1		mA
V_{SAMPLE}, GND_{SAMPLE}	Sampling Circuitry Supply	Operating Voltage		**-5%**	2.5	**+5%**	V
		Dynamic Current	Clock enabled, lux = 0		2		mA
		Peak Current	Clock enabled, lux = 0		42		mA
		Standby Current	Shutdown mode, lux = 0		1		mA
V_{RES}	Reset Supply	Operating Voltage		**-5%**	3.5	**+5%**	V
		Dynamic Current	Clock enabled, lux = 0		2	15	mA
		Peak Current	Clock enabled, lux = 0		65		mA
		Standby Current	Shutdown mode, lux = 0		2		mA

1. All parameters are characterized for DC conditions after thermal equilibrium is established.
2. The peak currents were measured without the load capacitor from the LDO (Low Dropout Regulator). The 100 nF capacitor bank was connected to the pin in question.
3. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is recommended that normal precautions be taken to avoid application of any voltages higher than the maximum rated voltages to this high-impedance circuit.
4. The VRES_AB and VPRECH power supply should be designed to have a sourcing and sinking current capability for frame rates of the order of 20k frames /sec.

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Table 4. POWER SUPPLY RATINGS (Notes 1, 2 and 3) (continued)
Boldface limits apply for $T_J = T_{MIN}$ to T_{MAX}, all other limits T_J = +30 °C. Clock = 315 MHz

Symbol	Power Supply	Parameter	Condition	Min	Typ	Max	Unit
V_{RES_AB} (Note 4)	Antiblooming Supply	Operating Voltage		**-10%**	0.7	**+10%**	V
		Dynamic Current	Clock enabled, lux = 0		1		mA
		Peak Current following edge reset	Clock enabled, lux = 0		50		mA
		Standby Current	Shutdown mode, lux = 0		1		mA
V_{RES_DS}	Reset Dual Slope Supply	Operating Voltage		**1.8**	2.5	**3.675**	V
		Dynamic Current	Clock enabled, lux = 0		0.4	3	mA
		Peak Current	Clock enabled, lux = 0		36		mA
V_{RES_TS}	Reset Triple Slope Supply	Operating Voltage		**1.8**	2.2	**3.675**	V
		Dynamic Current	Clock enabled, lux = 0		0.3	2	mA
		Peak Current	Clock enabled, lux = 0		14		mA
V_{MEM_L}	Memory Element low level supply	Operating Voltage		**-5%**	2.5	**+5%**	V
		Dynamic Current	Clock enabled, lux = 0		0.2	1	mA
		Peak Current during FOT	Clock enabled, lux = 0		62		mA
		Peak Current during FOT	Clock enabled, bright		30		mA
V_{MEM_H}	Memory Element high level supply	Operating Voltage		**-5%**	3.3	**+5%**	V
		Dynamic Current	Clock enabled, lux = 0		1		mA
		Peak Current during FOT	Clock enabled, lux = 0		45		mA
V_{PRECH} (Note 4)	Pre_charge Driver Supply	Operating Voltage		**-10%**	0.7	**+10%**	V
		Dynamic Current	Clock enabled, lux = 0		0.3	3	mA
		Peak Current during FOT	Clock enabled, lux = 0		32		mA
		Peak Current during FOT	Clock enabled, lux = bright		25		mA

1. All parameters are characterized for DC conditions after thermal equilibrium is established.
2. The peak currents were measured without the load capacitor from the LDO (Low Dropout Regulator). The 100 nF capacitor bank was connected to the pin in question.
3. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is recommended that normal precautions be taken to avoid application of any voltages higher than the maximum rated voltages to this high-impedance circuit.
4. The VRES_AB and VPRECH power supply should be designed to have a sourcing and sinking current capability for frame rates of the order of 20k frames /sec.

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Every module in the image sensor has its own power supply and ground. The grounds can be combined externally, but not all power supply inputs may be combined. Some power supplies must be isolated to reduce electrical crosstalk and improve shielding, dynamic range, and output swing. Internal to the image sensor, the ground lines of each module are kept separate to improve shielding and electrical crosstalk between them.

The LUPA1300-2 contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, take normal precautions to avoid voltages higher than the maximum rated voltages in this high impedance circuit. Unused inputs must always be tied to an appropriate logic level, for example, V_{DD} or GND. All cap_xxx pins must be connected to ground through a 100 nF capacitor.

The recommended combinations of supplies are:

- Analog group of +2.5 V supply: V_{SAMPLE}, V_{RES_DS}, V_{MEM_L}, V_{ADC}, V_{pix}, V_{ANA}, V_{BUF}
- Digital Group of +2.5 V supply: V_{DIG}, V_{LVDS}
- Combine V_{PRECH} and V_{RES_AB} to one supply (Note 4)

Table 5. POWER DISSIPATION (Note 1)
Power supply specifications according to Table 4.

Symbol	Parameter	Condition	Typ	Unit
$Power_{STDBY}$	Standby Power	Blocks in standby with SPI upload	400	mW
Power	Average Power Dissipation	lux = 0, clock = 315 MHz, 500 fps	1350	mW

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Table 6. AC ELECTRICAL CHARACTERISTICS (Note 1)
The following specifications apply for VDD = 2.5 V, Clock = 315 MHz, 500 fps.

Symbol	Parameter	Condition	Typ	Max	Units
F_{CLK}	Input Clock Frequency	fps = 500		315	MHz
DC_{CLK}	Clock Duty Cycle	At maximum clock	50		%
DCD	Duty Cycle Distortion	At maximum clock		250	ps
	Jitter	peak-to-peak	50		ps
fps	Frame Rate	Maximum clock speed		500	fps

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

OVERVIEW

This data sheet describes the interface of the LUPA1300-2 image sensor. The SXGA resolution CMOS active pixel sensor features synchronous shutter and a maximal frame rate of 500 fps in full resolution. The readout speed is boosted by sub sampling and the windowed region of interest (ROI) readout. FPN correction cannot be used in conjunction with sub-sampling and windowed region of interest readout for windows starting with non zero kernel address. High dynamic range scenes can be captured using the double and multiple slope functionality. User programmable row and column start and stop positions enables windowing. Sub sampling reduces resolution while maintaining the constant field of view and an increased frame rate.

The LUPA1300-2 sensor has 12 LVDS high speed outputs that transfer image data over longer distances. This simplifies the surrounding system. The LVDS interface can receive high speed and wide bandwidth data signals and maintain low noise and distortion. A special training mode enables the receiving system to synchronize the incoming data stream when switching to master, slave, or triggered mode. The image sensor also integrates a programmable offset and gain amplifier for each channel.

A 10-bit ADC converts the analog signal to a 10-bit digital word stream. The sensor uses a 3-wire Serial Peripheral Interface (SPI). It requires only one master clock for operation up to 500 fps.

The sensor is available in a monochrome version or Bayer (RGB) patterned color filter array. It is placed in a 168-pin ceramic µPGA package.

Figure 3 depicts the photovoltaic response of the LUPA1300-2. Figure 4 shows the spectral response for the mono and color versions of LUPA1300-2.

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Photovoltaic Response Curve

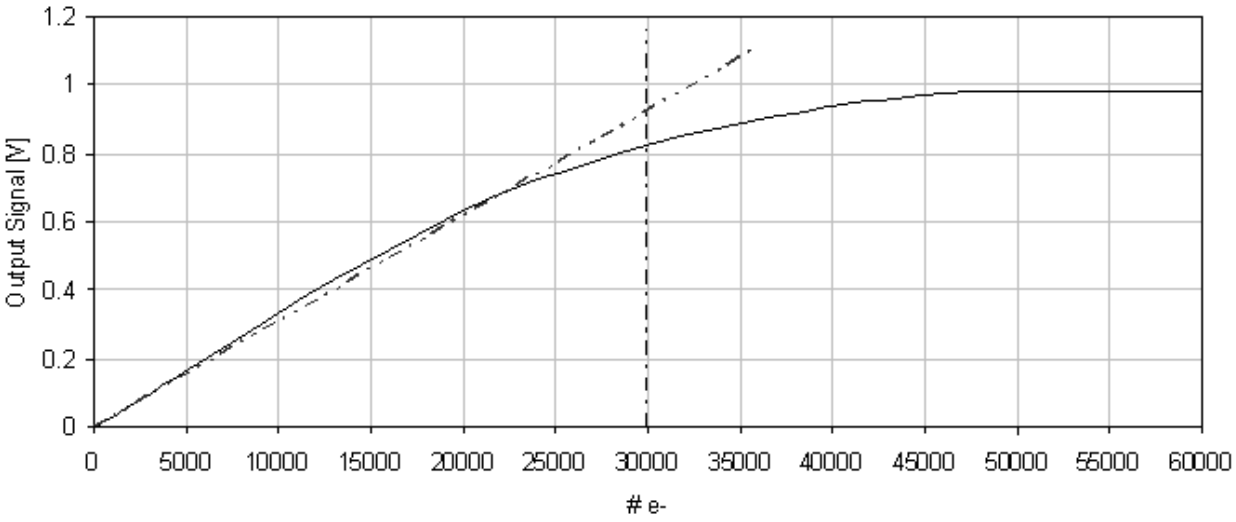


Figure 3. Photovoltaic Response of LUPA1300-2

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Spectral Response Curve

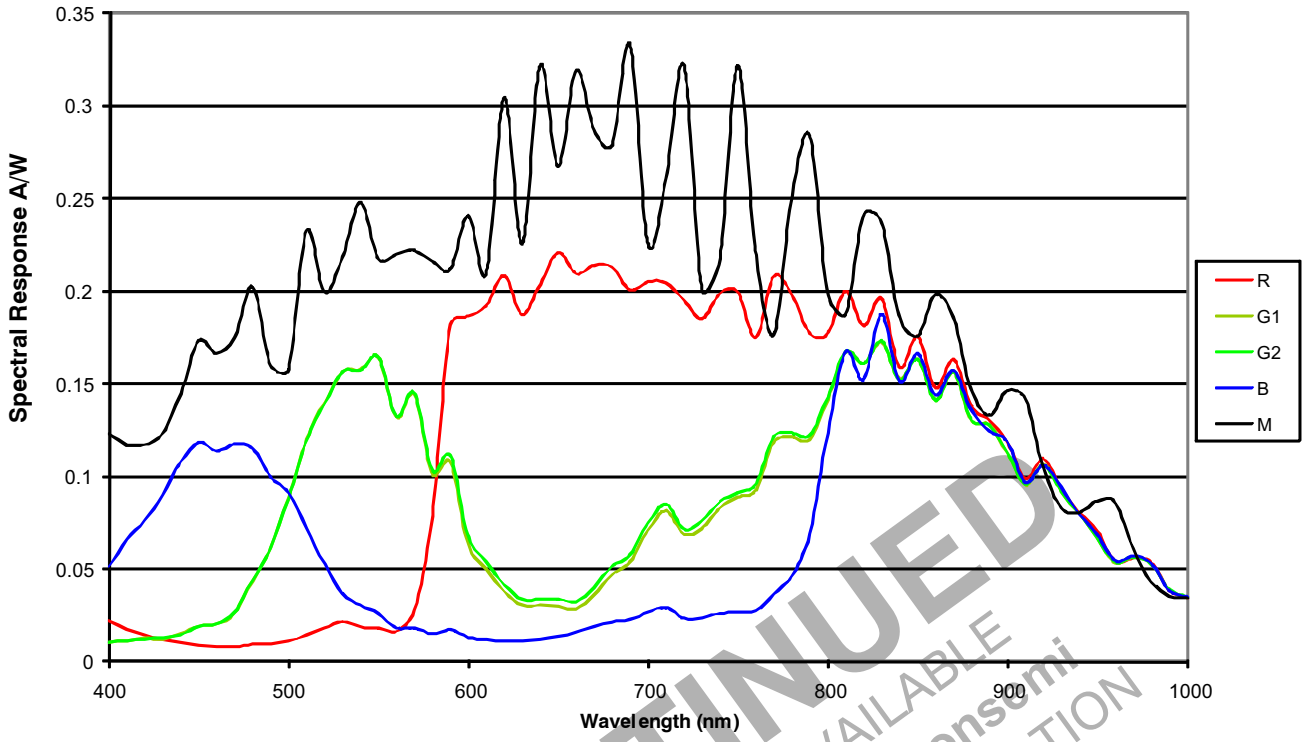


Figure 4. Spectral Response of LUPA1300-2 Mono and Color

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Color Filter Array

The color version of LUPA1300-2 is available in Bayer (RGB) patterned color filter array. The orientation of RGB is shown in Figure 5.

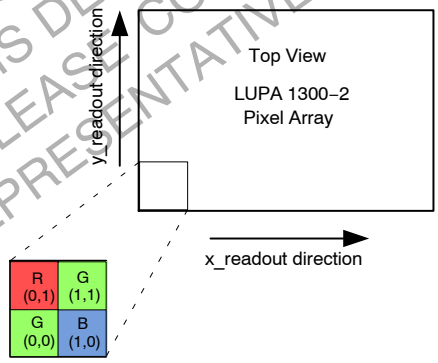


Figure 5. RGB Bayer

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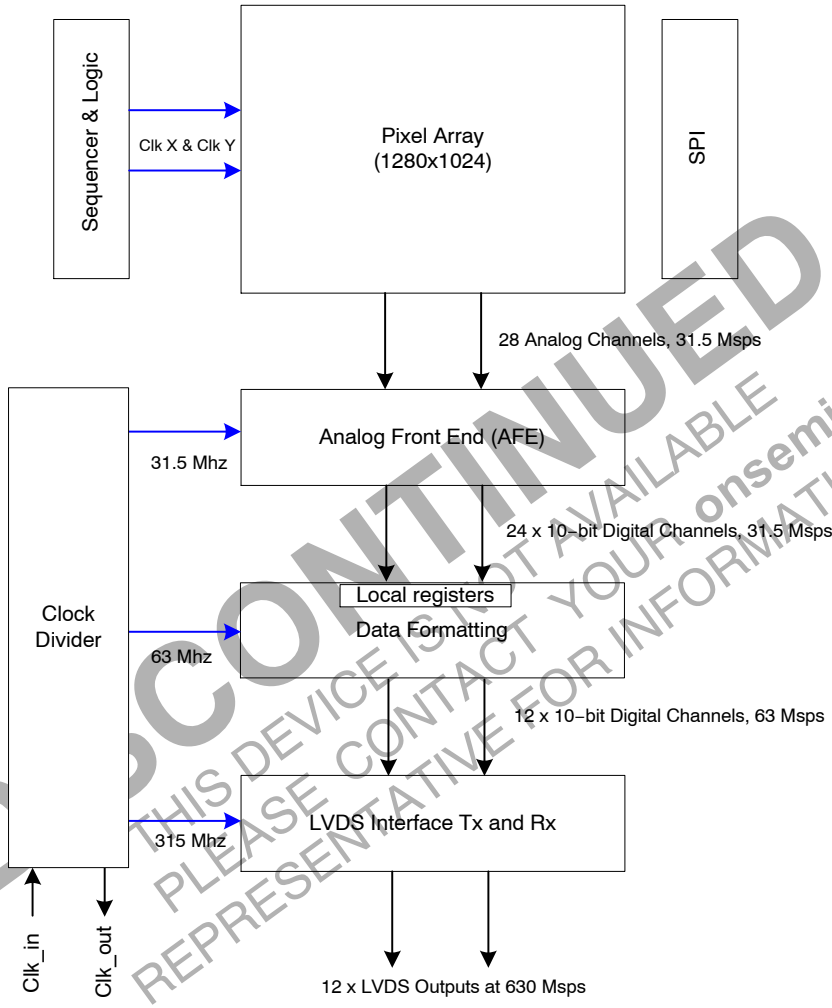
SENSOR ARCHITECTURE

Image Sensor Core

The floor plan of the architecture is shown in Figure 6. The sensor consists of a pixel array, analog front end, data block, and LVDS transmitters and receivers. Separate modules for the SPI, clock division, and sequencer are also integrated. The image sensor of 1280 x 1024 active pixels is read out in progressive scan.

This architecture enables programmable addressing in the x-direction in steps of 24 pixels, and in the y-direction in steps of one pixel. The starting point of the address can be uploaded by the SPI.

The AFE prepares the signal for the digital data block when the data is multiplexed and prepared for the LVDS interface.



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Figure 6. Floor Plan of the Sensor

The 6T Pixel

To obtain the global shutter feature combined with a high sensitivity and good parasitic light sensitivity (PLS), implement the pixel architecture shown in Figure 7. This pixel architecture is designed with a 14 μm x 14 μm pixel pitch to meet the specifications listed in Tables 1 and 2. This architecture also enables pipelined or triggered mode.

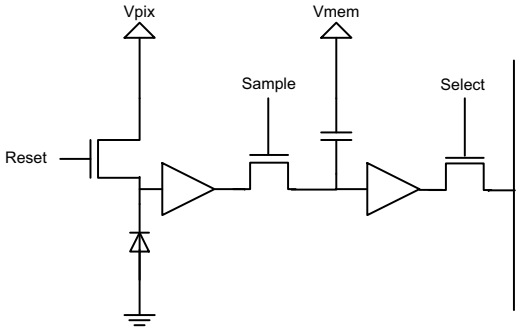


Figure 7. 6T Pixel Architecture

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Analog Front End

Programmable Gain Amplifiers

The PGAs amplify the signal before sending it to the ADCs.

The amplification inside the PGA is controlled by one SPI setting: afemode [5:3].

Six gain steps can be selected by the afemode<5:3> register.

Table 7 lists the six gain settings. The unity gain selection of the PGA is done by the default afemode<5:3> setting.

Table 7. GAIN SETTINGS

afemode<5:3>	Gain
000	1
001	1.5
010	2
011	2.25
100	3
101	4

Analog to Digital Converter

The sensor has 24 10-bit pipelined ADCs on board. The ADCs nominally operate at 31.5 Msamples/s.

Table 8. ADC PARAMETERS

Parameter	Specification
Data rate	31.5 Msamples/s
Quantization	10 bit
DNL	Typ. < 1 DN
INL	Typ. < 1 DN

Data Block

The data block is positioned in between the analog front end (output stage + ADCs) and the LVDS interface. It muxes the outputs of two ADCs to one LVDS block and performs some minor data handling:

- CRC calculation and insertion
- Training and test pattern generation

It also contains a huge part of the functionality for black level calibration and FPN correction.

A number of data blocks are placed in parallel to serve all data output channels. One additional channel generates the synchronization protocol. A high level overview is illustrated in the following figure.

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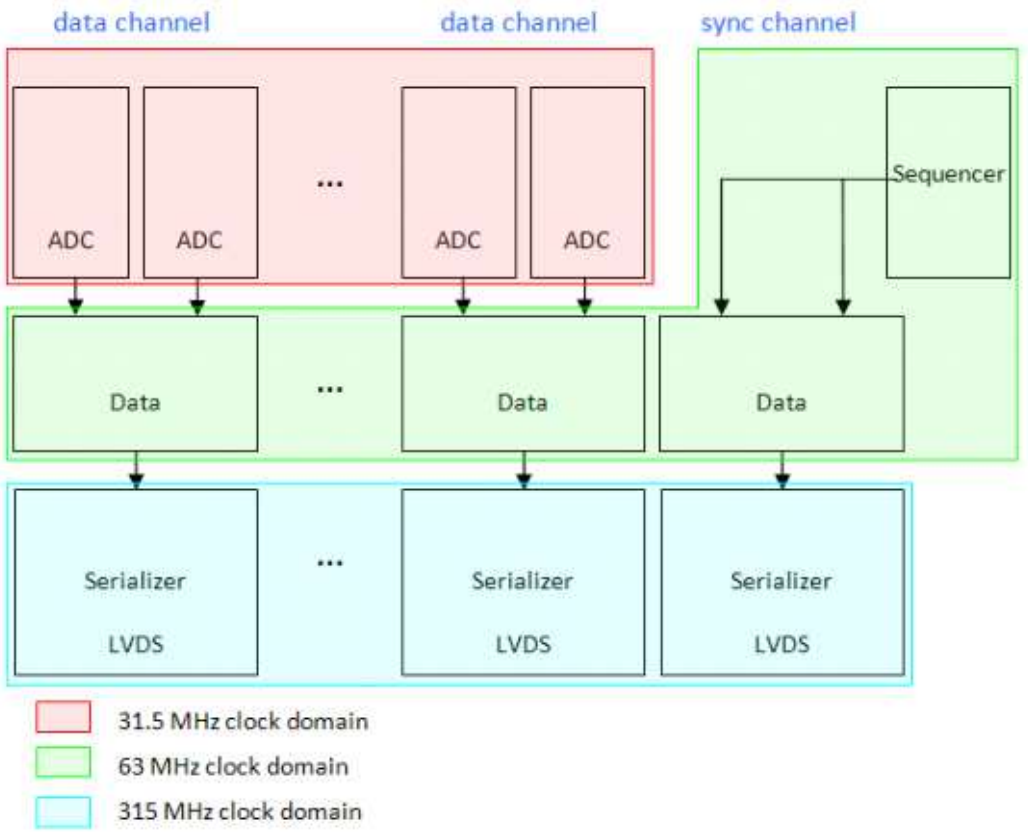


Figure 8. Data Block

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LVDS Block

The LVDS block is positioned below the data block. It receives a differential clock signal, transmits differential data over the 12 data channels, and transmits a LVDS clock signal and a synchronization signal over the clock and synchronization channel.

A number of LVDS transmitter blocks are placed in parallel to serve all data, clock, and synchronization output channels. A high level overview is illustrated in the following figure.

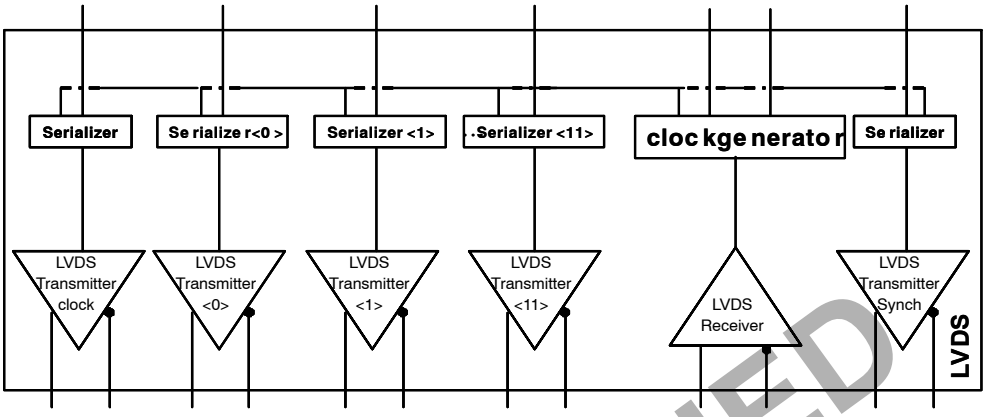


Figure 9. LVDS Block – High Level Overview

The function of this block is to take 10 bits of the protocol block, serialize these bits, and converts them to an LVDS standard (TIA/EIA 644A) compatible differential output signal. The block must also provide a clock to the host, to allow data recovery. This clock is an on-chip version of the clock coming from the host.

Sequencer and Logic

The sequencer generates the complete internal timing of the pixel array and the readout. The timing can be controlled by the user through the SPI register settings. The sequencer operates on the same clock as the data block. This is a division by 10 of the input clock (internally divided).

Table 9 lists the internal registers. These registers are discussed in detail in Detailed Description of Internal Registers on page 15.

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Table 9. INTERNAL REGISTERS

Block	Register Name	Address [6..0]	Field	Reset Value	Description
MBS (reserved)	Fix1	0	[7:0]	0x00	Reserved, fixed value
	Fix2	1	[7:0]	0xFF	Reserved, fixed value
	Fix3	2	[7:0]	0x00	Reserved, fixed value
	Fix4	3	[7:0]	0x00	Reserved, fixed value
	Fix5	4	[7:0]	0x08	Reserved, fixed value
LVDS clk divider	lvdsmain	5	[3:0]	'0110'	lvds trim
			[7:4]	0	clkadc phase (recommended value: 3)
	lvdspwd1	6	[7:0]	0x00	Power down channel 7:0
	lvdspwd2	7	[5:0]	0	Power down channel 13:8
			[6]	0	Power down all channels
			[7]	0	lvds test mode
	Fix6	8	[7:0]	0x00	Reserved, fixed value

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Table 9. INTERNAL REGISTERS (continued)

Block	Register Name	Address [6..0]	Field	Reset Value	Description
AFE	afebias	9	[3:0]	'1000'	afe current biasing
	afemode	10	[2:0]	'111'	vrefp, vrefm settings
			[5:3]	'000'	Pga settings
			[6]	0	Power down AFE
	afepwd1	11	[7:0]	0x00	Power down adc_channel_2x 7 to 0
AFE	afepwd2	12	[3:0]	0x00	Power down adc_channel_2x 11 to 8
Bias block	bandgap	13	[0]	'0'	Power down bandgap and currents
			[1]	'1'	External resistor
			[2]	'0'	External voltage reference
			[5:3]	'000'	Bandgap trimming
Image Core	imcmodes	14	[0]	0	Power down
			[1]	'1'	Enable vrefcol regulator
			[2]	'1'	Enable precharge regulator
			[3]	0	Disable internal bias for vprech
			[4]	'1'	Disable column load
			[5]	'0'	clkmain invert
	Fix7	15	[7:0]	0x00	Reserved, fixed value
	Fix8	16	[7:0]	0x00	Reserved, fixed value
	imcbias1	17	[3:0]	'1000'	Bias colfpn DAC buffer
			[7:4]	'1000'	Bias precharge regulator
	imcbias2	18	[3:0]	'1000'	Bias pixel precharge level
			[7:4]	'1000'	Bias column ota
	imcbias3	19	[3:0]	'1000'	Bias column unip fast
			[7:4]	'1000'	Bias column unip slow
	Imcbias4	20	[3:0]	'1000'	Bias column load
			[7:4]	'1000'	Bias column precharge

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Table 9. INTERNAL REGISTERS (continued)

Block	Register Name	Address [6..0]	Field	Reset Value	Description
Data Block	Fix9	21	[7:0]	0x20	Reserved, fixed value
	Fix10	22	[7:0]	0xC0	Reserved, fixed value
	dataconfig1	23	[1:0]	0x00	Reserved, fixed value
			[2]	1	'1': Enables user upload of dacvrefadc register value '0': Keeps default value
			[3]	0	Enable PRBS generation
			[4]	0	Reserved, fixed value
			[5]	0	Reserved, fixed value
			[7:6]	0x03	Training pattern inserted to sync LVDS receivers
	dataconfig2	24	[7:0]	0x2A	Training pattern inserted to sync LVDS receivers
	Fix11	25	[7:0]	0	Reserved, fixed value
	dacvrefadc	26	[7:0]	0x84	Input to DAC to set the offset at the input of the ADC
	Fix12	27	[7:0]	0x80	Reserved, fixed value
	Fix13	28	[7:0]		Reserved, fixed value
	Fix14	29	[7:0]		Reserved, fixed value
	datachannel0_1	30	[0]	0	Bypass the data block
			[1]	0	Enables the FPN correction
			[2]	0	Overwrite incoming ADC data by the data in the testpat register
			[3]	0	Reserved, fixed value
			[5:4]	0x00	Pattern inserted to generate a test image
Data Block	datachannel0_2	31	[7:0]	0x00	Pattern inserted to generate a test image
	datachannel1_1	32	[0]	0	Bypass the data block
			[1]	0	Enables the FPN correction
			[2]	0	Overwrite incoming ADC data by the data in the testpat register
			[3]	0	Reserved, fixed value
			[5:4]	0x00	Pattern inserted to generate a test image
	datachannel1_2	33	[7:0]	0x00	Pattern inserted to generate a test image
	datachannel12_1	54	[0]	0	Bypass the data block
			[1]	0	Enables the FPN correction
			[2]	0	Overwrite incoming ADC data by the data in the testpat register
			[3]	0	Reserved, fixed value
			[5:4]	0x00	Pattern inserted to generate a test image
	datachannel12_2	55	[7:0]	0x00	Pattern inserted to generate a test image

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Table 9. INTERNAL REGISTERS (continued)

Block	Register Name	Address [6..0]	Field	Reset Value	Description
Sequencer	seqmode1	56	[0]	1	Enables sequencer for image capture
			[1]	1	'1': Master mode, integration timing is generated on-chip '0': Slave mode, integration timing is controlled off-chip through INT_TIME1, INT_TIME2 and INT_TIME3 pins
			[2]	0	'0': Pipelined mode '1': Triggered mode
			[3]	0	Enables('1')/disables('0') subsampling
			[4]	0	'1': Color subsampling scheme: 1:1:0:0:1:1:0:0 '0': B&W subsampling scheme: 1:0:1:0:1
			[5]	0	Enable dual slope
			[6]	0	Enable triple slope
			[7]	0	Enables continued row select (that is, assert row select during pixel read out)
	seqmode2	57	[4:0]	'10000'	Must be overwritten with '10001' to this register after startup, before readout.
			[6:5]	'00'	Number of active windows: "00": 1 window "01": 2 windows "10": 3 windows "11": 4 windows
	seqmode3	58	[0]	'1'	Enables the generation of the CRC10 on the data and sync channels
			[1]	'0'	Enable readout black/grey columns
			[2]	'0'	Enable column fpn calibration/enable readout dummy line
			[5:3]	"001"	Number of frames in nondestructive read out: "000": invalid "001": one reset, one sample (default mode) "010": one reset, two samples …
Sequencer			[6]	0	Controls the granularity of the timer settings (only for those that have 'granularity selectable' in the description): '0': Expressed in number of lines '1': Expressed in clock cycles (multiplied by 2**seqmode4[3:0])
			[7]	0	Allows delaying the syncing of events that happen outside of ROT to the next ROT. This avoids image artefacts.
	seqmode4	59	[3:0]	0x00	Multiplier factor (=2**seqmode4[3:0]) for the timers when working in clock cycle mode
			[5:4]	0x0	Selects the source signals to put on the digital test pins (monitor pins): "00": integration time settings "01": EOS signals "10": frame sync signals "11": functional test mode
			[6]	'0'	Reverse read out in X direction
			[7]	'0'	Reverse read out in Y direction
	window1_1	60	[7:0]	0x00	Y start address for window 1
	window1_2	61	[1:0]	0x00	Y start address for window 1
			[7:2]	0x00	X start address for window 1
	window1_3	62	[7:0]	0xFF	Y end address for window 1
	window1_4	63	[1:0]	0x3	Y end address for window 1
			[7:2]	0x36	X width for window 1

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Table 9. INTERNAL REGISTERS (continued)

Block	Register Name	Address [6..0]	Field	Reset Value	Description
	window2_1	64	[7:0]	0x00	Y start address for window 2
	window2_2	65	[1:0]	0x00	Y start address for window 2
			[7:2]	0x00	X start address for window 2
	window2_3	66	[7:0]	0xFF	Y end address for window 2
	window2_4	67	[1:0]	0x3	Y end address for window 2
			[7:2]	0x36	X width for window 2
	window3_1	68	[7:0]	0x00	Y start address for window 3
	window3_2	69	[1:0]	0x00	Y start address for window 3
			[7:2]	0x00	X start address for window 3
	window3_3	70	[7:0]	0xFF	Y end address for window 3
	window3_4	71	[1:0]	0x3	Y end address for window 3
			[7:2]	0x36	X width for window 3
	window4_1	72	[7:0]	0x00	Y start address for window 4
	window4_2	73	[1:0]	0x00	Y start address for window 4
			[7:2]	0x00	X start address for window 4
	window4_3	74	[7:0]	0xFF	Y end address for window 4
	window4_4	75	[1:0]	0x3	Y end address for window 4
			[7:2]	0x36	X width for window 4
	res_length1	76	[7:0]	0x02	Length of pix_rst (granularity selectable)
	res_length2	77	[7:0]	0x00	Length of pix_rst (granularity selectable)
	res_dsts_length	78	[7:0]	0x01	Length of resetds and resetts (granularity selectable)
	tint_timer1	79	[7:0]	0xFF	Length of integration time (granularity selectable)
	tint_timer2	80	[7:0]	0x03	Length of integration time (granularity selectable)
	tint_ds_timer1	81	[7:0]	0x40	Length of DS integration time (granularity selectable)
	tint_ds_timer2	82	[1:0]	0x00	Length of DS integration time (granularity selectable)
	tint_ts_timer1	83	[7:0]	0x0C	Length of TS integration time (granularity selectable)
	tint_ts_timer2	84	[1:0]	0x00	Length of TS integration time (granularity selectable)
	tint_black_timer	85	[7:0]	0x06	Reserved, fixed value
	rot_timer	86	[7:0]	0x09	Length of ROT (granularity clock cycles)
	fot_timer	87	[7:0]	0x3B	Length of FOT (granularity clock cycles)
	fot_timer	88	[1:0]	0x01	Length of FOT (granularity clock cycles)
	prechpix_timer	89	[7:0]	0x7C	Length of pixel precharge (granularity clock cycles)
	prechpix_timer	90	[1:0]	0x00	Length of pixel precharge (granularity clock cycles)
	prechcol_timer	91	[7:0]	0x03	Length of column precharge (granularity clock cycles)
	rowselect_timer	92	[7:0]	0x06	Length of rowselect (granularity clock cycles)
	sample_timer	93	[7:0]	0xF8	Length of pixel_sample (granularity clock cycles)
	sample_timer	94	[1:0]	0x00	Length of pixel_sample (granularity clock cycles)
	vmem_timer	95	[7:0]	0x10	Length of pixel_vmem (granularity clock cycles)
	vmem_timer	96	[1:0]	0x01	Length of pixel_vmem (granularity clock cycles)
	delayed_rdt_timer	97	[7:0]	0	Readout delay for testing purposes (granularity selectable)

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Table 9. INTERNAL REGISTERS (continued)

Block	Register Name	Address [6..0]	Field	Reset Value	Description
	delayed_rdt_timer	98	[7:0]	0	Readout delay for testing purposes (granularity selectable)
	Fix29	99	[0]	0	Reserved, fixed value
	Fix30	100	[0]	0	Reserved, fixed value
	Fix31	101	[0]	0	Reserved, fixed value
	Fix32	102	[0]	0	Reserved, fixed value
	Fix33	103	[0]	0	Reserved, fixed value
	Fix34	104	[0]	0	Reserved, fixed value

Detailed Description of Internal Registers

The registers must be changed only during idle mode, that is, when seqmode1[0] is '0'. Uploaded registers have an immediate effect on how the frame is read out. Parameters uploaded during readout may have an undesired effect on the data coming out of the images.

MBS Block

The register block contains registers for sensor testing and debugging. All registers in this block must remain unchanged after startup.

LVDS Clock Divider Block

This block controls division of the input clock for the LVDS transmitters or receivers. This block also enables shutting down one or all LVDS channels. For normal operation, this register block must remain untouched after startup.

AFE Block

This register block contains registers to shut down ADC channels or the complete AFE block. This block also contains the register for setting the PGA gain: AFE_mode[5:3]. Refer to Absolute Maximum Ratings on page 3 for more details on the PGA settings.

Biasing Block

This block contains several registers for setting biasing currents for the sensor. Default values after startup must remain unchanged for normal operation of the sensor.

Image Core Block

The registers in this block have an impact on the pixel array itself. Default settings after startup must remain unchanged for normal operation of the image sensor.

Data Block

The data block is positioned in between the analog front end (output stage + ADCs) and the LVDS interface. It muxes the outputs of 2 ADCs to one LVDS block and performs some minor data handling:

- CRC calculation and insertion.

  All data can be protected by a 10-bit checksum. The CRC10 is calculated over all pixels between a Line Start and a Line End. It is inserted in the data stream after the line is completed, if input seq_data_crc is enabled.The polynomial used is (x^10+x^9+x^6+x^3+x^2+x+1) and 10 bits are calculated in parallel. When a new line is started, the seed is the first pixel value of a line. No CRC is calculated for that value. From then on, every incoming pixel is updated through the regular CRC.
- Training and test pattern generation

The most important registers in this block are:

Dataconfig. The dataconfig1[7:6] and dataconfig2[7:0] registers insert a training pattern in the LVDS channels to sync the LVDS receivers.

Datachannels. DatachannelX_1 and DatachannelX_2 (with X=0 to 12) are registers that allow you to enable or disable the FPN correction (DatachannelX_1[1]), and generate a test pattern if necessary (datachannelX_1[5:4] and datachannelX_2[7:0]).

Sequencer Block

The sequencer block group registers allow enabling or disabling image sensor features that are driven by the onboard sequencer. This block consists of the following registers:

Seqmode1. The seqmode1 registers have the following subregisters:

Seqmode1[0]: Enables sequencer for image capture, must be '1' during image acquisition.

Seqmode1[1]: This subregister has two modes:

'1': In this default mode the integration timing is generated on-chip.

'0': In this slave mode, the integration timing must be generated through the int_time1, int_time2, and int_time3 pins.

Seqmode1[2]: This bit enables pipelined (0) or triggered (1) mode.

Seqmode1[3]: Enable (1) or disable (0) subsampling.

Seqmode1[4]: This bit sets the type of subsampling scheme used when subsampling is enabled.

'1': Color (1:1:0:0:1:1:0:0:1…)

'0': Black and White (1:0:1:0:1)

Seqmode1[5]: This bit enables or disables the dual slope integration.

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Seqmode1[6]: This bit enables or disables the triple slope integration.

Seqmode2. The seqmode2 register consists of only two subregisters:

Seqmode2[4:0]: Default value after startup is ’10000’, but this must be overwritten with the new value ’10001’ immediately after startup.

Seqmode3[6:5]: These two bits set the number of active windows:

‘00’: 1 window

‘01’: 2 windows

‘10’: 3 windows

‘11’: 4 windows (max)

Seqmode3. The seqmode3 register consists of the following subregisters:

Seqmode3[0]: This bit enables or disables the CRC10 generation on the data and sync channels

Seqmode3[1]: Not applicable

Seqmode3[2]: Enables or disables column FPN correction

Seqmode3[5:3]: Enables or disables, and sets the number of frames grabbed in nondestructive readout mode.

‘000’: Invalid

‘001’: Default, 1 reset, 1 sample

‘010’: 1reset, 2 samples

‘011’: 1 reset, 3 samples

Seqmode3[6]: Controls the granularity of the timer settings (only for those that have ‘granularity selectable’ in the description). As a result, all timer settings are set either in number of applied clock cycles, or in the number of ‘readout lines’.

‘0’: expressed in number of lines

‘1’: expressed in clock cycles (multiplied by 2**seqmode4 [3:0])

Seqmode3[7]: Allows syncing of events that happen outside of ROT to be delayed to the next ROT to avoid image artifacts.

Seqmode4. This register consists of four subregisters:

Seqmode4[3:0]: Multiplier factor (2**seqmode4[3:0]) for the timers when working in clock cycle mode.

Seqmode4[5:4]: Selects the source signals to be put on the digital test pins (monitor1, monitor2, and monitor3 pins)

“00”: integration time settings

“01”: EOS signals

“10”: frame sync signals

“11”: functional test mode

Seqmode4[6]: Enables (1) and disables (0) reverse X read out.

Seqmode4[7]: Enables (1) and disables (0) reverse Y read out.

Y1_start (60 and 61, 10 bit). These registers set the Y start address for window 1 (default window).

X1_start (61, 6bit). This register sets the X start address for window 1 (default window).

Y1_end (62 and 63, 10 bit). These registers set the Y end address for window 1 (default window).

X1_kernels (63, 6 bit). This register sets the number of kernels or X width to be read out for window 1 (default window).

Y2_start (64 and 65, 10 bit). These registers set the Y start address for window 2 (if enabled).

X2_start (65, 6bit). This register sets the X start address for window 2 (if enabled).

Y2_end (66 and 67, 10 bit). These registers set the Y end address for window 2 (if enabled).

X2_kernels (67, 6 bit). This register sets the number of kernels or X width to be read out for window 2 (if enabled).

Y3_start (68 and 69, 10 bit). These registers set the Y start address for window 3 (if enabled).

X3_start (69, 6bit). This register sets the X start address for window 3 (if enabled).

Y3_end (70 and 71, 10 bit). These registers set the Y end address for window 3 (if enabled).

X3_kernels (71, 6 bit). This register sets the number of kernels or X width to be read out for window 3 (if enabled).

Y4_start (72 and 73, 10 bit). These registers set the Y start address for window 4 (if enabled).

X4_start (73, 6bit). This register sets the X start address for window 4 (if enabled).

Y4_end (74 and 75, 10 bit). These registers set the Y end address for window 4 (if enabled).

X4_kernels (75, 6 bit). This register sets the number of kernels or X width to be read out for window 4 (if enabled).

Res_length (76 and 77). This register sets the length of the internal pixel array reset (how long are all pixel reset simultaneously). This value is expressed in ’number of lines’ or in clock cycles (depends on seqmode3[6]).

Res_dsts_length. This register sets the length of the internal dual and triple slope reset pulses when enabled. This value is expressed in ’number of lines’ or in clock cycles (depends on seqmode3[6]).

Tint_timer (79 and 80). This register sets the length of the integration time. This value is expressed in ’number of lines’ or in clock cycles (depends on seqmode3[6]).

Tint_ds_timer (81 and 82). This register sets the length of the dual slope integration time. This value is expressed in ’number of lines’ or in clock cycles (depends on seqmode3[6]).

Tint_ts_timer (83 and 84). This register sets the length of the triple slope integration time. This value is expressed in ’number of lines’ or in clock cycles (depends on seqmode3[6]).

Serial Peripheral Interface (SPI)

The serial 4-wire interface (or SPI) uses a serial input or output to shift the data in or out the register buffer. The chip’s configuration registers are accessed from the outside world through the SPI protocol. A 4-wire bus runs over the chip and connects the SPI I/Os with the internal register blocks. To upload the sensor, follow this sequence:

Disable Sequencer → Upload Sensor for new setting → Enable Sequencer

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When sequencer is disabled, the training pattern appears on all the channels, including the sync. The interface consists of:

- cs_n: chip select, when LOW the chip is selected
- clk: the spi clock
- in: Master out, Slave in, the serial input of the register
- out: Master in, Slave out, the serial output of the register

SPI Protocol

The information on the data ‘in’ line is:

- A command bit C, indicating a write (‘1’) or a read (‘0’) access
- 7-bit address
- 8-bit data word (in case of a write access)

The data ’out’ line is generally in High Z mode, except when a read request is performed.

Data is always written on the bus on the falling edge of the clock, and sampled on the rising edge, as seen in Figure 9 and Figure 10. This is valid for both the ’in’ and ’out’ bus. The system clock must be active to keep the SPI uploads stored on the chip. The SPI clock speed must be slower by a factor of 30 when compared to the system clock (315 MHz nominal speed).

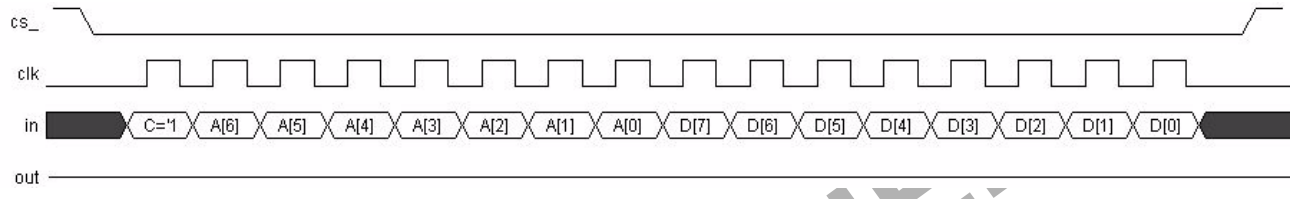


Figure 10. Write Access (C = ‘1’)

The ‘out’ line is held to High Z. The data for the address A is transferred from the shift register to the active register bank (that is, sampled) on a rising edge of cs_n. Only the register block with address A can write its data on the ‘out’ bus. The data on ‘in’ is ignored.

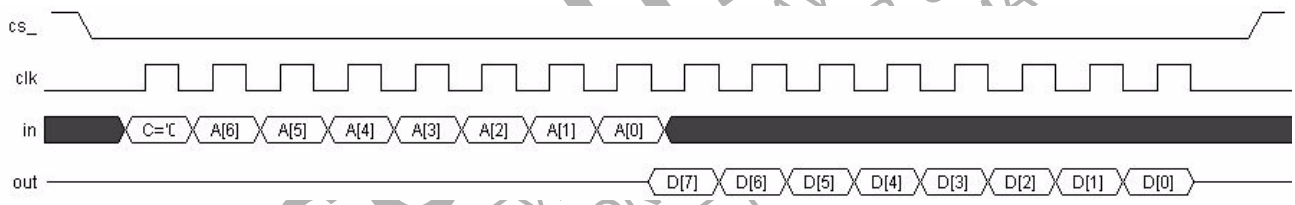


Figure 11. Read Access (C = ‘0’)

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IMAGE SENSOR TIMING AND READOUT

Frame Rate and Windowing

Frame Rate

The frame rate depends on the input clock, the frame overhead time (FOT), and the row overhead time (ROT). The frame period is calculated as follows:

1 kernel = 24 Pixels = 2 Timeslots = 2 Granularity clock cycles

Table 10. FRAME RATE PARAMETERS

Parameter	Comment	Clarification
FOT	Frame Overhead Time	Programmable: Default 315 granularity clock cycles (5 μs at 63 MHz)
ROT	Row Overhead Time	Programmable: Default 9 granularity clock cycles (143.1 ns at 63 MHz)
Nr. Lines	Number of lines read out each frame	Number of lines in ROI
Nr. Pixels	Number of pixels read out each line	Number of pixels in ROI
Clock Period	1/63 MHz = 15.9 ns	Every channel works at 63 MHz →12 channels result in 756 MHz data rate

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

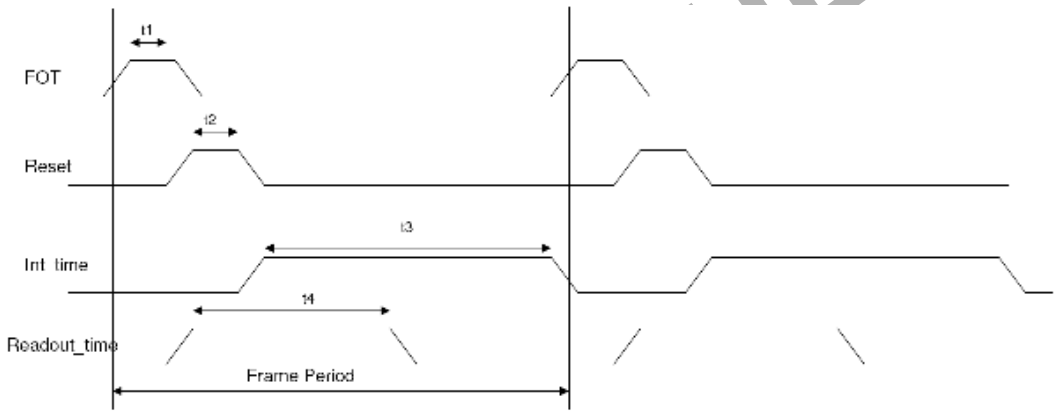


Figure 12. Timing Diagram

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Windowing

Windowing is easily achieved by SPI. The starting point of the x and y address and the window size can be uploaded. The minimum step size in the x-direction is 24 pixels (choose only multiples of 24 as start or stop addresses). The minimum step size in the y-direction is one line (every line can be addressed) in normal mode, and two lines in sub sampling mode.

The section Sequencer and Logic on page 10 discusses the use of registers to achieve the desired ROI.

Table 11. TYPICAL FRAME RATES AT 315 MHz

Image Resolution (X*Y)	Frame Read Out Time (ms)	Frame Rate (fps)
1296 x 1024	1.9760	506
1008 x 1000	1.5807	633
816 x 600	0.7997	1250
648 x 480	0.5370	1862
528 x 512	0.4887	2046
264 x 256	0.1596	6266
144 x 128	0.0640	15625
24 x 2	0.0098	102249

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Operation and Signaling

Digital Signals

Depending on the operation mode (Master or Slave), the pixel array of the image sensor requires different digital control signals. The function of each signal is listed in this table.

Table 12. OVERVIEW OF DIGITAL SIGNALS

Signal Name	I/O	Comments
MONITOR_1	Output	Output pin for integration timing, high during integration
MONITOR_2	Output	Output pin for dual slope integration timing, high during integration
MONITOR_3	Output	Output pin for triple slope integration timing, high during integration
INT_TIME_3	Input	Integration pin triple slope
INT_TIME_2	Input	Integration pin dual slope
INT_TIME_1	Input	Integration pin first slope
RESET_N	Input	Sequencer reset, active LOW
CLK	Input	System clock (315 MHz)
SPI_CS	Input	SPI chip select
SPI_CLK	Input	Clock of the SPI (< Sensor clock/30)
SPI_IN	Input	Data line of the SPI, serial input
SPI_OUT	Output	Data line of the SPI, serial output

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Global Shutter

In a global shutter, light integration occurs on all pixels in parallel, although subsequent readout is sequential. Figure 12 shows the integration and readout sequence for the global shutter. All pixels are light sensitive at the same period of time. The whole pixel core is reset simultaneously, and after the integration time, all pixel values are sampled together on the storage node inside each pixel. The pixel core is read out line by line after integration. Note that the integration and readout cycle can occur in parallel (refer to Pipelined Shutter on page 20) or in sequential (refer to Triggered Shutter on page 22) mode.

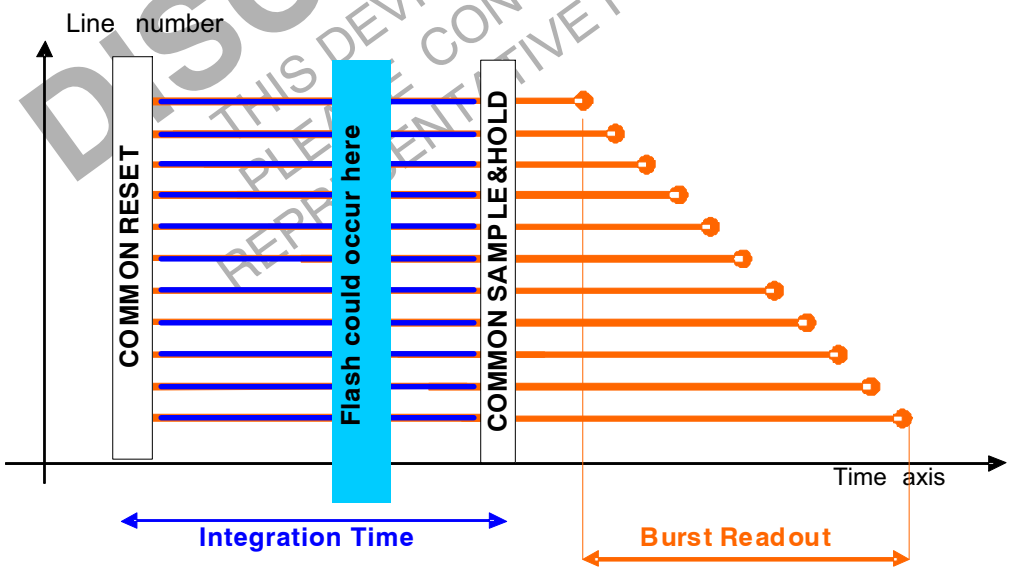


Figure 13. Global Shutter Operation

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The timing of the sensor consists of two parts. The first part is related to the exposure time and the control of the pixel. The second part is related to the read out of the image sensor. Integration and readout are in parallel or triggered. In the first case, the integration time of frame I is ongoing during the readout of frame I-1. Figure 13 shows this parallel timing structure.

The readout of every frame starts with a FOT, during which the analog value on the pixel diode is transferred to the pixel memory element. After this FOT, the sensor is read out line by line. The read out of every line starts with a ROT, during which the pixel value is put on the column lines. Then the pixels are selected in groups of 24 (12 on rising edge, and 12 on the falling edge of the internal clock). So in total, 54 kernels of 24 pixels are read out every line. The internal timing is generated by the sequencer. The sequencer can operate in two modes: master mode and slave mode. In master mode, all internal timing is controlled by the sequencer, based on the SPI settings. In slave mode, the integration timing is directly controlled by over three pins, and the readout timing is still controlled by the sequencer. The seqmode1[1] register of the SPI selects between the master and slave modes.

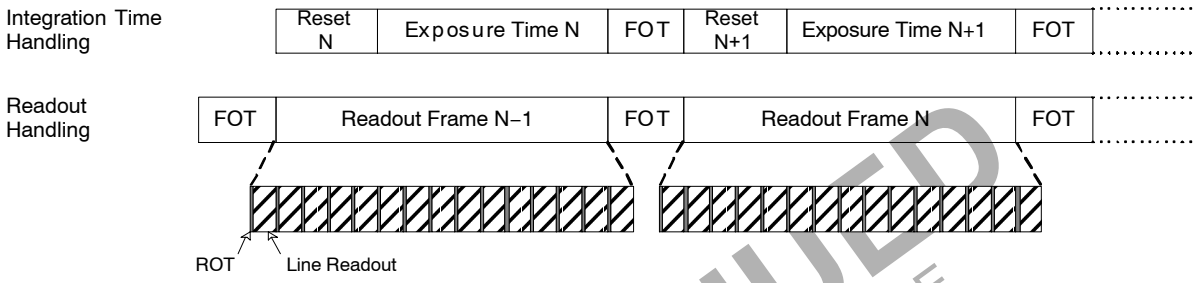


Figure 14. Global Readout Timing (Parallel)

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Pipelined Shutter

Integration and readout occur in parallel and are continuous. You only need to start and stop the batch of image captures.

Integration of frame N is always ongoing during readout of frame N-1. The readout of every frame starts with a FOT, during which the analog value on the pixel diode is transferred to the pixel memory element. After this FOT, the sensor is read out line by line. The readout of every line starts with a ROT, during which the pixel value is put on the column lines. Then the pixels are mixed in the correct ADCs, processed, and then sent to the LVDS output block.

You have two options in the pipelined shutter mode. The first option is to program the reset and integration through the configuration interface and let the sequencer handle integration time automatically. This mode is called master mode. The second option is to drive the integration time through an external pin. This mode is called slave mode.

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Programming the Exposure Time

In master mode, the exposure time is configured in two distinct methods (controlled by register seqmode3[6]):

- # lines: Obvious, changing signals that control integration time. They are always changed during ROT to avoid any image artefacts.
- # clock cycles: Must be multiplied by (2**seqmode4[3:0]). When the counter expires, changes are put into effect immediately. Asserting the configuration signal (seqmode3[7]) forces delaying signal updates until the next ROT.

Table 13 lists the user programmable timer settings and how they are interpreted by the hardware.

Table 13. USER PROGRAMMABLE TIMER SETTINGS

Setting	Granularity
reg_res_length	Lines/cycles
reg_tint_timer	Lines/cycles
reg_tint_ds_timer	Lines/cycles
reg_tint_ts_timer	Lines/cycles
res_dsts_length	Lines/cycles
reg_rot_timer	clock cycles
reg_fot_timer	clock cycles
reg_sel_pre_timer	clock cycles
reg_precharge_timer	clock cycles
reg_sample_timer	clock cycles
reg_vmem_timer	clock cycles
reg_delayed_rdt_timer	Lines/cycles

Note that the seqmode3[7] can also be used to sync the user signals in slave mode. The behavior is exactly the same.

Master Mode

In master mode the reset and exposure time is written in registers.

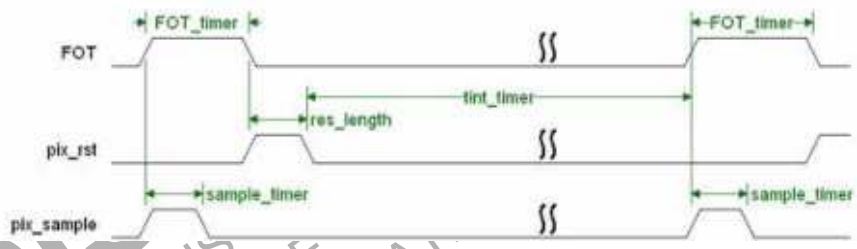


Figure 15. Integration and Image Readout in Master Mode

Ensure that the added value of the registers res_length and tint_timer always exceeds the number of lines that are read out. This is because the sequencer samples a new image after integration is complete, without checking if image readout is finished. Enlarging res_length to accommodate for this has no impact on image capture.

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Slave Mode

In slave mode, the register values of res_length and tint_timer are ignored. The integration time is controlled by the int_time pin. The relationship between the input pin and the integration time is shown in Figure 16. When the input pin int_time is asserted, the pixel array goes out of reset and exposure can begin. When int_time goes low again and the desired exposure time is reached, the image is sampled and read out can begin.

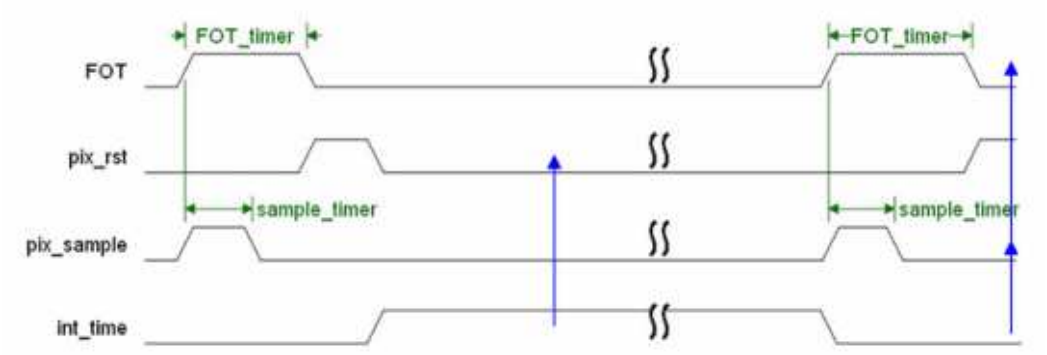


Figure 16. Integration and Image Readout in Slave Mode

Changing pixel's reset level during line readout might result in image artefacts during a small transient period. As a result, it is advised to only change the value of int_time during ROT.

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Triggered Shutter

The two main differences in the pipelined shutter mode are:

- One single image is read upon every user action.
- Integration (and read out) is under control of the user through pin int_time.

This means that for every frame, you need to manually intervene. The pixel array is kept in reset state until you assert the int_time input. Similar to the pipelined shutter mode, there is a master mode in which the sequencer can control the integration time, or a slave mode in which you can define the integration time.

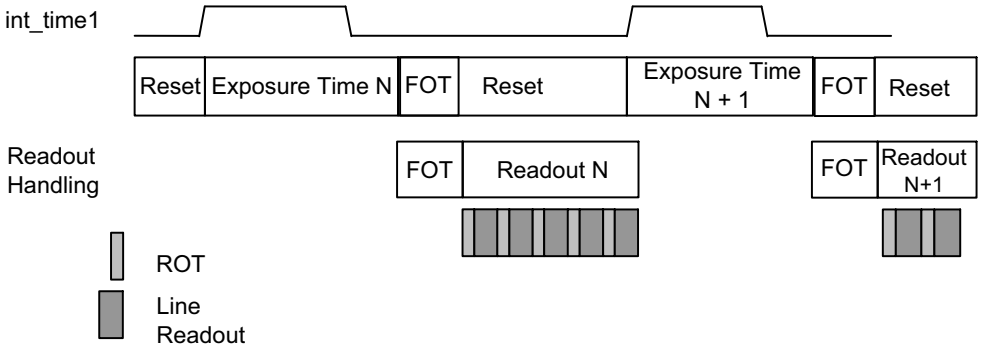


Figure 17. Integration and Readout for Triggered Shutter

The possible applications for this triggered shutter mode are:

- Synchronize external flash with exposure
- Apply extremely long integration times (only in slave mode)

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Master Mode

In this mode, a rising edge on int_time1 pin is used to trigger the start of integration and read out. The tint_timer defines the integration time independent of the assertion of the input pin int_time1. After the integration time counter runs out, the FOT automatically starts and the image readout is done. During readout, the image array is kept in reset. A request for a new frame is started again when a new rising edge on int_time is detected. The time of the falling edge is not important in this mode.

Slave Mode

Integration time control is identical to the pipelined shutter slave mode. The int_time1 pin controls the start of integration. When int_time is deasserted, the FOT starts (analog value on the pixel diode is transferred to the pixel memory element). Only at that time, image read out can start (similar to the pipelined read out). During read out, the image array is kept in reset. A request for a new frame is started when int_time goes high again.

Non Destructive Readout (NDR)

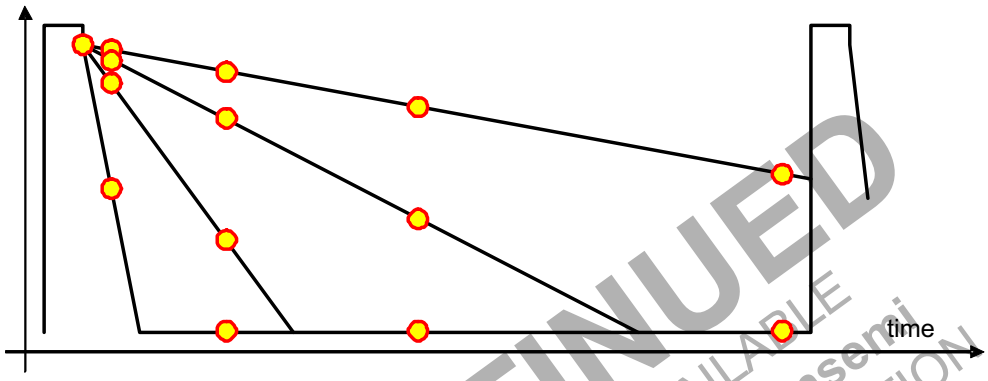


Figure 18. Principle of Non Destructive Readout

The sensor can also be read out in a nondestructive method. After a pixel is initially reset, it can be read multiple times, without being reset. You can record the initial reset level and all intermediate signals. High light levels saturate the pixels quickly, but a useful signal is obtained from the early samples. For low light levels, the later or latest samples must be used. Essentially, an active pixel array is read multiple times, and reset only once. The external system intelligence interprets the data. Table 14 summarizes the advantages and disadvantages of nondestructive readout.

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Table 14. ADVANTAGES AND DISADVANTAGES OF NON DESTRUCTIVE READOUT

Advantages	Disadvantages
Low noise, because it is true CDS	System memory required to record the reset level and the intermediate samples
High sensitivity. The conversion capacitance is kept low.	Requires multiples readings of each pixel, so there is higher data throughput
High dynamic range. The results include signals for short and long integration times.	Requires system level digital calculations

Note that the amount of samples taken with one initial reset is programmable in the nr_of_ndr_steps register. If nr_of_ndr_steps is one, the sensor operates in the default method, that is one reset and one sample. This is called the disable nondestructive read out mode.

When nr_of_ndr_steps is two, there is one reset and two samples, and so on. In the slave mode, nothing changes on the protocol of the signals int_time_*. The sequencer suppresses the internal reset signal to the pixel array.

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Image Format and Read Out Protocol

The active area read out by the sequencer in full frame mode is shown in Figure 18. Before the actual pixels are read out, one dummy line is read to enable column FPN correction. A reference voltage is applied to the columns and the entire line is read as if real pixel values are placed on the columns.

Pixels are always read in multiples of 24 (one value to every channel in the AFE). The last time slot contains not only valid pixels, but also two dummy columns, six grey columns, and eight black columns.

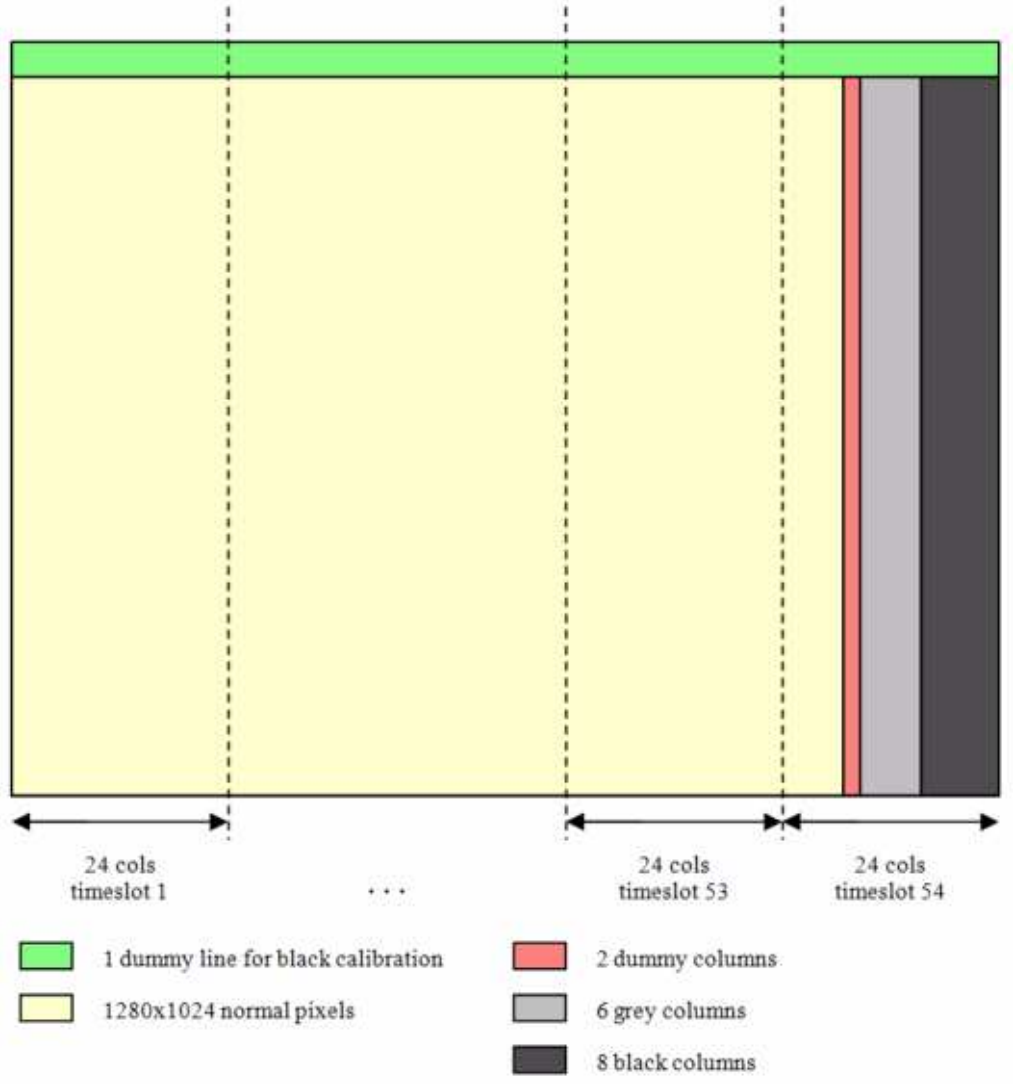


Figure 19. Sensor Read Out Format

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The following sections discuss the appearance of the output (data and synchronization codes) in several relevant configurations. Twelve output channels are connected to the 24 ADCs and handle the data. One additional channel contains all the synchronization codes for the receiver. This indicates, for example, the start of a frame, the end of a frame, whether the data channels contain data, CRC, a training pattern, and so on. The sequencer provides the synchronization channel with the correct synchronization or protocol signals, as shown in Figure 7. The synchronization codes are listed in Table 15. Note that a FS also serves as LS, and vice versa.

Table 15. SYNCHRONIZATION CODES

Sync code	Abbreviation	10-Bit Code
Frame Start	FS	0x059
Line Start	LS	0x056
Frame End	FE	0x05A
Line End	LE	0x055
Grey/Black Cols	GBC	0x0A9
CRC	CRC	0x0A6
FPN stored values	FPN	0x13C
Normal Data	D	0x193
Training Pattern	T	T

This table provides a detailed overview of remapping one full row read out.

Table 16. REMAPPING SCHEME FOR ONE ROW

timeslot	ch0	ch1	ch2	ch3	ch4	ch5	ch6	ch7	ch8	ch9	ch10	ch11
1a	0	2	4	6	8	10	12	14	16	18	20	22
1b	1	3	5	7	9	11	13	15	17	19	21	23
2a	47	45	43	41	39	37	35	33	31	29	27	25
2b	46	44	42	40	38	36	34	32	30	28	26	24
3a	48	50	52	54	56	58	60	62	64	66	68	70
3b	49	51	53	55	57	59	61	63	65	67	69	71
4a	95	93	91	89	87	85	83	81	79	77	75	73
4b	94	92	90	88	86	84	82	80	78	76	74	72
5a	96	98	100	102	104	106	108	110	112	114	116	118
5b	97	99	101	103	105	107	109	111	113	115	117	119
6a	143	141	139	137	135	133	131	129	127	125	123	121
6b	142	140	138	136	134	132	130	128	126	124	122	120
7a	144	146	148	150	152	154	156	158	160	162	164	166
7b	145	147	149	151	153	155	157	159	161	163	165	167
8a	191	189	187	185	183	181	179	177	175	173	171	169
8b	190	188	186	184	182	180	178	176	174	172	170	168
9a	192	194	196	198	200	202	204	206	208	210	212	214
9b	193	195	197	199	201	203	205	207	209	211	213	215
10a	239	237	235	233	231	229	227	225	223	221	219	217
10b	238	236	234	232	230	228	226	224	222	220	218	216
11a	240	242	244	246	248	250	252	254	256	258	260	262
11b	241	243	245	247	249	251	253	255	257	259	261	263
12a	287	285	283	281	279	277	275	273	271	269	267	265
12b	286	284	282	280	278	276	274	272	270	268	266	264
...	...	...	...	...	...	...	...	...	...	...	...	...
...	...	...	...	...	...	...	...	...	...	...	...	...
53a	1248	1250	1252	1254	1256	1258	1260	1262	1264	1266	1268	1270
53b	1249	1251	1253	1255	1257	1259	1261	1263	1265	1267	1269	1271

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Table 16. REMAPPING SCHEME FOR ONE ROW (continued)

timeslot	ch0	ch1	ch2	ch3	ch4	ch5	ch6	ch7	ch8	ch9	ch10	ch11
54a	1295	1293	1291	1289	1287	1285	1283	1281	1279	1277	1275	1273
54b	1294	1292	1290	1288	1286	1284	1282	1280	1278	1276	1274	1272
CRC												

Table 17. REMAPPING SCHEME FOR ONE ROW IN REVERSE X/Y READOUT MODE

Timeslot	ch0	ch1	ch2	ch3	ch4	ch5	ch6	ch7	ch8	ch9	ch10	ch11
54a	1295	1293	1291	1289	1287	1285	1283	1281	1279	1277	1275	1273
54b	1294	1292	1290	1288	1286	1284	1282	1280	1278	1276	1274	1272
53a	1248	1250	1252	1254	1256	1258	1260	1262	1264	1266	1268	1270
53b	1249	1251	1253	1255	1257	1259	1261	1263	1265	1267	1269	1271
...	...	...	...	...	...	...	...	...	...	...	...	...
...	...	...	...	...	...	...	...	...	...	...	...	...
2a	47	45	43	41	39	37	35	33	31	29	27	25
2b	46	44	42	40	38	36	34	32	30	28	26	24
1a	0	2	4	6	8	10	12	14	16	18	20	22
1b	1	3	5	7	9	11	13	15	17	19	21	23
CRC												

Table 18. REMAPPING SCHEME FOR ONE ROW IN COLOR SUBSAMPLING MODE

Timeslot	ch0	ch1	ch2	ch3	ch4	ch5	ch6	ch7	ch8	ch9	ch10	ch11
1a	0	45	4	41	8	37	12	33	16	29	20	25
1b	1	44	5	40	9	36	13	32	17	28	21	24
2a	48	93	52	89	56	85	60	81	64	77	68	73
2b	49	92	53	88	57	84	61	80	65	76	69	72
...	...	...	...	...	...	...	...	...	...	...	...	...
...	...	...	...	...	...	...	...	...	...	...	...	...
27a	1248	1293	1252	1289	1256	1285	1260	1281	1264	1277	1268	1273
27b	1249	1292	1253	1288	1257	1284	1261	1280	1265	1276	1269	1272
CRC												

Table 19. REMAPPING SCHEME FOR ONE ROW IN MONOCHROME SUBSAMPLING MODE

Timeslot	ch0	ch1	ch2	ch3	ch4	ch5	ch6	ch7	ch8	ch9	ch10	ch11
1a	0	2	4	6	8	10	12	14	16	18	20	22
1b	46	44	42	40	38	36	34	32	30	28	26	24
2a	48	50	52	54	56	58	60	62	64	66	68	70
2b	94	92	90	88	86	84	82	80	78	76	74	72
3a	96	98	100	102	104	106	108	110	112	114	116	118
3b	142	140	138	136	134	132	130	128	126	124	122	120
4a	144	146	148	150	152	154	156	158	160	162	164	166
...	...	...	...	...	...	...	...	...	...	...	...	...
...	...	...	...	...	...	...	...	...	...	...	...	...
27a	1248	1250	1252	1254	1256	1258	1260	1262	1264	1266	1268	1270

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Table 19. REMAPPING SCHEME FOR ONE ROW IN MONOCHROME SUBSAMPLING MODE (continued)

Timeslot	ch0	ch1	ch2	ch3	ch4	ch5	ch6	ch7	ch8	ch9	ch10	ch11
27b	1294	1292	1290	1288	1286	1284	1282	1280	1278	1276	1274	1272
CRC												

Single Window Mode Containing Timeslot 54

In this operation mode, only part of the sensor is read out, as shown by the shaded area in Figure 20. A clear distinction is made with the single window mode that does not contain the timeslot 54, because the output synchronization protocol is slightly different.

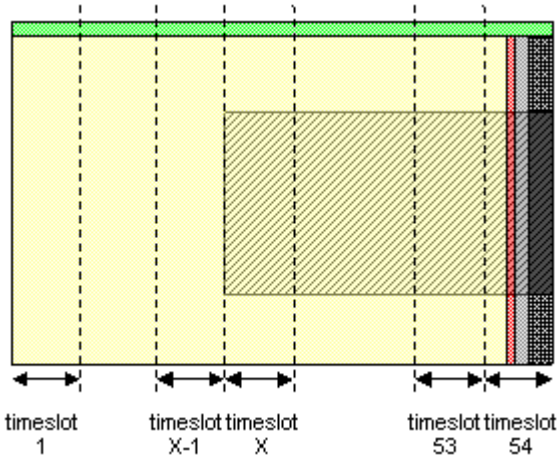


Figure 20. Single Window Containing Timeslot 54

Figure 21 shows the internal state of the sequencer, and the behavior of the data and sync channels (overview and detail of one line) for this window mode.

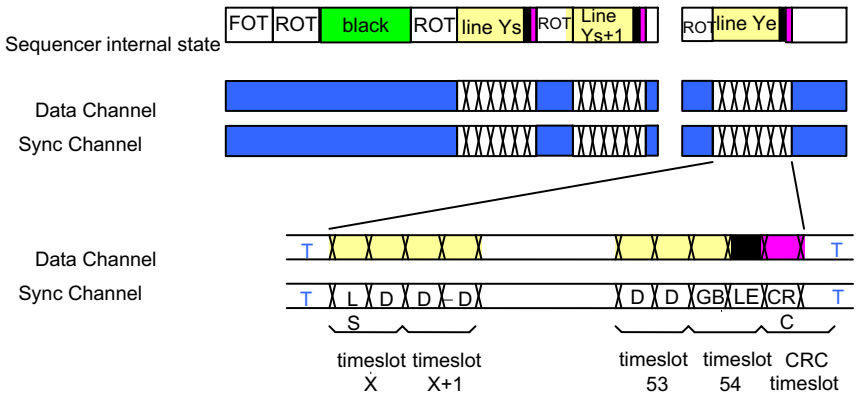


Figure 21. Waveform for Single Window Containing Timeslot 54

Single Window Mode Not Containing Timeslot 54

In this operation mode, only part of the sensor is read out, as shown in Figure 22. Although the window is defined as not containing any data from timeslot 54, it is read out to provide information on grey and black columns to the user.

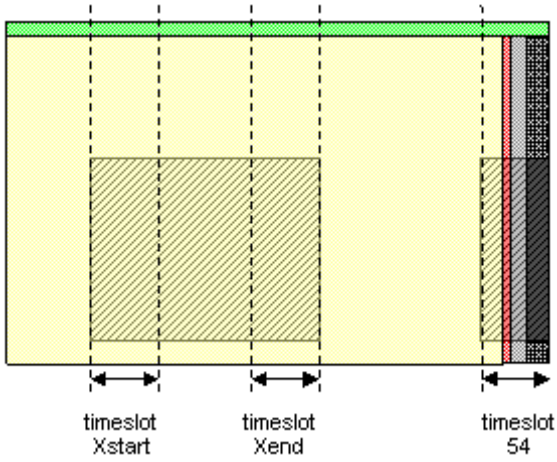


Figure 22. Single Window Not Containing Timeslot 54

Figure 23 shows the internal state of the sequencer, and the behavior of the data and sync channels (overview and detail of one line) for this window mode.

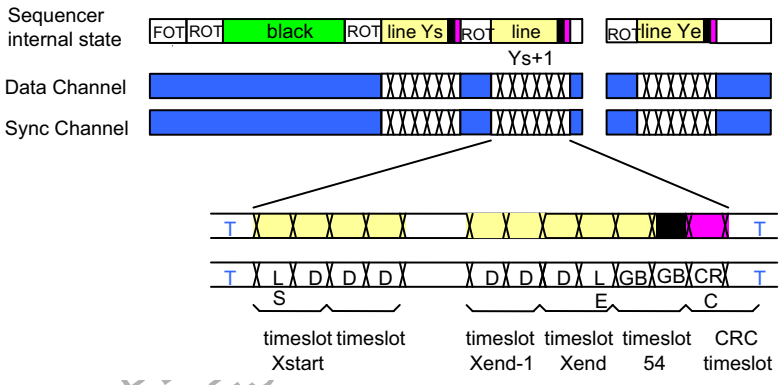


Figure 23. Waveform for Single Window NOT Containing Timeslot 54

Note that the dummy black line is read completely.

Reading out multiple windows does not differ from combining the windowed modes in sections Single Window Mode Containing Timeslot 54 on page 27 and Single Window Mode Not Containing Timeslot 54. The dummy black line again spans the entire width of the sensor and is processed only once, before all configured windows are read. The dummy black line is independent of the window sizes.

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ADDITIONAL FEATURES

Windowing

A fully configurable window can be selected for readout.

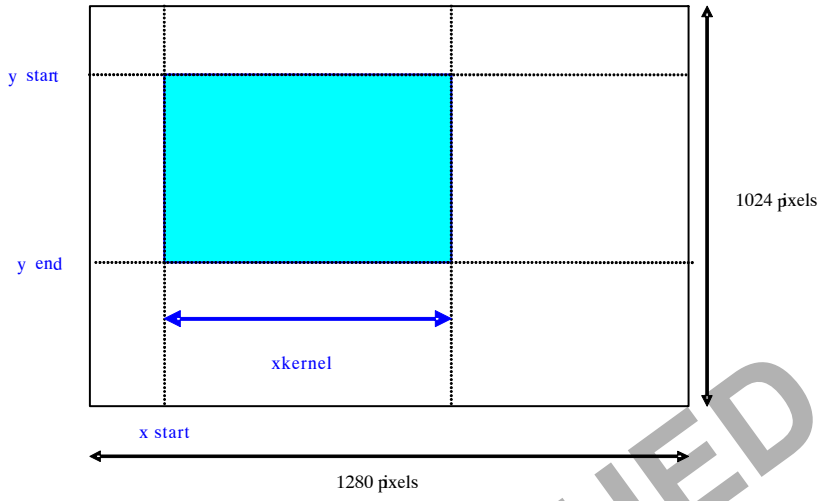


Figure 24. Window Selected for Readout

The parameters to configure this window are:

x_start. The sensor reads out 24 pixels in one single clock cycle. The granularity of configuring the X start position is also 24. Every value written to the windowX_2 register must be multiplied by 24 to find the corresponding column in the pixel array.

x_kernels. The number of columns that is read out (x_kernels*24 in full frame mode) in subsampling mode x_kernels*48 represents the number of columns over which subsampling is done. The x_kernels value must be written to the windowX_4 register.

y_start. The starting line of the readout window, granularity of 1. Note that in subsample mode, the correct y_start position must be uploaded (exact value depends on color or B/W subsampling mode). This value must be written to the windowX_1 and windowx_2 register.

y_end. The end line of the readout window, granularity of 1. In all cases (even in reverse scan), y_end are larger than y_start. Note that in subsample mode, the correct y_end position must be uploaded (exact value depends on color or B/W subsampling mode). This value must be written to the windowX_3 and windowX_4 register.

In case of windowing, the effective readout time is smaller than in full frame mode, because only the relevant part of the image array is accessed. As a result, it is possible to achieve higher frame rates.

Subsampling

Subsampling reduces resolution while maintaining the constant field of view and an increased frame rate. LUPA1300-2 supports monochrome and color subsampling modes of operation. The pixel order for one complete row is shown in Tables 18 and 19.

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Reverse Scan

Reverse scanning is supported in the X and Y direction. Line 0 (first line on the output) is the top line in normal mode and the bottom line in reverse scanning, as shown in Figure 24. As a result, the line numbers always increment. When reverse scanning in X, the operation is analogous. To enable reverse readout in X and Y, set the seqmode4[6:7] bits. In addition, the Y_start and X_start addresses must be changed to the new starting address.

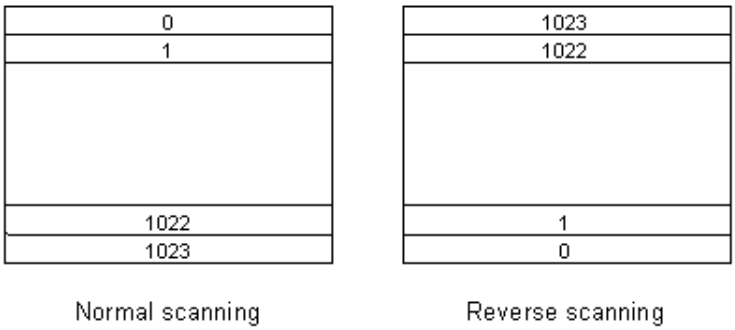


Figure 25. Normal and Reverse Scanning in Y

Multiple Windows

The sequencer supports the readout of four different windows, randomly positioned over the pixel array. The images are read out sequentially. That is, window 1 is read out before window 2, even if both windows show some overlap. Next, windows 3 and 4 are read out. Each window is treated as a frame and images are read out as shown in Figure 27. Also, the sum of readout times of all four windows should be less than or equal to the sum of reset time and integration time. (RTw1+RTw2+RTw3+RTw4) < (Reset time + Integration time). You can configure the number of windows used in the application (one to four). Figure 26 shows how to configure two windows spread over the image array.

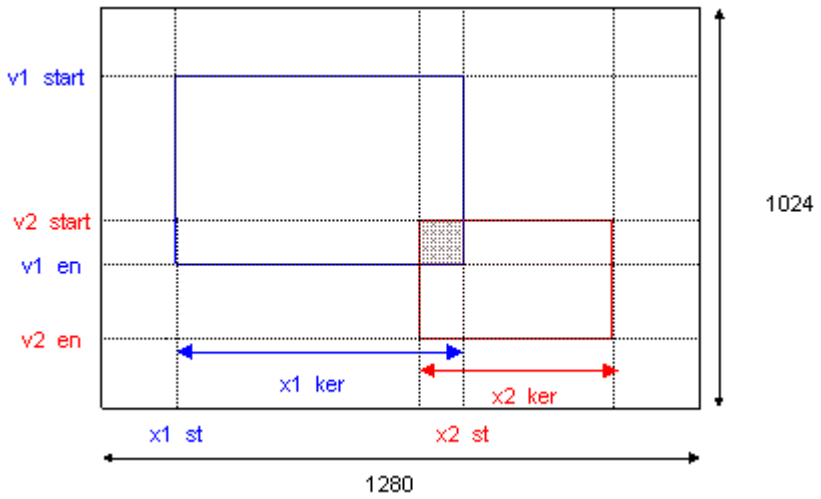


Figure 26. Multiple Windows Read from the Same Pixel Array

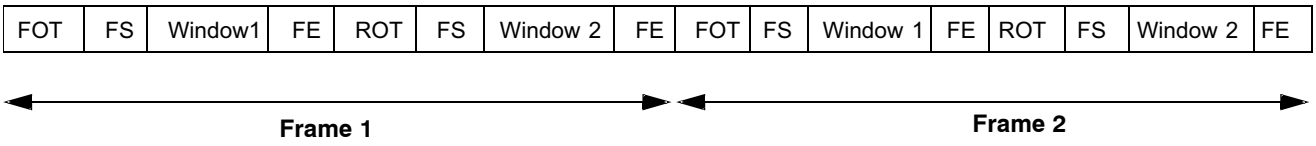


Figure 27. Readout from Windows

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Figure 28 shows the sequence of integration and read out for multiple windows. The handling of integration time is identical to the single window mode (except that in this case, the maximum integration time is equal to the sum of the y_widths of the two windows). Read out starts with a FOT that is similar to single window mode. After the FOT, all lines of window 1 are read, followed by the lines of window 2.

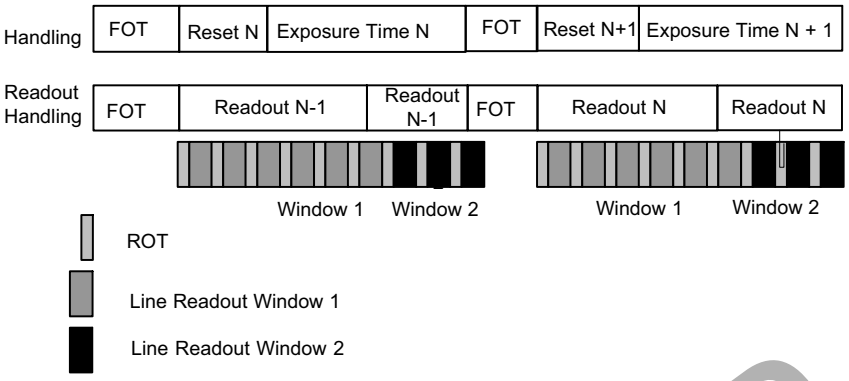


Figure 28. Exposure and Read Out of Multiple Windows

If the X size of the windows are not identical, the integration time in function of the number of lines read presents multiple slopes (proportional to the X size of these windows). Because this can cause confusion when programming the integration time, it is easier to configure all timer registers using the clock cycle configuration instead of the 'line' configuration.

Multiple Slopes

Dynamic range can be extended by the multiple slope capabilities of the sensor. The four colored lines in Figure 29 represent analog signals of the photodiode of four pixels, which decrease as a result of exposure. The slope is determined by the amount of light at each pixel (the more light, the steeper the slope). When the pixels reach the saturation level, the analog does not change despite further exposure. Without the multiple slope capabilities, the pixels p3 and p4 are saturated before the end of the exposure time, and no signal is received. However, when using multiple slopes, the analog signal is reset to a second or third reset level (lower than the original) before the integration time ends. The analog signal starts decreasing with the same slope as before, and pixels that were saturated before could be nonsaturated at read out time. For pixels that never reach any of the reset levels (for example, p1 and p2) there is no difference between single and multiple slope operation.

By choosing the time stamps of the double and triple slope resets (typical at 90% and 99% of the integration, configurable by the user), it is possible to have a nonsaturated pixel value even for pixels that receive a huge amount of light.

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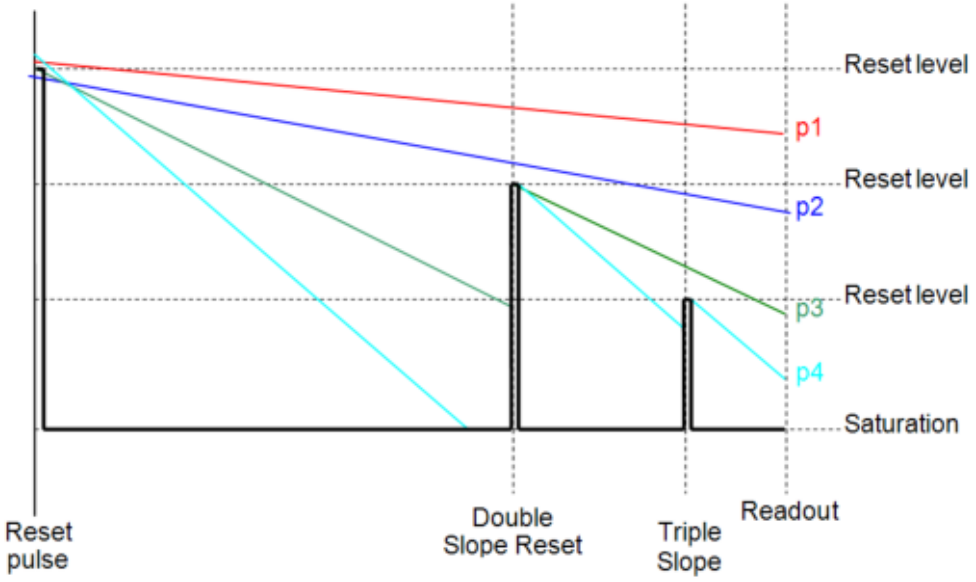


Figure 29. Dynamic Range Extended by Multiple Slope Capability

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The reset levels are configured through external (power) pins. In master mode, the time stamps of the double and triple slope resets are configured in a method similar to configuring the exposure time. The time stamps are enabled through the registers seqmode1[5] and seqmode1[6], and their values are expressed in line or clock cycles in the registers reg_tint_ds_timer and reg_tint_ts_timer.

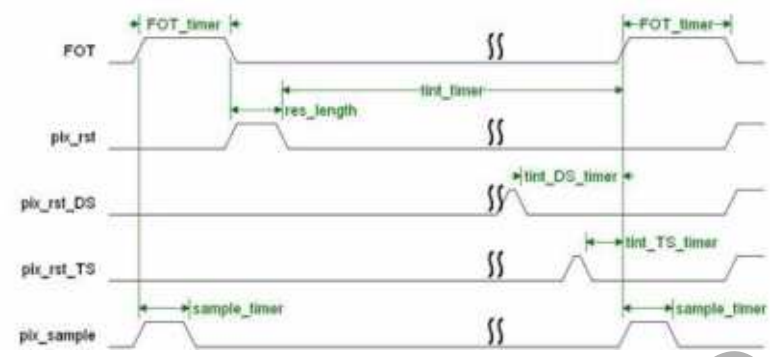


Figure 30. Triple Slope Timing in Master Mode

In slave mode, the values of res_length, tint_timer, tint_DS_timer, and tint_TS_timer in the configuration registers are ignored. You have full control through the pins int_time, int_time_ds, and int_time_ts. You must configure the multiple slope parameters for the application and interpret the pixel data accordingly.

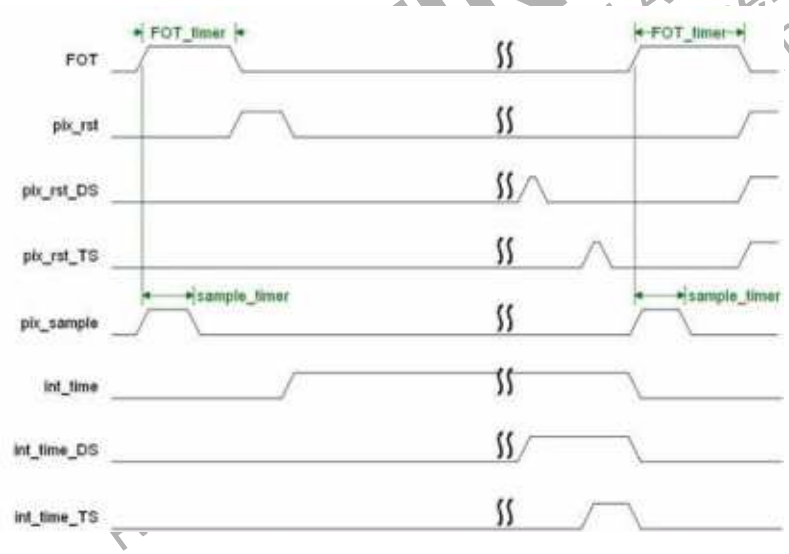


Figure 31. Triple Slope Timing in Slave Mode

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Column FPN Correction

The column FPN of the sensor is improved by the offset correction of the columns. At the start of every frame, before read out of the actual lines is done, a fixed voltage is applied at the columns and these values are read out like a real data line. Inside the data block, the 'pixel' data for that line is stored in an on-chip FPN memory. When the correction is enabled, the corresponding FPN value is subtracted from the incoming pixel data.

This FPN correction must be enabled for every output separately. The registers used to configure the correction are:

- **datachannelX_1 with X from 0 to 11.** The field [1] of these registers enables the offset corrections of the specific output channel.

NOTE: Do not change the settings of datachannel12_1. This channel contains synchronization data, not pixel data. If fpn correction is enabled on this channel, the synchronization data becomes corrupt.

- **seqmode3.** The field[2] must be '1'. It enables the generation of the line of reference voltages at the columns.

Figures 32 and 33 show the effect of enabling the column FPN correction. These images are magnified up to five times.

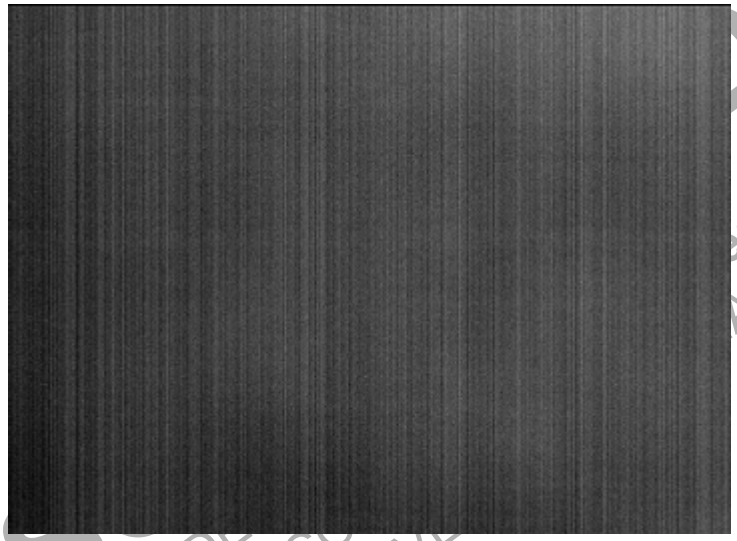


Figure 32. Dark Image Without FPN Correction (5x Amplified)

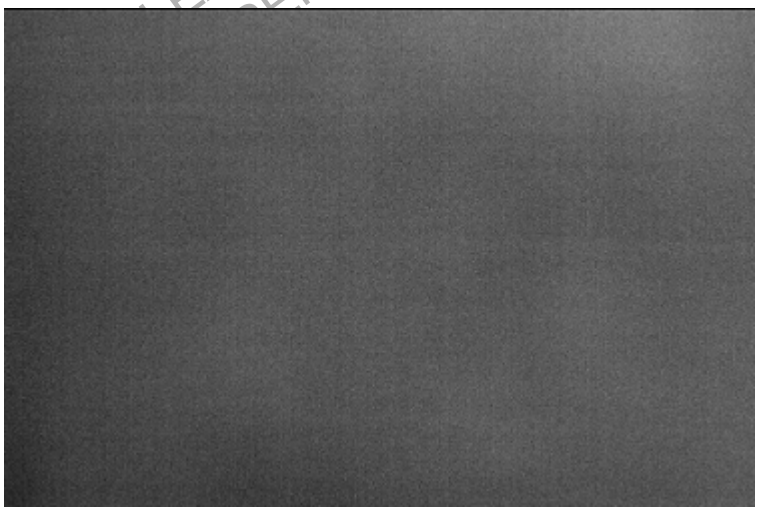


Figure 33. Dark Image With FPN Correction Enabled (5x Amplified)

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Full Frame Mode

In this operation mode, the entire sensor shown in Figure 18 is read out. Figure 34 shows the internal state of the sequencer, and the behavior of the data and sync channels (overview and detail of one line).

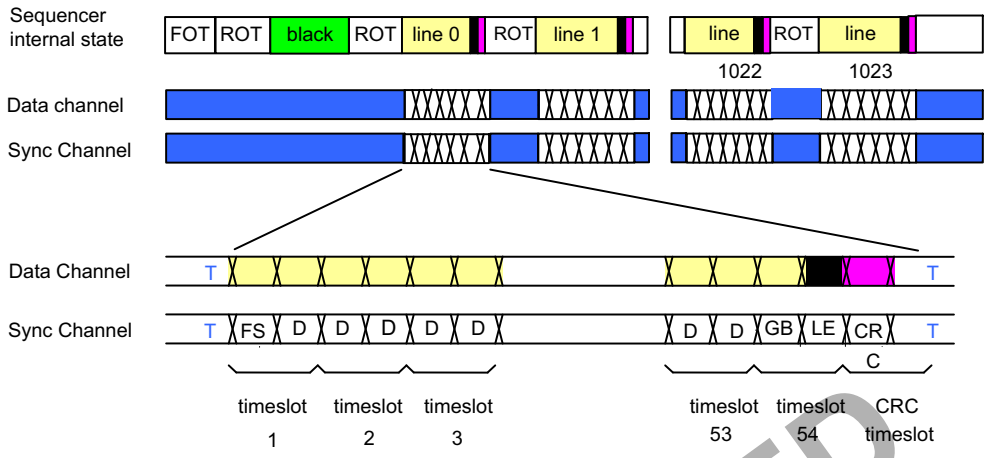
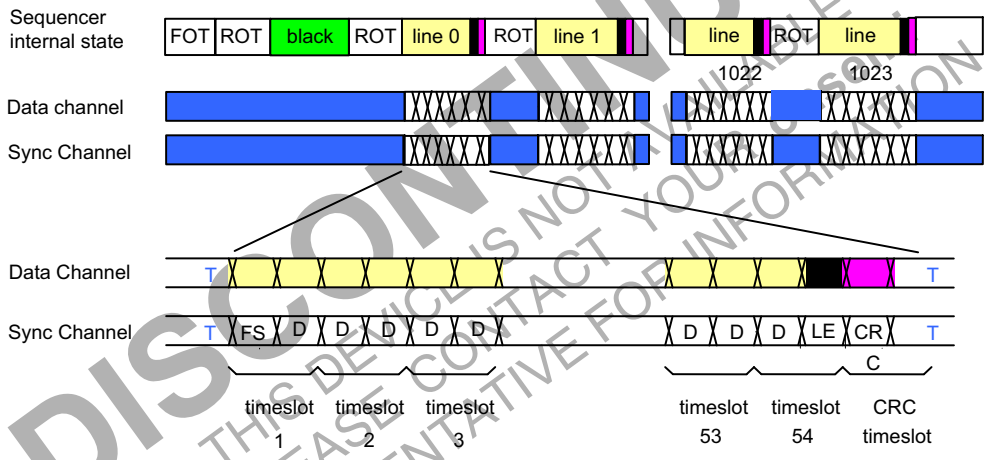


Figure 34. Full Frame Mode Readout



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Figure 35. Full Frame Mode Readout with On Chip Black Level Calibration Disabled

Off Chip Automatic Black Level Calibration

The last time slot not only contains valid pixels but also two dummy columns, six grey columns, and eight black columns. The grey column values are used to perform off chip black level calibration to maintain a constant black level against any type of drift. These values gauge the response of normal pixels in the dark conditions.

Grey columns are generated by applying a minimal integration time (black timer register) to the columns. Black columns share the same minimal integration time; additionally, the pixels in that column are shielded. Grey columns can be used if the integration time is large compared to the minimal integration time. Black columns are used if the integration time is in the same order of magnitude as the minimal integration time.

The procedure is as follows:

1. Decide what digital code should be the desired black level. 0x00 cannot be chosen to avoid underflow in FPN correction.
2. Set the sensor to safe settings; DACVREFADC must be on a value that never clips the grey (or black) columns.

- Make sure that the grey (or black) columns can be read out without clipping.
- Make sure that this is the case for every sensor including dc-shifts due to Vt and temperature differences.

3. Read-out the grey (or black) columns.

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4. Calculate the average value of this grey (or black) data; also average it out over the different grey columns.
5. Adapt the DACVREFADC if the calculated value deviate from the desired black level value and return to step (2).
6. Repeat the procedure for temperature changes.

PACKAGE

Pin List

Table 20. PIN PLACEMENT LAYOUT (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
A	134	130	127	124	121	118	115	112	109	106	103	100	99	96	93	90	87	84	81	78	75	72	69	65
B	*	131	128	125	122	119	116	113	110	107	104	101	98	95	92	89	86	83	80	77	74	71	68	*
C	133	132	129	126	123	120	117	114	111	108	105	102	97	94	91	88	85	82	79	76	73	70	67	66
D																								
E																								
F																								
G																								
H																								
J																								
K									TOP VIEW															
L																								
M																								
N																								
P																								
Q																								
R																								
S																								
T	135	139	140	137	145	*	5	7	*	17	19	*	*	31	29	*	43	41	*	54	62	60	59	64
U	136	144	141	138	146	*	8	6	*	20	18	*	*	30	32	*	42	44	*	53	61	55	58	63
V	149	147	142	*	1	3	9	11	13	15	21	23	25	27	33	35	37	39	45	47	*	52	57	50
W	150	148	143	*	2	4	10	12	14	16	22	24	26	28	34	36	38	40	46	48	*	51	56	49

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Table 21. PIN LIST

Pin No.	Pin Name	Type	Direction	Description	Position
1	clkoutp	LVDS	O	p clk output channel	V5
2	clkoutn	LVDS	O	n clk output channel	W5
3	chp[0]	LVDS	O	p output channel [0]	V6
4	chn[0]	LVDS	O	n output channel [0]	W6
5	gndlvds	Supply	I/O	LVDS ground	T7
6	gndadc	Supply	I/O	ADC ground	U8
7	vddadc	Supply	I/O	ADC power	T8
8	vddlvds	Supply	I/O	LVDS power	U7
9	chp[1]	LVDS	O	p output channel [1]	V7
10	chn[1]	LVDS	O	n output channel [1]	W7
11	chp[2]	LVDS	O	p output channel [2]	V8
12	chn[2]	LVDS	O	n output channel [2]	W8
13	chp[3]	LVDS	O	p output channel [3]	V9
14	chn[3]	LVDS	O	n output channel [3]	W9
15	chp[4]	LVDS	O	p output channel [4]	V10
16	chn[4]	LVDS	O	n output channel [4]	W10
17	gndlvds	Supply	I/O	LVDS ground	T10
18	gndadc	Supply	I/O	ADC ground	U11
19	vddadc	Supply	I/O	ADC power	T11
20	vddlvds	Supply	I/O	LVDS power	U10
21	chp[5]	LVDS	O	p output channel [5]	V11
22	chn[5]	LVDS	O	n output channel [5]	W11
23	chp[6]	LVDS	O	p output channel [6]	V12
24	chn[6]	LVDS	O	n output channel [6]	W12
25	chp[7]	LVDS	O	p output channel [7]	V13
26	chn[7]	LVDS	O	n output channel [7]	W13
27	chp[8]	LVDS	O	p output channel [8]	V14
28	chn[8]	LVDS	O	n output channel [8]	W14
29	gndlvds	Supply	I/O	LVDS ground	T15
30	gndadc	Supply	I/O	ADC ground	U14
31	vddadc	Supply	I/O	ADC power	T14
32	vddlvds	Supply	I/O	LVDS power	U15
33	chp[9]	LVDS	O	p output channel [9]	V15
34	chn[9]	LVDS	O	n output channel [9]	W15
35	chp[10]	LVDS	O	p output channel [10]	V16
36	chn[10]	LVDS	O	n output channel [10]	W16
37	chp[11]	LVDS	O	p output channel [11]	V17
38	chn[11]	LVDS	O	n output channel [11]	W17
39	n/a			not assigned	V18
40	n/a			not assigned	W18
41	gndlvds	Supply	I/O	LVDS ground	T18

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Table 21. PIN LIST (continued)

Pin No.	Pin Name	Type	Direction	Description	Position
42	gndadc	Supply	I/O	ADC ground	U17
43	vddadc	Supply	I/O	ADC power	T17
44	vddlvds	Supply	I/O	LVDS power	U18
45	clkinp	LVDS	I	LVDS input clock 315 MHz p-node	V19
46	clkinn	LVDS	I	LVDS input clock 315 MHz n-node	W19
47	syncp	LVDS	O	LVDS sync and output	V20
48	syncn	LVDS	O	LVDS sync and output	W20
49	gnddig	Supply	I/O	digital ground	W24
50	vdddig	Supply	I/O	digital power supply	V24
51	cap_vrefm	Analog	O	lower limit ADC range decoupling	W22
52	cap_vrefp	Analog	O	higher limit ADC range decoupling	V22
53	gndadc	Supply	I/O	ADC ground	U20
54	vddadc	Supply	I/O	ADC power supply	T20
55	gnddig	Supply	I/O	digital ground	U22
56	gndbuf	Supply	I/O	column buffers ground	W23
57	vddbuf	Supply	I/O	column buffers supply	V23
58	gndana	Supply	I/O	column buffers ground	U23
59	vddana	Supply	I/O	column buffers supply	T23
60	vpix	Supply	I/O	pixel core supply	T22
61	gndpix	Supply	I/O	pixel core ground	U21
62	vsamp	Supply	I/O	image core select and sample supply	T21
63	gndadc	Supply	I/O	ADC ground	U24
64	vdddig	Supply	I/O	digital power supply	T24
65	nbias_colload	Analog	O	column bias decouple	A24
66	test_ena	CMOS	I	scan pin for sequencer; Customer: connect to ground	C24
67	int_time1	CMOS	I	integration pin first slope	C23
68	int_time2	CMOS	I	integration pin dual slope	B23
69	int_time3	CMOS	I	integration pin triple slope	A23
70	monitor1	CMOS	O	output pin for integration timing, high during integration	C22
71	monitor2	CMOS	O	output pin for dual slope integration timing, high during integration	B22
72	monitor3	CMOS	O	output pin for triple slope integration timing, high during integration	A22
73	cap_vrefadc	Analog	O	ADC black reference decoupling	C21
74	vpix	Supply	I/O	pixel core supply	B21
75	cap_vrefcm	Analog	O	ADC common mode decoupling	A21
76	reset_n	CMOS	I/O	chip reset (active low)	C20
77	scan_en	CMOS	I	DFT scan enable; Customer: connect to ground	B20
78	scan_clk	CMOS	I	DFT clock; Customer: connect to ground	A20
79	scan_clk_en	CMOS	I	DFT clock enable; Customer: connect to ground	C19
80	gndpix	Supply	I/O	pixel core ground	B19
81	gnddig	Supply	I/O	digital ground	A19

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Table 21. PIN LIST (continued)

Pin No.	Pin Name	Type	Direction	Description	Position
82	vdddig	Supply	I/O	digital power supply	C18
83	vpix	Supply	I/O	pixel core supply	B18
84	pixdiode	Analog	O	pixel diode current pin; Customer: keep it floating	A18
85	gndpix	Supply	I/O	pixel core ground	C17
86	vsamp	Supply	I/O	image core select and sample supply	B17
87	vresetab	Supply	I/O	anti blooming lower reset level	A17
88	vprech	Supply	I/O	pixel precharge level/decoupling pin	C16
89	vmemh	Supply	I/O	pixel memory reference high	B16
90	vmeml	Supply	I/O	pixel memory reference low	A16
91	vreset	Supply	I/O	pixel reset level	C15
92	vresetds	Supply	I/O	pixel dual slope reset level/decoupling pin	B15
93	vresetts	Supply	I/O	pixel triple slope reset level/decoupling pin	A15
94	vresetab	Supply	I/O	anti blooming lower reset level	C14
95	gndpix	Supply	I/O	pixel core ground	B14
96	vresetts	Supply	I/O	pixel triple slope reset level/decoupling pin	A14
97	vresetds	Supply	I/O	pixel dual slope reset level/decoupling pin	C13
98	vreset	Supply	I/O	pixel reset level	B13
99	vsamp	Supply	I/O	image core select and sample supply	A13
100	vmeml	Supply	I/O	pixel memory reference low	A12
101	vmemh	Supply	I/O	pixel memory reference high	B12
102	vprech	Supply	I/O	pixel precharge level/decoupling pin	C12
103	n/a			not assigned	A11
104	gndpix	Supply	I/O	pixel core ground	B11
105	vresetab	Supply	I/O	anti blooming lower reset level	C11
106	vresetts	Supply	I/O	pixel triple slope reset level/decoupling pin	A10
107	vresetds	Supply	I/O	pixel dual slope reset level/decoupling pin	B10
108	vreset	Supply	I/O	pixel reset level	C10
109	vmeml	Supply	I/O	pixel memory reference low	A9
110	vmemh	Supply	I/O	pixel memory reference high	B9
111	vprech	Supply	I/O	pixel precharge level/decoupling pin	C9
112	vresetab	Supply	I/O	anti blooming lower reset level	A8
113	vsamp	Supply	I/O	image core select and sample supply	B8
114	gndpix	Supply	I/O	pixel core ground	C8
115	ibiaspre	Analog	I	external current bias for vprech (not connected by default); Customer: connect with 0.1 μf to ground	A7
116	vpix	Supply	I/O	pixel core supply	B7
117	vdddig	Supply	I/O	digital power supply	C7
118	gnddig	Supply	I/O	digital ground	A6
119	gndpix	Supply	I/O	pixel core ground	B6
120	n/a			not assigned	C6
121	n/a			not assigned	A5

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Table 21. PIN LIST (continued)

Pin No.	Pin Name	Type	Direction	Description	Position
122	n/a			not assigned	B5
123	n/a			not assigned	C5
124	cap_vrefcm	Analog	O	ADC common mode decoupling	A4
125	vpix	Supply	I/O	pixel core supply	B4
126	cap_vrefadc	Analog	O	ADC black reference decoupling	C4
127	spics	CMOS	I	SPI chip select	A3
128	spiclk	CMOS	I	SPI clock	B3
129	spiin	CMOS	I	SPI serial input	C3
130	spiout	CMOS	O	SPI serial output	A2
131	mbsbus[0]	Analog	I/O	first mixed boundary scan bus; Customer: keep it floating	B2
132	mbsbus[1]	Analog	I/O	second mixed boundary scan bus; Customer: keep it floating	C2
133	refbg	Analog	I/O	external bias resistor; Customer: connect with 47 kΩ to ground	C1
134	cmdmbs	Analog	I	bias current for mbs buffers; Customer: connect with 0.1 µf to ground	A1
135	vdddig	Supply	I/O	digital power supply	T1
136	gndadc	Supply	I/O	ADC ground	U1
137	vsamp	Supply	I/O	image core select and sample supply	T4
138	gndpix	Supply	I/O	pixel core ground	U4
139	vpix	Supply	I/O	pixel core supply	T2
140	vddana	Supply	I/O	analog power supply	T3
141	gndana	Supply	I/O	analog ground	U3
142	vddbuf	Supply	I/O	column buffers supply	V3
143	gndbuf	Supply	I/O	column buffers ground	W3
144	gnddig	Supply	I/O	digital ground	U2
145	vddadc	Supply	I/O	ADC power supply	T5
146	gndadc	Supply	I/O	ADC ground	U5
147	cap_vrefp	Analog	I/O	higher limit ADC range decoupling	V2
148	cap_vrefm	Analog	I/O	lower limit ADC range decoupling	W2
149	vdddig	Supply	I/O	digital power supply	V1
150	gnddig	Supply	I/O	digital ground	W1

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Table 22. MECHANICAL SPECIFICATIONS

Parameter	Description	Min	Typ	Max	Unit
Die (Pin 1 is located bottom left)	Die thickness	NA	750	NA	μm
	Die position, X offset to the package center	NA	-42	NA	μm
	Die position, Y offset to the package center	NA	-150	NA	μm
	Die position, X tilt	-1	0	1	deg
	Die position, Y tilt	-1	0	1	deg
	Die placement accuracy in package	-50	0	50	μm
	Die rotation accuracy	-1	0	1	deg
	Optical center referenced from the die center (X-dir)	NA	-121	NA	μm
	Optical center referenced from the die center (Y-dir)	NA	+2280	NA	μm
	Distance from PCB plane to top of the die surface	NA	1.75	NA	mm
	Distance from top of the die surface to top of the glass lid	NA	1.15	NA	mm
Glass Lid	XY size	NA	27.4 x 27.4	NA	mm
	Thickness	NA	0.9	NA	mm
	Spectral range for optical coating of window	400	-	1100	nm
	Reflection coefficient for window (refer to Figure 36)	NA	<0.8	NA	%
Mechanical Shock	JESD22-B104C; Condition G	NA	2000	NA	G
Vibration	JESD22-B103B; Condition 1	20	-	2000	Hz
Mounting Profile	Pb-free wave soldering profile for pin grid array package if no socket is used				
Recommended Socket Manufacturer	Andon Electronics (www.andonelectronics.com)	BGA Socket: 10-24-05-168-319T-P27-L14			
		Thru Hole: 10-24-05-168-347T-P27-L14			

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Glass Lid

The LUPA1300-2 monochrome and color image sensor uses a glass lid without any coatings. Figure 36 shows the transmission characteristics of the glass lid.

As shown in Figure 36, no infrared attenuating color filter glass is used. A filter must be provided in the optical path when color devices are used
(source: http://www.pgo−online.com).

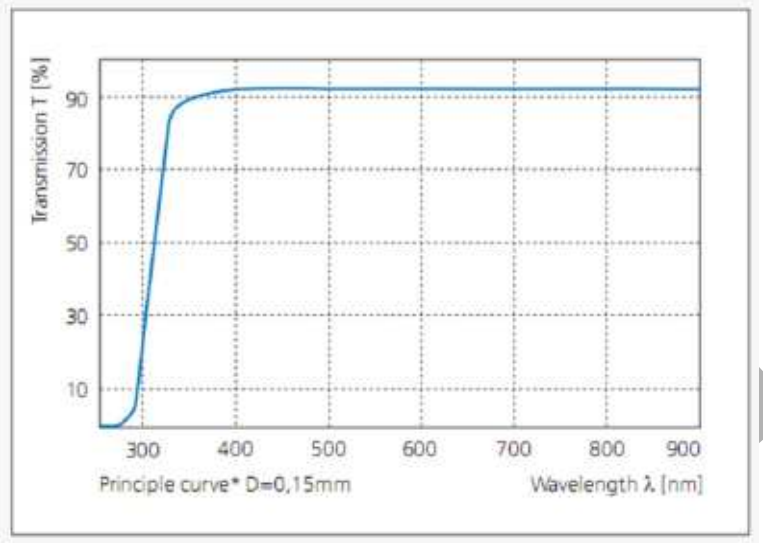


Figure 36. Transmission Characteristics of the Glass Lid

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SPECIFICATIONS AND USEFUL REFERENCES

Specifications, Application Notes and useful resources can be accessed via customer login account at MyON − CISP Extranet.
https://www.onsemi.com/PowerSolutions/myon/erCispFolder.do

Useful References

For information on ESD and cover glass care and cleanliness, please download the *Image Sensor Handling and Best Practices* Application Note (AN52561/D) from www.onsemi.com.

For quality and reliability information, please download the *Quality & Reliability* Handbook (HBD851/D) from www.onsemi.com.

For information on Standard terms and Conditions of Sale, please download Terms and Conditions from www.onsemi.com.

Product Application Notes

- AN54468: Interfacing the LUPA1300-2 with FPGA

This application note describes the interface between the LUPA1300-2 and the FPGA, as implemented in the LUPA1300-2 demonstration kit. It also provides an overview of the architecture of the demonstration kit and the method used to synchronize channels.

- AN54214: High Speed Layout Guidelines for the LUPA1300-2 Image Sensor
- AN54598: Pixel Remapping Implementation in LUPA1300-2 Demonstration Kit

This application note explains the remapping technique implemented in LUPA1300-2 demonstration system to align non consecutive pixels readout to consecutive pixels for creating proper images. It also describes the remapping method during Reverse-X/Y readout and subsampling modes of operation.

Acceptance Criteria Specification

The Product Acceptance Criteria is available on request. This document contains the criteria to which the LUPA1300-2 is tested before being shipped.

Return Material Authorization (RMA)

Refer to the **onsemi** RMA policy procedure at http://www.onsemi.com/site/pdf/CAT_Returns_FailureAnalysis.pdf

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ACRONYMS

Acronym	Description
ADC	Analog-to-Digital Converter
AFE	Analog Front End
BL	Black pixel data
CDM	Charged Device Model
CDS	Correlated Double Sampling
CMOS	Complementary Metal Oxide Semiconductor
CRC	Cyclic Redundancy Check
DAC	Digital-to-Analog Converter
DDR	Double Data Rate
DNL	Differential Non-Linearity
DS	Double Sampling
DSNU	Dark Signal Non-Uniformity
EIA	Electronic Industries Alliance
ESD	Electrostatic Discharge
FE	Frame End
FF	Fill Factor
FOT	Frame Overhead Time
FPGA	Field Programmable Gate Array
FPN	Fixed Pattern Noise
FPS	Frames per Second
FS	Frame Start
HBM	Human Body Model
IMG	Image data (regular pixel data)
INL	Integral Non-Linearity

Acronym	Description
IP	Intellectual Property
LE	Line End
LS	Line Start
LSB	Least Significant Bit
LVDS	Low-Voltage Differential Signaling
MSB	Most Significant Bit
PGA	Programmable Gain Amplifier
PLS	Parasitic Light Sensitivity
PRBS	Pseudo-Random Binary Sequence
PRNU	Pixel Random Non-Uniformity
QE	Quantum Efficiency
RGB	Red-Green-Blue
RMA	Return Material Authorization
RMS	Root Mean Square
ROI	Region of Interest
ROT	Row Overhead Time
S/H	Sample and Hold
SNR	Signal-to-Noise Ratio
SPI	Serial Peripheral Interface
TIA	Telecommunications Industry Association
T_J	Junction Temperature
TR	Training Pattern
% RH	Percent Relative Humidity

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GLOSSARY

conversion gain	A constant that converts the number of electrons collected by a pixel into the voltage swing of the pixel. Conversion gain = q/C where q is the charge of an electron (1.602E 19 Coulomb) and C is the capacitance of the photodiode or sense node.
CDS	Correlated double sampling. This is a method for sampling a pixel where the pixel voltage after reset is sampled and subtracted from the voltage after exposure to light.
CFA	Color filter array. The materials deposited on top of pixels that selectively transmit color.
DNL	Differential nonlinearity (for ADCs)
DSNU	Dark signal nonuniformity. This parameter characterizes the degree of nonuniformity in dark leakage currents, which can be a major source of fixed pattern noise.
fill-factor	A parameter that characterizes the optically active percentage of a pixel. In theory, it is the ratio of the actual QE of a pixel divided by the QE of a photodiode of equal area. In practice, it is never measured.
INL	Integral nonlinearity (for ADCs)
IR	Infrared. IR light has wavelengths in the approximate range 750 nm to 1 mm.
Lux	Photometric unit of luminance (at 550 nm, 1lux = 1 lumen/m^2 = 1/683 W/m^2)
pixel noise	Variation of pixel signals within a region of interest (ROI). The ROI typically is a rectangular portion of the pixel array and may be limited to a single color plane.
photometric units	Units for light measurement that take into account human physiology.
PLS	Parasitic light sensitivity. Parasitic discharge of sampled information in pixels that have storage nodes.
PRNU	Photo-response nonuniformity. This parameter characterizes the spread in response of pixels, which is a source of FPN under illumination.
QE	Quantum efficiency. This parameter characterizes the effectiveness of a pixel in capturing photons and converting them into electrons. It is photon wavelength and pixel color dependent.
read noise	Noise associated with all circuitry that measures and converts the voltage on a sense node or photodiode into an output signal.
reset	The process by which a pixel photodiode or sense node is cleared of electrons. "Soft" reset occurs when the reset transistor is operated below the threshold. "Hard" reset occurs when the reset transistor is operated above threshold.
reset noise	Noise due to variation in the reset level of a pixel. In 3T pixel designs, this noise has a component (in units of volts) proportionality constant depending on how the pixel is reset (such as hard and soft). In 4T pixel designs, reset noise can be removed with CDS.
responsivity	The standard measure of photodiode performance (regardless of whether it is in an imager or not). Units are typically A/W and are dependent on the incident light wavelength. Note that responsivity and sensitivity are used interchangeably in image sensor characterization literature so it is best to check the units.
ROI	Region of interest. The area within a pixel array chosen to characterize noise, signal, crosstalk, and so on. The ROI can be the entire array or a small subsection; it can be confined to a single color plane.
sense node	In 4T pixel designs, a capacitor used to convert charge into voltage. In 3T pixel designs it is the photodiode itself.
sensitivity	A measure of pixel performance that characterizes the rise of the photodiode or sense node signal in Volts upon illumination with light. Units are typically V/(W/m^2)/sec and are dependent on the incident light wavelength. Sensitivity measurements are often taken with 550 nm incident light. At this wavelength, 1 683 lux is equal to 1 W/m^2; the units of sensitivity are quoted in V/lux/sec. Note that responsivity and sensitivity are used interchangeably in image sensor characterization literature so it is best to check the units.
spectral response	The photon wavelength dependence of sensitivity or responsivity.
SNR	Signal-to-noise ratio. This number characterizes the ratio of the fundamental signal to the noise spectrum up to half the Nyquist frequency.
temporal noise	Noise that varies from frame to frame. In a video stream, temporal noise is visible as twinkling pixels.

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REVISION HISTORY

Revision	Description of Changes	Date
12	Rebranded the Data Sheet to **onsemi** format. NOIL2SC1300A−GDC, NOIL2SM1300A−GWC OPNs Marked as Discontinued.	10/23/2025
13	Document Discontinued.	8/17/2026

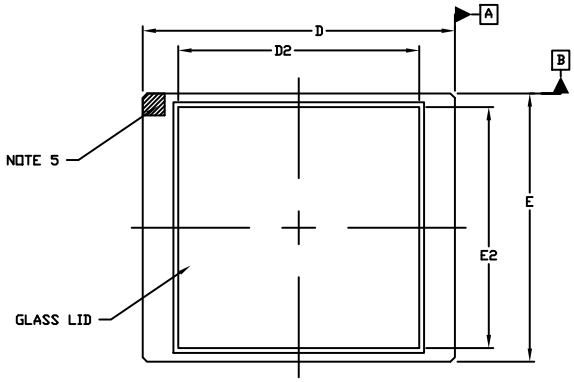
This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

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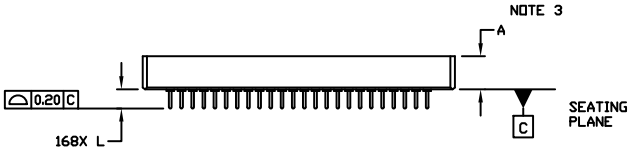
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CASE 107DH
ISSUE O

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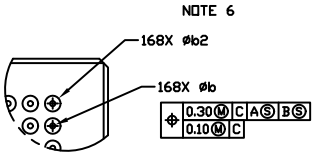
TOP VIEW



SIDE VIEW

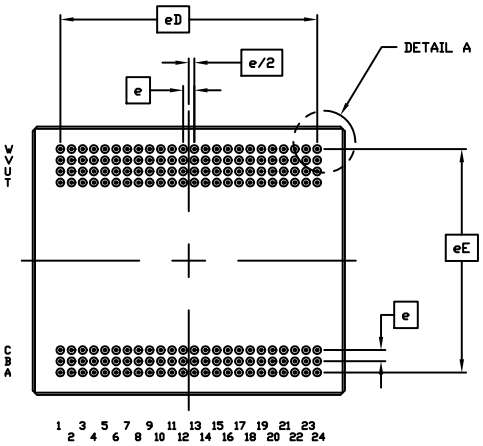
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION A INCLUDES THE PACKAGE BODY AND LID BUT DOES NOT INCLUDE HEATSINKS OR OTHER ATTACHED FEATURES.
4. DIMENSIONS D AND E DO NOT INCLUDE PROTRUSIONS. SUCH PROTRUSIONS SHALL NOT EXTEND MORE THAN 0.08 ON ANY SIDE. CORNERS AND EDGES OF THE PACKAGE MAY HAVE CHAMFERS.
5. PIN A1 IDENTIFICATION WILL BE IN THIS AREA. ID TYPE MAY CONSIST OF NOTCHES, METALLIZED MARKINGS, OR OTHER FEATURES.
6. THIS DIMENSION DEFINES THE MAXIMUM SIZE FOR THE PIN BRAZE PADS.



DETAIL A
2X SCALE

DIM	MILLIMETERS MIN.	MAX.
A	3.37	4.13
b	0.25	0.35
b2	---	0.95
D	35.14	35.86
D2	27.40 REF	
E	30.19	30.81
E2	27.40 REF	
e	1.27 BSC	
eD	29.21 BSC	
eE	25.40 BSC	
L	1.83	2.23



BOTTOM VIEW

GENERIC MARKING
DIAGRAM ON PAGE 2

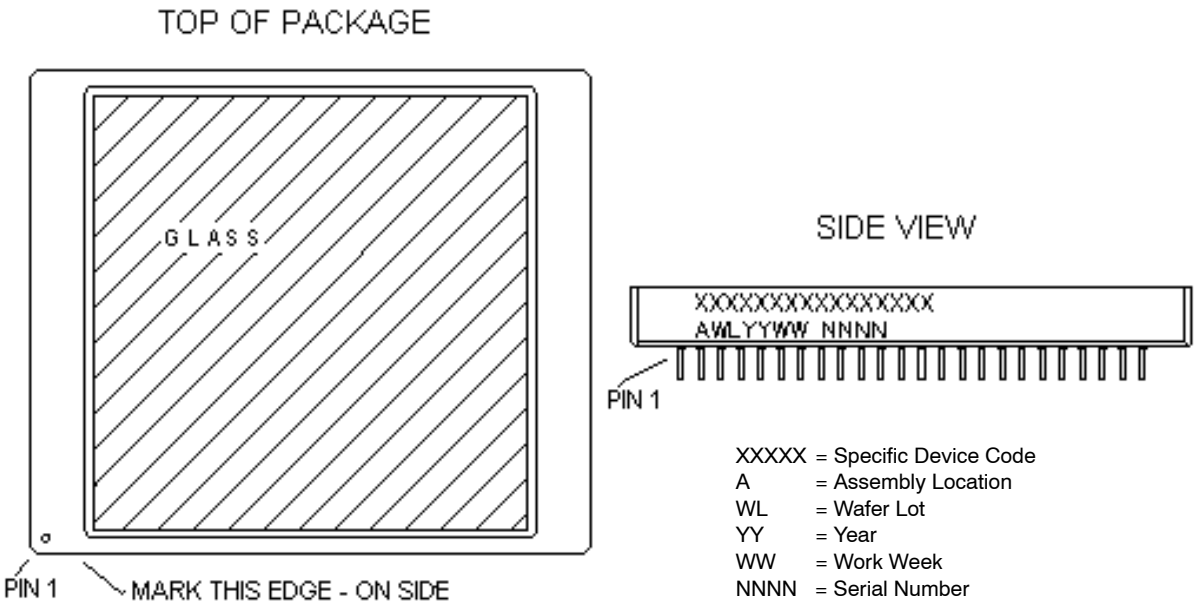
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CPGA168, 35.50x30.50
CASE 107DH
ISSUE O

DATE 30 JUN 2011

GENERIC
MARKING DIAGRAM



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
NNNN = Serial Number

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