# NTD5406N, STD5406N

# Power MOSFET
## 40 V, 70 A, Single N−Channel, DPAK

### Features
- Low $R_{DS(on)}$
- High Current Capability
- Low Gate Charge
- STD Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

### Applications
- Electronic Brake Systems
- Electronic Power Steering
- Bridge Circuits

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise stated)

| Parameter | | | Symbol | Value | Unit |
|---|---|---|---|---|---|
| Drain−to−Source Voltage | | | $V_{DSS}$ | 40 | V |
| Gate−to−Source Voltage | | | $V_{GS}$ | ±20 | V |
| Continuous Drain Current − $R_{\theta JC}$ | Steady State | $T_C$ = 25°C | $I_D$ | 70 | A |
| | | $T_C$ = 125°C | | 40 | |
| Power Dissipation − $R_{\theta JC}$ | Steady State | $T_C$ = 25°C | $P_D$ | 100 | W |
| Continuous Drain Current − $R_{\theta JA}$ (Note 1) | Steady State | $T_A$ = 25°C | $I_D$ | 12.2 | A |
| | | $T_A$ = 125°C | | 7.0 | |
| Power Dissipation − $R_{\theta JA}$ (Note 1) | Steady State | $T_A$ = 25°C | $P_D$ | 3.0 | W |
| Pulsed Drain Current | $t_p$ = 10 μs | | $I_{DM}$ | 150 | A |
| Operating Junction and Storage Temperature | | | $T_J$, $T_{STG}$ | −55 to 175 | °C |
| Source Current (Body Diode) Pulsed | | | $I_S$ | 63.5 | A |
| Single Pulse Drain−to Source Avalanche Energy − ($V_{DD}$ = 50 V, $V_{GS}$ = 10 V, $I_{PK}$ = 30 A, L = 1 mH, $R_G$ = 25 Ω) | | | EAS | 450 | mJ |
| Lead Temperature for Soldering Purposes (1/8" from case for 10 s) | | | $T_L$ | 260 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**THERMAL RESISTANCE RATINGS** (Note 1)

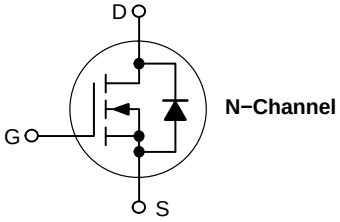
| Parameter | Symbol | Max | Unit |
|---|---|---|---|
| Junction−to−Case (Drain) | $R_{\theta JC}$ | 1.5 | °C/W |
| Junction−to−Ambient (Note 1) | $R_{\theta JA}$ | 49 | |

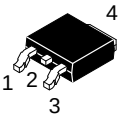
1. Surface mounted on FR4 board using 1 sq in pad size, (Cu Area 1.127 sq in [2 oz] including traces).

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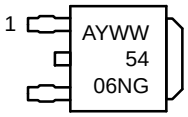
| $V_{(BR)DSS}$ | $R_{DS(ON)}$ TYP | $I_D$ MAX (Note 1) |
|---|---|---|
| 40 V | 8.7 mΩ @ 10 V | 70 A |




**DPAK**
**CASE 369C**
**STYLE 2**

**MARKING DIAGRAM**




A = Assembly Location*
Y = Year
WW = Work Week
5406N = Specific Device Code
G = Pb−Free Device

* The Assembly Location code (A) is front side optional. In cases where the Assembly Location is stamped in the package, the front side assembly code may be blank.

**ORDERING INFORMATION**

| Device | Package | Shipping† |
|---|---|---|
| NTD5406NT4G | DPAK (Pb−Free) | 2500 / Tape & Reel |
| STD5406NT4G* | DPAK (Pb−Free) | 2500 / Tape & Reel |
| STD5406NT4G−VF01 | DPAK (Pb−Free) | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise stated)

| Parameter | Symbol | Test Condition | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | | |
| Drain−to−Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS}$ = 0 V, $I_D$ = 250 μA | | 40 | | | V |
| Drain−to−Source Breakdown Voltage Temperature Coefficient | $V_{(BR)DSS}/T_J$ | | | | 42 | | mV/°C |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{GS}$ = 0 V, $V_{DS}$ = 40 V | $T_J$ = 25°C | | | 1.0 | μA |
| | | | $T_J$ = 100°C | | | 10 | |
| Gate−to−Source Leakage Current | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS}$ = ±30 V | | | | ±100 | nA |
| **ON CHARACTERISTICS** (Note 2) | | | | | | | |
| Gate Threshold Voltage | $V_{GS(TH)}$ | $V_{GS}$ = $V_{DS}$, $I_D$ = 250 μA | | 1.5 | | 3.5 | V |
| Gate Threshold Temperature Coefficient | $V_{GS(TH)}/T_J$ | | | | −7.0 | | mV/°C |
| Drain−to−Source On Resistance | $R_{DS(on)}$ | $V_{GS}$ = 10 V, $I_D$ = 30 A | | | 8.7 | 10 | mΩ |
| | | $V_{GS}$ = 5.0 V, $I_D$ = 10 A | | | 13.2 | 17 | |
| Forward Transconductance | $g_{FS}$ | $V_{GS}$ = 10 V, $I_D$ = 10 A | | | 19 | | S |
| **CHARGES AND CAPACITANCES** | | | | | | | |
| Input Capacitance | $C_{ISS}$ | $V_{GS}$ = 0 V, f = 1.0 MHz, $V_{DS}$ = 32 V | | | 1375 | 2500 | pF |
| Output Capacitance | $C_{OSS}$ | | | | 370 | 700 | |
| Reverse Transfer Capacitance | $C_{RSS}$ | | | | 160 | 300 | |
| Total Gate Charge | $Q_{G(TOT)}$ | $V_{GS}$ = 10 V, $V_{DS}$ = 32 V, $I_D$ = 30 A | | | 45 | | nC |
| Threshold Gate Charge | $Q_{G(TH)}$ | | | | 2.0 | | |
| Gate−to−Source Charge | $Q_{GS}$ | | | | 5.4 | | |
| Gate−to−Drain Charge | $Q_{GD}$ | | | | 20 | | |
| **SWITCHING CHARACTERISTICS, $V_{GS}$ = 10 V** (Note 3) | | | | | | | |
| Turn−On Delay Time | $t_{d(ON)}$ | $V_{GS}$ = 10 V, $V_{DD}$ = 32 V, $I_D$ = 30 A, $R_G$ = 2.5 Ω | | | 7.2 | | ns |
| Rise Time | $t_r$ | | | | 57 | | |
| Turn−Off Delay Time | $t_{d(OFF)}$ | | | | 30 | | |
| Fall Time | $t_f$ | | | | 67 | | |
| **SWITCHING CHARACTERISTICS, $V_{GS}$ = 5 V** (Note 3) | | | | | | | |
| Turn−On Delay Time | $t_{d(ON)}$ | $V_{GS}$ = 5.0 V, $V_{DD}$ = 20 V, $I_D$ = 30 A, $R_G$ = 2.5 Ω | | | 15 | | ns |
| Rise Time | $t_r$ | | | | 147 | | |
| Turn−Off Delay Time | $t_{d(OFF)}$ | | | | 20 | | |
| Fall Time | $t_f$ | | | | 29 | | |
| **DRAIN−SOURCE DIODE CHARACTERISTICS** | | | | | | | |
| Forward Diode Voltage | $V_{SD}$ | $V_{GS}$ = 0 V, $I_S$ = 10 A | $T_J$ = 25°C | | 0.82 | 1.1 | V |
| | | | $T_J$ = 125°C | | 0.67 | | |
| Reverse Recovery Time | $t_{RR}$ | $V_{GS}$ = 0 V, $dI_{SD}/dt$ = 100 A/μs, $I_S$ = 10 A | | | 46 | | ns |
| Charge Time | $t_a$ | | | | 24 | | |
| Discharge Time | $t_b$ | | | | 22 | | |
| Reverse Recovery Charge | $Q_{RR}$ | | | | 65 | | nC |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperatures.

## TYPICAL PERFORMANCE CURVES

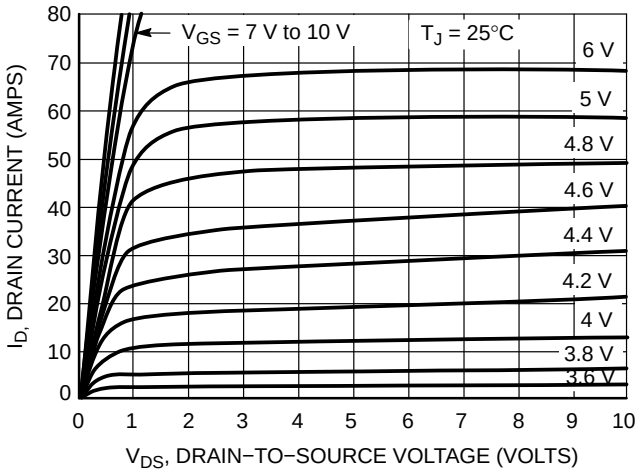



**Figure 1. On−Region Characteristics**

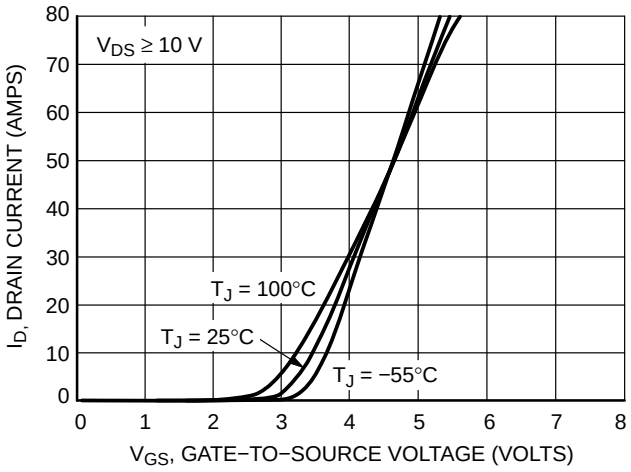



**Figure 2. Transfer Characteristics**

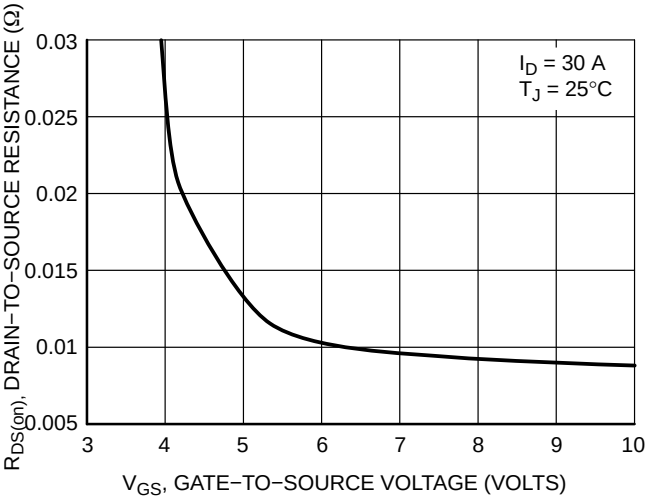



**Figure 3. On−Resistance vs. Gate−to−Source Voltage**

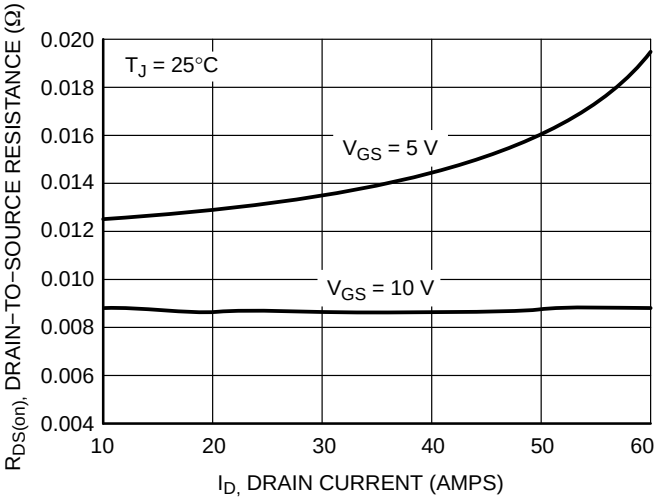



**Figure 4. On−Resistance vs. Drain Current and Gate Voltage**

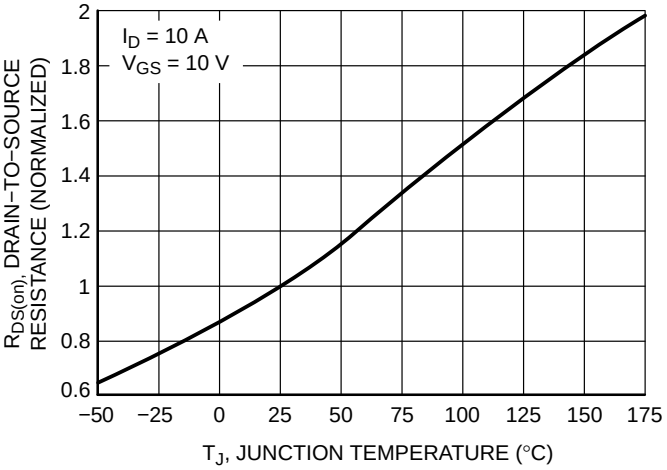



**Figure 5. On−Resistance Variation with Temperature**

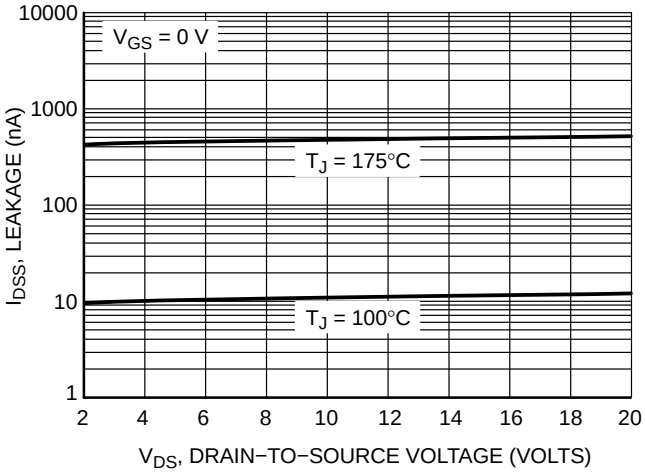



**Figure 6. Drain−to−Source Leakage Current vs. Voltage**

## TYPICAL PERFORMANCE CURVES

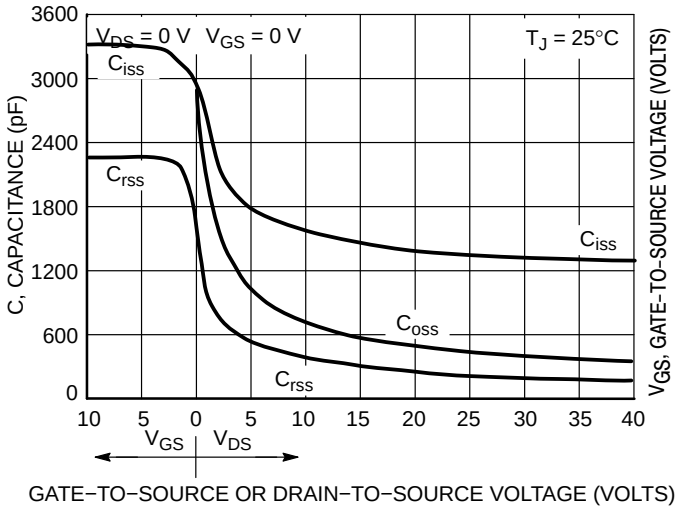



**Figure 7. Capacitance Variation**

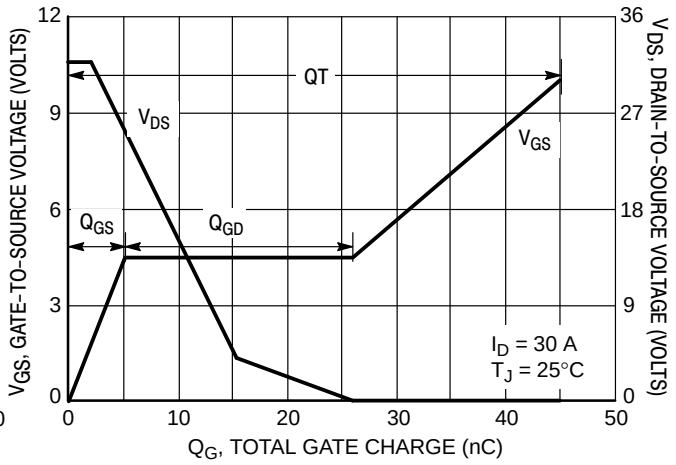



**Figure 8. Gate−To−Source and Drain−To−Source Voltage vs. Total Charge**

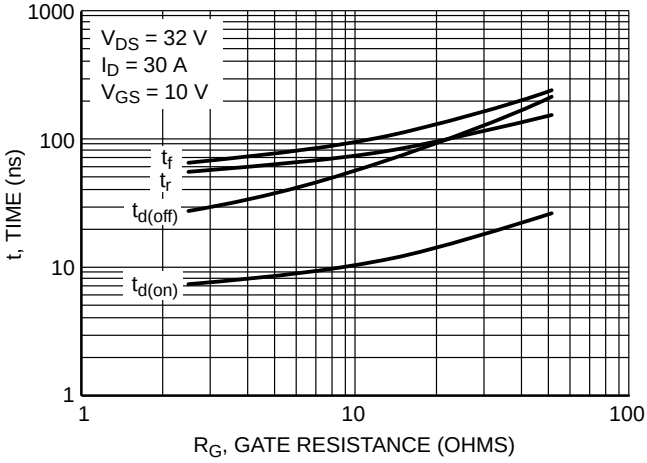



**Figure 9. Resistive Switching Time Variation vs. Gate Resistance**

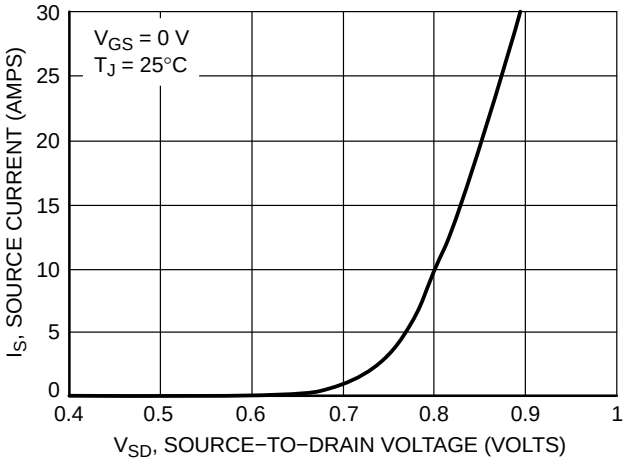



**Figure 10. Diode Forward Voltage vs. Current**

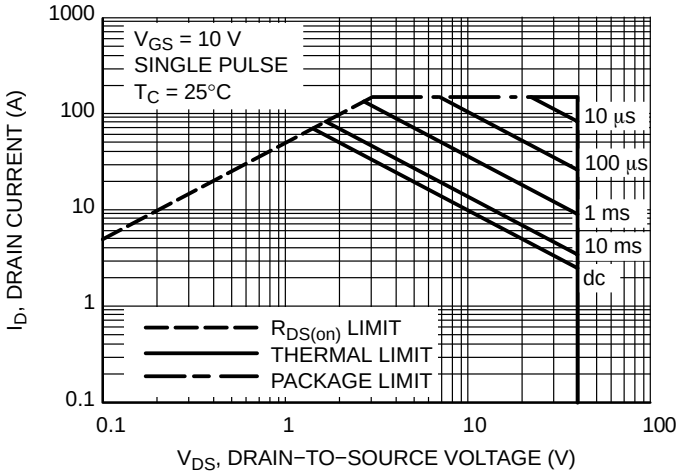



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

## TYPICAL PERFORMANCE CURVES

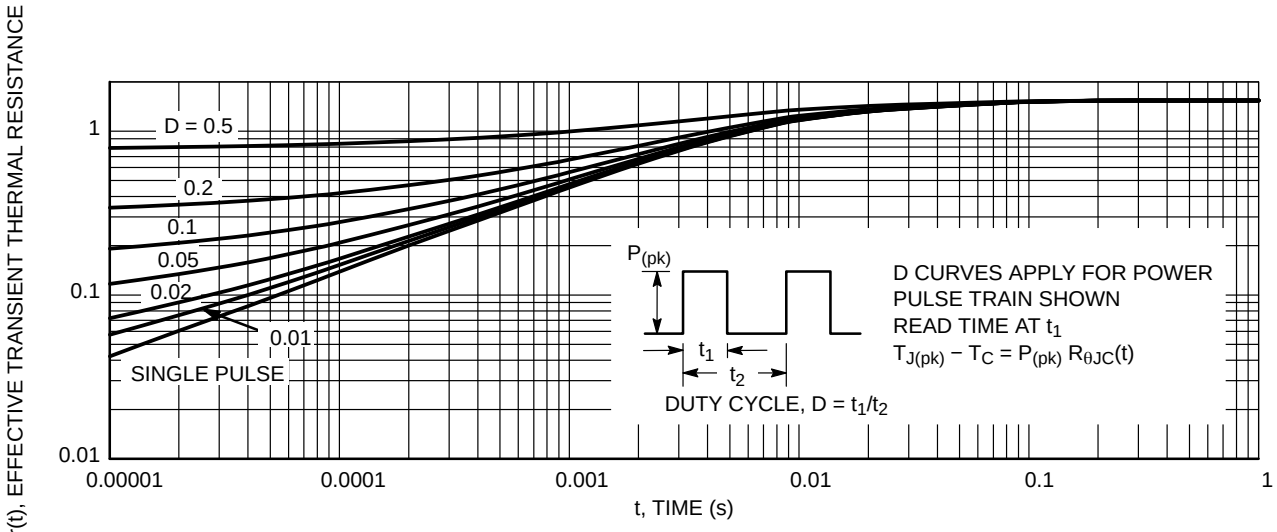
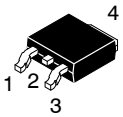


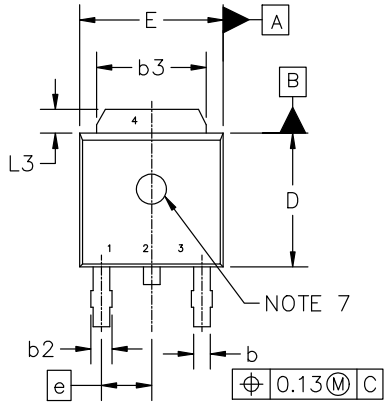

**Figure 12. Thermal Response**



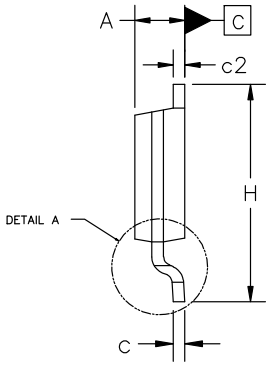

**SCALE 1:1**

**DPAK−3 6.10x6.54x2.28, 2.29P**
CASE 369C
ISSUE L

DATE 24 AUG 2026

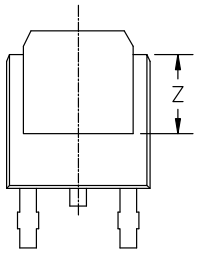



TOP VIEW

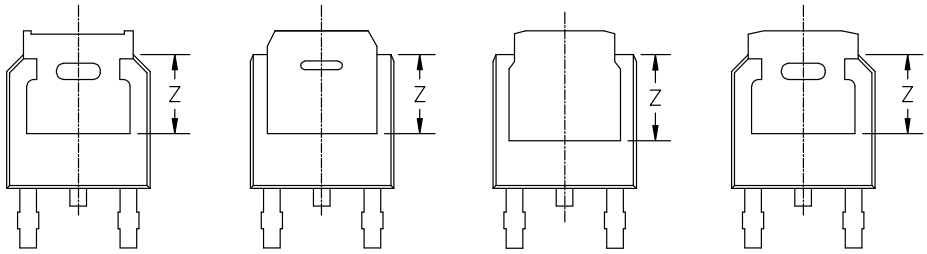



SIDE VIEW

| MILLIMETERS | | | |
|---|---|---|---|
| DIM | MIN | NOM | MAX |
| A | 2.18 | 2.28 | 2.38 |
| A1 | 0.00 | −−− | 0.13 |
| b | 0.63 | 0.76 | 0.89 |
| b2 | 0.72 | 0.93 | 1.14 |
| b3 | 4.57 | 5.02 | 5.46 |
| c | 0.46 | 0.54 | 0.61 |
| c2 | 0.46 | 0.54 | 0.61 |
| D | 5.97 | 6.10 | 6.22 |
| E | 6.35 | 6.54 | 6.73 |
| e | 2.29 BSC | | |
| H | 9.40 | 9.91 | 10.41 |
| L | 1.40 | 1.59 | 1.78 |
| L1 | 2.90 REF | | |
| L2 | 0.51 BSC | | |
| L3 | 0.89 | −−− | 1.27 |
| L4 | −−− | −−− | 1.01 |
| Z | 3.93 | −−− | −−− |



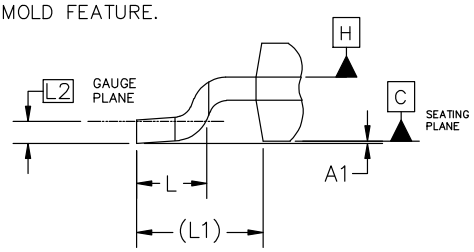

BOTTOM VIEW



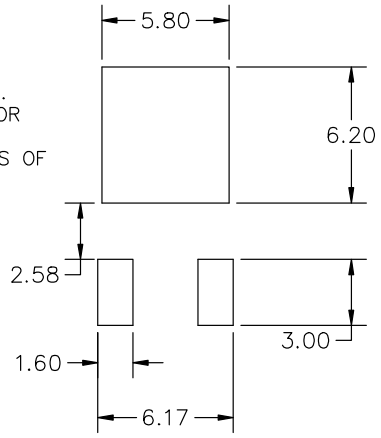

ALTERNATE CONSTRUCTIONS

NOTES:

1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.




DETAIL A
ROTATED 90° CW




RECOMMENDED MOUNTING FOOTPRINT*
*For additional information on our Pb−Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques reference manual, SOLDERRM/D.

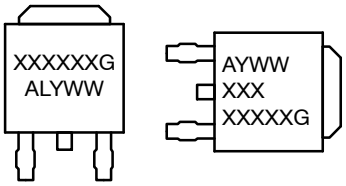
| | | |
|---|---|---|
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| **DESCRIPTION:** | **DPAK−3 6.10x6.54x2.28, 2.29P** | **PAGE 1 OF 2** |

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**DPAK−3 6.10x6.54x2.28, 2.29P**
CASE 369C
ISSUE L

DATE 24 AUG 2026

## GENERIC MARKING DIAGRAM*




**IC** **Discrete**

| | |
|---|---|
| XXXXXX | = Device Code |
| A | = Assembly Location |
| L | = Wafer Lot |
| Y | = Year |
| WW | = Work Week |
| G | = Pb−Free Package |

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE




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