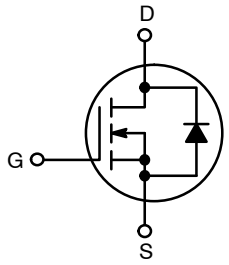
MOSFET – Power, N-Channel, SUPERFET® III, FRFET®

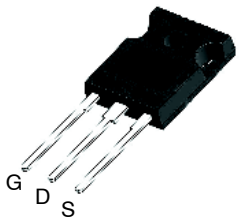
650 V, 65 A, 40 mΩ

NVHL040N65S3F

V_{DSS}	$R_{DS(ON)}$ MAX	I_D MAX
650 V	40 mΩ @ 10 V	65 A



POWER MOSFET



TO-247-3LD
CASE 340CX

Description

SUPERFET III MOSFET is **onsemi**'s brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate.

Consequently, SUPERFET III MOSFET is very suitable for the various power system for miniaturization and higher efficiency.

SUPERFET III FRFET MOSFET's optimized reverse recovery performance of body diode can remove additional component and improve system reliability.

Features

- 700 V @ T_J = 150 °C
- Typ. $R_{DS(on)}$ = 33.8 mΩ
- Ultra Low Gate Charge (Typ. Q_g = 153 nC)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)}$ = 1333 pF)
- 100% Avalanche Tested
- AEC-Q101 Qualified and PPAP Capable

Applications

- Automotive On Board Charger HEV-EV
- Automotive DC/DC converter for HEV-EV

MARKING DIAGRAM



$Y	= **onsemi** Logo
&Z	= Assembly Plant Code
&3	= Data Code (Year & Week)
&K	= Lot
NVHL040N65S3F	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

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ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, Unless otherwise noted)

Symbol	Parameter		NVHL040N65S3F	Unit
V_{DSS}	Drain to Source Voltage		650	V
V_{GSS}	Gate to Source Voltage	– DC	±30	V
		– AC (f > 1 Hz)	±30	
I_D	Drain Current	– Continuous (T_C = 25 °C)	65	A
		– Continuous (T_C = 100 °C)	45	
I_{DM}	Drain Current	– Pulsed (Note 1)	162.5	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		1009	mJ
E_{AR}	Repetitive Avalanche Energy (Note 1)		4.46	mJ
dv/dt	MOSFET dv/dt		100	V/ns
	Peak Diode Recovery dv/dt (Note 3)		50	
P_D	Power Dissipation	(T_C = 25 °C)	446	W
		– Derate Above 25 °C	3.57	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		–55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8″ from Case for 5 seconds		300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. I_{AS} = 9 A, R_G = 25 Ω, starting T_J = 25 °C.
3. $I_{SD} \le$ 32.5 A, di/dt ≤ 200 A/μs, $V_{DD} \le$ 400 V, starting T_J = 25 °C.

THERMAL CHARACTERISTICS

Symbol	Parameter	NVHL040N65S3F	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.28	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	40	

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Packing Method	Reel Size	Tape Width	Quantity
NVHL040N65S3F	NVHL040N65S3F	TO-247-3LD	Tube	N/A	N/A	30 Units

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ELECTRICAL CHARACTERISTICS (T_C = 25 °C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	V_{GS} = 0 V, I_D = 1 mA, T_J = 25 °C	650	–	–	V
		V_{GS} = 0 V, I_D = 10 mA, T_J = 150 °C	700	–	–	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 10 mA, Referenced to 25 °C	–	0.64	–	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 650 V, V_{GS} = 0 V	–	–	10	μA
		V_{DS} = 520 V, T_C = 125 °C	–	103	–	
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±30 V, V_{DS} = 0 V	–	–	±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 2.1 mA	3.0	–	5.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 32.5 A	–	33.8	40	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 20 V, I_D = 32.5 A	–	40	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 400 V, V_{GS} = 0 V, f = 1 MHz	–	5875	–	pF
C_{oss}	Output Capacitance		–	140	–	pF
$C_{oss(eff.)}$	Effective Output Capacitance	V_{DS} = 0 V to 400 V, V_{GS} = 0 V	–	1333	–	pF
$C_{oss(er.)}$	Energy Related Output Capacitance	V_{DS} = 0 V to 400 V, V_{GS} = 0 V	–	241	–	pF
$Q_{g(tot)}$	Total Gate Charge at 10 V	V_{DS} = 400 V, I_D = 32.5 A, V_{GS} = 10 V (Note 4)	–	153	–	nC
Q_{gs}	Gate to Source Gate Charge		–	51	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	61	–	nC
ESR	Equivalent Series Resistance	f = 1 MHz	–	1.9	–	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 400 V, I_D = 32.5 A, V_{GS} = 10 V R_g = 2.2 Ω (Note 4)	–	41	–	ns
t_r	Turn-On Rise Time		–	53	–	ns
$t_{d(off)}$	Turn-Off Delay Time		–	96	–	ns
t_f	Turn-Off Fall Time		–	28	–	ns
SOURCE-DRAIN DIODE CHARACTERISTICS						
I_S	Maximum Continuous Source to Drain Diode Forward Current		–	–	65	A
I_{SM}	Maximum Pulsed Source to Drain Diode Forward Current		–	–	162.5	A
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 32.5 A	–	–	1.3	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_{SD} = 32.5 A, dI_F/dt = 100 A/μs	–	159	–	ns
Q_{rr}	Reverse Recovery Charge		–	840	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature typical characteristics.

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TYPICAL CHARACTERISTICS

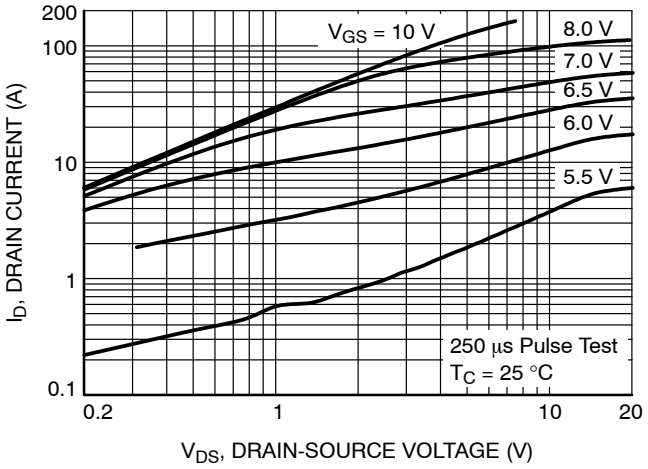


Figure 1. On-Region Characteristics

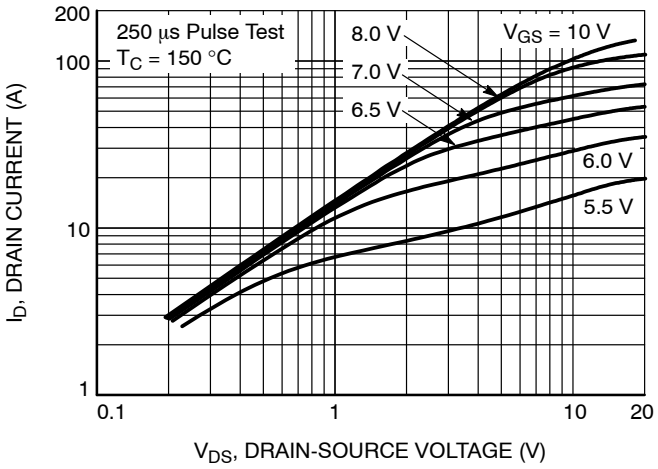


Figure 2. On-Region Characteristics

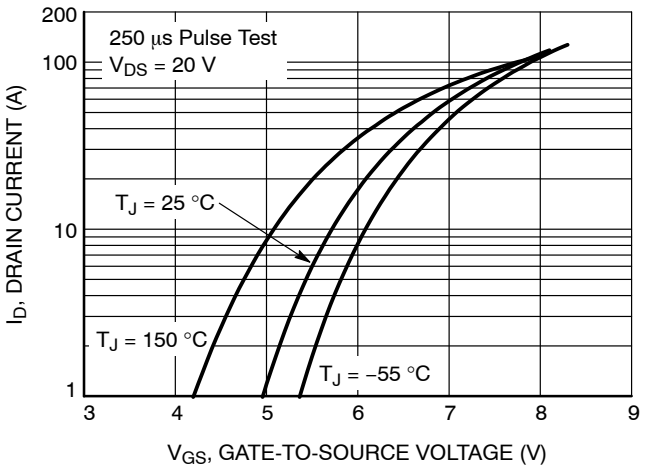


Figure 3. Transfer Characteristics

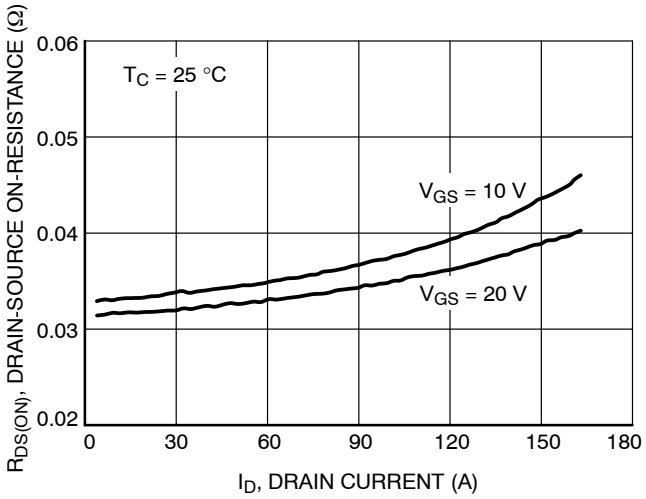


Figure 4. On-Resistance Variation vs. Drain Current and Gate Voltage

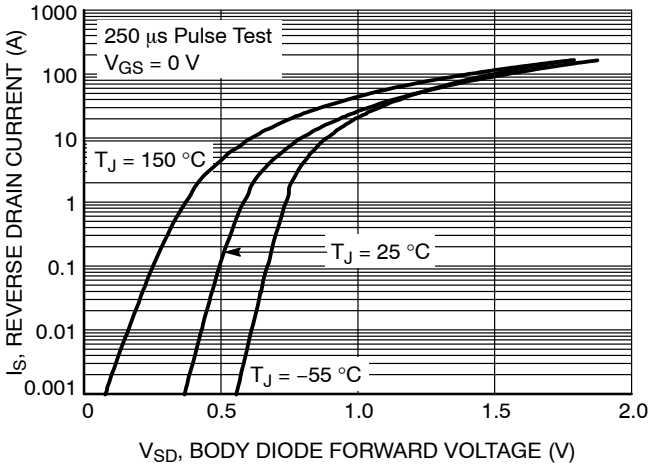


Figure 5. Body Diode Forward Voltage Variation vs. Source Current and Temperature

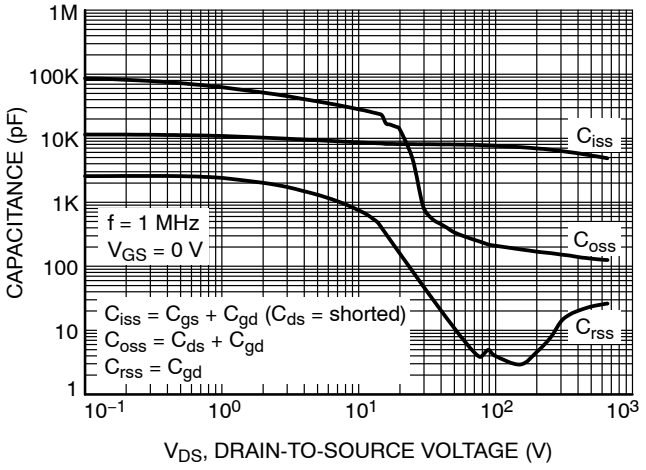


Figure 6. Capacitance Characteristics

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TYPICAL CHARACTERISTICS

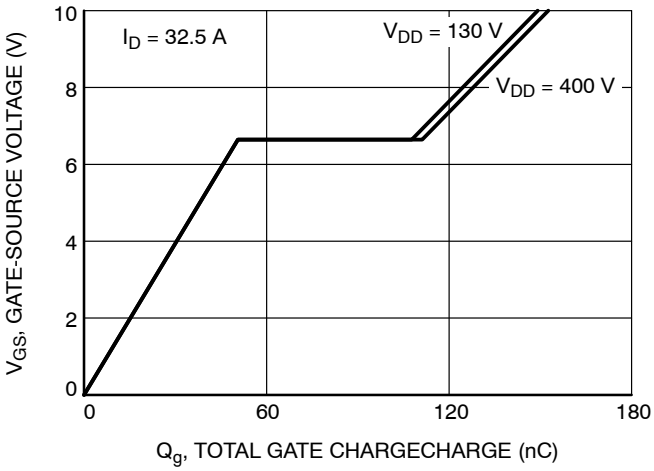


Figure 7. Gate Charge Characteristics

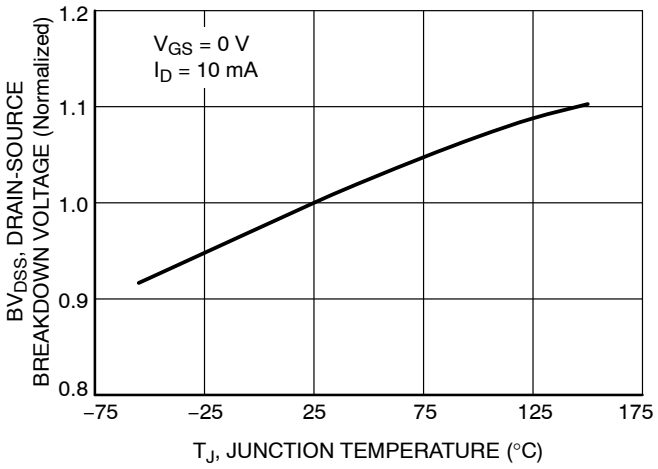


Figure 8. Breakdown Voltage Variation vs. Temperature

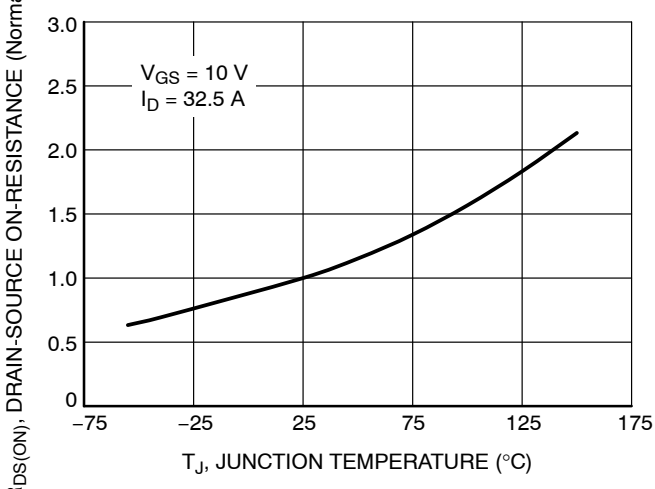


Figure 9. On-Resistance Variation vs. Temperature

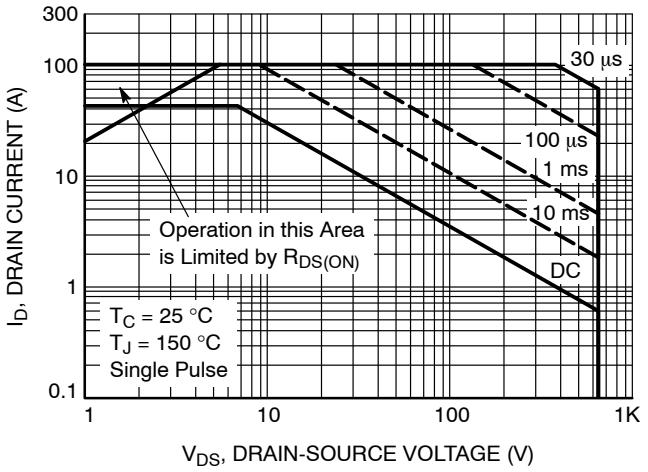


Figure 10. Maximum Safe Operating Area

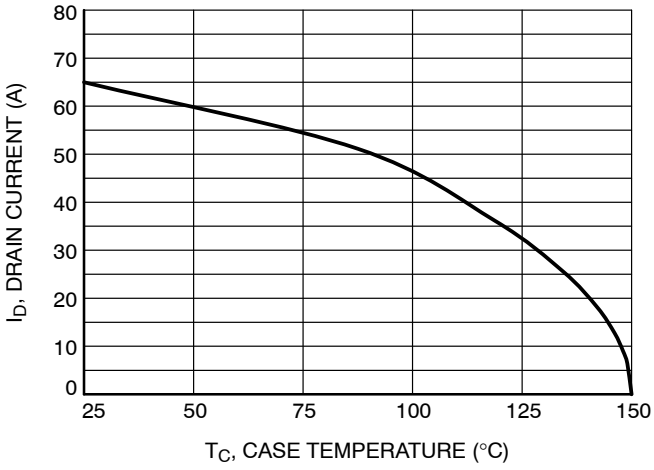


Figure 11. Maximum Drain Current vs. Case Temperature

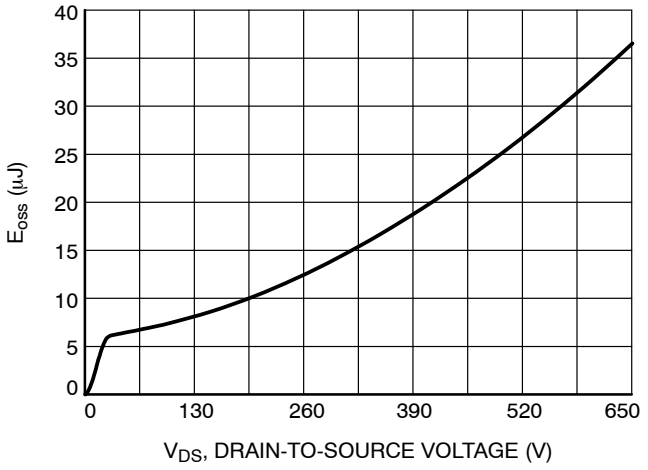


Figure 12. EOSS vs. Drain-to-Source Voltage

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TYPICAL CHARACTERISTICS

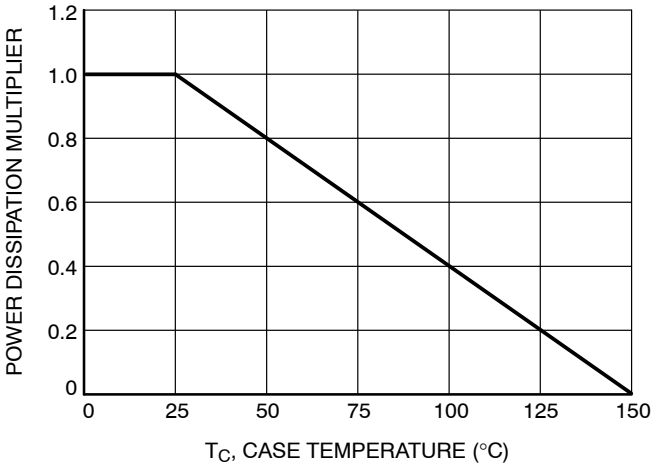


Figure 13. Normalized Power Dissipation vs. Case Temperature

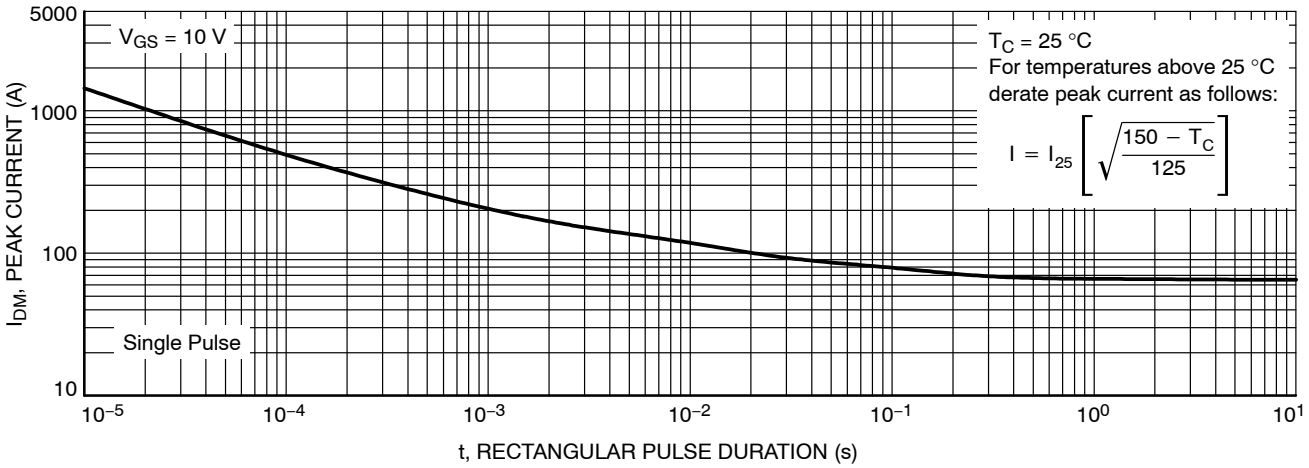


Figure 14. Peak Current Capability

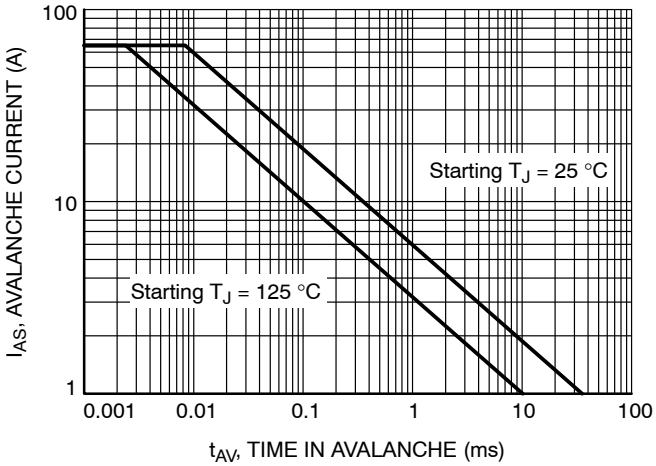


Figure 15. Unclamped Inductive Switching Capability

If R = 0
$t_{AV} = (L)(I_{AS})/(1.3*\text{RATED } BV_{DSS} - V_{DD})$
If R ≠ 0
$t_{AV} = (L/R)\ln[(I_{AS}*R)/(1.3*\text{RATED } BV_{DSS} - V_{DD}) + 1]$

NOTE: Refer to Application Notes AN7514 and AN7515

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TYPICAL CHARACTERISTICS

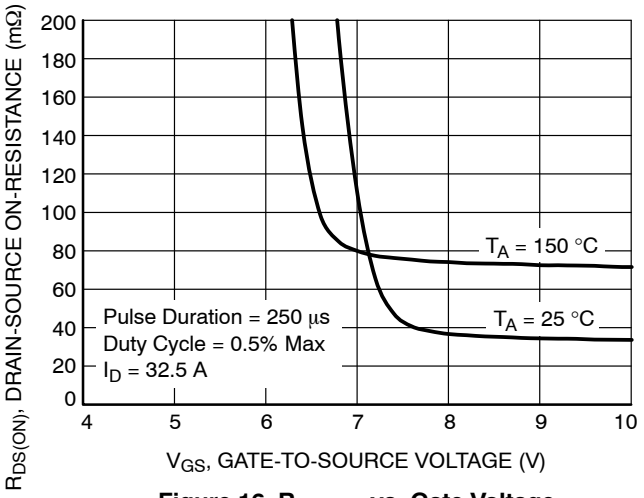


Figure 16. $R_{DS(ON)}$ vs. Gate Voltage

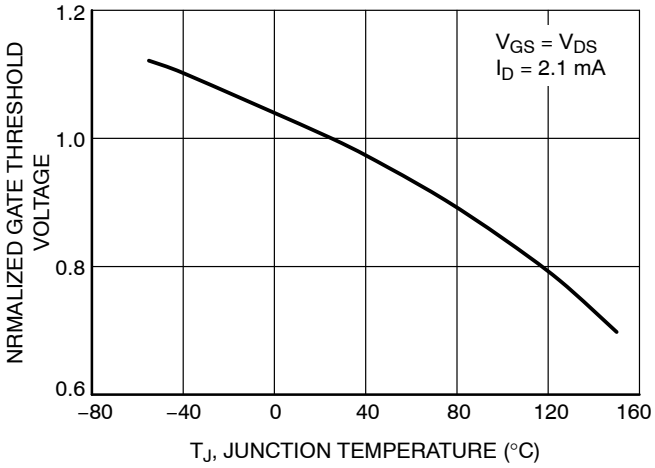


Figure 17. Normalized Gate Threshold Voltage vs. Temperature

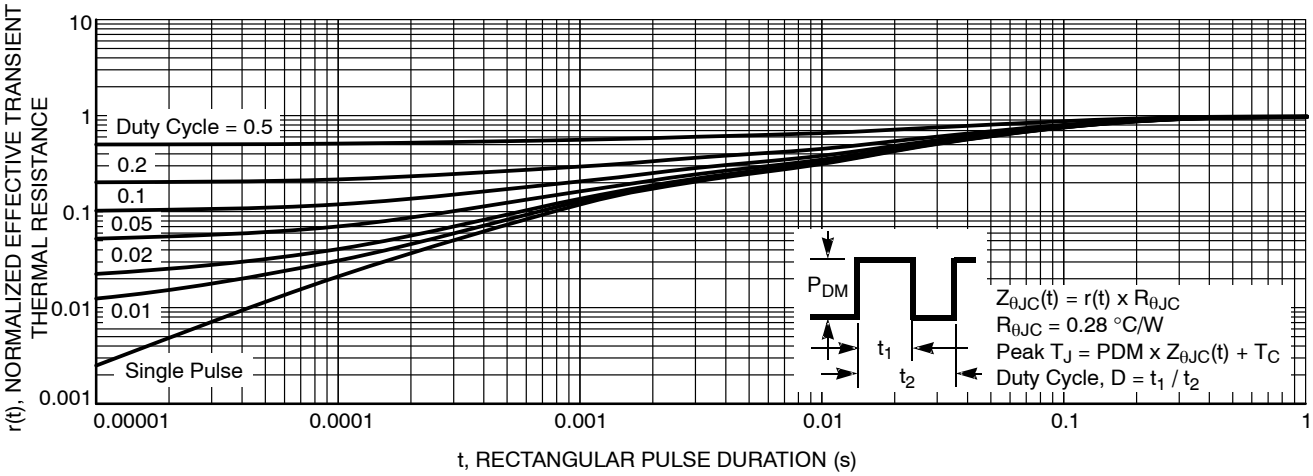


Figure 18. Transient Thermal Response Curve

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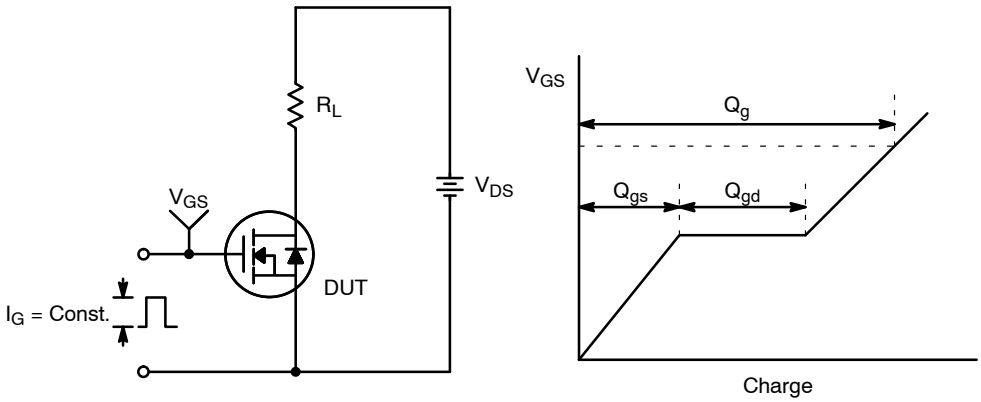


Figure 19. Gate Charge Test Circuit & Waveform

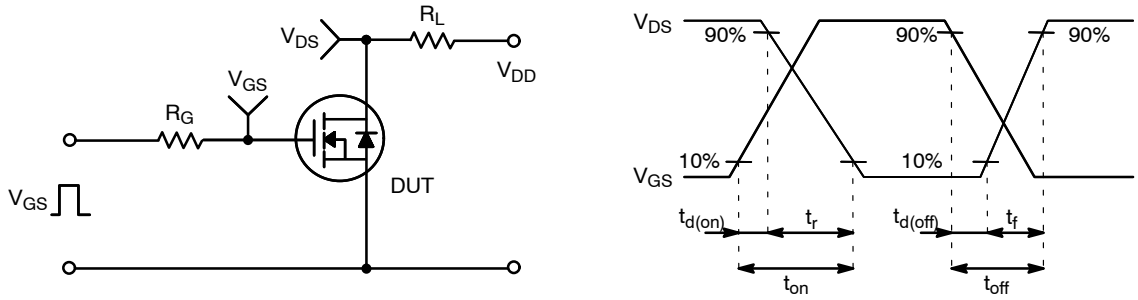


Figure 20. Resistive Switching Test Circuit & Waveforms

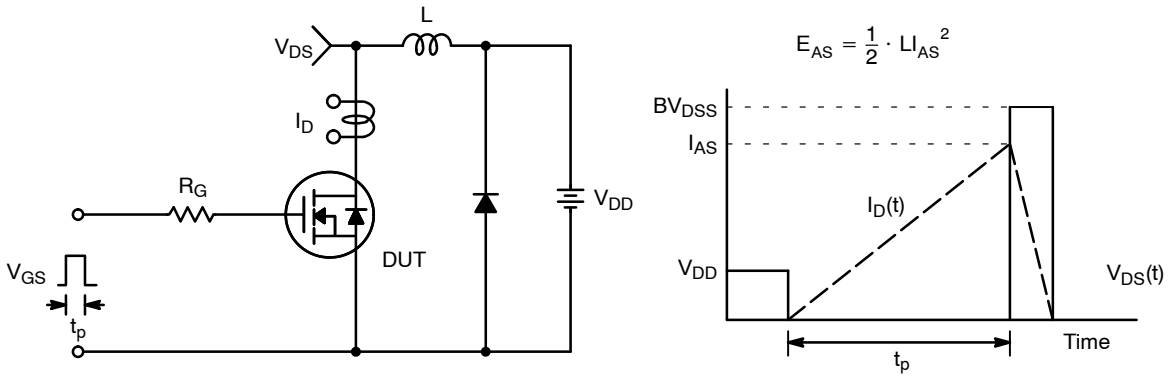


Figure 21. Unclamped Inductive Switching Test Circuit & Waveforms

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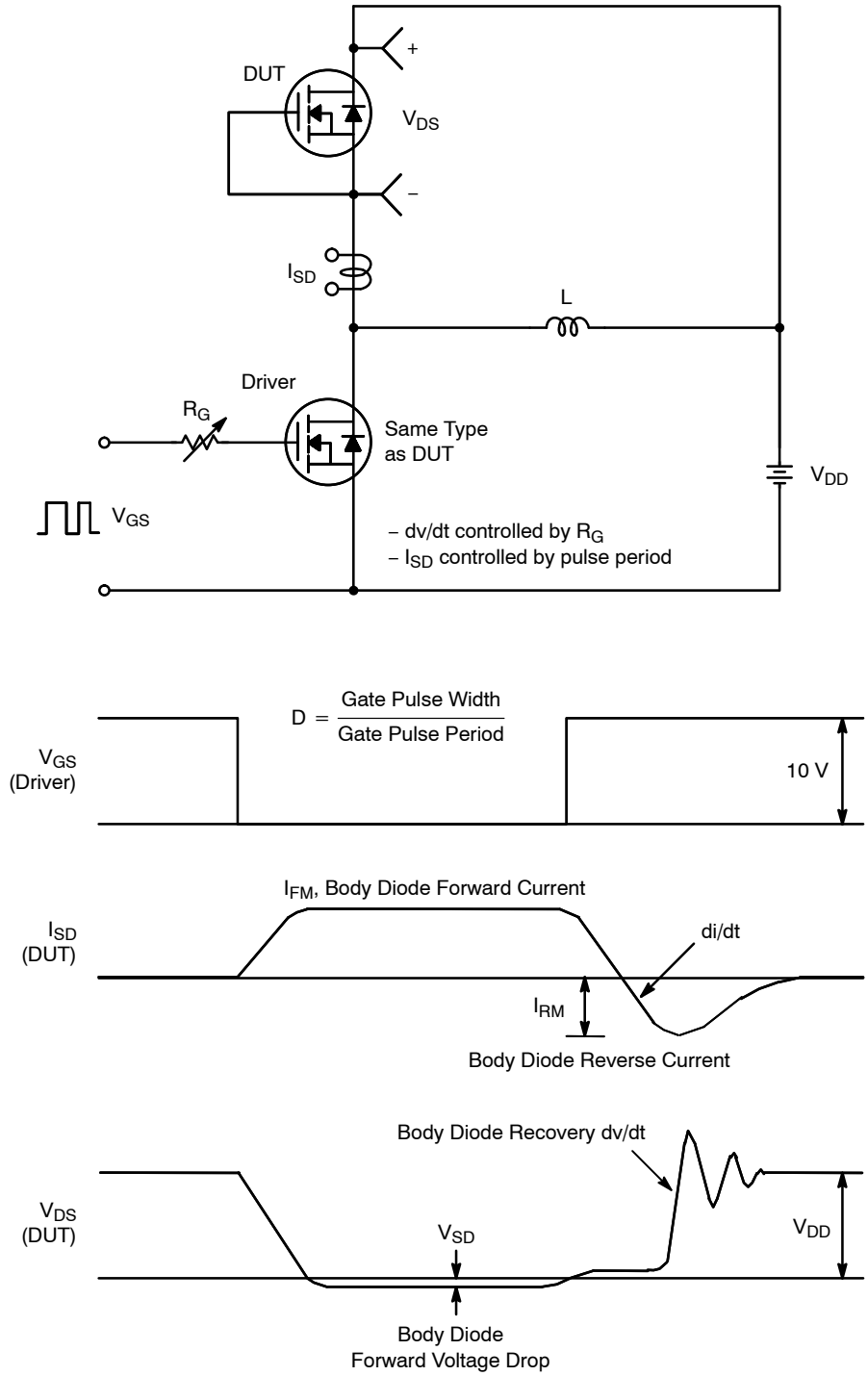


Figure 22. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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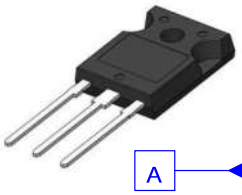
Revision	Description of Changes	Date
2	Document rebranded to **onsemi** format.	10/9/2025

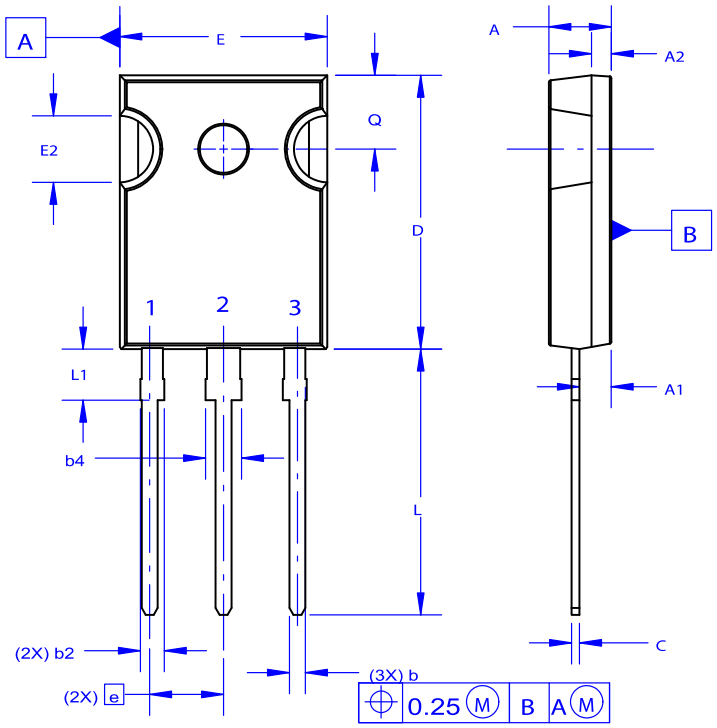
This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

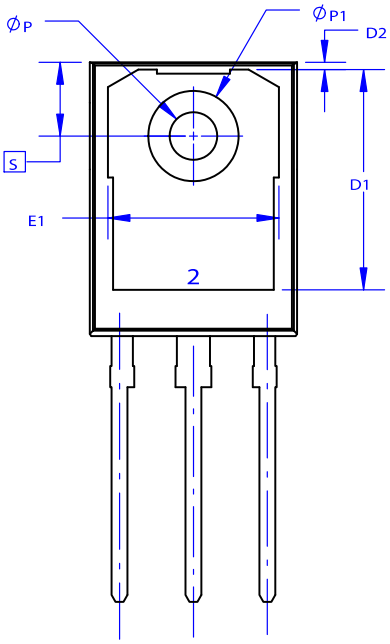
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TO−247−3LD
CASE 340CX
ISSUE A

DATE 06 JUL 2020







NOTES: UNLESS OTHERWISE SPECIFIED.

A. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
B. ALL DIMENSIONS ARE IN MILLIMETERS.
C. DRAWING CONFORMS TO ASME Y14.5 - 2009.
D. DIMENSION A1 TO BE MEASURED IN THE REGION DEFINED BY L1.
E. LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY L1.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.58	4.70	4.82
A1	2.20	2.40	2.60
A2	1.40	1.50	1.60
D	20.32	20.57	20.82
E	15.37	15.62	15.87
E2	4.96	5.08	5.20
e	~	5.56	~
L	19.75	20.00	20.25
L1	3.69	3.81	3.93
ØP	3.51	3.58	3.65
Q	5.34	5.46	5.58
S	5.34	5.46	5.58
b	1.17	1.26	1.35
b2	1.53	1.65	1.77
b4	2.42	2.54	2.66
c	0.51	0.61	0.71
D1	13.08	~	~
D2	0.51	0.93	1.35
E1	12.81	~	~
ØP1	6.60	6.80	7.00

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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