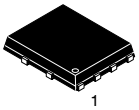
MOSFET – Power, Dual N-Channel

60 V, 11.9 mΩ, 40 A

NVMFD5C672NL

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
60 V	11.9 mΩ @ 10 V	40 A
	16.8 mΩ @ 4.5 V	

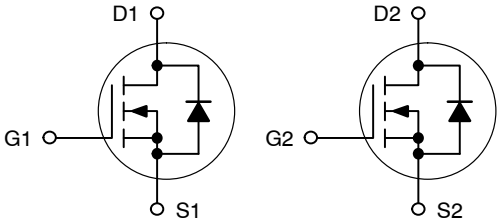


DFN8 5x6
(SO8FL)
CASE 506BT

Features

- Small Footprint (5x6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- NVMFD5C672NLWF – Wettable Flank Option for Enhanced Optical Inspection
- AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

Dual N−Channel



MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Symbol	Parameter			Value	Unit
V_{DSS}	Drain−to−Source Voltage			60	V
V_{GS}	Gate−to−Source Voltage			±20	V
I_D	Continuous Drain Current $R_{\theta JC}$ (Notes 1, 2, 3)	Steady State	T_C = 25°C	40	A
			T_C = 100°C	31	
P_D	Power Dissipation $R_{\theta JC}$ (Notes 1, 2)		T_C = 25°C	42	W
			T_C = 100°C	21	
I_D	Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	T_A = 25°C	11	A
			T_A = 100°C	8.0	
P_D	Power Dissipation $R_{\theta JA}$ (Notes 1, 2)		T_A = 25°C	3.1	W
			T_A = 100°C	1.5	
I_{DM}	Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		161	A
T_J, T_{stg}	Operating Junction and Storage Temperature Range			−55 to +175	°C
I_S	Source Current (Body Diode)			35.2	A
E_{AS}	Single Pulse Drain−to−Source Avalanche Energy (T_J = 25°C, $I_{L(pk)}$ = 2 A)			66	mJ
T_L	Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			260	°C

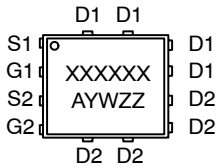
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Junction−to−Case − Steady State	3.55	°C/W
$R_{\theta JA}$	Junction−to−Ambient − Steady State (Note 2)	47.51	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface−mounted on FR4 board using a 650 mm^2, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

MARKING DIAGRAM



A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
$V_{(BR)DSS}$	Drain−to−Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA		60			V
$V_{(BR)DSS}/T_J$	Drain−to−Source Breakdown Voltage Temperature Coefficient				27		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{GS} = 0 V, V_{DS} = 60 V	T_J = 25 °C			10	μA
			T_J = 125°C			100	
I_{GSS}	Gate−to−Source Leakage Current	V_{DS} = 0 V, V_{GS} = 20 V				100	nA
ON CHARACTERISTICS (Note 4)							
$V_{GS(TH)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 30 μA		1.2		2.2	V
$V_{GS(TH)}/T_J$	Negative Threshold Temperature Coefficient				−5.7		mV/°C
$R_{DS(on)}$	Drain−to−Source On Resistance	V_{GS} = 10 V	I_D = 10 A		9.8	11.9	mΩ
		V_{GS} = 4.5 V	I_D = 10 A		13.4	16.8	
g_{FS}	Forward Transconductance	V_{DS} = 15 V, I_D = 10 A			27.5		S
CHARGES, CAPACITANCES							
C_{ISS}	Input Capacitance	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 25 V			793		pF
C_{OSS}	Output Capacitance				383		
C_{RSS}	Reverse Transfer Capacitance				9.0		
$Q_{G(TOT)}$	Total Gate Charge	V_{GS} = 4.5 V, V_{DS} = 48 V; I_D = 10 A			5.7		nC
$Q_{G(TOT)}$	Total Gate Charge	V_{GS} = 10 V, V_{DS} = 48 V; I_D = 10 A			12.3		
$Q_{G(TH)}$	Threshold Gate Charge	V_{DS} = 48 V; I_D = 10 A			1.5		
Q_{GS}	Gate−to−Source Charge				2.7		
Q_{GD}	Gate−to−Drain Charge				1.2		
V_{GP}	Plateau Voltage				2.8		V
SWITCHING CHARACTERISTICS (Note 5)							
$t_{d(ON)}$	Turn−On Delay Time	V_{GS} = 4.5 V, V_{DS} = 48 V, I_D = 10 A, R_G = 1.0 Ω			11		ns
t_r	Rise Time				30		
$t_{d(OFF)}$	Turn−Off Delay Time				22		
t_f	Fall Time				28		
DRAIN−SOURCE DIODE CHARACTERISTICS							
V_{SD}	Forward Diode Voltage	V_{GS} = 0 V, I_S = 10 A	T_J = 25°C		0.9	1.2	V
			T_J = 125°C		0.8		
t_{RR}	Reverse Recovery Time	V_{GS} = 0 V, dIS/dt = 20 A/μs, I_S = 10 A			26		ns
t_a	Charge Time				12.3		
t_b	Discharge Time				13.5		
Q_{RR}	Reverse Recovery Charge				13		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.

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TYPICAL CHARACTERISTICS

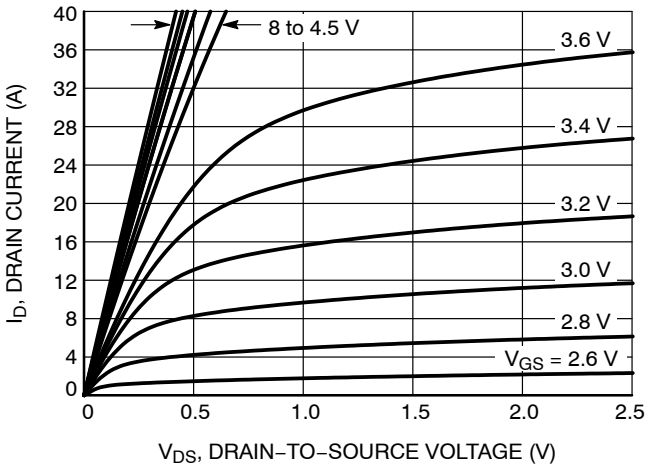

Figure 1. On−Region Characteristics

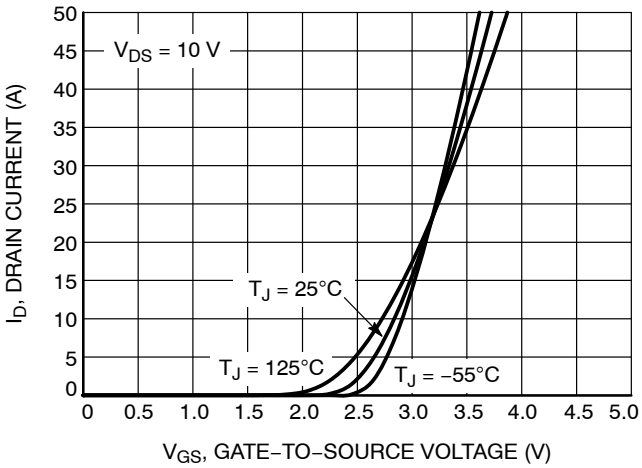

Figure 2. Transfer Characteristics

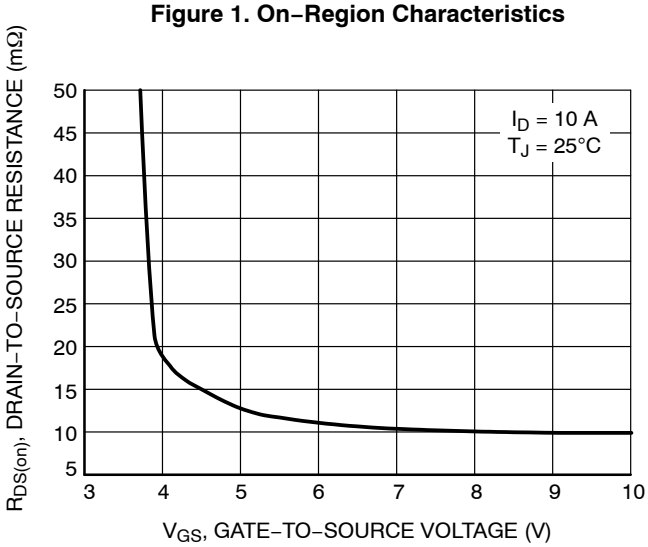

Figure 3. On−Resistance vs. Gate−to−Source Voltage

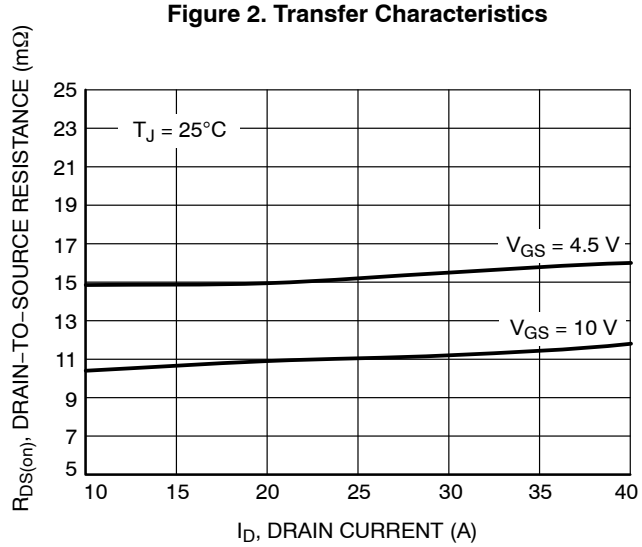

Figure 4. On−Resistance vs. Drain Current and Gate Voltage

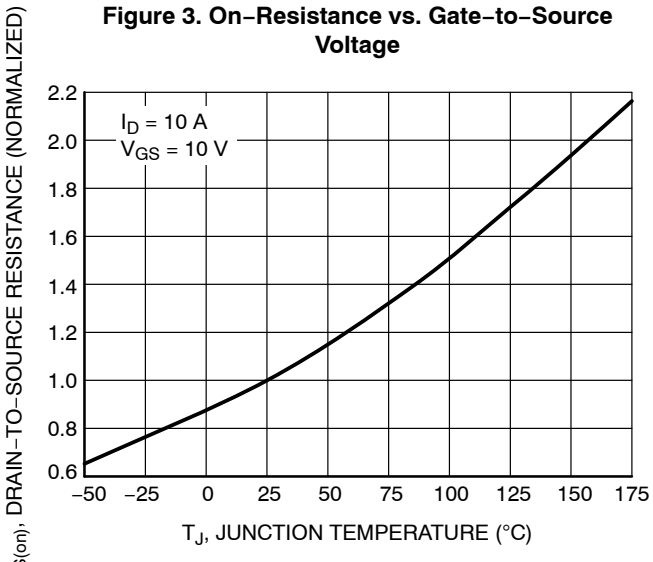

Figure 5. On−Resistance Variation with Temperature

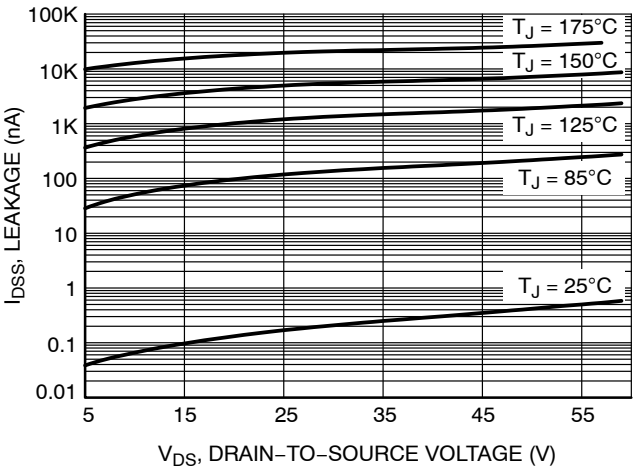

Figure 6. Drain−to−Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS (continued)

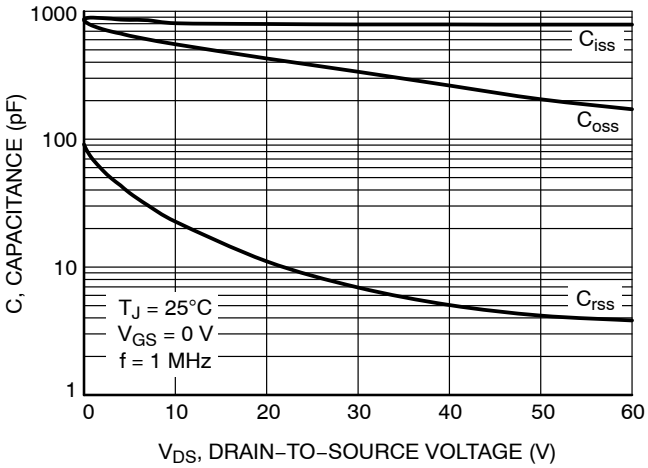

Figure 7. Capacitance Variation

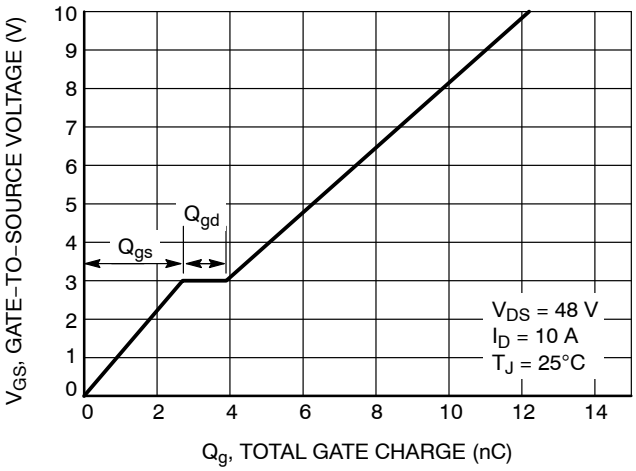

Figure 8. Gate−to−Source vs. Total Charge

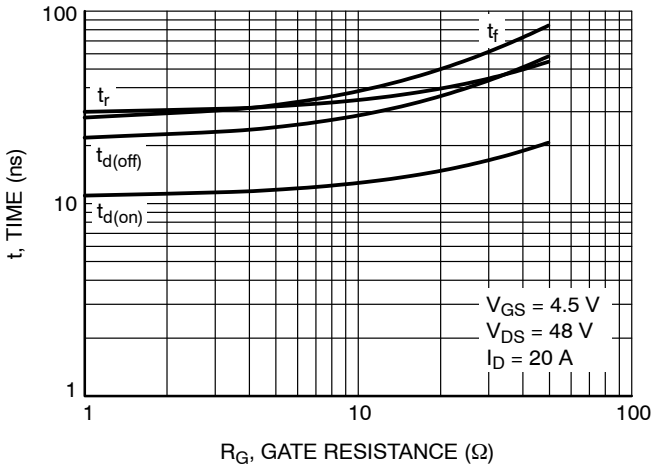

Figure 9. Resistive Switching Time Variation vs. Gate Resistance

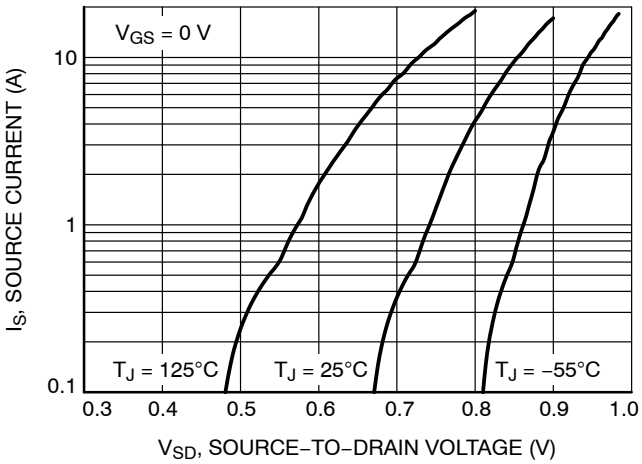

Figure 10. Diode Forward Voltage vs. Current

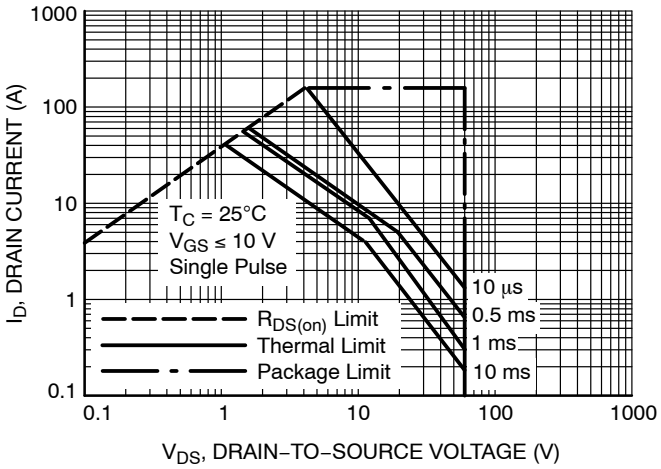

Figure 11. Maximum Rated Forward Biased Safe Operating Area

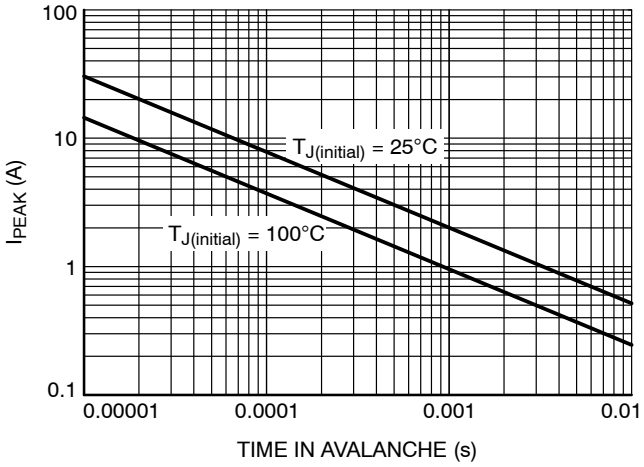

Figure 12. Maximum Drain Current vs. Time in Avalanche

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TYPICAL CHARACTERISTICS (continued)

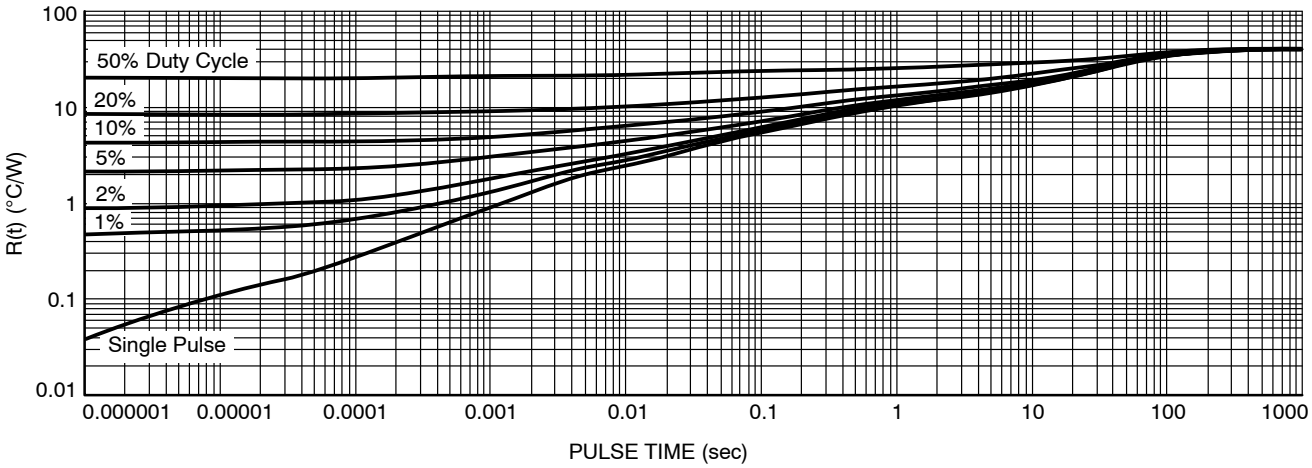

Figure 13. Thermal Response

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping†
NVMFD5C672NLT1G	5C672L	DFN8 (Pb−Free)	1,500 / Tape & Reel
NVMFD5C672NLWFT1G	672LWF	DFN8 (Pb−Free, Wettable Flanks)	1,500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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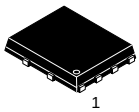
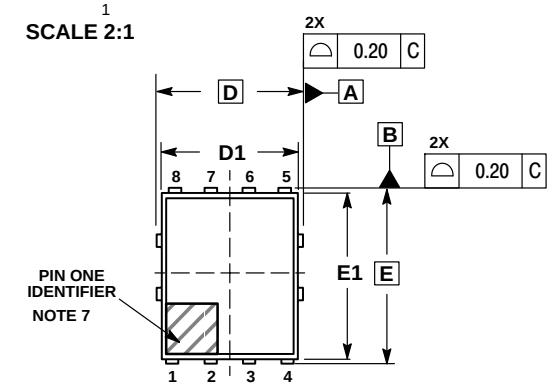


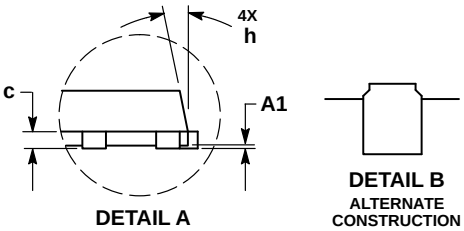
SCALE 2:1

DFN8 5x6, 1.27P Dual Flag (SO8FL−Dual)
CASE 506BT
ISSUE F

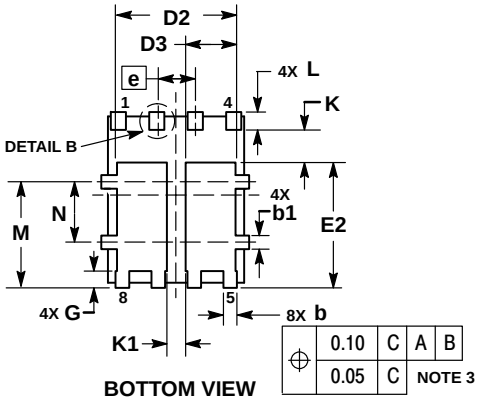
DATE 23 NOV 2021

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. PROFILE TOLERANCE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
6. SEATING PLANE IS DEFINED BY THE TERMINALS. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
7. A VISUAL INDICATOR FOR PIN 1 MUST BE LOCATED IN THIS AREA.

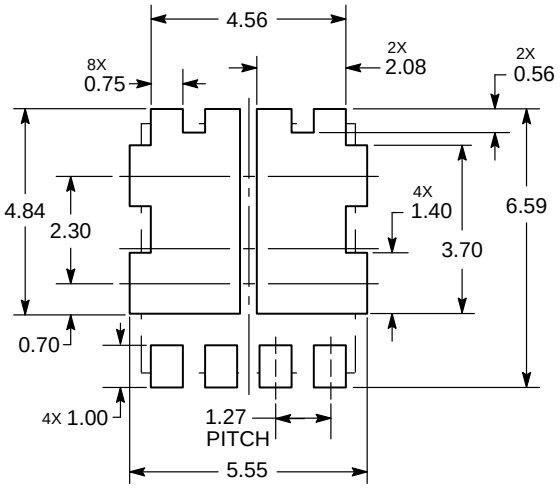




DIM	MILLIMETERS MIN	NOM	MAX
A	0.90	–––	1.10
A1	–––	–––	0.05
b	0.33	0.42	0.51
b1	0.33	0.42	0.51
c	0.20	–––	0.33
D	5.15 BSC		
D1	4.70	4.90	5.10
D2	3.90	4.10	4.30
D3	1.50	1.70	1.90
E	6.15 BSC		
E1	5.70	5.90	6.10
E2	3.90	4.15	4.40
e	1.27 BSC		
G	0.45	0.55	0.65
h	–––	–––	12 °
K	0.51	–––	–––
K1	0.56	–––	–––
L	0.48	0.61	0.71
M	3.25	3.50	3.75
N	1.80	2.00	2.20



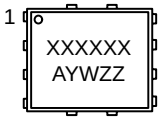
SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98AON50417E	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	DFN8 5X6, 1.27P DUAL FLAG (SO8FL−DUAL)	PAGE 1 OF 1

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