Silicon Carbide (SiC) Module – EliteSiC, 40 mohm SiC M1 MOSFET, 1200 V, 4-PACK Full Bridge Topology, F1 Package

NXH040F120MNF1PTG, NXH040F120MNF1PG

The NXH040F120MNF1 is a power module containing an 40 mΩ/1200 V SiC MOSFET full bridge and a thermistor in an F1 package.

Features

- 40 mΩ/1200 V SiC MOSFET Half−Bridge
- Thermistor
- Options with Pre−Applied Thermal Interface Material (TIM) and without Pre−Applied TIM
- Press−Fit Pins
- These Devices are Pb−Free, Halide Free and are RoHS Compliant

Typical Applications

- Solar Inverter
- Uninterruptible Power Supplies
- Electric Vehicle Charging Stations
- Industrial Power

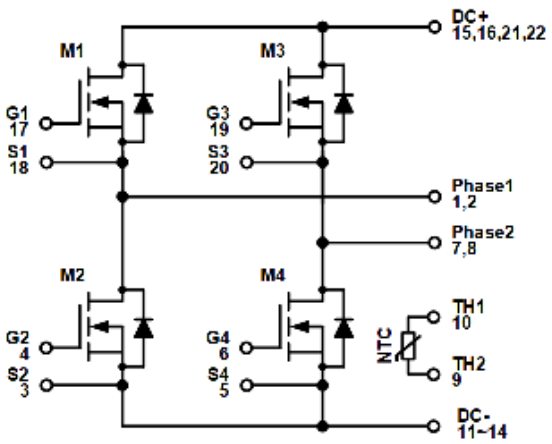
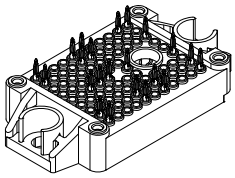


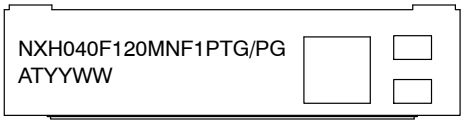
Figure 1. NXH040F120MNF1 Schematic Diagram

PACKAGE PICTURE



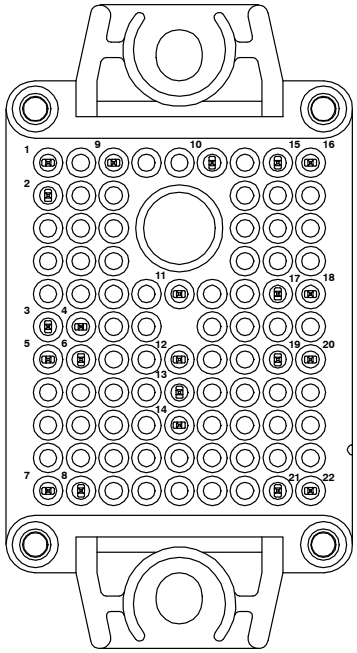
PIM22 33.8x42.5 (PRESS FIT)
CASE 180BX

MARKING DIAGRAM



XXXXX = Specific Device Code
AT = Assembly & Test Site Code
YWW = Year and Work Week Code

PIN CONNECTIONS



See Pin Function Description for pin names

ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

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PIN FUNCTION DESCRIPTION

Pin	Name	Description
1	Phase 1	Center point of M1 and M2
2	Phase 1	Center point of M1 and M2
3	S2	M2 Kelvin Emitter (High side switch)
4	G2	M2 Gate (High side switch)
5	S4	M4 Kelvin Emitter (High side switch)
6	G4	M4 Gate (High side switch)
7	AC2	Center point of M3 and M4
8	AC2	Center point of M3 and M4
9	TH2	Thermistor Connection 2
10	TH1	Thermistor Connection 1
11	DC–	DC Negative Bus connection
12	DC–	DC Negative Bus connection
13	DC–	DC Negative Bus connection
14	DC–	DC Negative Bus connection
15	DC+	DC Positive Bus connection
16	DC+	DC Positive Bus connection
17	G1	M1 Gate (High side switch)
18	S1	M1 Kelvin Emitter (High side switch)
19	G3	M3 Gate (Low side switch)
20	S3	M3 Kelvin Emitter (High side switch)
21	DC+	DC Positive Bus connection
22	DC+	DC Positive Bus connection

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
SiC MOSFET			
Drain−Source Voltage	V_{DSS}	1200	V
Gate−Source Voltage	V_{GS}	+25/−15	V
Continuous Drain Current @ T_C = 80°C (T_J = 175°C)	I_D	30	A
Pulsed Drain Current (T_J = 175°C)	I_{Dpulse}	60	A
Maximum Power Dissipation @ T_C = 80°C (T_J = 175°C)	P_{tot}	113	W
Minimum Operating Junction Temperature	T_{JMIN}	−40	°C
Maximum Operating Junction Temperature	T_{JMAX}	175	°C
THERMAL PROPERTIES			
Storage Temperature Range	T_{stg}	−40 to 150	°C
INSULATION PROPERTIES			
Isolation Test Voltage, t = 1 s, 60 Hz	V_{is}	4800	V_{RMS}
Creepage Distance		12.7	mm

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.

RECOMMENDED OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Module Operating Junction Temperature	T_J	−40	175	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS

T_J = 25 °C unless otherwise noted

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
SiC MOSFET CHARACTERISTICS						
Drain−Source Breakdown Voltage	V_{GS} = 0 V, I_D = 200 μA	$V_{(BR)DSS}$	1200	–	–	V
Zero Gate Voltage Drain Current	V_{GS} = 0 V, V_{DS} = 1200 V	I_{DSS}	–	–	100	μA
Drain−Source On Resistance	V_{GS} = 20 V, I_D = 25 A, T_J = 25°C	$R_{DS(ON)}$	–	42	56	mΩ
	V_{GS} = 20 V, I_D = 25 A, T_J = 125°C		–	55	–	
	V_{GS} = 20 V, I_D = 25 A, T_J = 150°C		–	61	–	
Gate−Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 10 mA	$V_{GS(TH)}$	1.8	2.81	4.3	V
Gate Leakage Current	V_{GS} = −10 V/20 V, V_{DS} = 0 V	I_{GSS}	−500	–	500	nA
Input Capacitance	V_{DS} = 800 V, V_{GS} = 0 V, f = 1 MHz	C_{ISS}	–	1 505	–	pF
Reverse Transfer Capacitance		C_{RSS}	–	12	–	
Output Capacitance		C_{OSS}	–	159	–	
Total Gate Charge	V_{DS} = 800 V, V_{GS} = 20 V, I_D = 25 A	$Q_{G(TOTAL)}$	–	122.1	–	nC
Gate−Source Charge		Q_{GS}	–	32.2	–	nC
Gate−Drain Charge		Q_{GD}	–	34.7	–	nC
Turn−on Delay Time	T_J = 25°C, V_{DS} = 600 V, I_D = 25 A, V_{GS} = −5 V/18 V, R_G = 2.2 Ω	$t_{d(on)}$	–	30.8	–	ns
Rise Time		t_r	–	3.04	–	
Turn−off Delay Time		$t_{d(off)}$	–	59.8	–	
Fall Time		t_f	–	7.42	–	
Turn−on Switching Loss per Pulse		E_{ON}	–	0.06	–	mJ
Turn off Switching Loss per Pulse		E_{OFF}	–	0.10	–	
Turn−on Delay Time	T_J = 150°C, V_{DS} = 600 V, I_D = 25 A, V_{GS} = −5 V/18 V, R_G = 2.2 Ω	$t_{d(on)}$	–	30.2	–	ns
Rise Time		t_r	–	3.19	–	
Turn−off Delay Time		$t_{d(off)}$	–	64.4	–	
Fall Time		t_f	–	5.83	–	
Turn−on Switching Loss per Pulse		E_{ON}	–	0.05	–	mJ
Turn off Switching Loss per Pulse		E_{OFF}	–	0.12	–	
Diode Forward Voltage	I_D = 25 A, T_J = 25°C	V_{SD}	–	3.97	6	V
	I_D = 25 A, T_J = 125°C		–	3.52	–	
	I_D = 25 A, T_J = 150°C		–	3.44	–	
Reverse Recovery Time	T_J = 25°C, V_{DS} = 600 V, I_D = 25 A, V_{GS} = −5 V/18 V, R_G = 2.2 Ω	t_{rr}	–	18.25	–	ns
Reverse Recovery Charge		Q_{rr}	–	700	–	nC
Peak Reverse Recovery Current		I_{RRM}	–	61	–	A
Peak Rate of Fall of Recovery Current		di/dt	–	7629	–	A/μs
Reverse Recovery Energy		E_{rr}	–	405	–	μJ

ELECTRICAL CHARACTERISTICS (continued)
T_J = 25 °C unless otherwise noted

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
SiC MOSFET CHARACTERISTICS						
Reverse Recovery Time	T_J = 25°C, V_{DS} = 600 V, I_D = 25 A, V_{GS} = −5 V/18 V, R_G = 2.2 Ω	t_{rr}	–	20.81	–	ns
Reverse Recovery Charge		Q_{rr}	–	1250	–	nC
Peak Reverse Recovery Current		I_{RRM}	–	97	–	A
Peak Rate of Fall of Recovery Current		di/dt	–	11 414	–	A/μs
Reverse Recovery Energy		E_{rr}	–	753	–	μJ
Thermal Resistance – Chip−to−Case	M1, M2, M3, M4	R_{thJC}	–	0.8356	–	°C/W
Thermal Resistance – Chip−to−Heatsink	Thermal grease, Thickness = 2 Mil ±2%, A = 2.8 W/mK	R_{thJH}	–	1.291	–	°C/W
THERMISTOR CHARACTERISTICS						
Nominal Resistance	T_{NTC} = 25°C	R_{25}	–	5	–	kΩ
Nominal Resistance	T_{NTC} = 100°C	R_{100}	–	493	–	Ω
Nominal Resistance	T_{NTC} = 150°C	R_{150}	–	159.5	–	Ω
Deviation of R_{100}	T_{NTC} = 100°C	ΔR/R	−5	–	5	%
Power dissipation – recommended limit	0.15 mA, non−self−heating effect	P_D	–	0.1	–	mW
Power dissipation – absolute maximum	5 mA	P_D	–	34.2	–	mW
Power Dissipation Constant	–	–	–	1.4	–	mW/K
B−value	B(25/50), tolerance ±2%	–	–	3375	–	K
B−value	B(25/100), tolerance ±2%	–	–	3436	–	K

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

ORDERING INFORMATION

Orderable Part Number	Marking	Package	Shipping
NXH040F120MNF1PTG	NXH040F120MNF1PTG	F1−4PACK Press−fit Pins with pre−applied thermal interface material (TIM) (Pb−Free and Halide−Free)	28 Units / Blister Tray
NXH040F120MNF1PG	NXH040F120MNF1PG	F1−4PACK Press−fit Pins (Pb−Free and Halide−Free)	28 Units / Blister Tray

TYPICAL CHARACTERISTICS

(25°C UNLESS OTHERWISE NOTED)

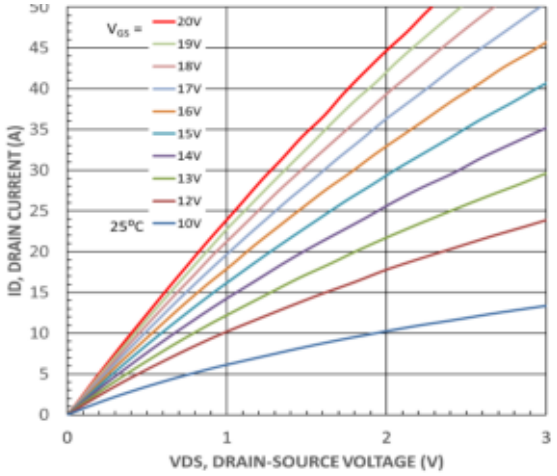


Figure 2. MOSFET Typical Output Characteristics

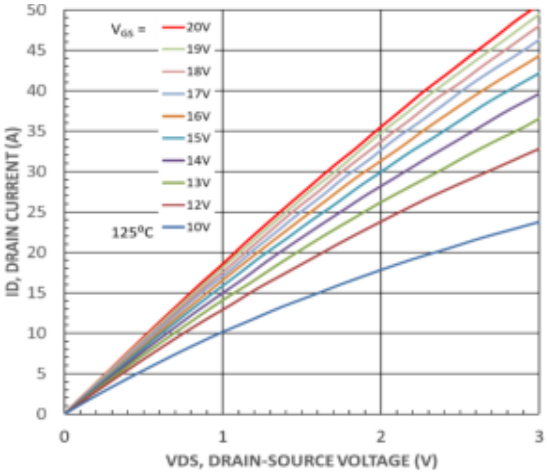


Figure 3. MOSFET Typical Output Characteristics

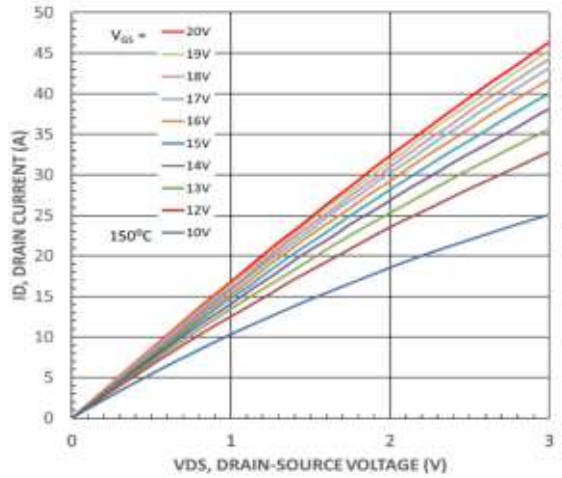


Figure 4. MOSFET Typical Output Characteristics

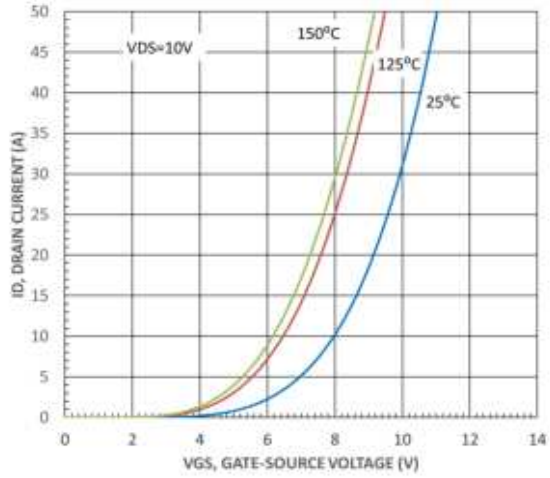


Figure 5. MOSFET Typical Transfer Characteristics

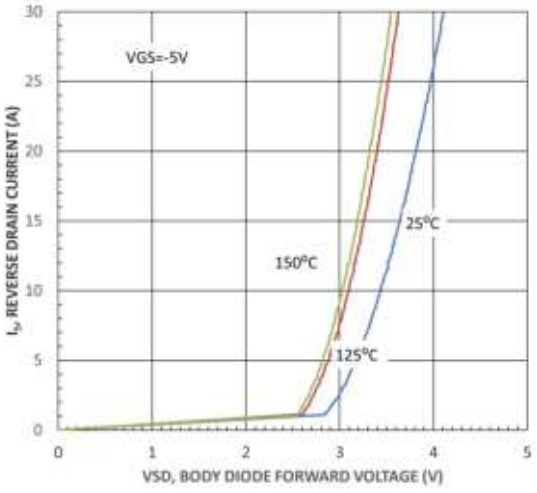


Figure 6. Body Diode Forward Characteristic

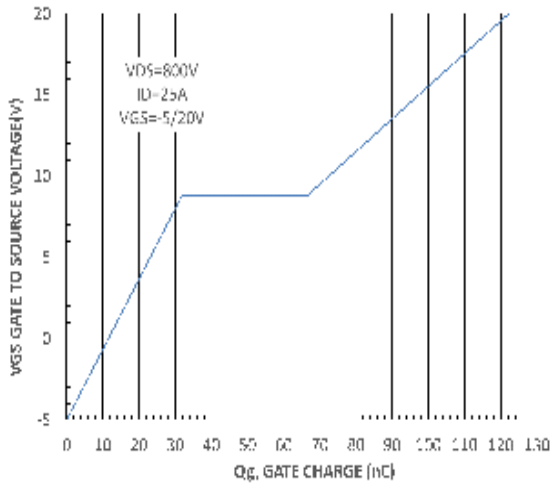


Figure 7. Gate−to−Source Voltage vs. Total Charge

TYPICAL CHARACTERISTICS (CONTINUED)

(25°C UNLESS OTHERWISE NOTED)

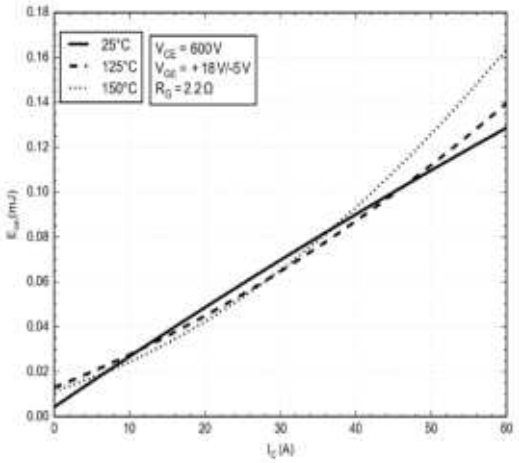


Figure 8. Typical Switching Loss E_{ON} vs. I_C

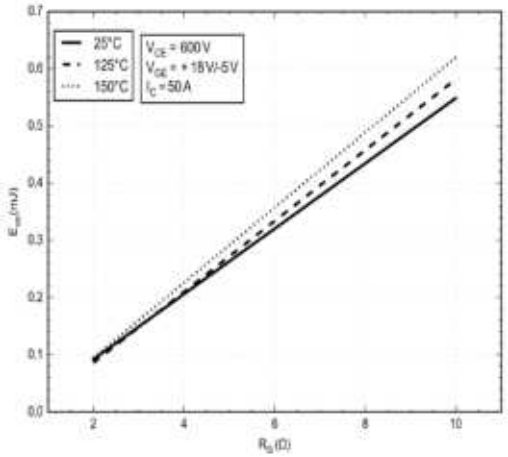


Figure 9. Typical Switching Loss E_{ON} vs. R_G

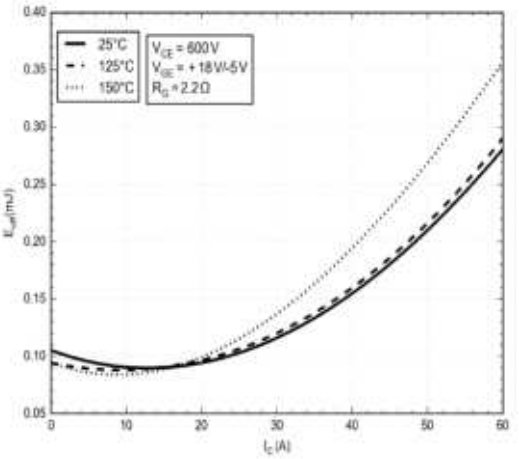


Figure 10. Typical Switching Loss E_{OFF} vs. I_C

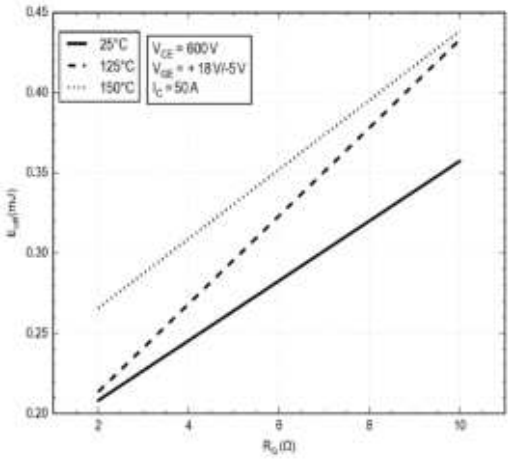


Figure 11. Typical Switching Loss E_{OFF} vs. R_G

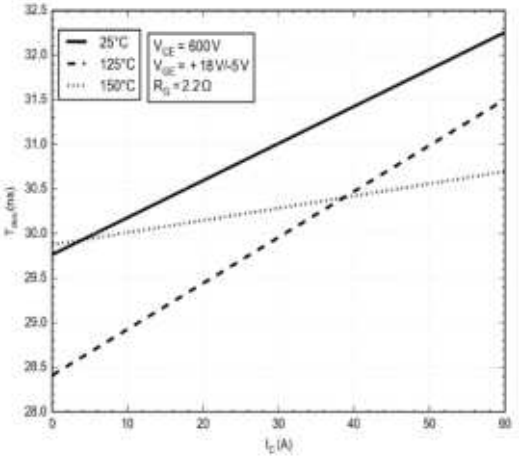


Figure 12. Typical Turn−On Switching T_{don} vs. I_C

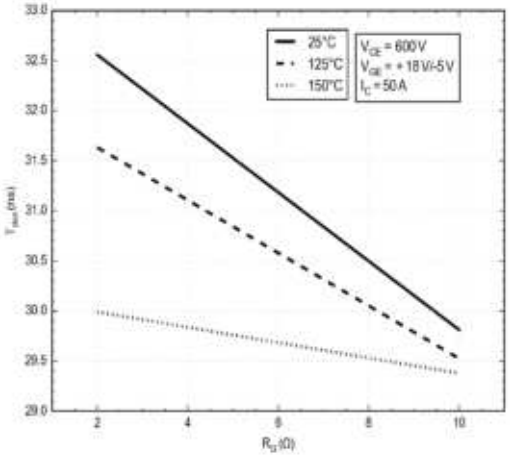


Figure 13. Typical Turn−On Switching T_{don} vs. R_G

TYPICAL CHARACTERISTICS (CONTINUED)

(25°C UNLESS OTHERWISE NOTED)

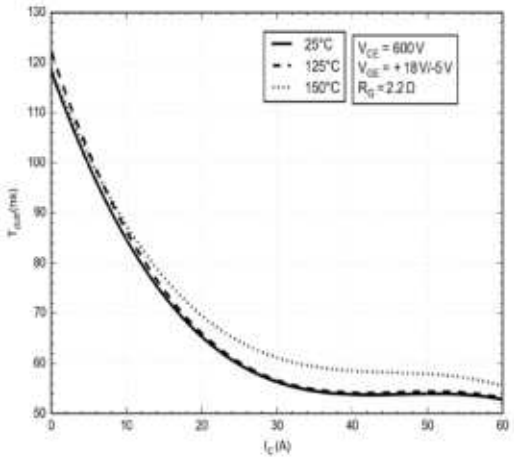


Figure 14. Typical Turn−Off Switching T_{doff} vs. I_C

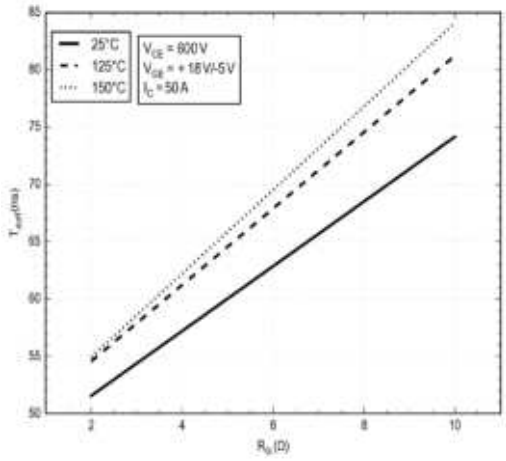


Figure 15. Typical Turn−Off Switching T_{doff} vs. R_G

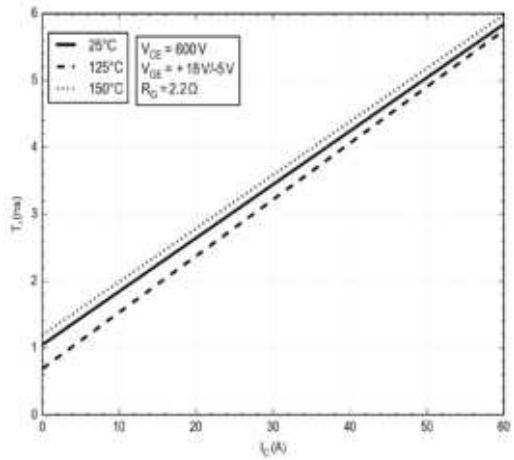


Figure 16. Typical Turn−On Switching T_r vs. I_C

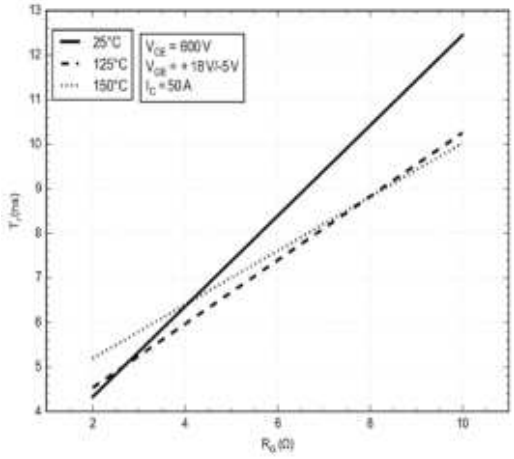


Figure 17. Typical Turn−On Switching T_r vs. R_G

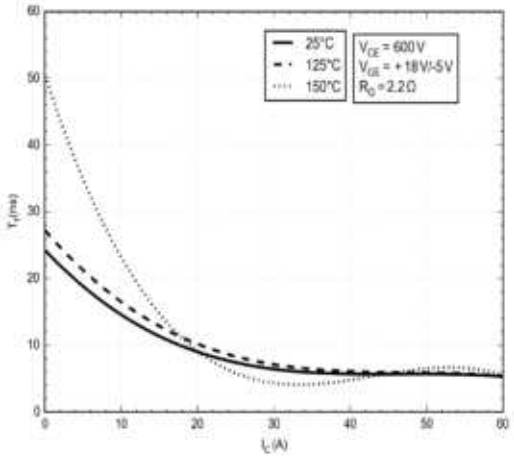


Figure 18. Typical Turn−Off Switching T_f vs. I_C

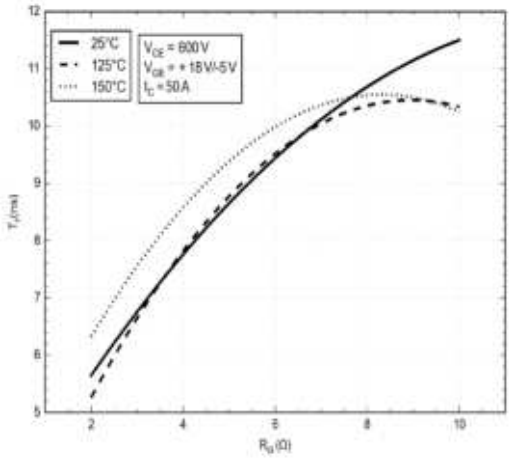


Figure 19. Typical Turn−Off Switching T_f vs. R_G

TYPICAL CHARACTERISTICS (CONTINUED)

(25°C UNLESS OTHERWISE NOTED)

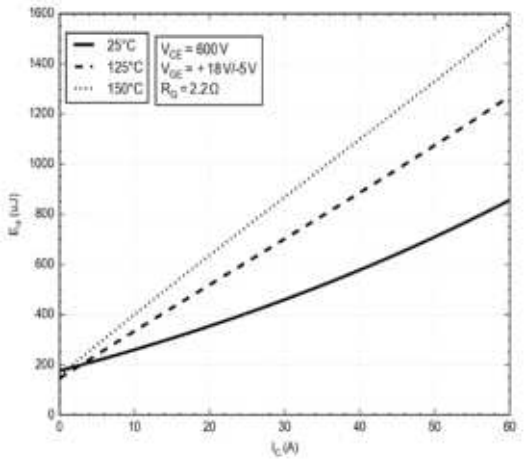


Figure 20. Typical Reverse Recovery Energy vs. I_C

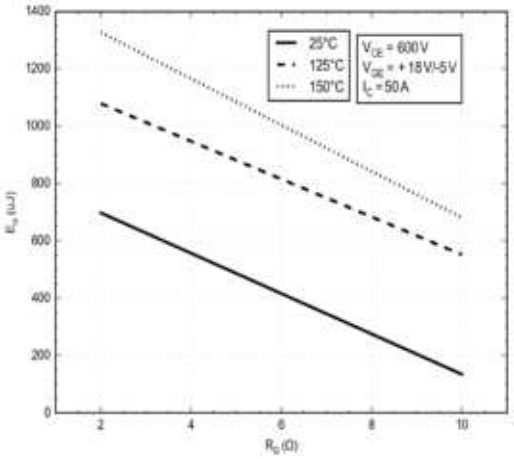


Figure 21. Typical Reverse Recovery Energy vs. R_G

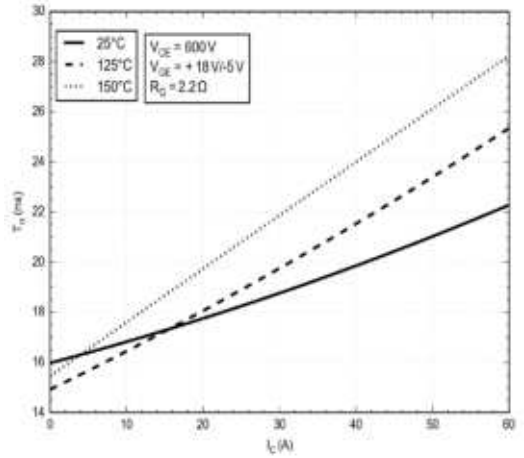


Figure 22. Typical Reverse Recovery Time vs. I_C

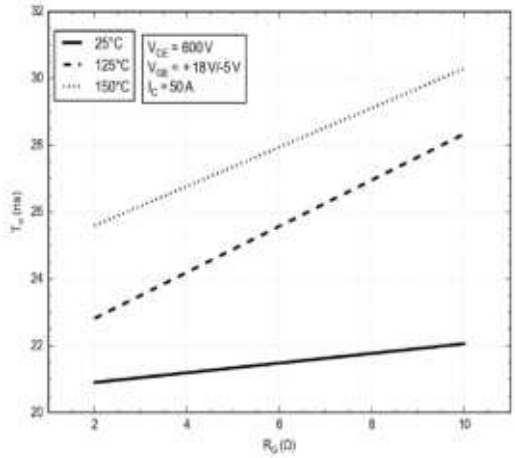


Figure 23. Typical Reverse Recovery Time vs. R_G

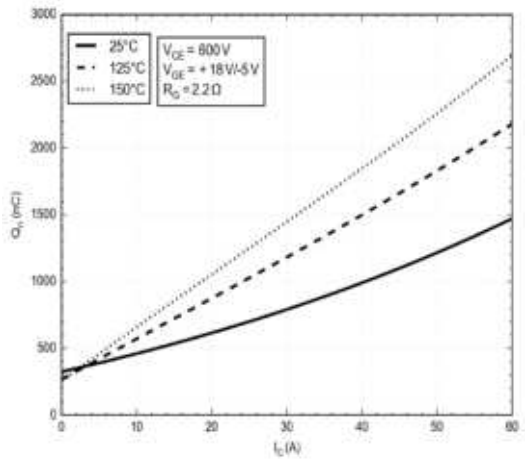


Figure 24. Typical Reverse Recovery Charge vs. I_C

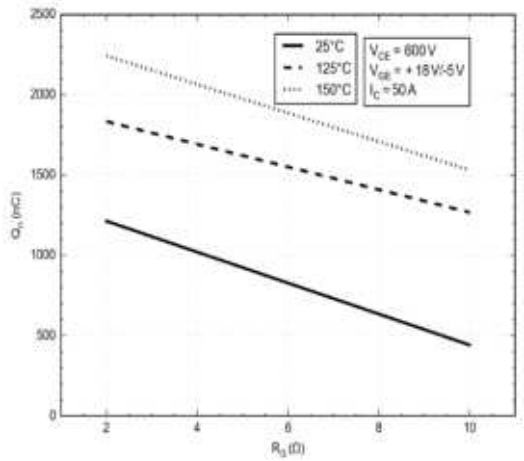


Figure 25. Typical Reverse Recovery Charge vs. R_G

TYPICAL CHARACTERISTICS (CONTINUED)

(25°C UNLESS OTHERWISE NOTED)

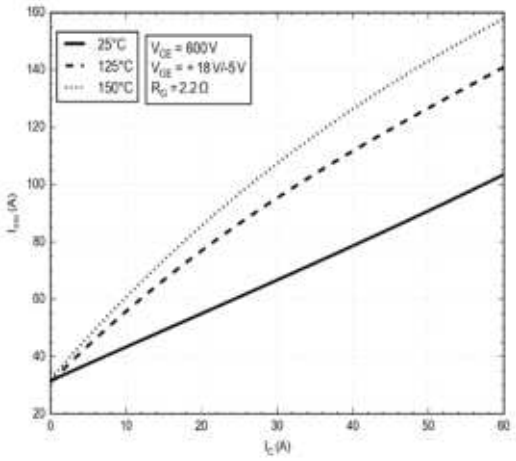


Figure 26. Typical Reverse Recovery Current vs. I_C

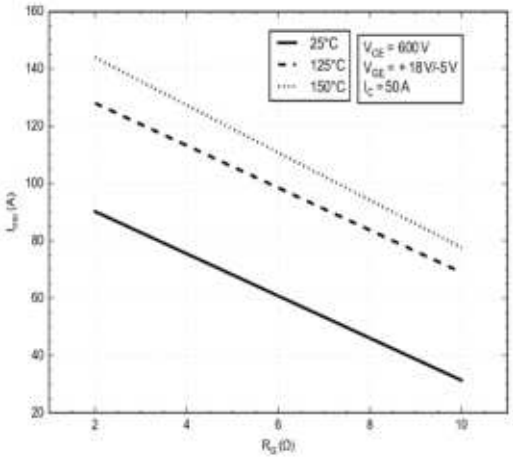


Figure 27. Typical Reverse Recovery Current vs. R_G

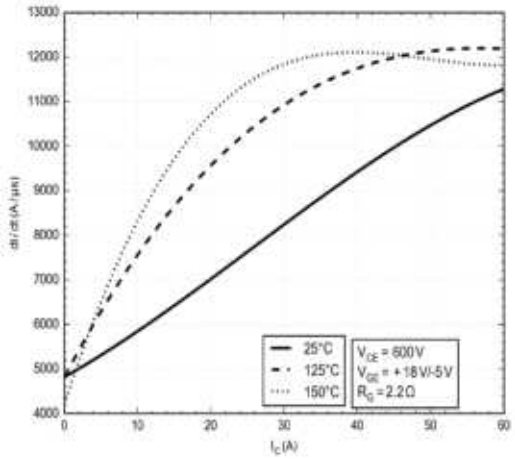


Figure 28. Typical di/dt vs. I_C

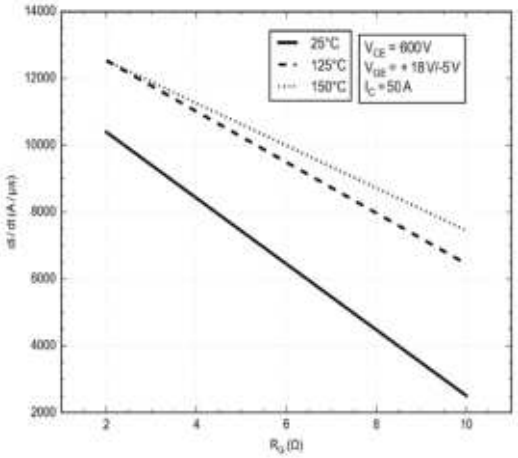


Figure 29. Typical di/dt vs. R_G

TYPICAL CHARACTERISTICS (CONTINUED)

(25°C UNLESS OTHERWISE NOTED)

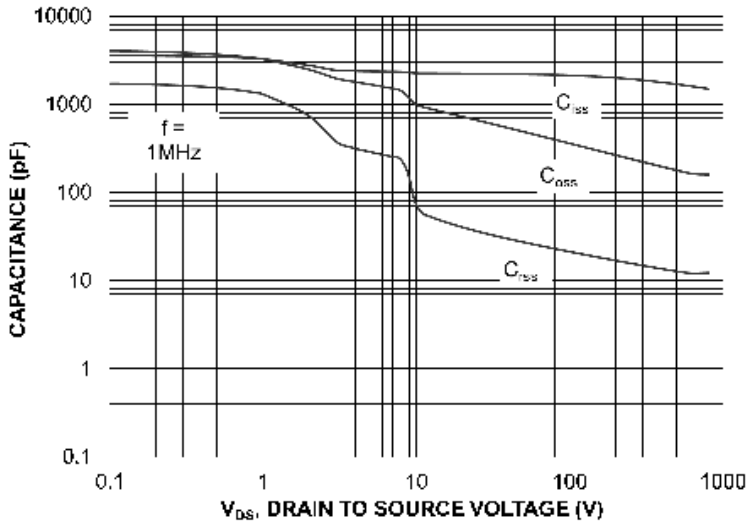


Figure 30. Capacitance vs. Drain−to−Source Voltage

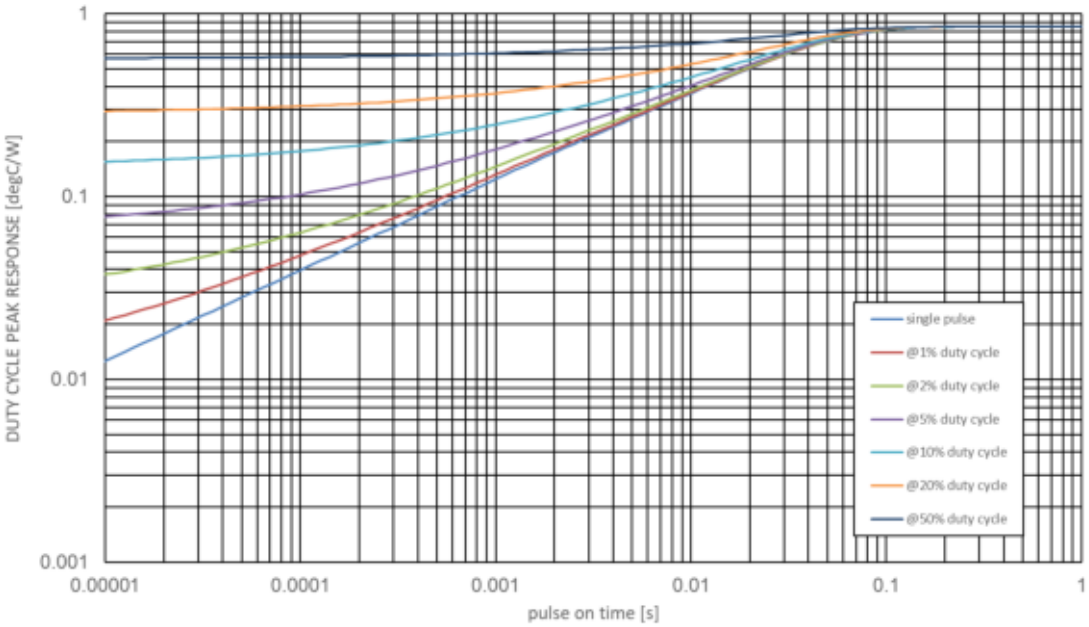


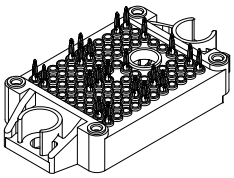
Figure 31. MOSFET Junction−to−Case Transient Thermal Impedance

Table 1. FOSTER NETWORKS – M1, M2, M3, M4

Foster Element #	M1, M3		M2, M4	
	Rth (K/W)	Cth (Ws/K)	Rth (K/W)	Cth (Ws/K)
1	0.051996	0.002404	0.054881	0.002284
2	0.046504	0.020373	0.010554	0.082427
3	0.008903	0.221087	0.064895	0.028973
4	0.165341	0.039489	0.094862	0.058574
5	0.600991	0.065660	0.610507	0.052914

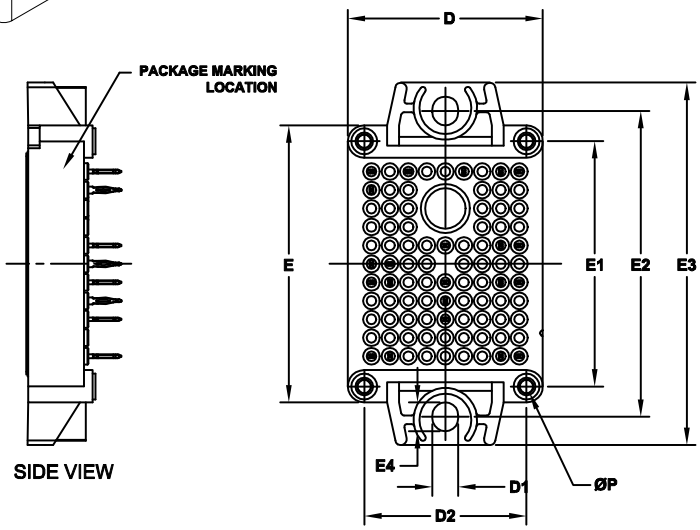
Table 2. CAUER NETWORKS – M1, M2, M3, M4

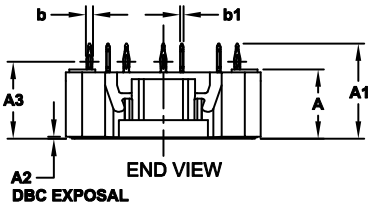
Cauer Element #	M1, M3		M2, M4	
	Rth (K/W)	Cth (Ws/K)	Rth (K/W)	Cth (Ws/K)
1	0.076857	0.001961	0.076754	0.001921
2	0.141063	0.010485	0.182594	0.011596
3	0.274014	0.018050	0.136313	0.018196
4	0.113973	0.038620	0.215815	0.019717
5	0.267827	0.046224	0.224225	0.049799



PIM22 33.8x42.5 (PRESS FIT)
CASE 180BX
ISSUE A

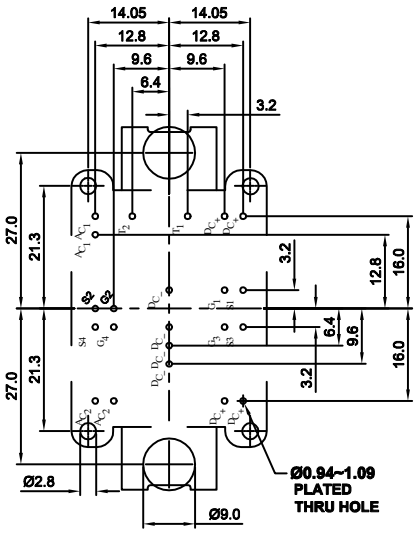
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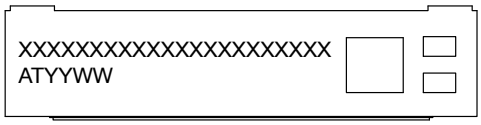
NOTES:
1. CONTROLLING DIMENSION: MILLIMETERS
2. PIN POSITION TOLERANCE IS ± 0.4mm

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	11.65	12.00	12.35
A1	16.00	16.50	17.00
A2	0.00	0.35	0.60
A3	12.85	13.35	13.85
b	1.15	1.20	1.25
b1	0.59	0.64	0.69
D	33.50	33.80	34.10
D1	4.40	4.50	4.60
D2	27.95	28.10	28.25
E	47.70	48.00	48.30
E1	42.35	42.50	42.65
E2	52.90	53.00	53.10
E3	62.30	62.80	63.30
E4	4.90	5.00	5.10
P	2.20	2.30	2.40

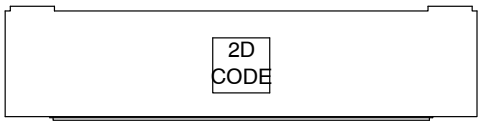


RECOMMENDED MOUNTING PATTERN

GENERIC MARKING DIAGRAM*



FRONTSIDE MARKING



BACKSIDE MARKING

XXXXX = Specific Device Code
AT = Assembly & Test Site Code
YYWW = Year and Work Week Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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