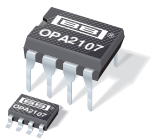
OPA2107



SBOS161A – JANUARY 1989 – REVISED JULY 2003

Precision Dual *Difet* ® Operational Amplifier

FEATURES

- **Very Low Noise: 8nV/$\sqrt{Hz}$ at 10kHz**
- **Low V_{OS}: 1mV max**
- **Low Drift: 10μV/°C max**
- **Low I_B: 10pA max**
- **Fast Settling Time: 2μs to 0.01%**
- **Unity-Gain Stable**

APPLICATIONS

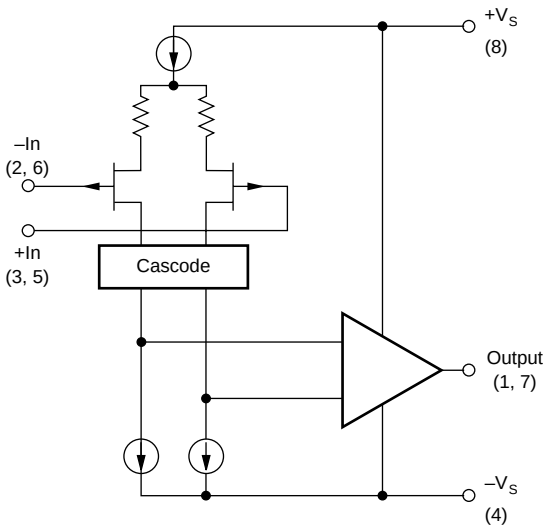
- **Data Acquisition**
- **DAC Output Amplifiers**
- **Optoelectronics**
- **High-Impedance Sensor Amps**
- **High-Performance Audio Circuitry**
- **Medical Equipment, CT Scanners**

DESCRIPTION

The OPA2107 dual operational amplifier provides precision ***Difet*** performance with the cost and space savings of a dual op amp. It is useful in a wide range of precision and low-noise analog circuitry and can be used to upgrade the performance of designs currently using BIFET® type amplifiers.

The OPA2107 is fabricated on a proprietary dielectrically isolated (***Difet***) process. This holds input bias currents to very low levels without sacrificing other important parameters, such as input offset voltage, drift and noise. Laser-trimmed input circuitry yields excellent dc performance. Superior dynamic performance is achieved, yet quiescent current is held to under 2.5mA per amplifier. The OPA2107 is unity-gain stable.

The OPA2107 is available in DIP-8 and SO-8 packages.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage	±18V
Input Voltage Range	$\pm V_S$ ±2V
Differential Input Voltage	Total V_S ±4V
Operating Temperature	
P and U Packages	–25°C to + 85°C
Storage Temperature	
P and U Packages	–40°C to +125°C
Output Short Circuit to Ground (T_A = +25°C)	Continuous
Junction Temperature	+175°C
Lead Temperature	
P Package (soldering, 10s)	+300°C
U Package, SOIC (3s)	+260°C

NOTE: Stresses above these ratings may cause permanent damage.

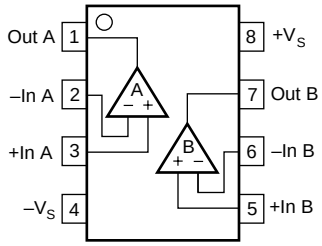
ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PIN CONFIGURATION

Top View **DIP, SO**



PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR(1)	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA2107	DIP-8	P	–25°C to +85°C	OPA2107AP	OPA2107AP	Tube, 50
OPA2107	SO-8	D	–25°C to +85°C	OPA2107AU	OPA2107AU	Tube, 100
"	"	"	"	"	OPA2107AU/2K5	Tape and Reel, 2500

NOTE: (1) For the most current specifications and package information, refer to our web site at www.ti.com.

ELECTRICAL CHARACTERISTICS

At T_A = +25°C, V_S = ±15V, unless otherwise noted.

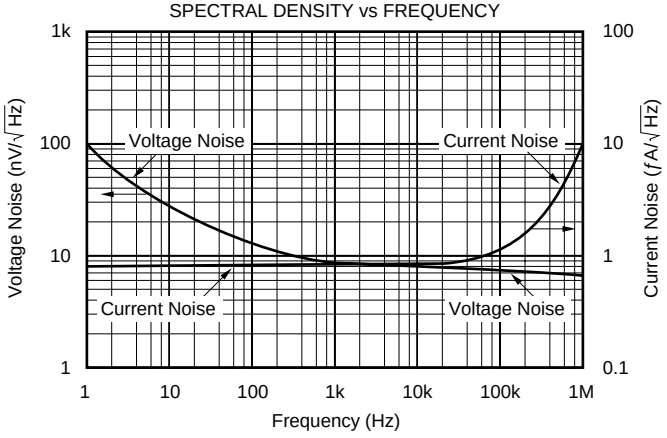
PARAMETER	CONDITION	OPA2107AP, AU			UNITS
		MIN	TYP	MAX	
OFFSET VOLTAGE(1)					
Input Offset Voltage	V_{CM} = 0V		0.1	1	mV
Over Specified Temperature			0.5	2	mV
Average Drift Over Specified Temperature			3	10	µV/°C
Power Supply Rejection	V_S = ±10 to ±18V	80	96		dB
INPUT BIAS CURRENT(1)					
Input Bias Current	V_{CM} = 0V		4	10	pA
Over Specified Temperature			0.25	1.5	nA
Input Offset Current	V_{CM} = 0V		1	8	pA
Over Specified Temperature				1	nA
INPUT NOISE					
Voltage: f = 10Hz	R_S = 0		30		nV/√Hz
f = 100Hz			12		nV/√Hz
f = 1kHz			9		nV/√Hz
f = 10kHz			8		nV/√Hz
BW = 0.1 to 10Hz			1.2		µVp-p
BW = 10 to 10kHz			0.85		µVrms
Current: f = 0.1Hz thru 20kHz			1.2		fA/√Hz
BW = 0.1Hz to 10Hz			23		fAp-p
INPUT IMPEDANCE					
Differential			10^{13} || 2		Ω || pF
Common-Mode			10^{14} || 4		Ω || pF
INPUT VOLTAGE RANGE					
Common-Mode Input Range		±10.5	±11		V
Over Specified Temperature		±10.2	±10.5		V
Common-Mode Rejection	V_{CM} = ±10V	80	94		dB
OPEN-LOOP GAIN					
Open-Loop Voltage Gain	V_O = ±10V, R_L = 2kΩ	82	96		dB
Over Specified Temperature		80	94		dB
DYNAMIC RESPONSE					
Slew Rate	G = +1	13	18		V/µs
Settling Time: 0.1%	G = –1, 10V Step		1.5		µs
0.01%			2		µs
Gain Bandwidth Product	G = 100		4.5		MHz
THD + Noise	G = +1, f = 1kHz		0.001		%
Channel Separation	f = 100Hz, R_L = 2kΩ		120		dB
POWER SUPPLY					
Specified Operating Voltage			±15		V
Operating Voltage Range		±4.5			V
Current			±4.5		mA
OUTPUT					
Voltage Output	R_L = 2kΩ	±11	±12		V
Over Specified Temperature		±10.5	±11.5		V
Short Circuit Current		±10	±40		mA
Output Resistance, Open-Loop	1MHz		70		Ω
Capacitive Load Stability	G = +1		1000		pF
TEMPERATURE RANGE					
Specification		–25		+85	°C
Operating		–25		+85	°C
Storage		–40		+125	°C
Thermal Resistance (θ_{J-A})					
DIP-8			90		°C/W
SO-8			175		°C/W

NOTE: (1) Specified with devices fully warmed up.

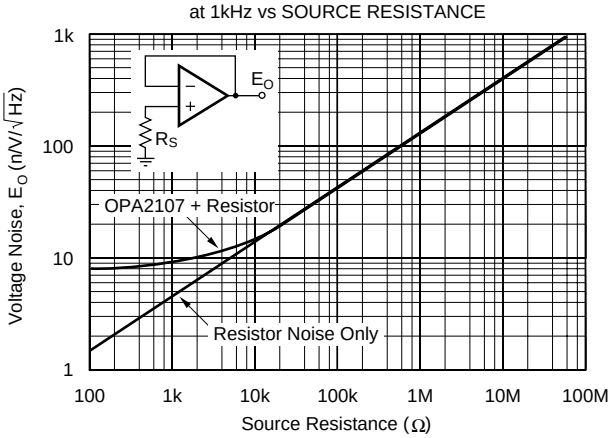
TYPICAL CHARACTERISTICS

T_A = +25°C, V_S = ±15V unless otherwise noted.

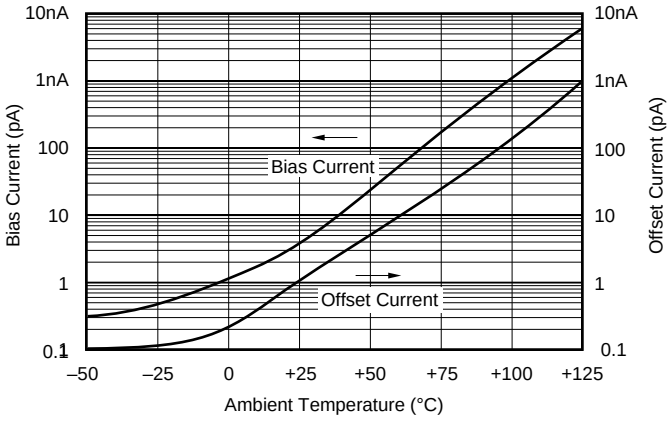
INPUT VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY vs FREQUENCY



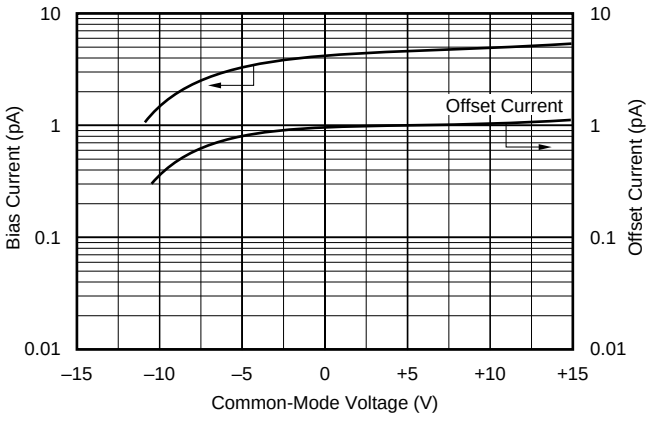
TOTAL INPUT VOLTAGE NOISE SPECTRAL DENSITY at 1kHz vs SOURCE RESISTANCE



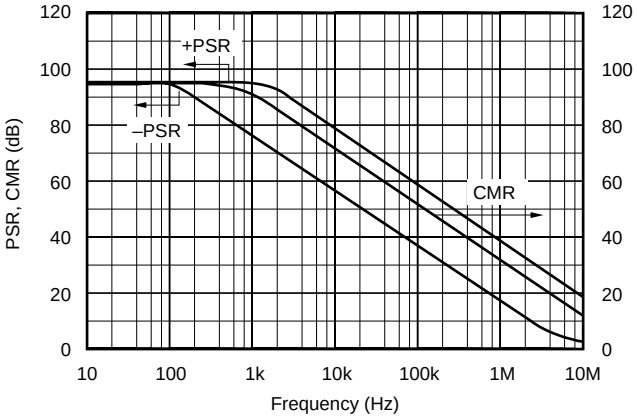
INPUT BIAS AND OFFSET CURRENT vs TEMPERATURE



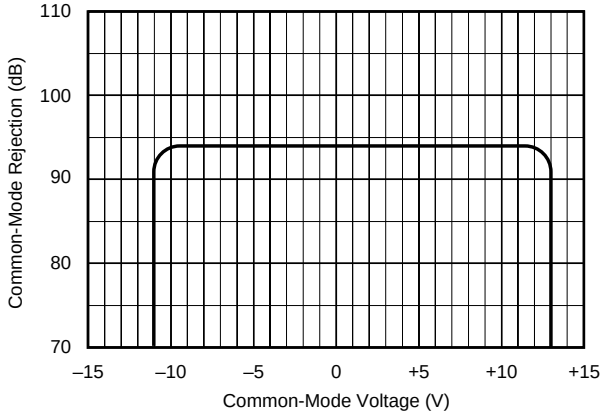
INPUT BIAS AND OFFSET CURRENT vs INPUT COMMON-MODE VOLTAGE



POWER SUPPLY AND COMMON-MODE REJECTION vs FREQUENCY



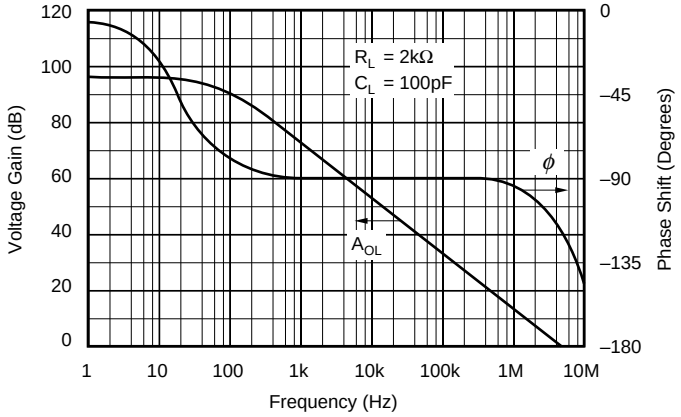
COMMON-MODE REJECTION vs INPUT COMMON-MODE VOLTAGE



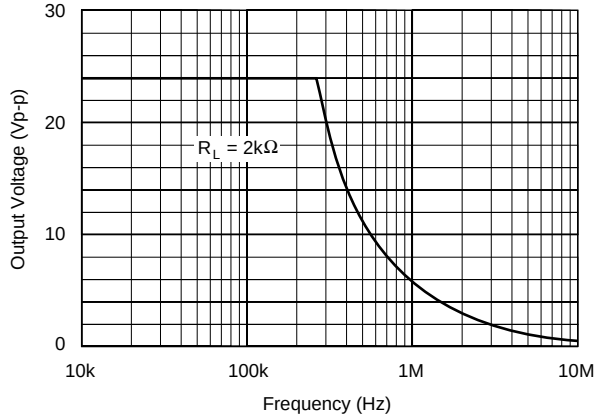
TYPICAL CHARACTERISTICS (Cont.)

T_A = +25°C, V_S = ±15V unless otherwise noted.

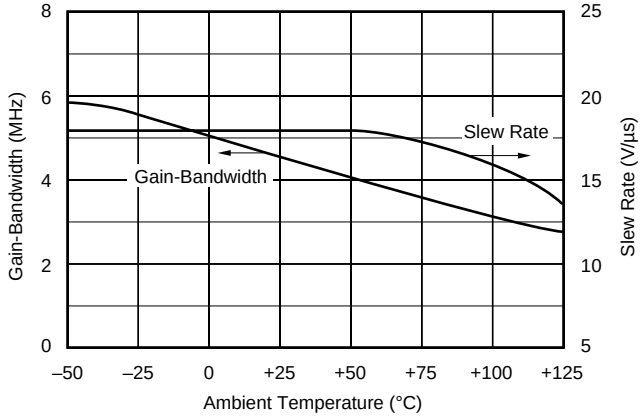
OPEN-LOOP FREQUENCY RESPONSE



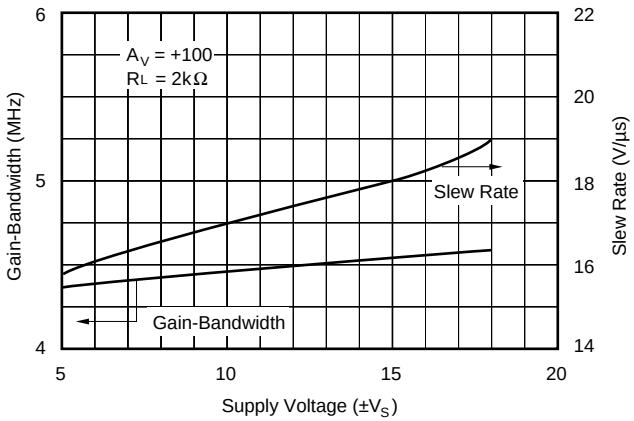
MAXIMUM OUTPUT VOLTAGE SWING vs FREQUENCY



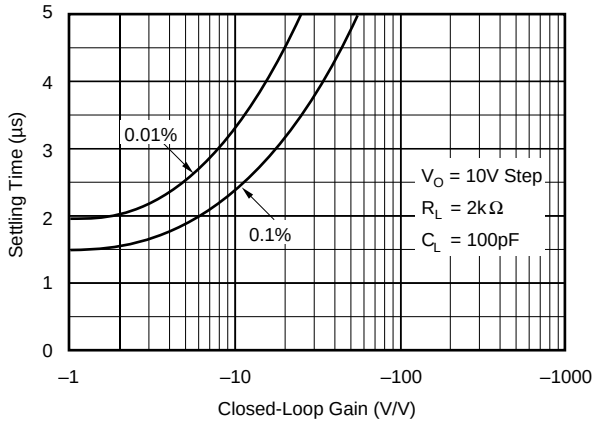
GAIN-BANDWIDTH AND SLEW RATE vs TEMPERATURE



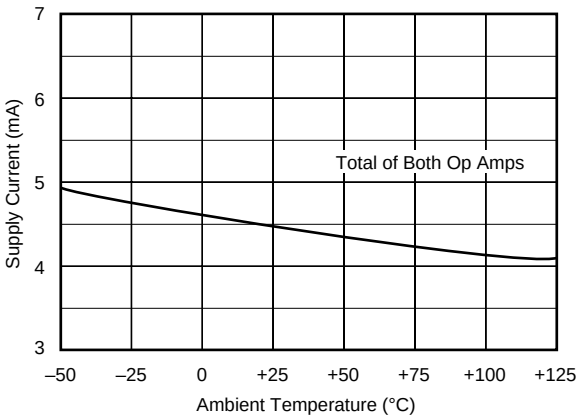
GAIN-BANDWIDTH AND SLEW RATE vs SUPPLY VOLTAGE



SETTLING TIME vs CLOSED-LOOP GAIN



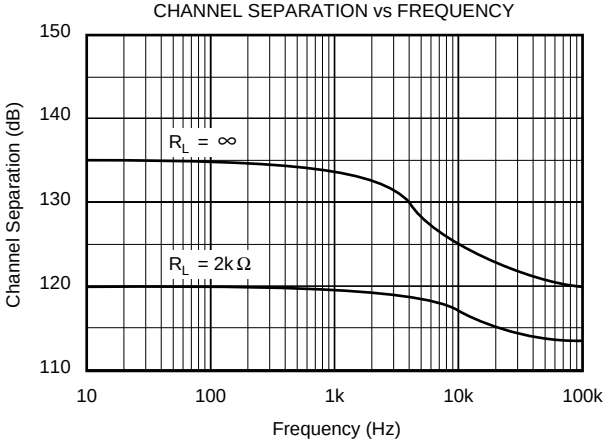
SUPPLY CURRENT vs TEMPERATURE



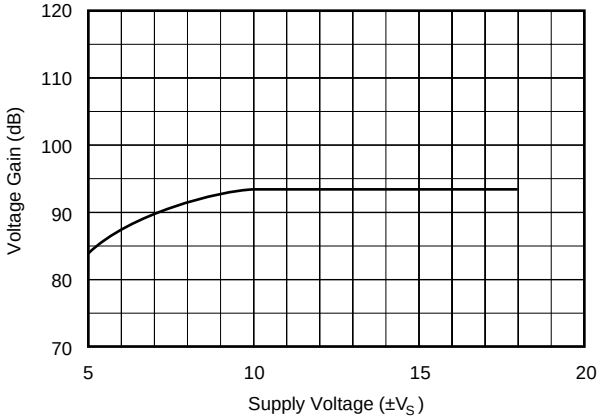
TYPICAL CHARACTERISTICS (Cont.)

T_A = +25°C, V_S = ±15V unless otherwise noted.

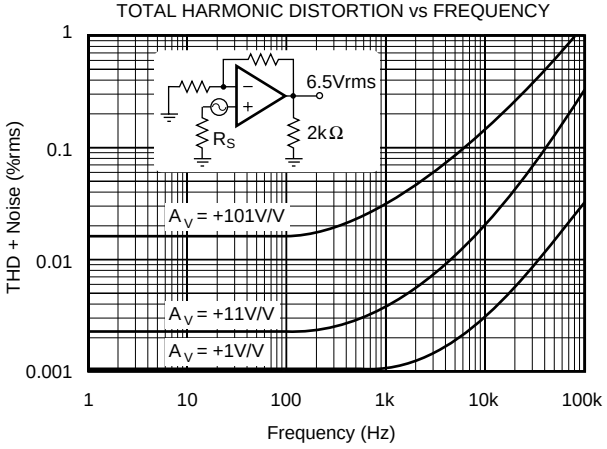
CHANNEL SEPARATION vs FREQUENCY



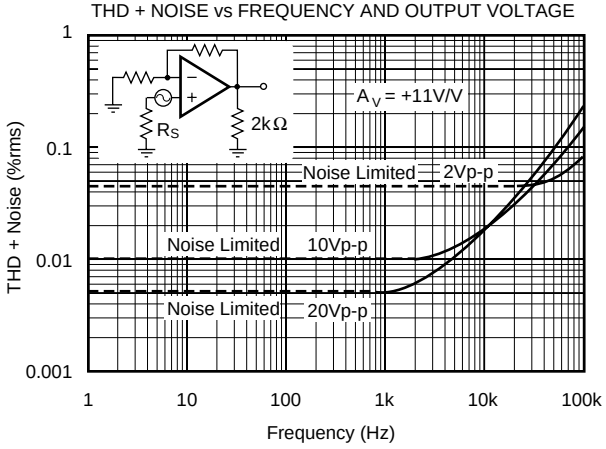
OPEN-LOOP GAIN vs SUPPLY VOLTAGE



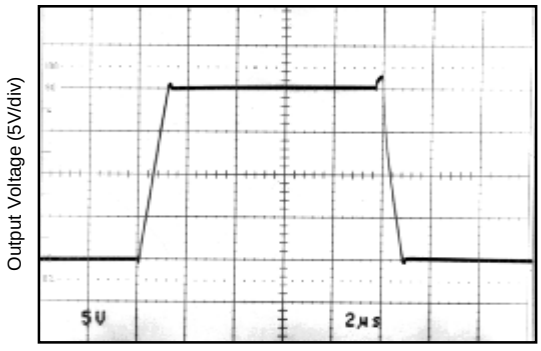
TOTAL HARMONIC DISTORTION vs FREQUENCY



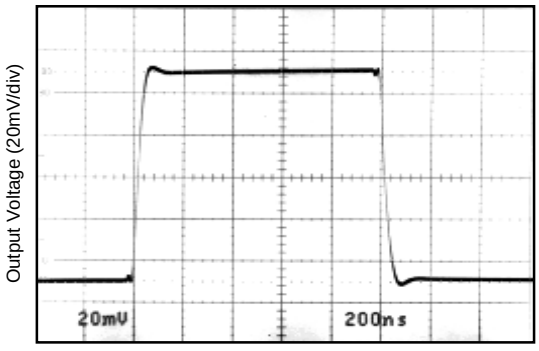
THD + NOISE vs FREQUENCY AND OUTPUT VOLTAGE



LARGE-SIGNAL RESPONSE



SMALL-SIGNAL RESPONSE



APPLICATIONS INFORMATION AND CIRCUITS

The OPA2107 is unity-gain stable and has an excellent phase margin. This makes it easy to use in a wide variety of applications.

Power-supply connections should be bypassed with capacitors positioned close to the amplifier pins. In most cases, 0.1µF ceramic capacitors are adequate. Applications with larger load currents and fast transient signals may need up to 1µF tantalum bypass capacitors.

INPUT BIAS CURRENT

The OPA2107 ***Difet*** input stages have very low input bias current—an order of magnitude lower than BIFET op amps. Circuit-board leakage paths can significantly degrade performance. This is especially evident with the SO-8 surface-mount package where pin-to-pin dimensions are particularly small. Residual soldering flux, dirt, and oils, which conduct leakage current, can be removed by proper cleaning. In most instances, a two-step cleaning process is adequate using a clean organic solvent rinse followed by deionized water. Each rinse should be followed by a 30-minute bake at 85°C.

A circuit-board guard pattern effectively reduces errors due to circuit-board leakage (Figure 1). By encircling critical high-impedance nodes with a low-impedance connection at the same circuit potential, any leakage currents will flow harmlessly to the low-impedance node. Guard traces should be placed on all levels of a multiple-layer circuit board.

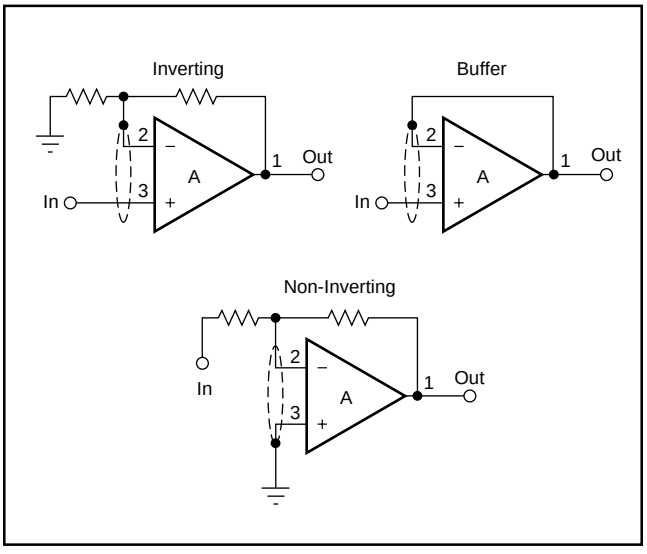


FIGURE 1. Connection of Input Guard.

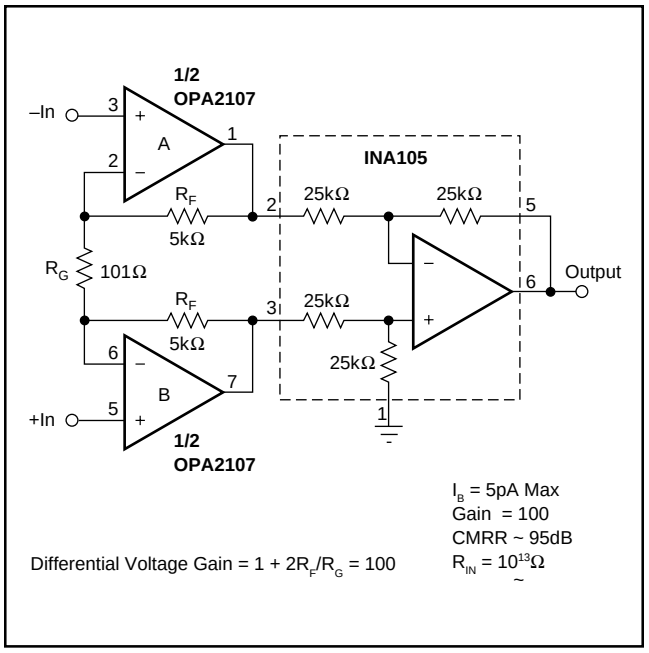
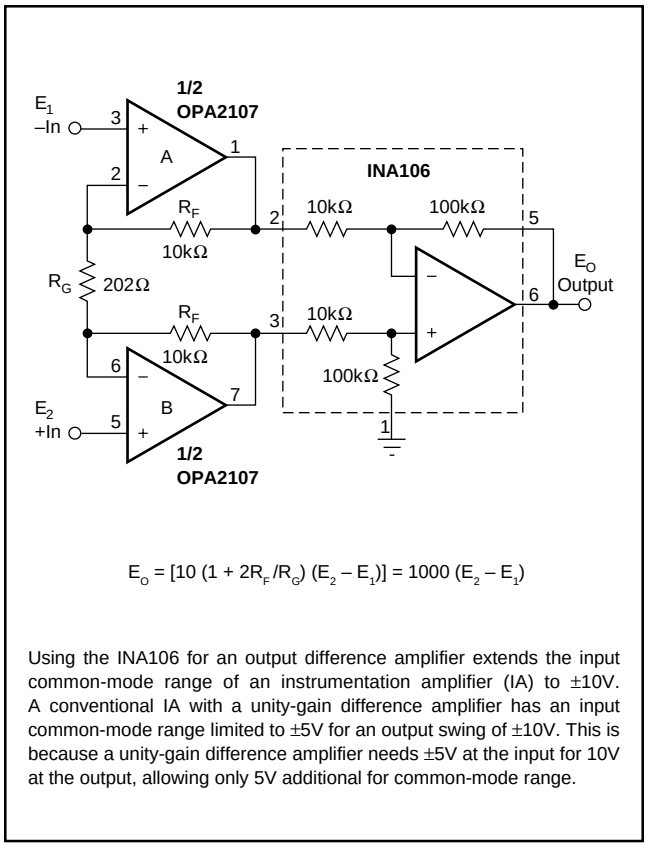


FIGURE 2. FET Input Instrumentation Amplifier.



Using the INA106 for an output difference amplifier extends the input common-mode range of an instrumentation amplifier (IA) to ±10V. A conventional IA with a unity-gain difference amplifier has an input common-mode range limited to ±5V for an output swing of ±10V. This is because a unity-gain difference amplifier needs ±5V at the input for 10V at the output, allowing only 5V additional for common-mode range.

FIGURE 3. Precision Instrumentation Amplifier.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2107AU	Last Time Buy	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-25 to 80	OPA 2107AU
OPA2107AU.A	Last Time Buy	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-25 to 80	OPA 2107AU
OPA2107AU/2K5	Last Time Buy	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-25 to 85	OPA 2107AU
OPA2107AU/2K5.A	Last Time Buy	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-25 to 85	OPA 2107AU

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

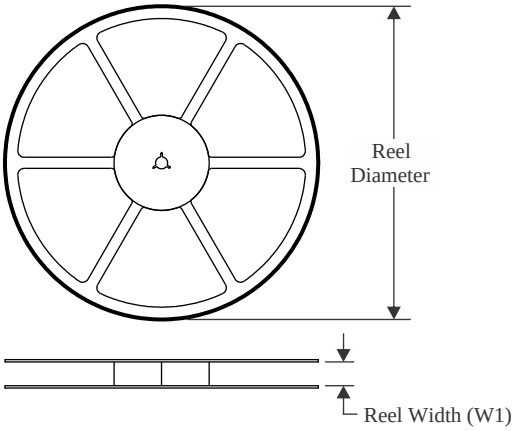
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

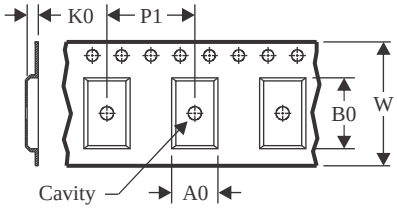
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

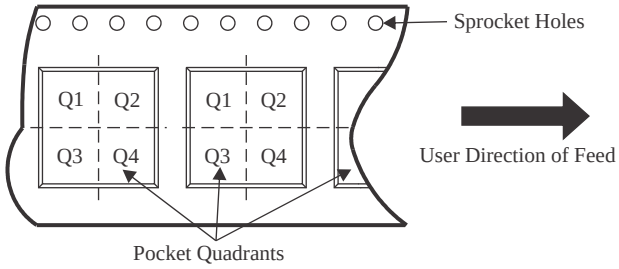


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

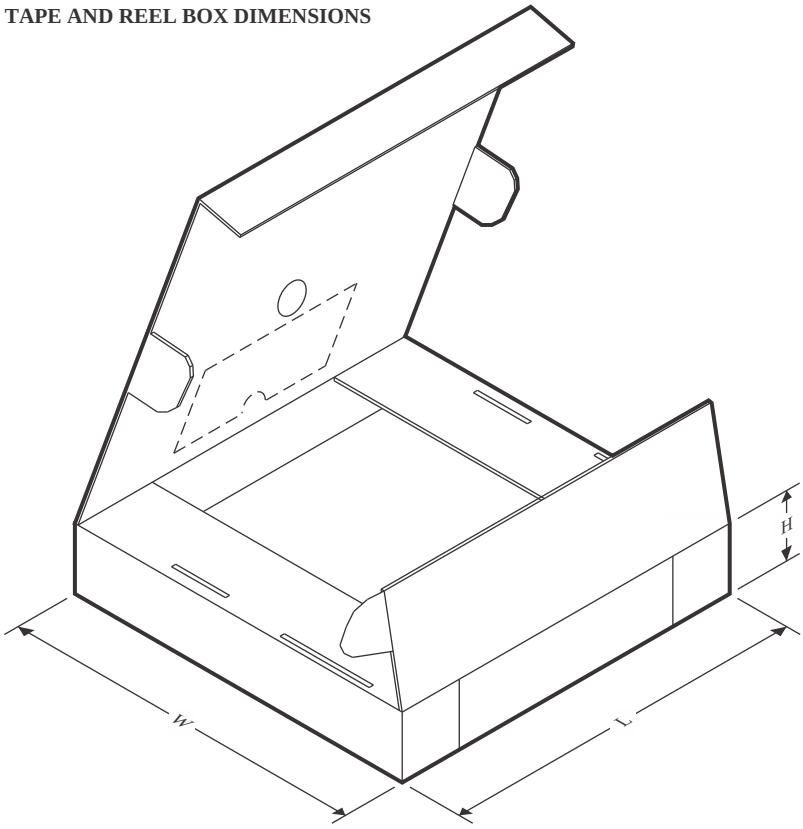
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2107AU/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

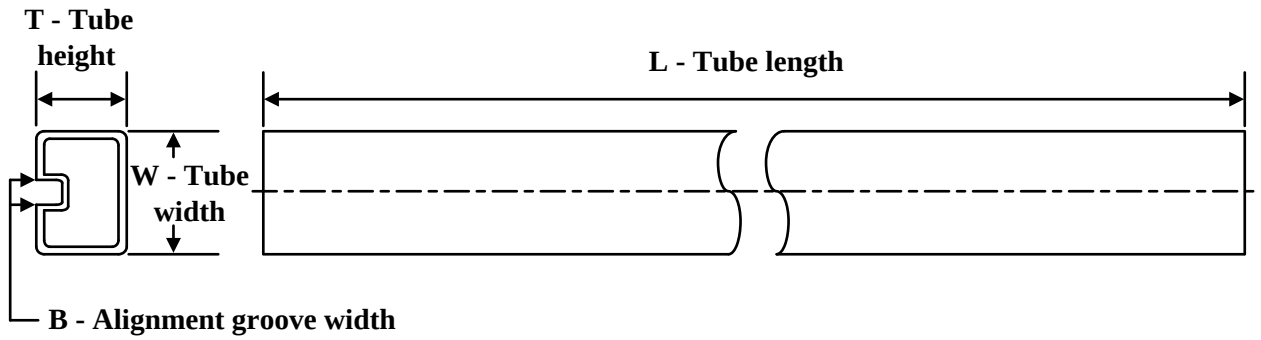
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2107AU/2K5	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA2107AU	D	SOIC	8	75	506.6	8	3940	4.32
OPA2107AU.A	D	SOIC	8	75	506.6	8	3940	4.32

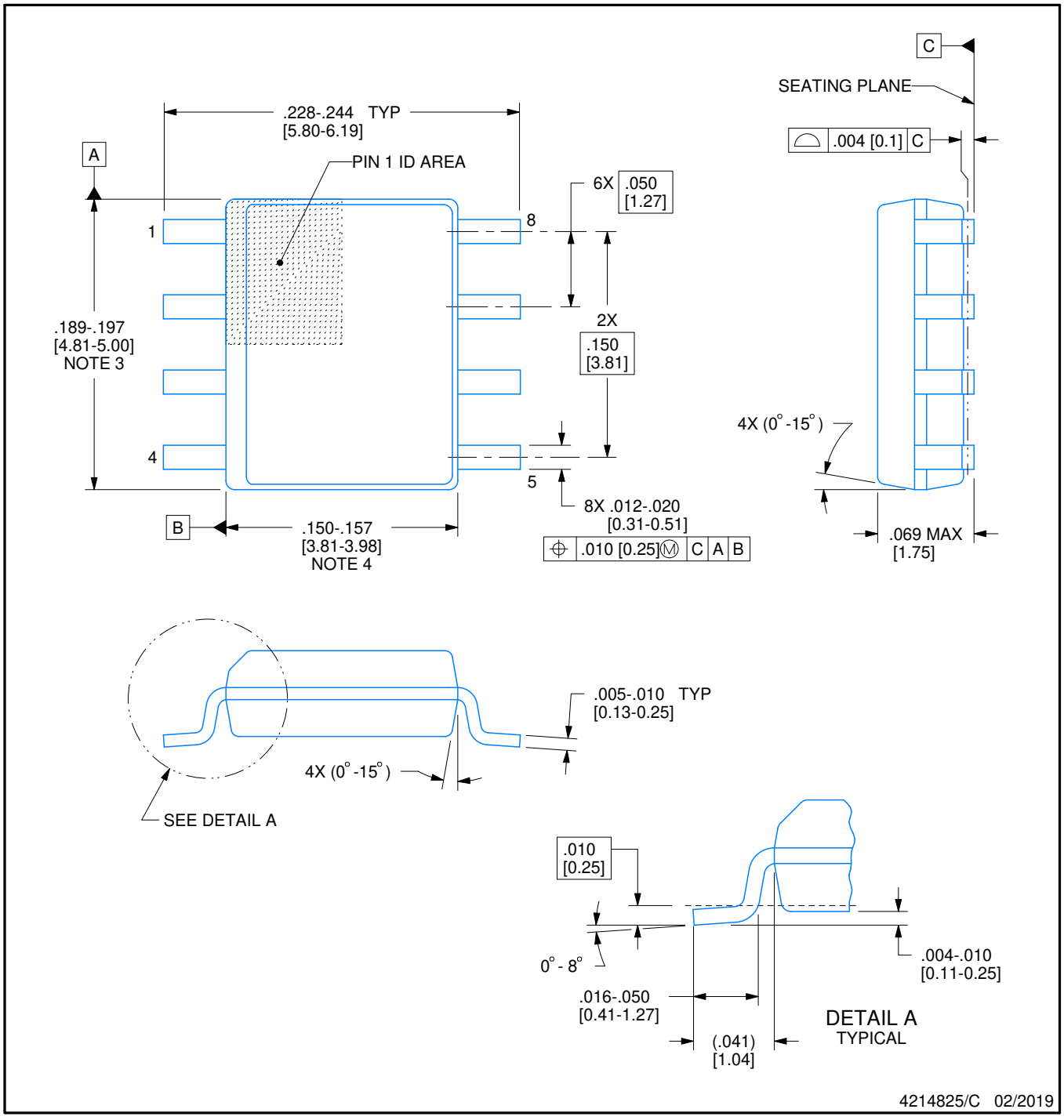


PACKAGE OUTLINE

D0008A

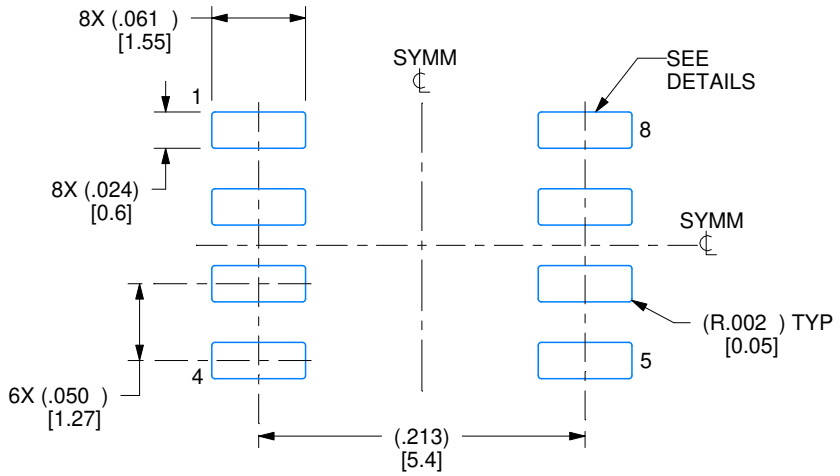
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

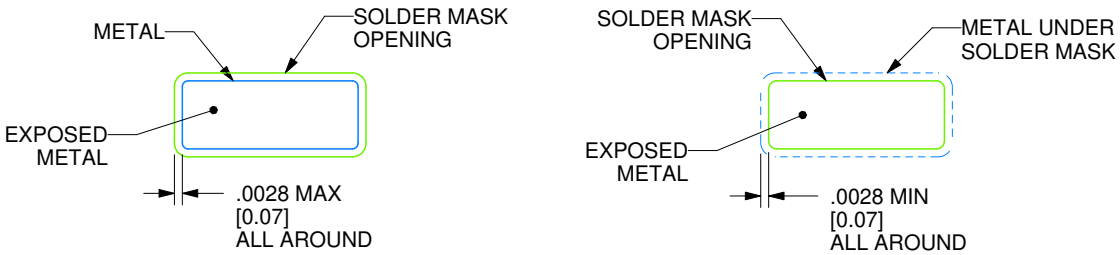


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

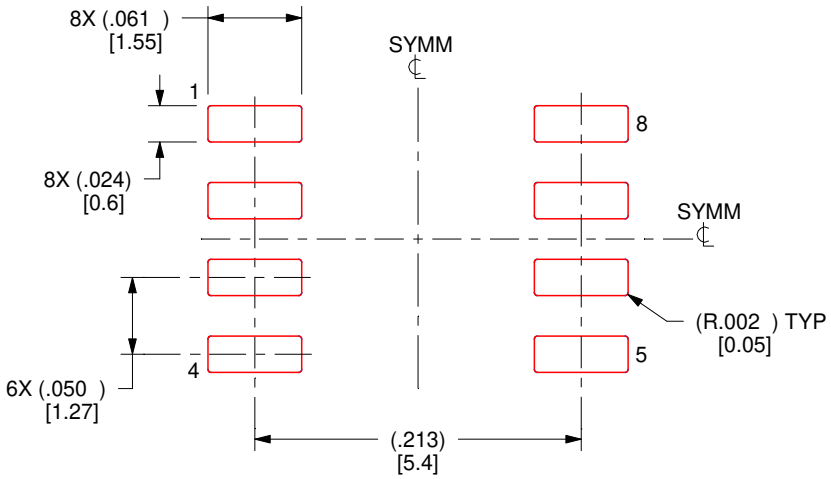
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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