OPAx322-Q1 20-MHz, Low-Noise, 1.8-V, RRI/O, CMOS Operational Amplifier

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H3A
  - Device CDM ESD Classification Level C5
- Gain Bandwidth: 20 MHz
- Low Noise: 8.5 nV/√Hz at 1 kHz
- Slew Rate: 10 V/μs
- Low THD+N: 0.0005%
- Rail-to-Rail I/O
- Offset Voltage: 2 mV (Maximum)
- Supply Voltage: 1.8 V to 5.5 V
- Supply Current:
  - Single-Supply Current: 1.6 mA/ch
  - Dual-Supply Current: 1.5 mA/ch
  - Quad-Supply Current: 1.4 mA/ch
- Unity-Gain Stable
- Small Packages:
  - SOT-23, VSSOP, TSSOP

2 Applications

- Automotive
- Sensor Signal Conditioning
- Consumer Audio
- Multi-Pole Active Filters
- Control-Loop Amplifiers
- Communications
- Security
- Scanners

3 Description

The OPAx322-Q1 series consists of single-, dual-, and quad-channel CMOS operational amplifiers featuring low noise and rail-to-rail inputs and outputs optimized for low-power, single-supply applications. Specified over a wide supply range from 1.8 V to 5.5 V, the low quiescent current of only 1.5 mA per channel makes these devices well-suited for power-sensitive applications.

The combination of very-low noise (8.5 nV/√Hz at 1 kHz), high-gain bandwidth (20 MHz), and fast slew rate (10 V/μs) make the OPAx322-Q1 family ideal for a wide range of applications, including signal conditioning and sensor amplification requiring high gains. Featuring low THD+N, the OPAx322-Q1 family is also excellent for consumer audio applications, particularly for single-supply systems.

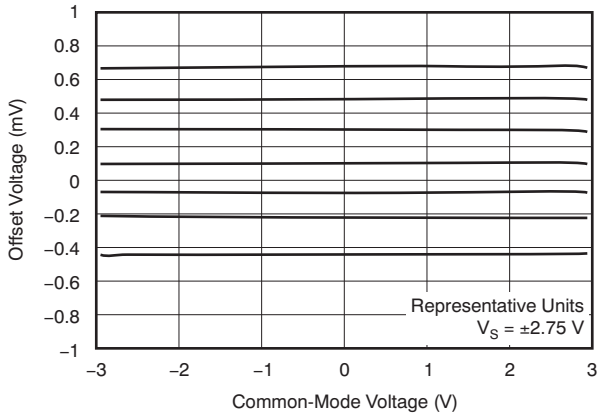
The OPA322-Q1 (single version) is available in 5-pin SOT-23 package, while the OPA2322-Q1 (dual version) is offered in a 8-pin VSSOP package. The OPA4322-Q1 (quad version) is available in a 14-pin TSSOP package. All versions are specified for operation from –40°C to +125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA322-Q1	SOT-23 (5)	2.90 mm × 1.60 mm
OPA2322-Q1	VSSOP (8)	3.00 mm × 3.00 mm
OPA4322-Q1	TSSOP (14)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Zero-Crossover Rail-to-Rail Input Stage Eliminates Distortion



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (June 2013) to Revision B **Page**

- Updated data sheet text to the latest documentation and translation standards ... 1
- Deleted "x" device marking and "with shutdown" from document title ... 1
- Deleted "Shutdown: 0.1 µA/ch" from *Features* list ... 1
- Deleted SON package from *Features* list ... 1
- Deleted OPA322S-Q1, OPA2322S-Q1, OPA4322S-Q1 devices from data sheet ... 1
- Changed single-supply current from 1.5 mA/ch to 1.6 mA/ch in *Features* section ... 1
- Changed quad-supply current from 1.5 ma/ch to 1.4 ma/ch in *Features* section ... 1
- Deleted "x" device marking, 6-pin SOT-23, 16-pin TSSOP, 10-pin VSSOP, 8-pin SOIC, 8-pin SON packages and shutdown text from *Description* section ... 1
- Deleted OPA322S-Q1, OPA2322S-Q1, and OPA4322S-Q1 devices from *Device Information* table ... 1
- Deleted 8-pin SOIC and 8-pin SON packages from *Device Information* table ... 1
- Deleted OPA322S-Q1 pinout drawing and pin table information in *Pin Configuration and Functions* section ... 4
- Deleted OPA2322-Q1 DRG package pinout drawing in *Pin Configuration and Functions* section ... 4
- Deleted OPA2322S-Q1 pinout drawing and table information in *Pin Configuration and Functions* section ... 4
- Deleted OPA4322S-Q1 pinout drawing and table information in *Pin Configuration and Functions* section ... 4
- Updated OPA2322-Q1 pinout tables in *Pin Configuration and Functions* section ... 5
- Updated OPA4322-Q1 pinout table in *Pin Configuration and Functions* section ... 6
- Deleted Operating Temperature, T_A values from *Absolute Maximum Ratings* table ... 7
- Added automotive *ESD Ratings* table to the *Specifications* section ... 7
- Added *Recommended Operating Conditions* table to the *Specifications* section ... 7
- Deleted OPA322S-Q1 *Thermal Information* table ... 8
- Deleted OPA2322S-Q1 D and DRG package *Thermal Information* values ... 8
- Deleted OPA2322S-Q1 *Thermal Information* table values ... 8
- Deleted OPA4322S-Q1 *Thermal Information* table values ... 8

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Revision History (continued)

- Deleted shutdown information from *Electrical Characteristics* table 9
- Changed typical input voltage noise value from 2.8 to 4.5 μV_{PP} in *Electrical Characteristics* table 9
- Deleted repeating Open-Loop Gain test conditions in *Electrical Characteristics* table 9
- Deleted Figure 26, Figure 27, Figure 28, and Figure 29 from *Typical Characteristics* section 11
- Updated x-axis of Figure 2 11
- Updated x-axis of Figure 5 11
- Added *Detailed Description* section and Functional Block Diagram 16
- Added *Feature Description* section 16
- Deleted shutdown text in *Feature Description* section 16
- Deleted text regarding the unity-gain stability of the OPAx322-Q1 in 1-nF capacitive loads *Capacitive Load and Stability* section 18
- Added *Device Functional Modes* section 20
- Deleted shutdown text in *Device Functional Modes* section 20
- Changed FilterPro™ link in *Application Information* section 21
- Updated Figure 35 22
- Added *Power Supply Recommendations* section 23
- Added *Layout* section 24
- Deleted *Leadless DFN Package* subsection in *Layout* section 24
- Updated Figure 37 (Layout Example) 24
- Deleted OPA322S-Q1, OPA2322S-Q1, and OPA4322S-Q1 devices from *Related Links* table 26

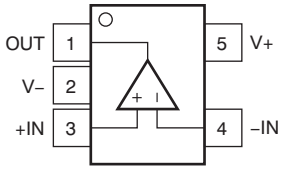
Changes from Original (June 2013) to Revision A **Page**

- Changed document status to *Production Data* 1

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5 Pin Configuration and Functions

OPA322-Q1 DBV Package
5-Pin SOT-23
Top View

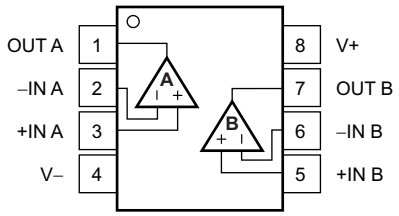


Pin Functions: OPA322-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN	4	I	Inverting input
+IN	3	I	Noninverting input
OUT	1	O	Output
V–	2	—	Negative (lowest) power supply
V+	5	—	Positive (highest) power supply

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OPA2322-Q1 DGK Packages
8-Pin VSSOP
Top View

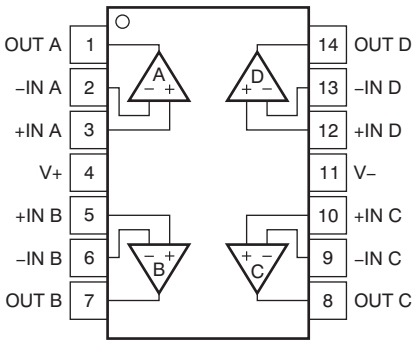


Pin Functions: OPA2322-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN A	2	I	Inverting input, channel A
+IN A	3	I	Noninverting input, channel A
–IN B	6	I	Inverting input, channel B
+IN B	5	I	Noninverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V–	4	—	Negative (lowest) power supply
V+	8	—	Positive (highest) power supply

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OPA4322-Q1 PW Package
14-Pin TSSOP
Top View



Pin Functions: OPA4322-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN A	2	I	Inverting input, channel A
+IN A	3	I	Noninverting input, channel A
–IN B	6	I	Inverting input, channel B
+IN B	5	I	Noninverting input, channel B
–IN C	9	I	Inverting input, channel C
+IN C	10	I	Noninverting input, channel C
–IN D	13	I	Inverting input, channel D
+IN D	12	I	Noninverting input, channel D
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
OUT C	8	O	Output, channel C
OUT D	14	O	Output, channel D
V–	11	—	Negative (lowest) power supply
V+	4	—	Positive (highest) power supply

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Supply voltage, V_S = (V+) – (V–)		6	V
	Signal input pins(2)	(V–) – 0.5	(V+) + 0.5	V
Current	Signal input pins(2)	–10	10	mA
	Output short-circuit(3)	Continuous		
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±4000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Specified voltage	1.8	5.5	V
T_A	Specified temperature	–40	125	°C

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6.4 Thermal Information: OPA322-Q1

THERMAL METRIC(1)		OPA322-Q1 DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	219.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	107.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	57.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	56.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Thermal Information: OPA2322-Q1

THERMAL METRIC(1)		OPA2322-Q1 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	174.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	95	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	93.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.6 Thermal Information: OPA4322-Q1

THERMAL METRIC(1)		OPA4322-Q1 PW (TSSOP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	109.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	34.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	52.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	51.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.7 Electrical Characteristics

at V_S = 1.8 V to 5.5 V, or ±0.9 V to ±2.75 V, T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, V_{OUT} = V_S / 2, (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				0.5	2	mV
dV_{OS}/dT	vs temperature	V_S = 5.5 V			1.8	6	µV/°C
PSR	vs power supply	V_S = 1.8 V to 5.5 V	T_A = 25°C		10	50	µV/V
			T_A = –40°C to 125°C		20	65	
	Channel separation	at 1 kHz			130		dB
INPUT VOLTAGE							
V_{CM}	Common-mode voltage range			(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	(V–) – 0.1 V < V_{CM} < (V+) + 0.1 V	T_A = 25°C	90	100		dB
			T_A = –40°C to 125°C	90			
INPUT BIAS CURRENT							
I_B	Input bias current	T_A = 25°C			±0.2	±10	pA
		T_A = –40°C to 85°C				±50	
		OPA322-Q1: T_A = –40°C to 125°C				±800	
		OPA2322-Q1: T_A = –40°C to 125°C				±400	
		OPA4322-Q1: T_A = –40°C to 125°C				±400	
I_{OS}	Input offset current	T_A = 25°C			±0.2	±10	pA
		T_A = –40°C to 85°C				±50	
		T_A = –40°C to 125°C				±400	
NOISE							
	Input voltage noise	f = 0.1 Hz to 10 Hz			4.5		μV_{PP}
e_n	Input voltage noise density	f = 1 kHz			8.5		$nV/\sqrt{Hz}$
		f = 10 kHz			7		
i_n	Input current noise density	f = 1 kHz			0.6		$fA/\sqrt{Hz}$
INPUT CAPACITANCE							
	Differential				5		pF
	Common-mode				4		pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	0.1 V < V_O < (V+) – 0.1 V R_L = 10 kΩ		100	130		dB
PM	Phase margin	V_S = 5 V C_L = 50 pF			47		°
FREQUENCY RESPONSE							
GBP	Gain bandwidth product	V_S = 5 V C_L = 50 pF, unity gain			20		MHz
SR	Slew rate	V_S = 5 V C_L = 50 pF, G = 1			10		V/µs
t_S	Settling time	V_S = 5 V C_L = 50 pF, to 0.1%, 2-V step, G = 1			0.25		µs
		V_S = 5 V C_L = 50 pF, to 0.01%, 2-V step, G = 1			0.32		
	Overload recovery time	V_S = 5 V C_L = 50 pF V_{IN} × G > V_S			100		ns
THD+N	Total harmonic distortion + noise(1)	V_S = 5 V C_L = 50 pF V_O = 4 V_{PP}, G = 1, f = 10 kHz R_L = 10 kΩ			0.0005%		
		V_S = 5 V, C_L = 50 pF, V_O = 2 V_{PP}, G = 1, f = 10 kHz R_L = 600 Ω			0.0011%		

(1) Third-order filter; bandwidth = 80 kHz at –3 dB

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Electrical Characteristics (continued)

at V_S = 1.8 V to 5.5 V, or ±0.9 V to ±2.75 V, T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, V_{OUT} = V_S / 2, (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT							
V_O	Voltage output (swing from both rails)	R_L = 10 kΩ	T_A = 25°C		10	20	mV
			T_A = –40°C to 125°C			30	
I_{SC}	Short-circuit current	V_S = 5.5 V			±65		mA
C_L	Capacitive load drive				See *Typical Characteristics*		
R_O	Open-loop output resistance	I_O = 0 mA f = 1 MHz			90		Ω
POWER SUPPLY							
V_S	Specified voltage range			1.8		5.5	V
I_Q	Quiescent current per amplifier	OPA322-Q1: I_O = 0 mA V_S = 5.5 V	T_A = 25°C		1.6	1.9	mA
			T_A = –40°C to 125°C			2	
		OPA2322-Q1: I_O = 0 mA V_S = 5.5 V	T_A = 25°C		1.5	1.75	
			T_A = –40°C to 125°C			1.85	
		OPA4322-Q1: I_O = 0 mA V_S = 5.5 V	T_A = 25°C		1.4	1.65	
			T_A = –40°C to 125°C			1.75	
	Power-on time	V_{S+} = 0 V to 5 V, to 90% I_Q level			28		µs

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7 Typical Characteristics

at T_A = 25°C, V_{CM} = V_{OUT} = midsupply, and R_L = 10 kΩ (unless otherwise noted)

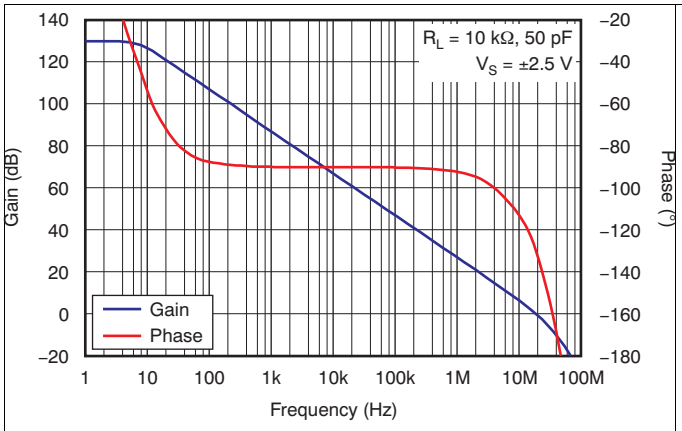


Figure 1. Open-Loop Gain and Phase vs Frequency

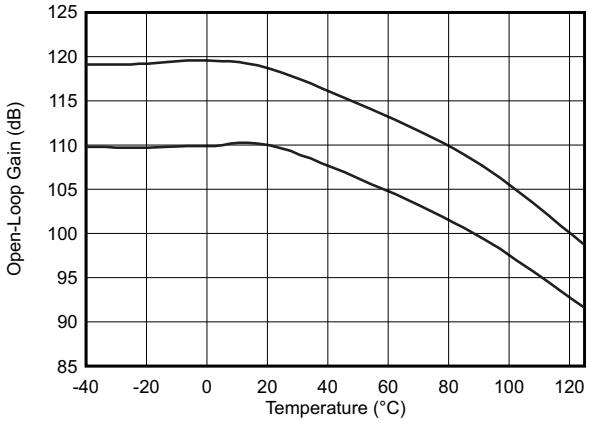


Figure 2. Open-Loop Gain vs Temperature

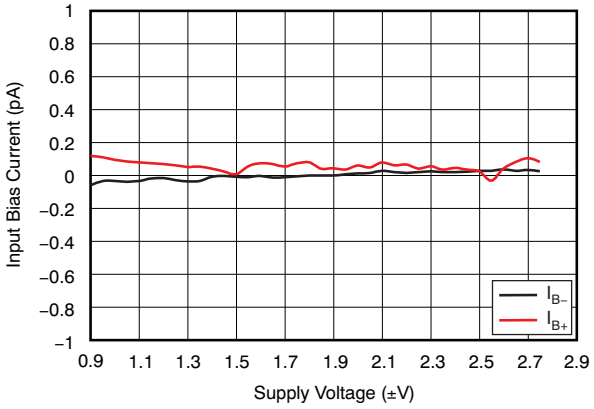


Figure 3. Input Bias Current vs Supply Voltage

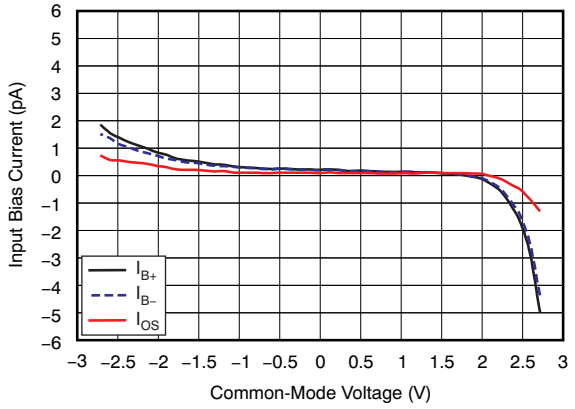


Figure 4. Input Bias Current vs Common-Mode Voltage

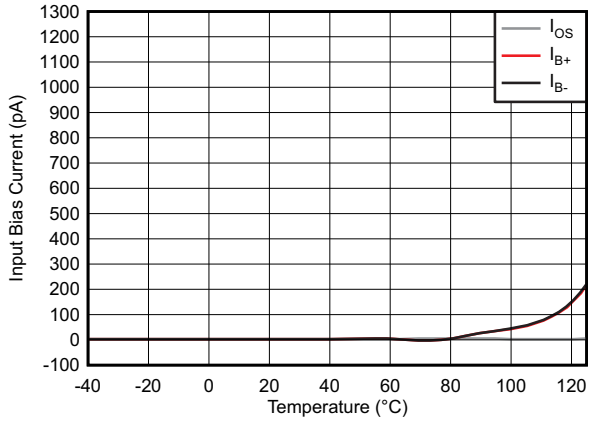


Figure 5. Input Bias Current vs Temperature

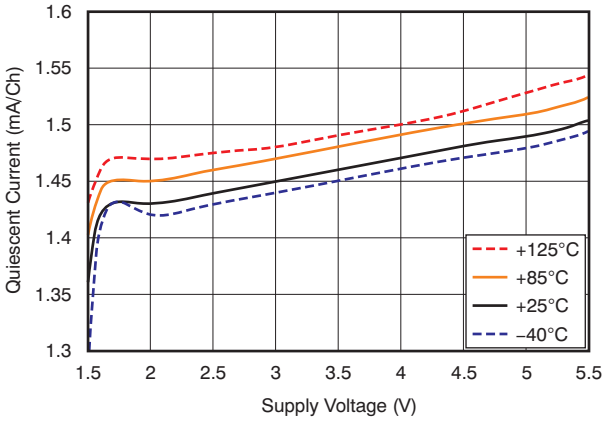


Figure 6. Quiescent Current vs Supply Voltage Per Amplifier

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Typical Characteristics (continued)

at T_A = 25°C, V_{CM} = V_{OUT} = midsupply, and R_L = 10 kΩ (unless otherwise noted)

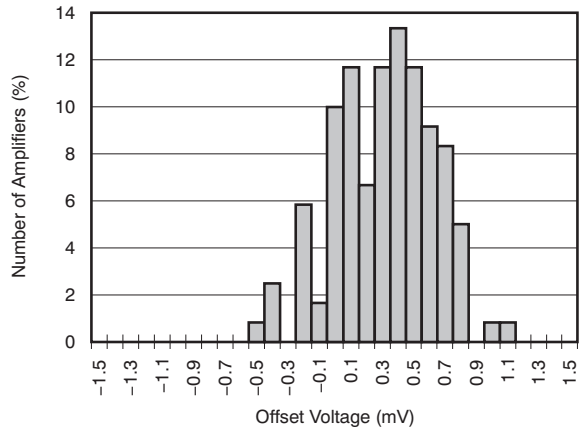


Figure 7. Offset Voltage Production Histogram

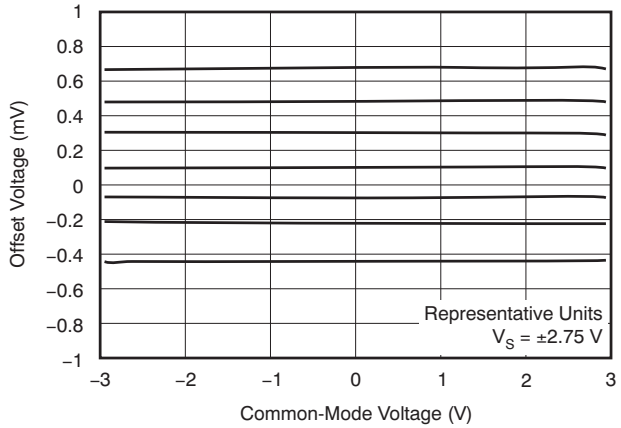


Figure 8. Offset Voltage vs Common-Mode Voltage

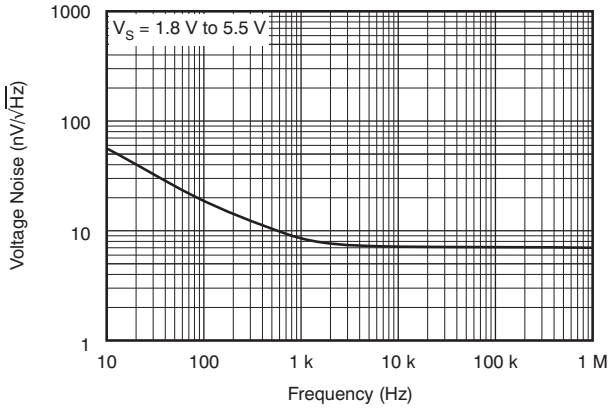


Figure 9. Input Voltage Noise Spectral Density vs Frequency

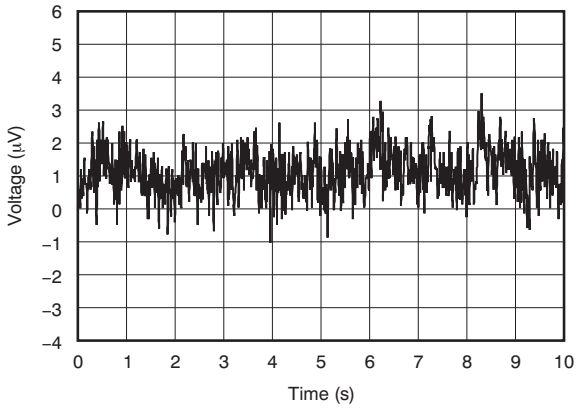


Figure 10. 0.1-Hz to 10-Hz Input Voltage Noise

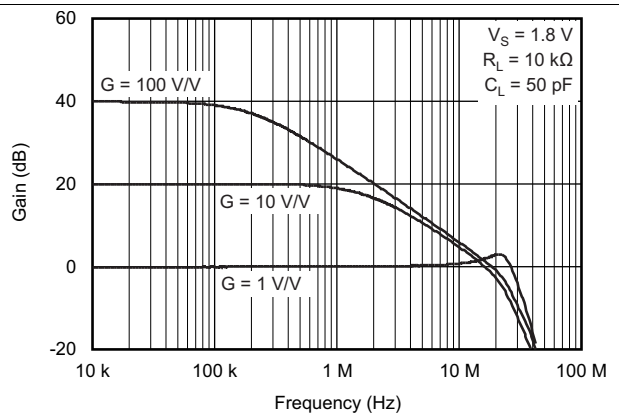


Figure 11. Closed-Loop Gain vs Frequency

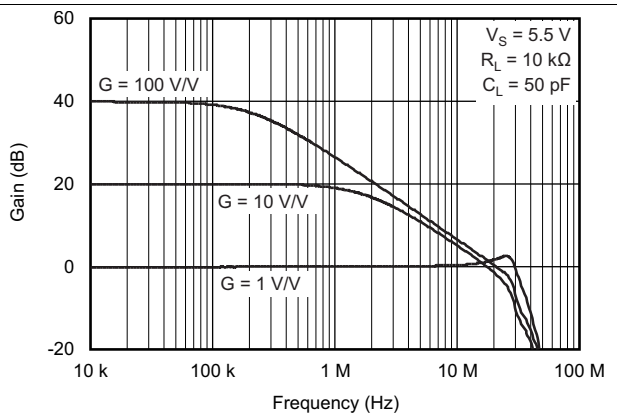


Figure 12. Closed-Loop Gain vs Frequency

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Typical Characteristics (continued)

at T_A = 25°C, V_{CM} = V_{OUT} = midsupply, and R_L = 10 kΩ (unless otherwise noted)

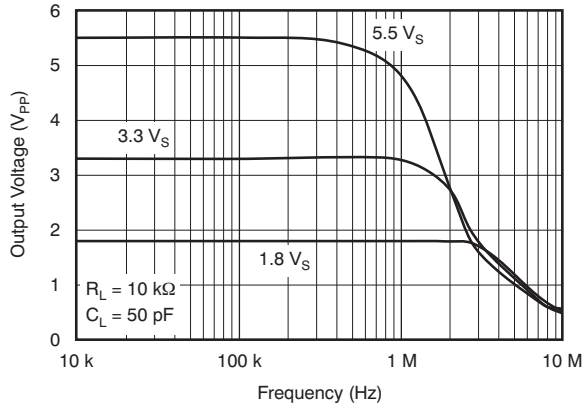


Figure 13. Maximum Output Voltage vs Frequency

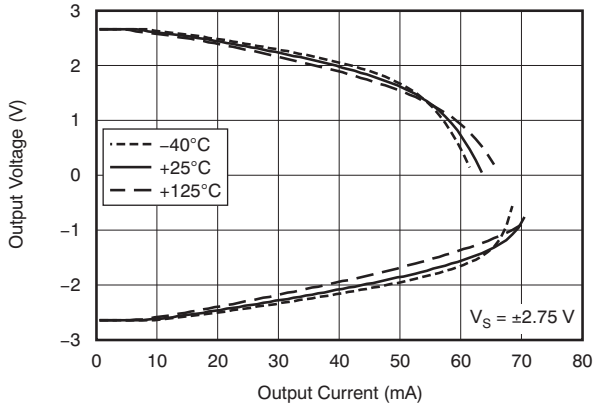


Figure 14. Output Voltage Swing vs Output Current

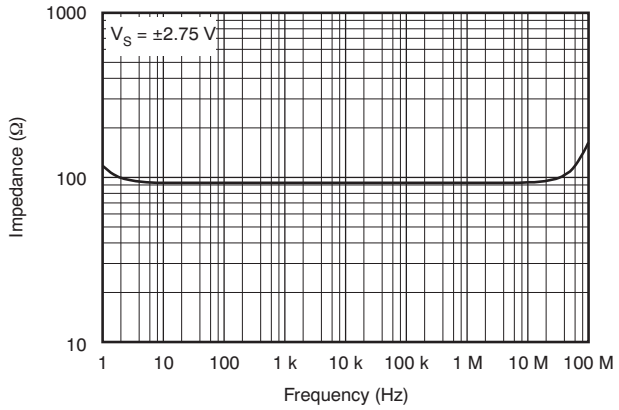


Figure 15. Open-Loop Output Impedance vs Frequency

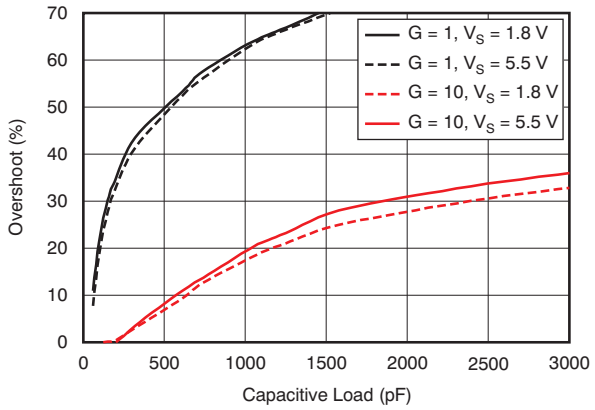


Figure 16. Small-Signal Overshoot vs Load Capacitance

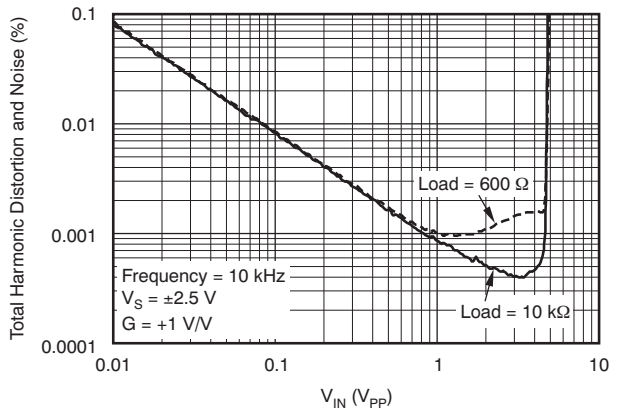


Figure 17. THD+N vs Amplitude

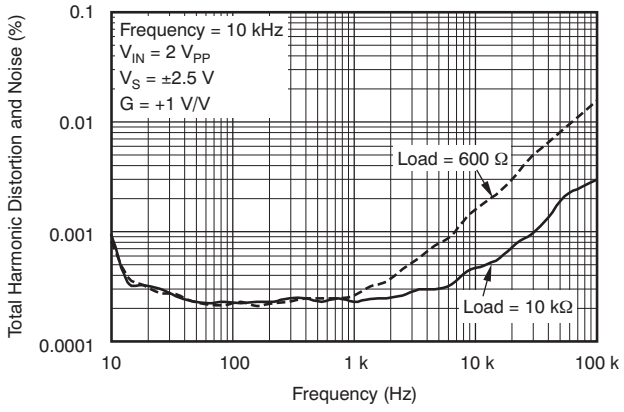


Figure 18. THD+N vs Frequency

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Typical Characteristics (continued)

at T_A = 25°C, V_{CM} = V_{OUT} = midsupply, and R_L = 10 kΩ (unless otherwise noted)

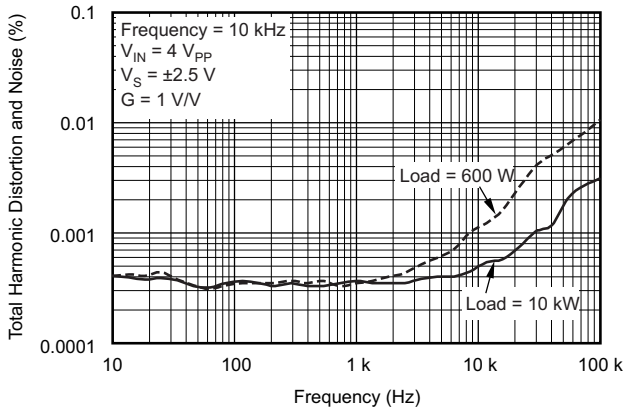


Figure 19. THD+N vs Frequency

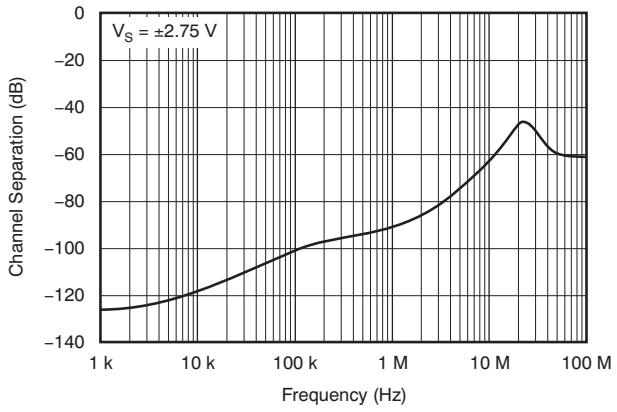


Figure 20. Channel Separation vs Frequency (Dual-Channel)

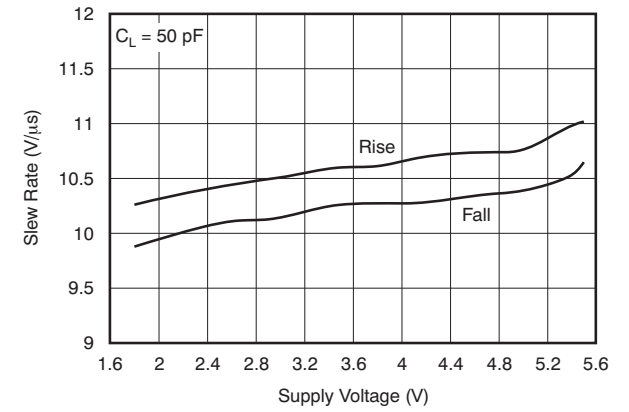


Figure 21. Slew Rate vs Supply Voltage

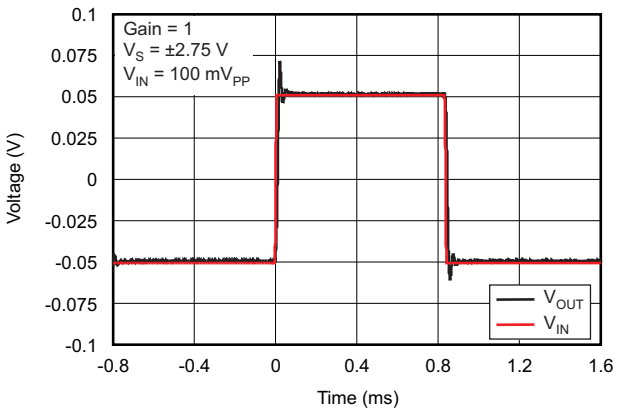


Figure 22. Small-Signal Step Response

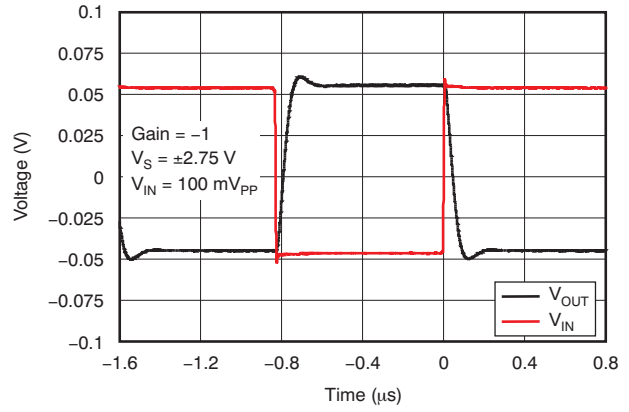


Figure 23. Small-Signal Step Response

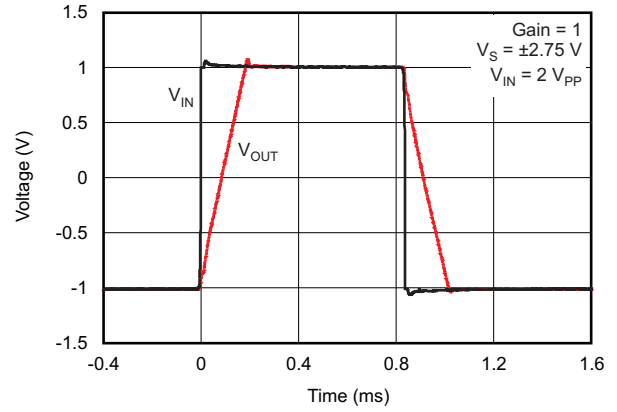


Figure 24. Large-Signal Step Response vs Time

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Typical Characteristics (continued)

at T_A = 25°C, V_{CM} = V_{OUT} = midsupply, and R_L = 10 kΩ (unless otherwise noted)

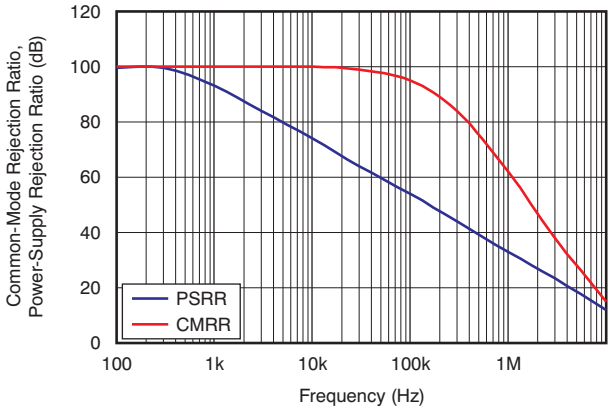


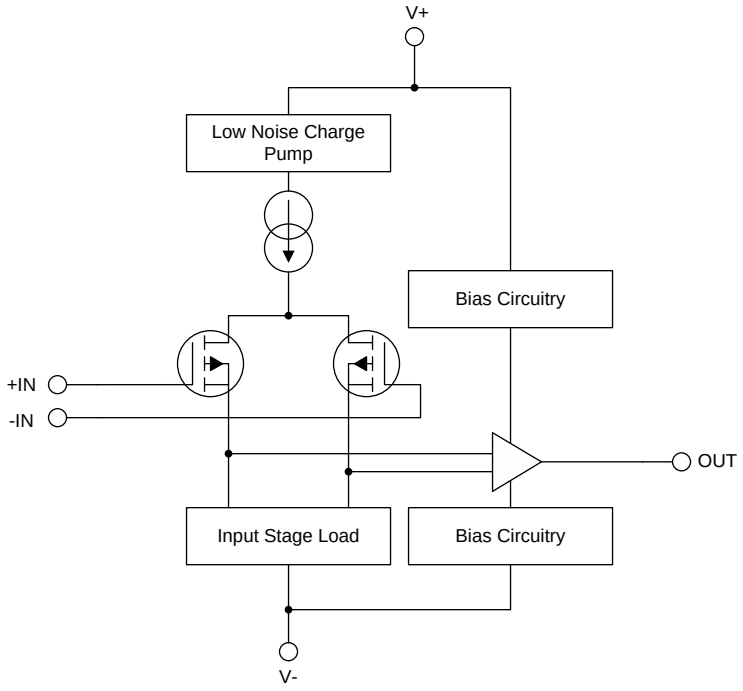
Figure 25. CMRR and PSRR vs Frequency

8 Detailed Description

8.1 Overview

The OPAx322-Q1 family of operational amplifiers (op amps) are high-speed precision amplifiers well-suited to drive 12-, 14-, and 16-bit analog-to-digital converters. Low-output impedance with flat frequency characteristics and zero-crossover distortion circuitry enable high linearity over the full input common-mode range, achieving true rail-to-rail input from a 1.8-V to 5.5-V single-supply.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Operating Voltage

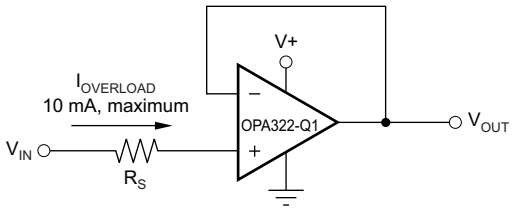
The OPAx322-Q1 series op amps are unity-gain stable and can operate on a single-supply voltage (1.8 V to 5.5 V), or a split-supply voltage (±0.9 V to ±2.75 V), which makes the op amps highly versatile and easy to use. The power-supply pins must have local bypass ceramic capacitors (typically 0.001 μF to 0.1 μF). These amplifiers are fully specified from 1.8 V to 5.5 V and over the extended temperature range from –40°C to +125°C. Parameters that can exhibit variance with regard to operating voltage or temperature are presented in *Typical Characteristics*.

8.3.2 Input and ESD Protection

The OPAx322-Q1 incorporates internal electrostatic discharge (ESD) protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes also provide in-circuit input overdrive protection, as long as the current is limited to 10 mA as stated in *Absolute Maximum Ratings*. Many input signals are inherently current-limited to less than 10 mA; therefore, a limiting resistor is not required. Figure 26 shows how a series input resistor (R_S) may be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value must be kept to the minimum in noise-sensitive applications.

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Feature Description (continued)



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Figure 26. Input Current Protection

8.3.3 Phase Reversal

The OPAx322-Q1 family of op amps are designed to be immune to phase reversal when the input pins exceed the supply voltages, which provides further in-system stability and predictability. Figure 27 shows the input voltage exceeding the supply voltage without any phase reversal.

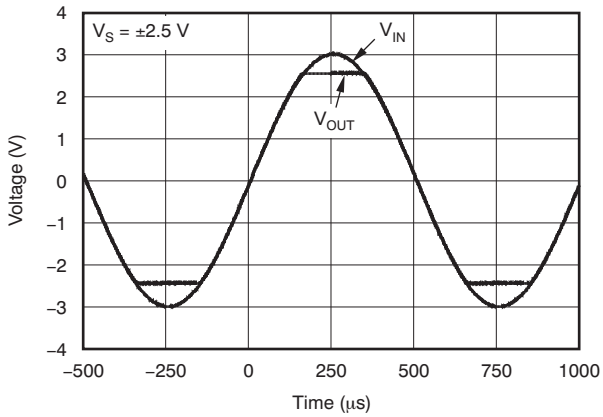
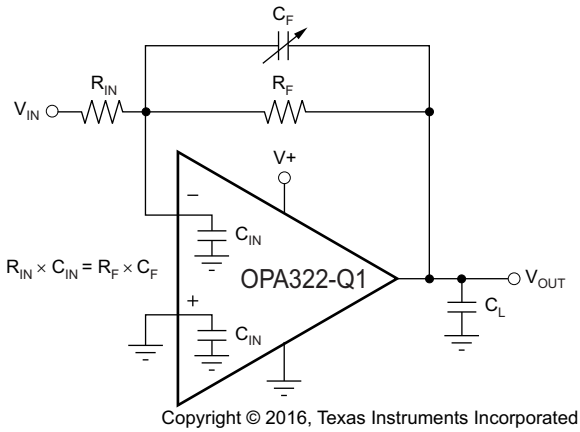


Figure 27. No Phase Reversal

8.3.4 Feedback Capacitor Improves Response

For optimum settling time and stability with high-impedance feedback networks, it may be necessary to add a feedback capacitor across the feedback resistor (R_F), as shown in Figure 28. This capacitor compensates for the zero created by the feedback network impedance and the OPAx322-Q1 input capacitance (and any parasitic layout capacitance). The effect becomes more significant with higher impedance networks.



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NOTE: Where C_{IN} is equal to the OPAx322-Q1 input capacitance (approximately 9 pF) plus any parasitic layout capacitance.

Figure 28. Feedback Capacitor Improves Dynamic Performance

Feature Description (continued)

For the circuit shown in Figure 28, the value of the variable feedback capacitor must be selected so that the input resistance times the input capacitance of the OPAx322-Q1 (typically 9 pF) plus the estimated parasitic layout capacitance equals the feedback capacitor times the feedback resistor with Equation 1.

$$R_{IN} \times C_{IN} = R_F \times C_F \quad (1)$$

where

- C_{IN} is equal to the OPAx322-Q1 input capacitance (sum of differential and common-mode) plus the layout capacitance

The capacitor value can be adjusted until optimum performance is obtained.

8.3.5 EMI Susceptibility and Input Filtering

Operational amplifiers vary in susceptibility to electromagnetic interference (EMI). If conducted EMI enters the device, the DC offset observed at the amplifier output may shift from the nominal value while EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. While all operational amplifier pin functions can be affected by EMI, the input pins are likely to be the most susceptible. The OPAx322-Q1 operational amplifier family incorporates an internal input low-pass filter that reduces the amplifier response to EMI. Both common-mode and differential mode filtering are provided by the input filter. The filter is designed for a cutoff frequency of approximately 580 MHz (–3 dB), with a roll-off of 20 dB per decade.

8.3.6 Output Impedance

The open-loop output impedance of the OPAx322-Q1 common-source output stage is approximately 90 Ω. When the op amp is connected with feedback, the loop gain significantly reduces this value. For each decade rise in the closed-loop gain, the loop gain is reduced by the same amount, which results in a tenfold increase in effective output impedance. While the OPAx322-Q1 output impedance remains flat over a wide frequency range. At higher frequencies the output impedance rises as the open-loop gain of the op amp drops. However, at these frequencies the output becomes capacitive as a result of parasitic capacitance. This characteristic prevents the output impedance from becoming too high, which can cause stability problems when driving large capacitive loads. As mentioned previously, the OPAx322-Q1 has excellent capacitive load drive capability for an op amp with a bandwidth of this value.

8.3.7 Capacitive Load and Stability

The OPAx322-Q1 is designed to be used in applications where driving a capacitive load is required. As with all op amps, there may be specific instances where the OPAx322-Q1 can become unstable. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier is stable in operation. An op amp in the unity-gain (1-V/V) buffer configuration and driving a capacitive load exhibits a greater tendency to become unstable than an amplifier operating at a higher noise gain. The capacitive load, in conjunction with the op amp output resistance, creates a pole within the feedback loop that degrades the phase margin.

The equivalent series resistance (ESR) of some very large capacitors (C_L > 1 µF) is sufficient to alter the phase characteristics in the feedback loop so the amplifier remains stable. Increasing the amplifier closed-loop gain allows the amplifier to drive increasingly larger capacitance. This increased capability is evident when observing the overshoot response of the amplifier at higher voltage gains, as shown in Figure 29. One technique for increasing the capacitive load drive capability of the amplifier operating in unity gain is to insert a small resistor (R_S, typically 10-Ω to 20-Ω) in series with the output, as shown in Figure 30.

This resistor significantly reduces the overshoot and ringing associated with large capacitive loads. A possible problem with this technique is that a voltage divider is created with the added series resistor and any resistor connected in parallel with the capacitive load. The voltage divider introduces a gain error at the output that reduces the output swing. However, the error contributed by the voltage divider may be insignificant. For example, with a load resistance of R_L = 10 kΩ and R_S = 20 Ω, the gain error is approximately 0.2%. When R_L decreases to 600 Ω (which the OPAx322-Q1 is able to drive), the error increases to 7.5%.

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Feature Description (continued)

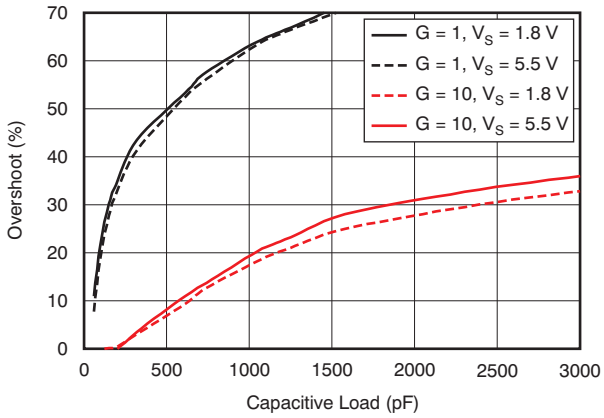
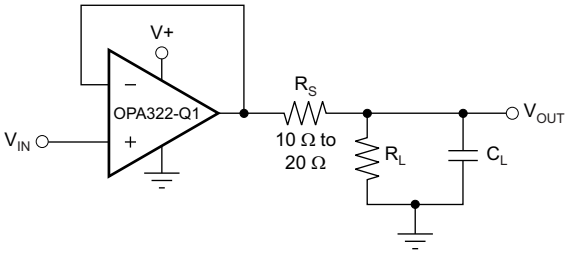


Figure 29. Small-Signal Overshoot vs Capacitive Load (100-mV$_{PP}$ Output Step)



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Figure 30. Improving Capacitive Load Drive

8.3.8 Overload Recovery Time

Overload recovery time is the time required for the output of the amplifier to come out of saturation and recover to the linear region. Overload recovery is particularly important in applications where small signals must be amplified in the presence of large transients. Figure 31 and Figure 32 show the positive and negative overload recovery times of the OPAx322-Q1, respectively. In both cases, the time elapsed before the OPAx322-Q1 comes out of saturation is less than 100 ns. The symmetry between the positive and negative recovery times allows excellent signal rectification without distortion of the output signal.

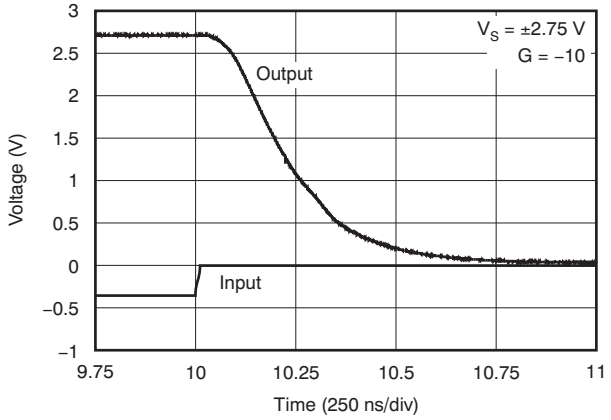


Figure 31. Positive Recovery Time

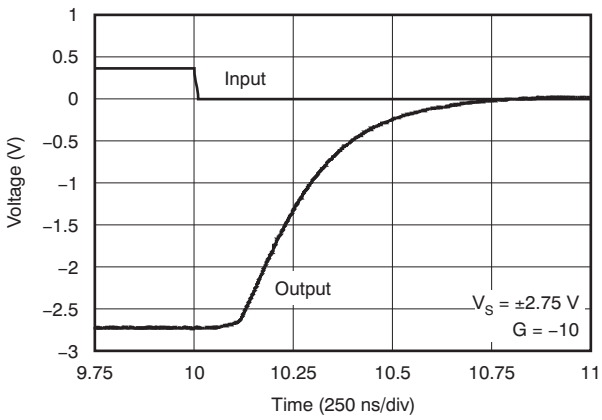


Figure 32. Negative Recovery Time

8.4 Device Functional Modes

The OPAx322-Q1 family of operational amplifiers are operational when power-supply voltages between 1.8 V to 5.5 V are applied.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The OPAx322-Q1 family offers outstanding DC and AC performance. These devices operate up to a 5.5-V power supply and offer ultra-low input bias current and 20-MHz bandwidth. These features make the OPAx322-Q1 family a robust operational amplifier for both battery-powered and industrial applications.

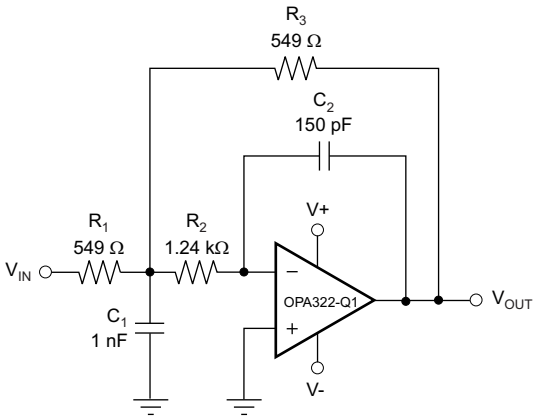
9.1.1 Active Filter

The OPAx322-Q1 is well-suited for active filter applications that require a wide bandwidth, fast slew rate, low-noise, single-supply operational amplifier. Figure 33 shows a 500-kHz, second-order, low-pass filter using the multiple-feedback (MFB) topology. The components are selected to provide a maximally flat Butterworth response. Beyond the cutoff frequency, roll-off is –40 dB/dec. The Butterworth response is ideal for applications that require predictable gain characteristics, such as the anti-aliasing filter used in front of an ADC.

One point to observe when considering the MFB filter is that the output is inverted relative to the input. If this inversion is not required (or not desired) a noninverting output can be achieved through one of these options:

1. Adding an inverting amplifier
2. Adding an additional second-order MFB stage
3. Using a noninverting filter topology, such as the Sallen-Key (shown in Figure 34).

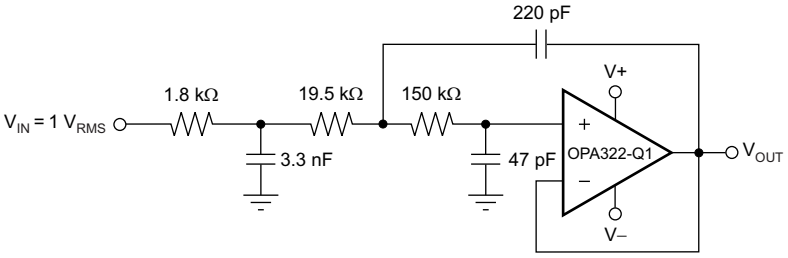
MFB, Sallen-Key, low-pass, and high-pass filter synthesis is quickly accomplished using TI's FilterPro™ program. This software is available as a free download at www.ti.com.



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Figure 33. Second-Order, Butterworth, 500-kHz Low-Pass Filter

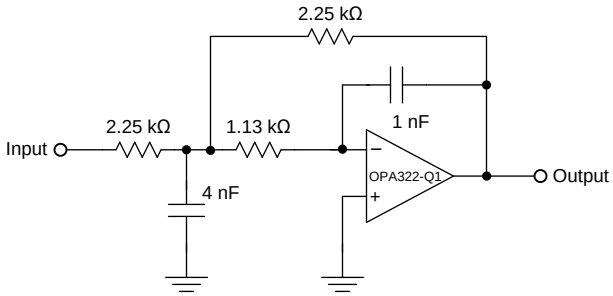
Application Information (continued)



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Figure 34. OPAx322-Q1 Configured as a Three-Pole, 20-kHz, Sallen-Key Filter

9.2 Typical Application



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Figure 35. Second-Order, Low-Pass Filter Schematic

9.2.1 Design Requirements

- Gain = 1 V/V
- Low-pass cutoff frequency = 50 kHz
- –40-db/dec filter response
- Maintain less than 3-dB gain peaking in the gain versus frequency response

9.2.2 Detailed Design Procedure

The infinite-gain multiple-feedback circuit for a low-pass network function is shown in Equation 2. Use Equation 2 to calculate the voltage transfer function.

$$\frac{\text{Output}}{\text{Input}}(s) = \frac{-1/R_1R_3C_2C_5}{s^2 + (s/C_2)(1/R_1 + 1/R_3 + 1/R_4) + 1/R_3R_4C_2C_5} \quad (2)$$

This circuit produces a signal inversion. For this circuit, the gain at DC and the low-pass cutoff frequency are calculated by Equation 3.

$$\text{Gain} = \frac{R_4}{R_1}$$

$$f_C = \frac{1}{2\pi}\sqrt{(1/R_3R_4C_2C_5)} \quad (3)$$

Software tools are readily available to simplify filter design. WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH® Filter Designer allows the user to create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

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Typical Application (continued)

Available as a web-based tool from the WEBENCH® Design Center, WEBENCH® Filter Designer allows the user to design, optimize, and simulate complete multistage active filter solutions within minutes.

9.2.3 Application Curve

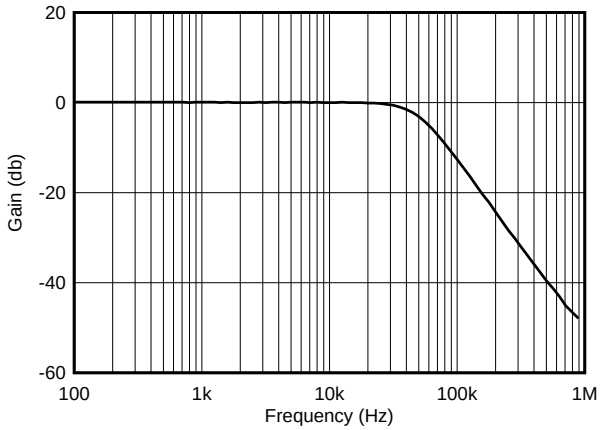


Figure 36. OPAx322-Q1 Second-Order, 50-kHz, Low-Pass Filter

10 Power Supply Recommendations

The OPAx322-Q1 family is specified for operation from 1.8 V to 5.5 V (±0.9 V to ±2.75 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in *Typical Characteristics*.

CAUTION

Supply voltages larger than 6 V can permanently damage the device; see the *Absolute Maximum Ratings*.

Place 0.1-μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see *Layout*.

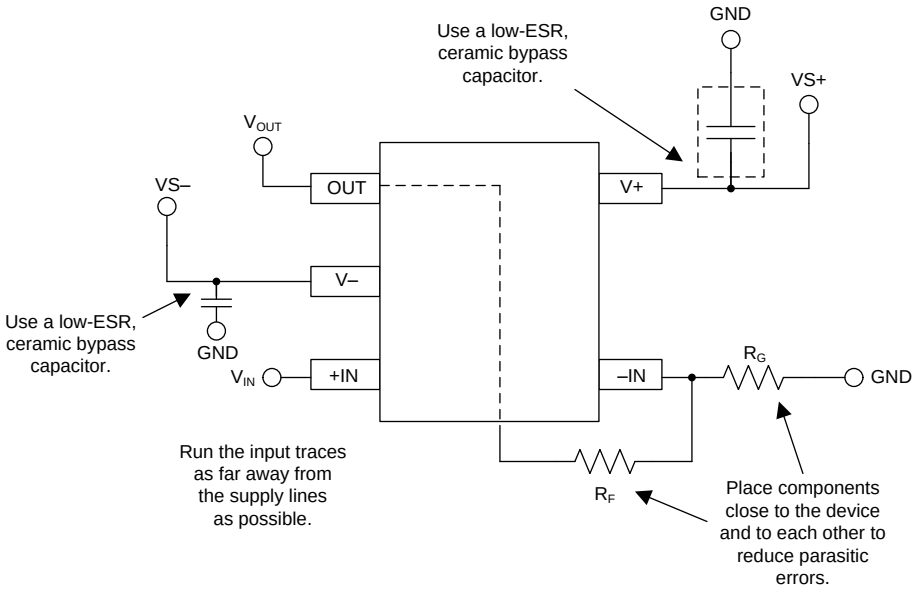
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11 Layout

11.1 Layout Guidelines

The OPAx322-Q1 is a wideband amplifier. To realize the full operational performance of the device, follow good high-frequency printed-circuit board (PCB) layout practices. The bypass capacitors must be connected between each supply pin and ground as close as possible to the device. The bypass capacitor traces must be designed for minimum inductance.

11.2 Layout Example



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Figure 37. Layout Example

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12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.1.2 Development Support

12.1.2.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI™ is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional DC, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

NOTE

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

12.1.2.2 DIP Adapter EVM

The DIP Adapter EVM tool provides an easy, low-cost way to prototype small surface mount devices. The evaluation tool these TI packages: D or U (SOIC-8), PW (TSSOP-8), DGK (VSSOP-8), DBV (SOT23-6, SOT23-5 and SOT23-3), DCK (SC70-6 and SC70-5), and DRL (SOT563-6). The DIP Adapter EVM may also be used with terminal strips or may be wired directly to existing circuits.

12.1.2.3 Universal Operational Amplifier EVM

The Universal Op Amp EVM is a series of general-purpose, blank circuit boards that simplify prototyping circuits for a variety of device package types. The evaluation module board design allows many different circuits to be constructed easily and quickly. Five models are offered, with each model intended for a specific package type. PDIP, SOIC, VSSOP, TSSOP and SOT-23 packages are all supported.

NOTE

These boards are unpopulated, so users must provide their own devices. TI recommends requesting several op amp device samples when ordering the Universal Op Amp EVM.

12.1.2.4 TI Precision Designs

TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits. TI Precision Designs are available online at http://www.ti.com/ww/en/analog/precision-designs/.

12.1.2.5 WEBENCH® Filter Designer

WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH® Filter Designer allows the user to create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

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Device Support (continued)

Available as a web-based tool from the WEBENCH® Design Center, WEBENCH® Filter Designer allows the user to design, optimize, and simulate complete multistage active filter solutions within minutes.

12.2 Documentation Support

12.2.1 Related Documentation

The following documents are relevant to using the OPAx322x-Q1 family, and recommended for reference. All are available for download at www.ti.com unless otherwise noted.

- *QFN/SON PCB Attachment*(SLVA271)
- *Quad Flatpack No-Lead Logic Packages* (SCBA017)
- *OPA322, OPA2322, OPA4322 EMIR Immunity Performance* (SBOT005)
- *FilterPro™ User's Guide* (SBFA001)
- *AFE for Transient Recorder and Digital Fault Recorder Using High-Speed ADCs and Differential Amplifiers* (TIDUAT7)
- *Reference Design for Interfacing Current Output Hall Sensors and CTs With Differential ADCs/MCUs* (TIDUA57A)
- *Single-Ended Signal Conditioning Circuit for Current and Voltage Measurement Using Fluxgate Sensors* (TIDU585)
- *Differential Signal Conditioning Circuit for Current and Voltage Measurement Using Fluxgate Sensors* (TIDU569)

12.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
OPA322-Q1	Click here	Click here	Click here	Click here	Click here
OPA2322-Q1	Click here	Click here	Click here	Click here	Click here
OPA4322-Q1	Click here	Click here	Click here	Click here	Click here

12.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.5 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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12.7 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2322AQDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OVDQ
OPA2322AQDGKRQ1.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OVDQ
OPA322AQDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	19AD
OPA322AQDBVRQ1.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	19AD
OPA4322AQPWRQ1	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	4322AQ1
OPA4322AQPWRQ1.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	4322AQ1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF OPA2322-Q1, OPA322-Q1, OPA4322-Q1 :

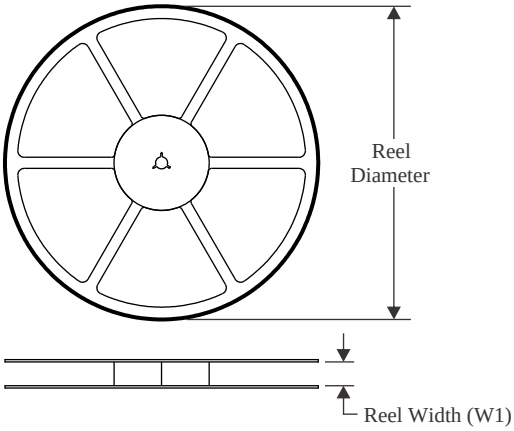
- Catalog : OPA2322, OPA322, OPA4322

NOTE: Qualified Version Definitions:

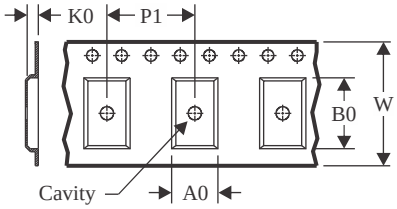
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

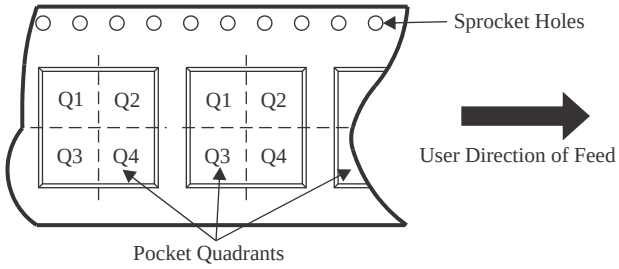


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

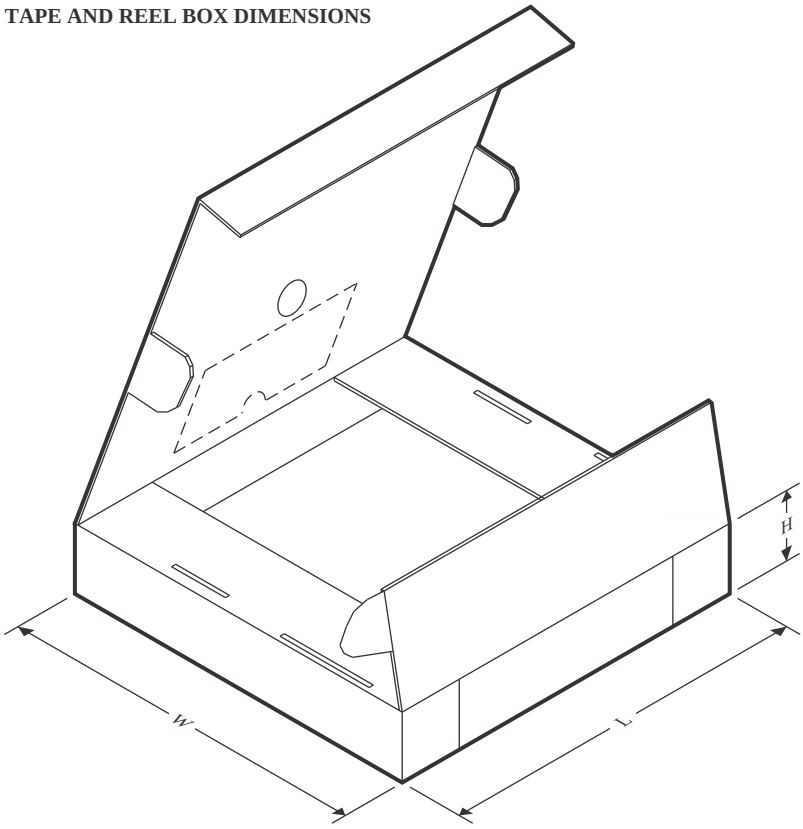
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2322AQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2322AQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA322AQDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA4322AQPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

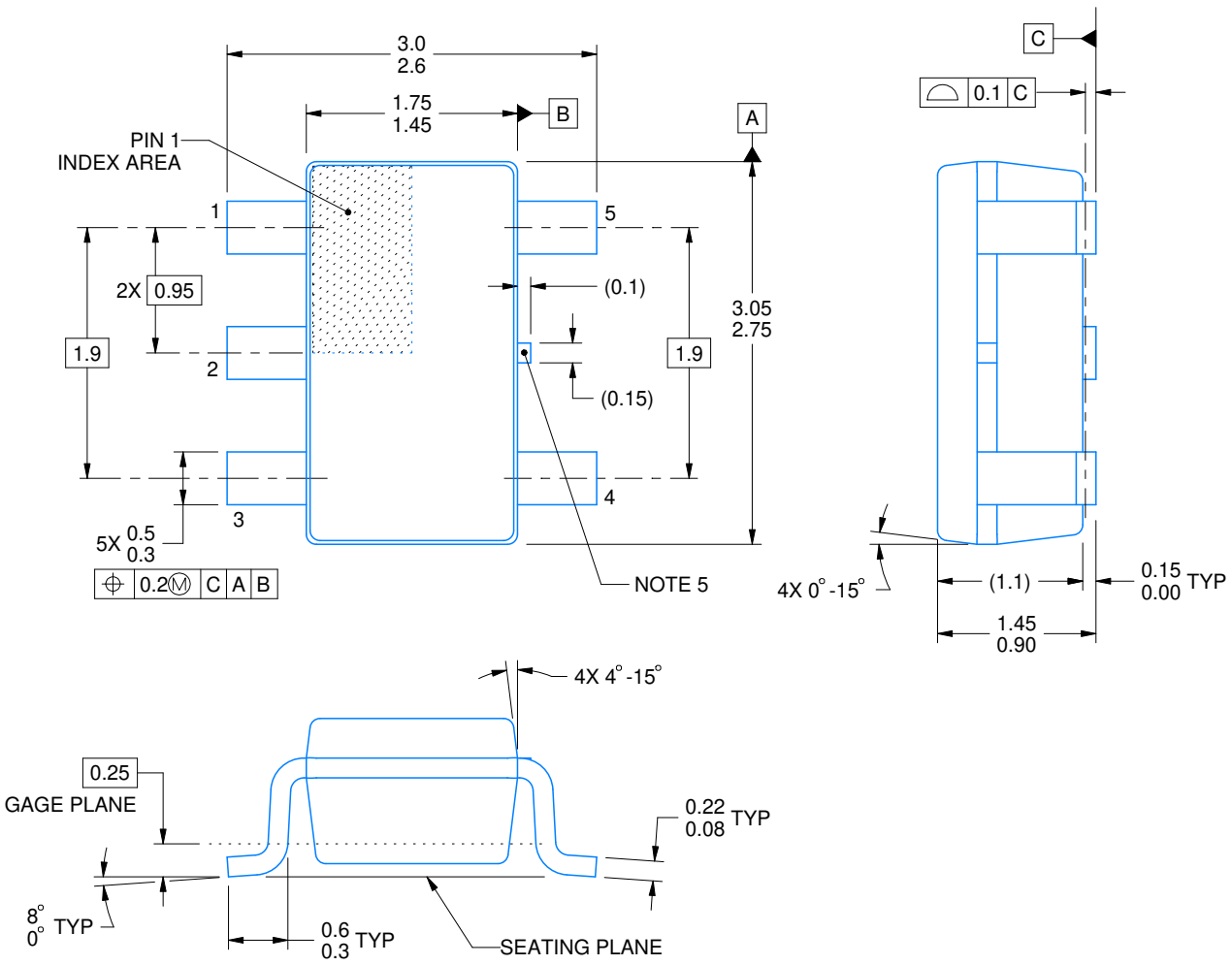
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2322AQDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2322AQDGKRQ1	VSSOP	DGK	8	2500	353.0	353.0	32.0
OPA322AQDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
OPA4322AQPWRQ1	TSSOP	PW	14	2000	353.0	353.0	32.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

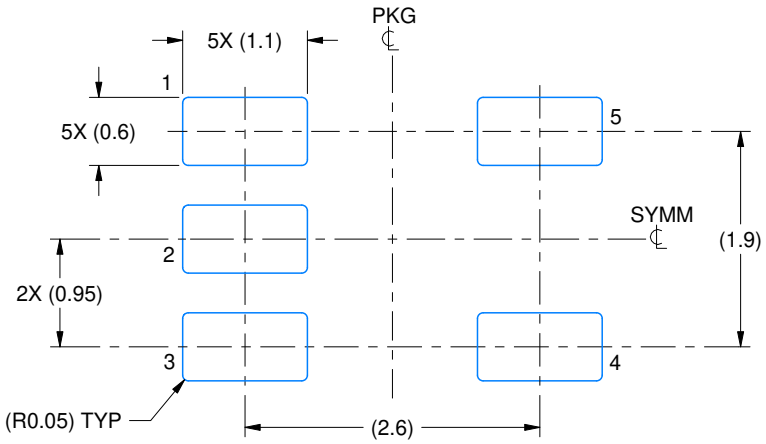
SMALL OUTLINE TRANSISTOR



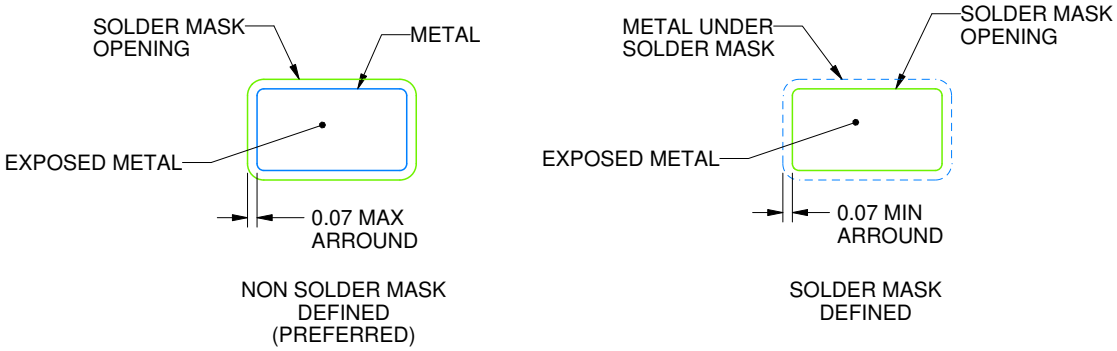
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

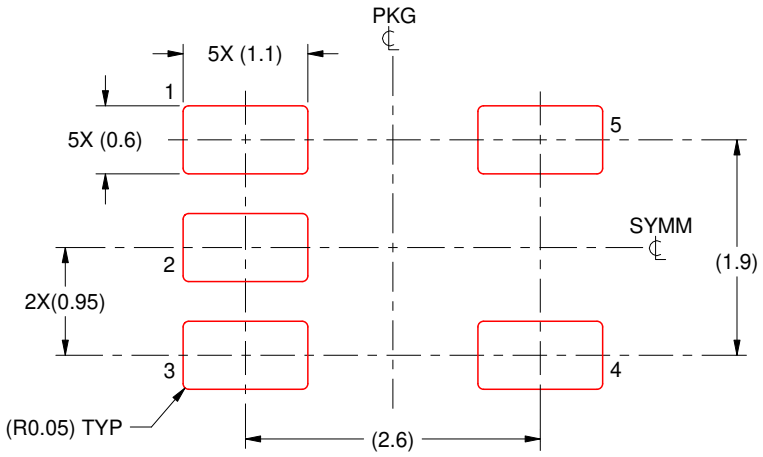


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

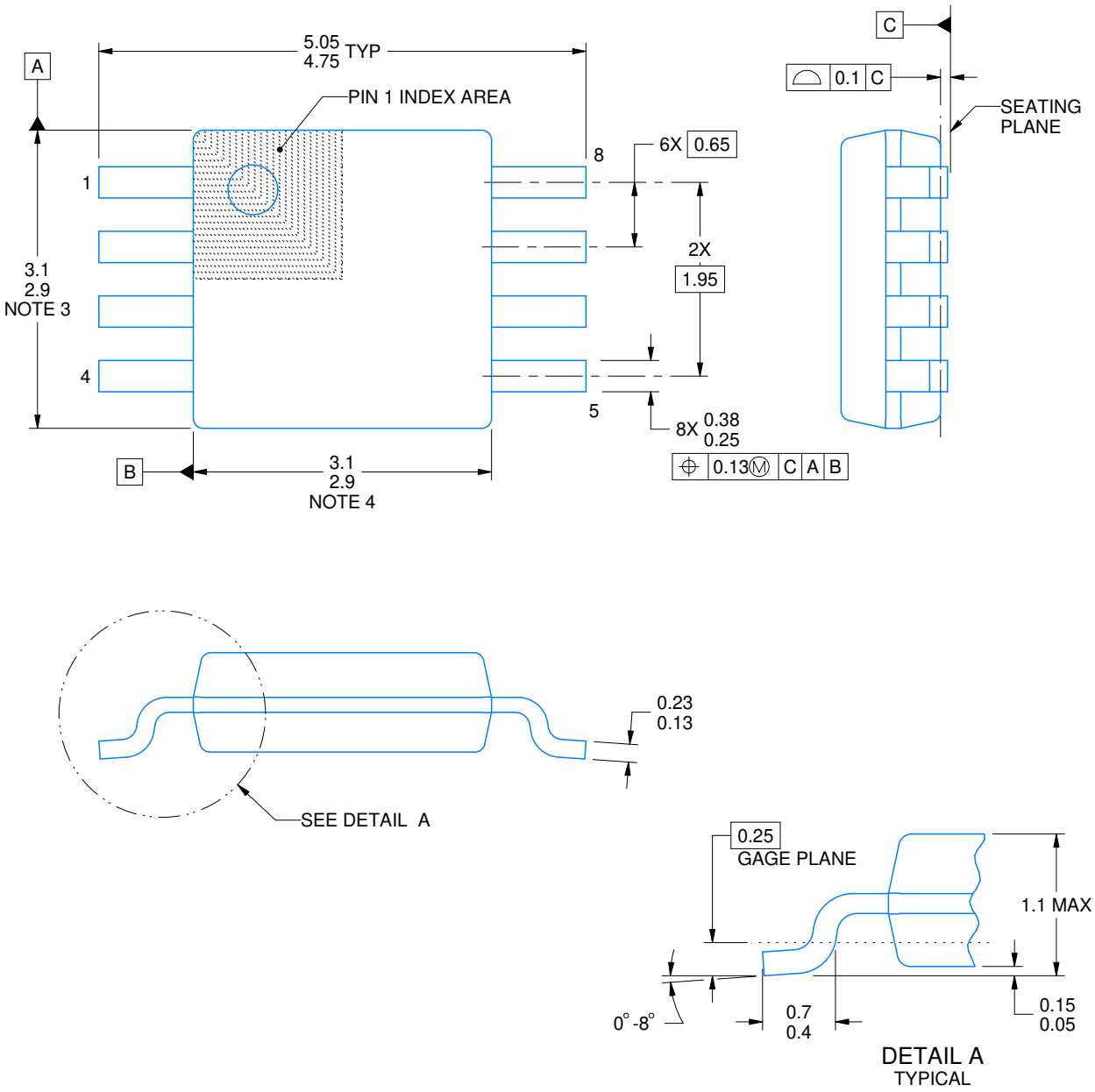
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

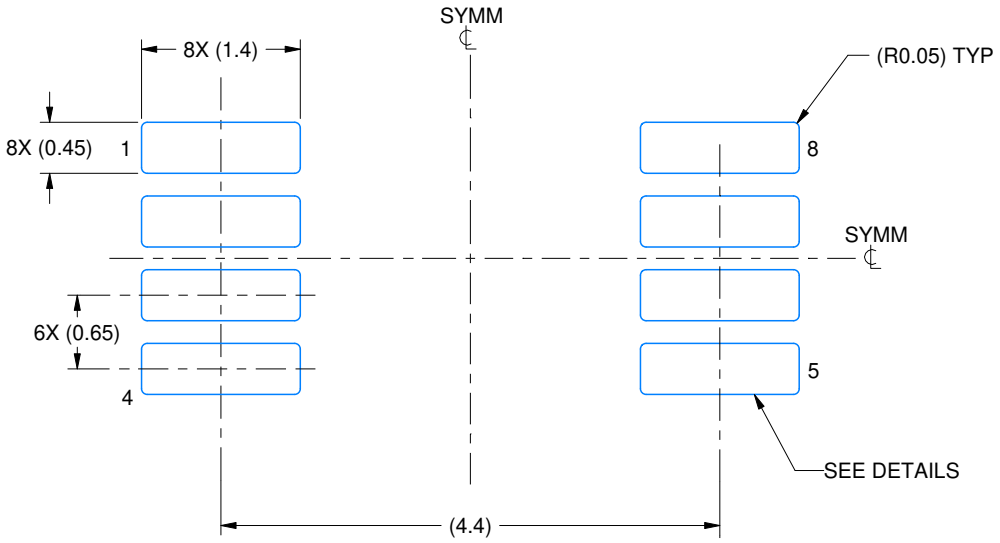


4214862/A 04/2023

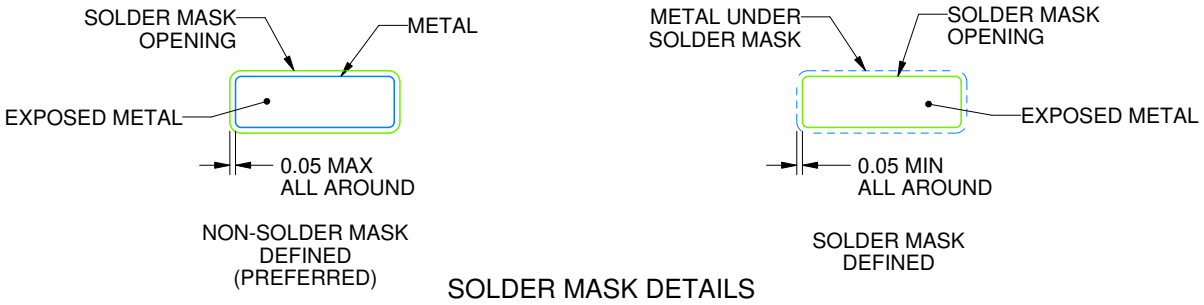
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

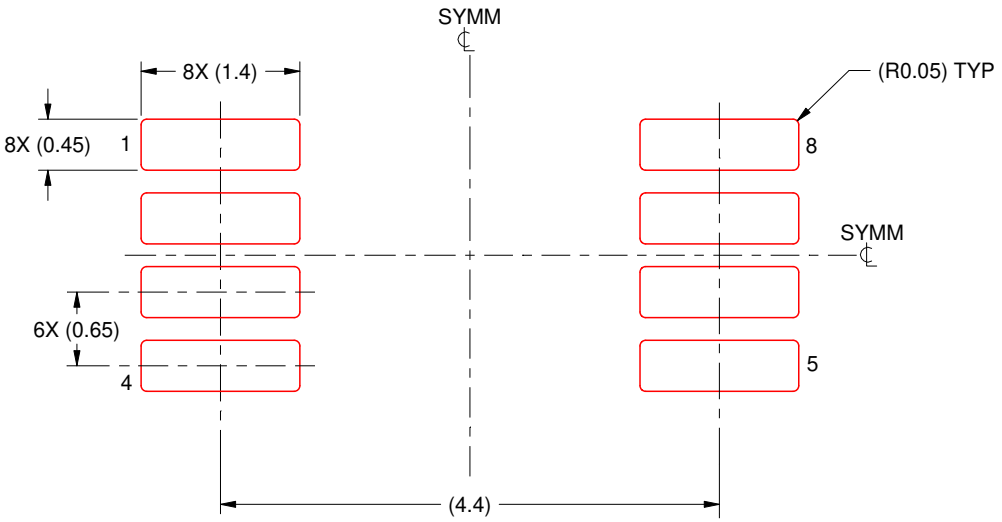


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

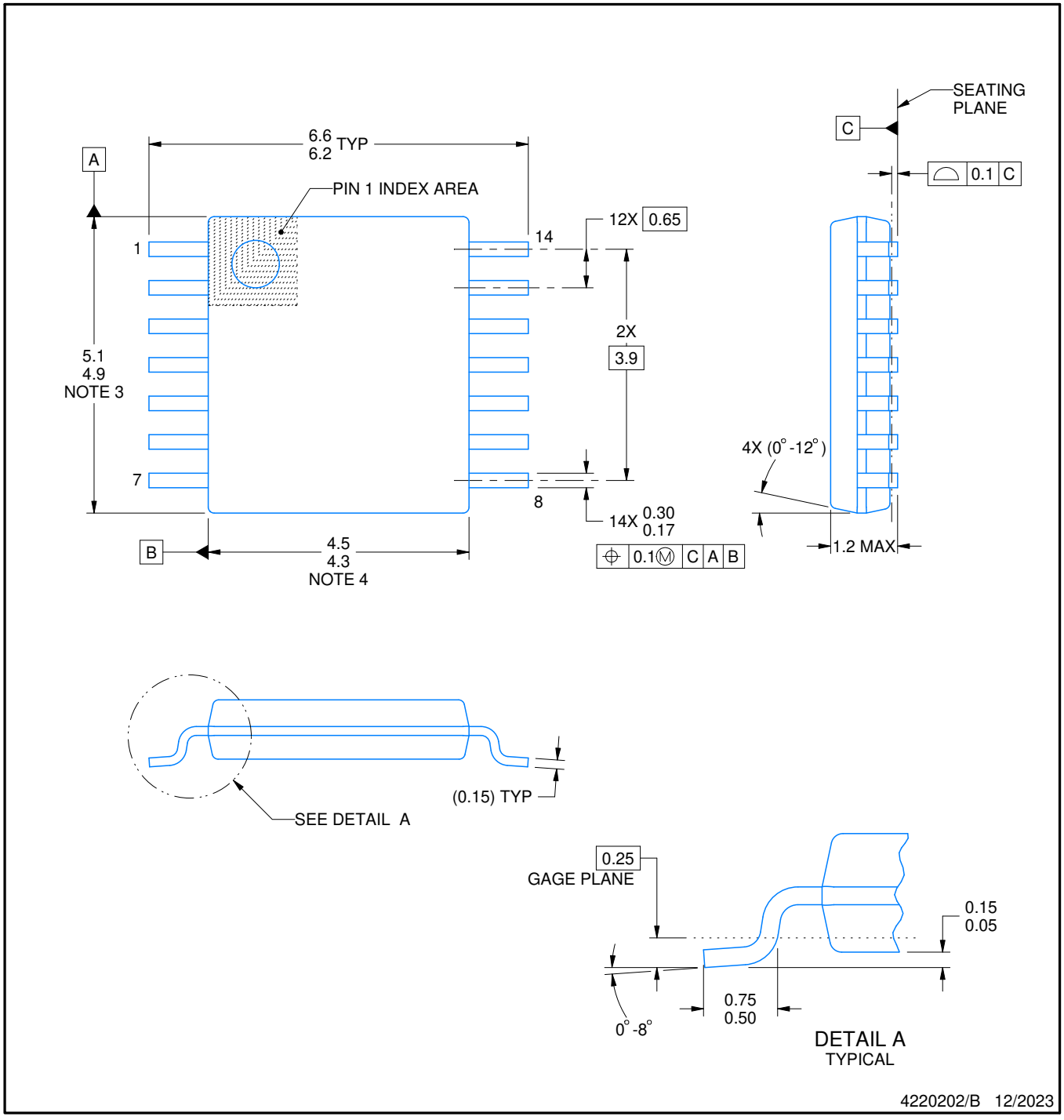
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0014A

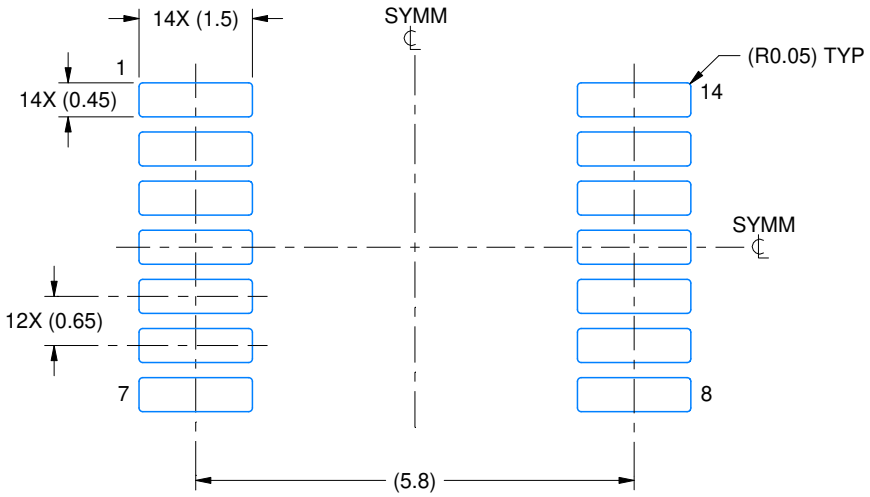
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



NON-SOLDER MASK DEFINED (PREFERRED)

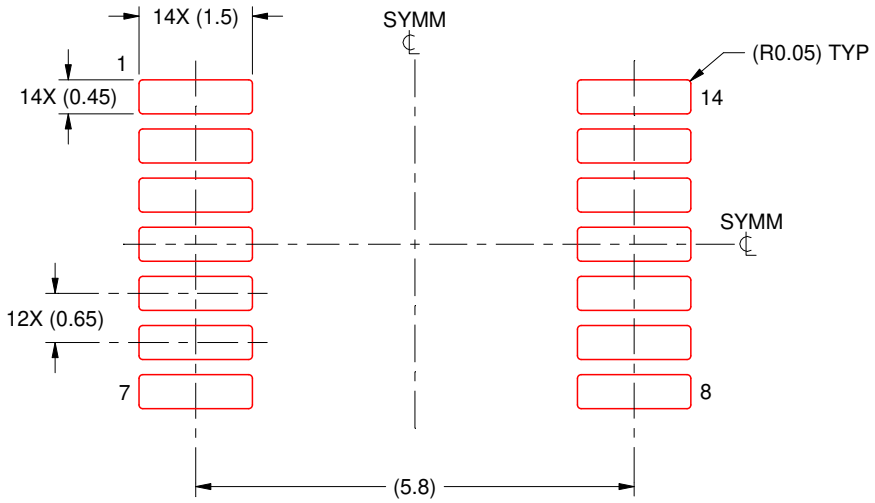
SOLDER MASK DETAILS

SOLDER MASK DEFINED

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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