TEXAS INSTRUMENTS
OPA186, OPA2186, OPA4186
SBOS968C – JUNE 2022 – REVISED JULY 2023

OPAx186 Precision, Rail-to-Rail Input/Output, 24-V, Zero-Drift Operational Amplifiers

1 Features

- High precision:
  - Offset drift: 0.01 µV/°C
  - Low offset voltage: 1 µV
- Low quiescent current: 90 µA
- Excellent dynamic performance:
  - Gain bandwidth: 750 kHz
  - Slew rate: 0.35 V/µs
- Robust design:
  - RFI/EMI filtered inputs
- Rail-to-rail input/output
- Supply range: 4.5 V to 24 V
- Temperature: –40°C to +125°C

2 Applications

- PC PSU and game console unit
- Merchant DC/DC
- Flow transmitter
- Pressure transmitter
- Merchant battery charger
- Electricity meter

3 Description

The OPA186, OPA2186, and OPA4186 (OPAx186) are low-power, 24-V, rail-to-rail input and output, zero-drift operational amplifiers (op amps). These op amps feature only 10 µV of offset voltage (maximum) and 0.04 µV/°C of offset voltage drift over temperature (maximum). These devices are a great choice for precision instrumentation, signal measurement, and active-filtering applications.

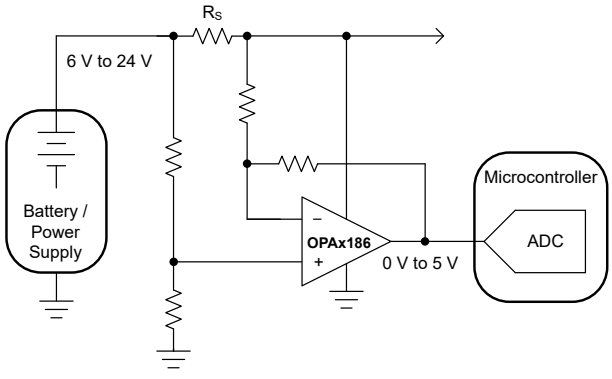
The low quiescent current consumption of 90 µA makes the OPAx186 an excellent option for power-sensitive applications, such as battery-powered instrumentation and portable systems.

Moreover, the high common-mode architecture along with low offset voltage allows for high-side current shunt monitoring at the positive rail. These devices also provide robust ESD protection during shipment, handling, and assembly.

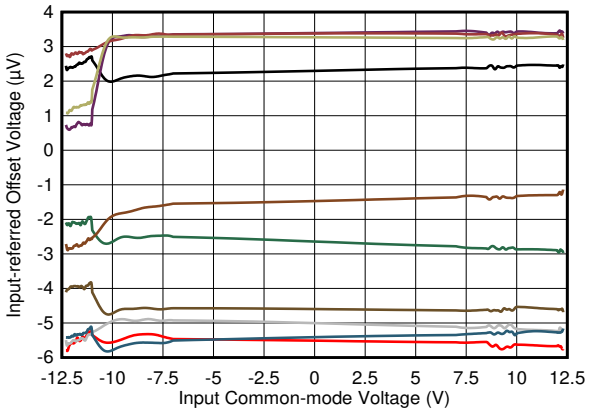
Device Information

PART NUMBER	CHANNELS	PACKAGE(1)
OPA186	Single	D (SOIC, 8)
		DBV (SOT-23, 5)
OPA2186	Dual	D (SOIC, 8)
		DDF (SOT-23, 8)
OPA4186	Quad	D (SOIC, 14)

(1) For all available packages, see the package option addendum at the end of the data sheet.



High-Side Current Shunt Monitor Application



V_{OS} vs Input Common Mode Voltage

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (November 2022) to Revision C (July 2023)	Page
• Added OPA186 D (SOIC, 8) package and associated content as production data (active)	1

Changes from Revision A (June 2022) to Revision B (November 2022)	Page
• Added OPA186 and OPA4186 devices and associated content	1
• Changed *ESD Ratings* table HBM value	5
• Changed *ESD Ratings* table CDM value	5

Changes from Revision * (June 2022) to Revision A (September 2022)	Page
• Changed OPA2186 from advanced information (preview) to production data (active)	1

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5 Pin Configuration and Functions

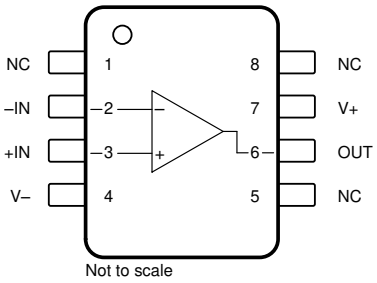


Figure 5-1. OPA186: D Package, 8-Pin SOIC (Top View)

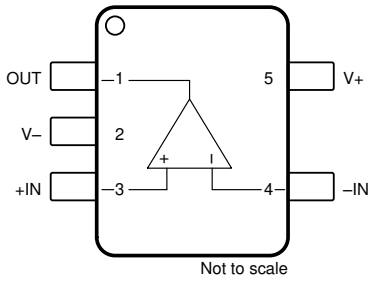


Figure 5-2. OPA186: DBV Package, 5-Pin SOT-23 (Top View)

Table 5-1. Pin Functions: OPA186

PIN			TYPE	DESCRIPTION
NAME	NO.			
	D (SOIC)	DBV (SOT-23)		
–IN	4	2	Input	Inverting input
+IN	3	3	Input	Noninverting input
OUT	1	6	Output	Output
V–	2	4	Power	Negative (lowest) power supply
V+	5	7	Power	Positive (highest) power supply
NC	—	1, 8, 5	—	No connection (can be left floating)

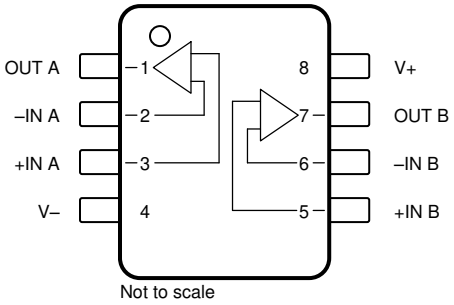


Figure 5-3. OPA2186: D Package, 8-Pin SOIC and DDF Package, 8-Pin SOT-23 (Top View)

Table 5-2. Pin Functions: OPA2186

PIN		TYPE	DESCRIPTION
NAME	NO.		
–IN A	2	Input	Inverting input channel A
+IN A	3	Input	Noninverting input channel A
–IN B	6	Input	Inverting input channel B
+IN B	5	Input	Noninverting input channel B
OUT A	1	Output	Output channel A
OUT B	7	Output	Output channel B
V–	4	Power	Negative supply
V+	8	Power	Positive supply

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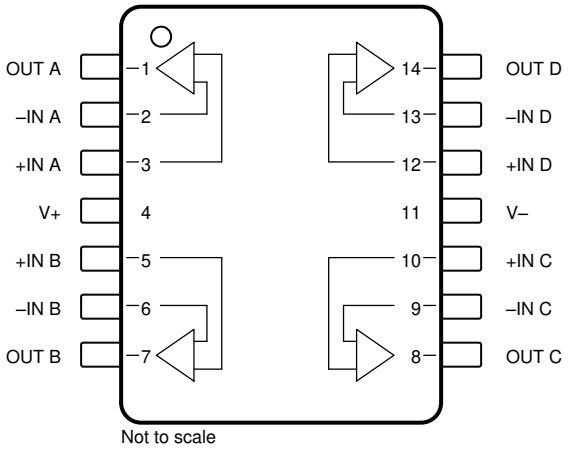


Figure 5-4. OPA4186: D Package, 14-Pin SOIC (Top View)

Table 5-3. Pin Functions: OPA4186

PIN		TYPE	DESCRIPTION
NAME	NO.		
–IN A	2	Input	Inverting input channel A
+IN A	3	Input	Noninverting input channel A
–IN B	6	Input	Inverting input channel B
+IN B	5	Input	Noninverting input channel B
–IN C	9	Input	Inverting input channel C
+IN C	10	Input	Noninverting input channel C
–IN D	13	Input	Inverting input channel D
+IN D	12	Input	Noninverting input channel D
OUT A	1	Output	Output channel A
OUT B	7	Output	Output channel B
OUT C	8	Output	Output channel C
OUT D	14	Output	Output channel D
V–	11	Power	Negative supply
V+	4	Power	Positive supply

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)			26	V
	Input voltage	Common-mode	(V–) –0.5	(V+) + 0.5	V
		Differential		(V+) – (V–) + 0.2	
	Output short-circuit(2)		Continuous		
T_J	Operating junction temperature		-40	150	°C
T_{stg}	Storage temperature		-65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply voltage	Single supply	4.5		24	V
		Dual supply	±2.25		±12	
T_A	Specified temperature		–40		125	°C

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6.4 Thermal Information: OPA186

THERMAL METRIC(1)		OPA186		UNIT
		D (SOIC)	DBV (SOT-23)	
		8 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	135.3	166.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	75.6	62.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	78.7	38.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	25.4	12.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	78.0	38.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Thermal Information: OPA2186

THERMAL METRIC(1)		OPA2186		UNIT
		DDF (SOT-23)	D (SOIC)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	150.4	128.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	85.6	69.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	70.0	72.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	8.1	20.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	69.6	71.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.6 Thermal Information: OPA4186

THERMAL METRIC(1)		OPA4186	UNIT
		D (SOIC)	
		14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	84.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	37.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	41.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	6.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	40.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.7 Electrical Characteristics

at T_A = 25°C, V_S = ±2.25 V to ±12 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	OPA186, OPA2186[1]			±1	±10	µV
		OPA4186[1]			±6	±40	
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +125°C[1]	OPA186, OPA2186		±0.01	±0.04	µV/°C
			OPA4186		±0.025	±0.1	
PSRR	Power-supply rejection ratio	T_A = –40°C to +125°C[1]	OPA186, OPA2186		±0.02	±0.2	µV/V
			OPA4186		±0.08	±0.4	
INPUT BIAS CURRENT							
I_B	Input bias current	V_S = ±12 V			±5	±55	pA
			T_A = –40°C to +85°C[1]			±550	
			T_A = –40°C to +125°C[1], OPA186, OPA2186			±4.8	nA
			T_A = –40°C to +125°C[1], OPA4186			±6.2	
I_{OS}	Input offset current				±10	±100	pA
		T_A = –40°C to +85°C[1]				±1	nA
		T_A = –40°C to +125°C[1]	OPA186, OPA2186			±1.25	
			OPA4186			±3.8	
NOISE							
	Input voltage noise	f = 0.1 Hz to 10 Hz			125		nV_{RMS}
e_N	Input voltage noise density	f = 1 kHz			40		nV/√Hz
i_N	Input current noise	f = 1 kHz			120		fA/√Hz
INPUT VOLTAGE							
V_{CM}	Common-mode voltage			(V–) – 0.2		(V+) + 0.2	V
CMRR	Common-mode rejection ratio	V_S = ±2.25 V, (V–) – 0.1 < V_{CM} < (V+) + 0.1 V	OPA2186	120	140		dB
			OPA186	118	140		
			OPA4186	105	120		
		V_S = ±12 V, (V–) – 0.1 < V_{CM} < (V+) + 0.1 V	OPA186, OPA2186	120	146		
			OPA4186	118	134		
		V_S = ±2.25 V, (V–) – 0.1 < V_{CM} < (V+) + 0.1 V, T_A = –40°C to +125°C[1]	OPA186, OPA2186	106	120		
			OPA4186	100	114		
		V_S = ±12 V, (V–) – 0.1 < V_{CM} < (V+) + 0.1 V, T_A = –40°C to +125°C[1]	OPA186, OPA2186	115	124		
			OPA4186	115	124		
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product				750		kHz
SR	Slew rate	1-V step, G = 1			0.35		V/µs
t_S	Settling time	To 0.1%, 1-V step, G = 1			7.5		µs
	Overload recovery time	V_{IN} × gain > V_S			10		µs
INPUT CAPACITANCE							
Z_{ID}	Differential				100 || 5		MΩ || pF
Z_{ICM}	Common-mode				50 || 2.5		GΩ || pF
OPEN-LOOP VOLTAGE GAIN							
A_{OL}	Open-loop voltage gain	V_S = ±12 V, R_L = 10 kΩ, (V–) + 0.3 V < V_O < (V+) – 0.3 V		123	148		dB
			T_A = –40°C to +125°C[1]	123	146		
		V_S = ±12 V, R_L = 2 kΩ, (V–) + 0.65 V < V_O < (V+) – 0.65 V		123	148		
			T_A = –40°C to +125°C[1]	123	146		

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6.7 Electrical Characteristics (continued)

at T_A = 25°C, V_S = ±2.25 V to ±12 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT							
V_O	Voltage output swing from the rail	Positive rail	No load		5	10	mV
			R_L = 10 kΩ		65		
			R_L = 2 kΩ		345	425	
			R_L = 10 kΩ, T_A = –40°C to +125°C(1)		95	120	
		Negative rail	No load		5	10	
			R_L = 10 kΩ		30		
			R_L = 2 kΩ		90	120	
			R_L = 10 kΩ, T_A = –40°C to +125°C(1)		35	50	
I_{SC}	Short-circuit current				±20		mA
C_{LOAD}	Capacitive load drive				See typical curves		
R_O	Open-loop output impedance				See typical curves		
POWER SUPPLY							
I_Q	Quiescent current per amplifier	V_S = ±2.25 V to ±12 V			90	130	µA
			T_A = –40°C to +125°C(1)			150	

(1) Specification established from device population bench system measurements across multiple lots.

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6.8 Typical Characteristics

at T_A = 25°C, V_S = ±12 V, V_{CM} = V_S / 2, R_L = 10 kΩ (unless otherwise noted)

Table 6-1. Typical Characteristic Graphs

DESCRIPTION	FIGURE
Offset Voltage Distribution	Figure 6-1
Offset Voltage Drift (-40°C to +125C°C)	Figure 6-2
Input Bias Current Distribution	Figure 6-3
Input Offset Current Distribution	Figure 6-4
Offset Voltage vs Common-Mode Voltage	Figure 6-5
Offset Voltage vs Supply Voltage	Figure 6-6
Input Bias Current vs Common-Mode Voltage	Figure 6-7
Open-Loop Gain and Phase vs Frequency	Figure 6-8
Closed-Loop Gain vs Frequency	Figure 6-9
Input Bias Current and Offset Current vs Temperature	Figure 6-10
Output Voltage Swing vs Output Current (Sourcing)	Figure 6-11
Output Voltage Swing vs Output Current (Sinking)	Figure 6-12
CMRR and PSRR vs Frequency	Figure 6-13
CMRR vs Temperature	Figure 6-14
PSRR vs Temperature	Figure 6-15
0.1-Hz to 10-Hz Voltage Noise	Figure 6-16
Input Voltage Noise Spectral Density vs Frequency	Figure 6-17
THD+N vs Frequency	Figure 6-18
THD+N vs Output Amplitude	Figure 6-19
Quiescent Current vs Supply Voltage	Figure 6-20
Quiescent Current vs Temperature	Figure 6-21
Open-Loop Gain vs Temperature (10 kΩ)	Figure 6-22
Open-Loop Gain vs Temperature (2 kΩ)	Figure 6-23
Open-Loop Output Impedance vs Frequency	Figure 6-24
Small-Signal Overshoot vs Capacitive Load (Gain = –1, 10-mV step)	Figure 6-25
Small-Signal Overshoot vs Capacitive Load (Gain = 1, 10-mV step)	Figure 6-26
No Phase Reversal	Figure 6-27
Positive Overload Recovery	Figure 6-28
Negative Overload Recovery	Figure 6-29
Small-Signal Step Response (Gain = 1, 10-mV step)	Figure 6-30
Small-Signal Step Response (Gain = –1, 10-mV step)	Figure 6-31
Large-Signal Step Response (Gain = 1, 10-V step)	Figure 6-32
Large-Signal Step Response (Gain = –1, 10-V step)	Figure 6-33
Phase Margin vs Capacitive Load	Figure 6-34
Settling Time (1-V Step, 0.1% Settling)	Figure 6-35
Short Circuit Current vs Temperature	Figure 6-36
Maximum Output Voltage vs Frequency	Figure 6-37
EMIRR vs Frequency	Figure 6-38
Channel Separation	Figure 6-39

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6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±12 V, V_{CM} = V_S / 2, R_L = 10 kΩ (unless otherwise noted)

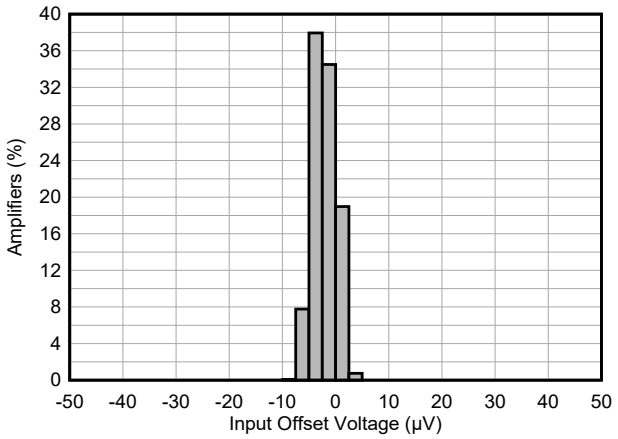


Figure 6-1. Offset Voltage Distribution

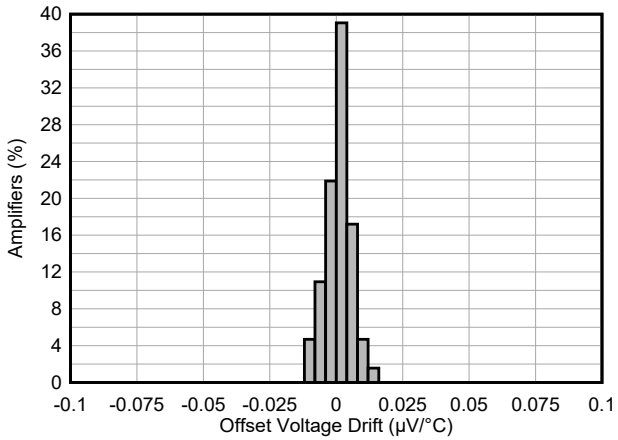


Figure 6-2. Offset Voltage Drift (-40°C to 125C°C)

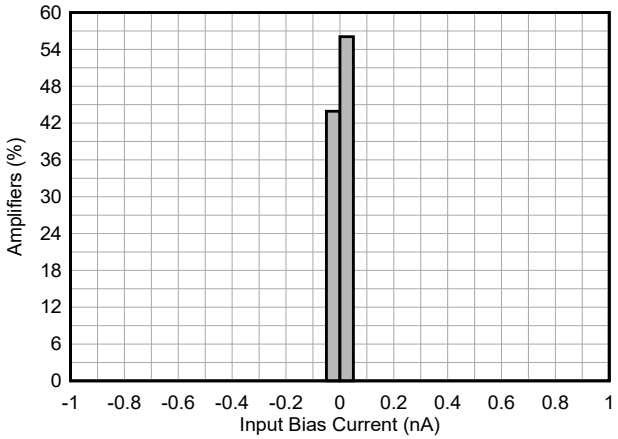


Figure 6-3. Input Bias Current Distribution

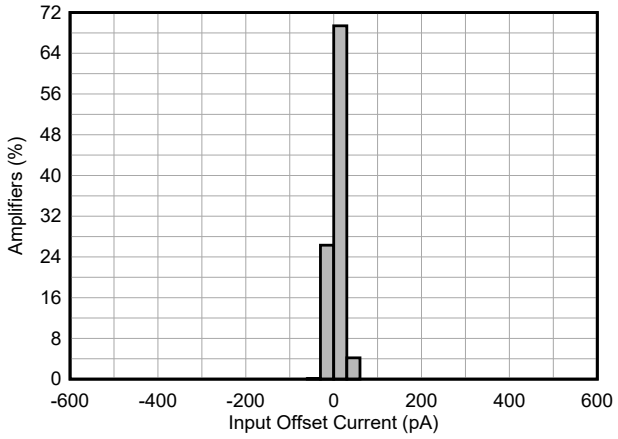


Figure 6-4. Input Offset Current Distribution

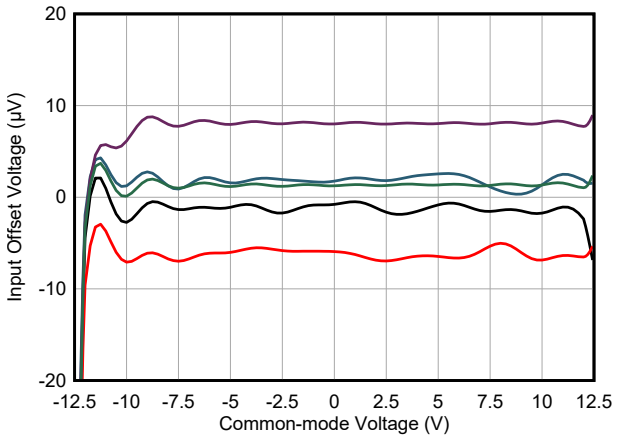


Figure 6-5. Offset Voltage vs Common-Mode Voltage

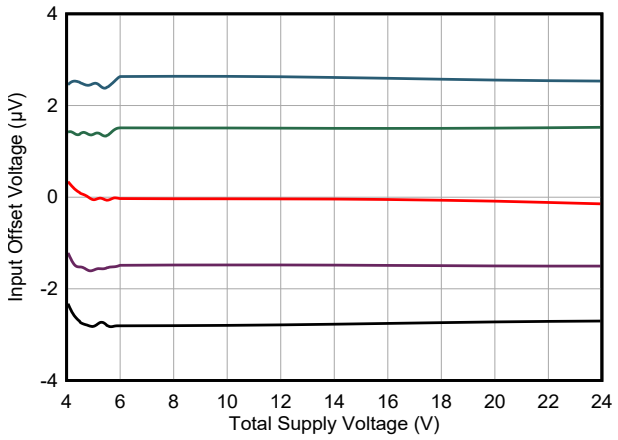


Figure 6-6. Offset Voltage vs Supply Voltage

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6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±12 V, V_{CM} = V_S / 2, R_L = 10 kΩ (unless otherwise noted)

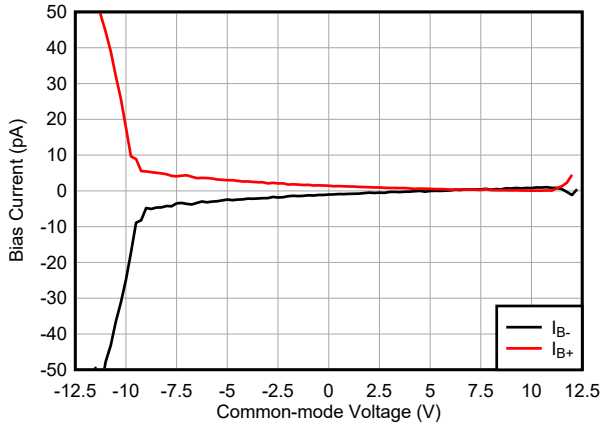


Figure 6-7. Input Bias Current vs Common-Mode Voltage

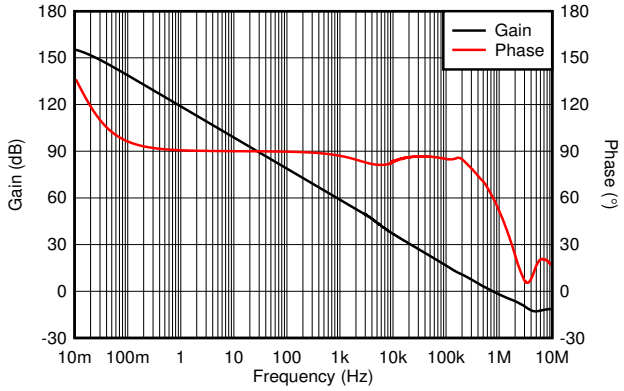


Figure 6-8. Open-Loop Gain and Phase vs Frequency

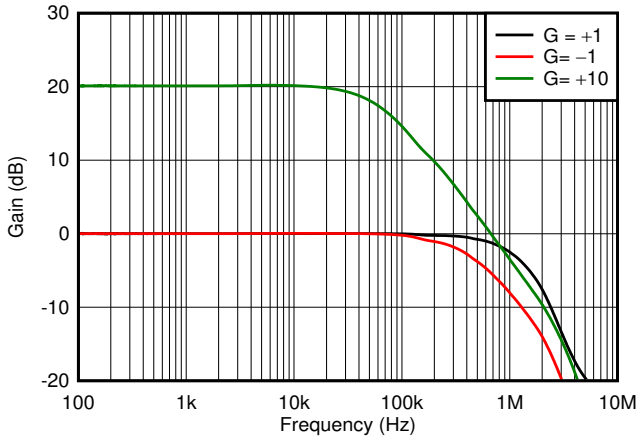


Figure 6-9. Closed-Loop Gain vs Frequency

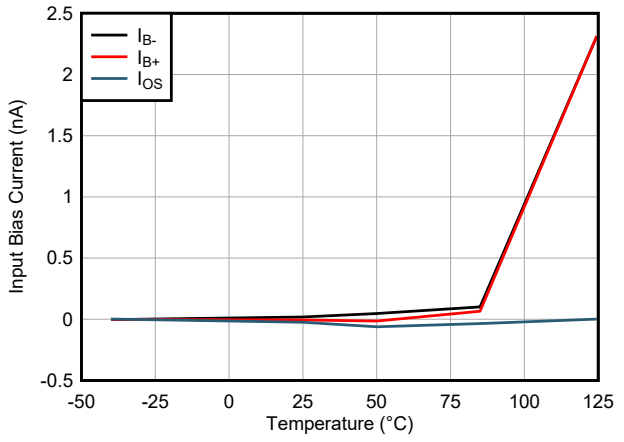


Figure 6-10. Input Bias Current and Offset Current vs Temperature

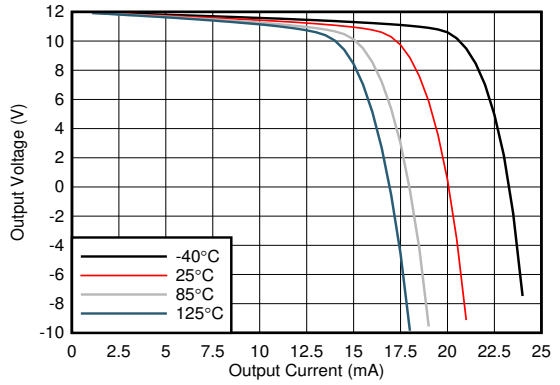


Figure 6-11. Output Voltage Swing vs Output Current (Sourcing)

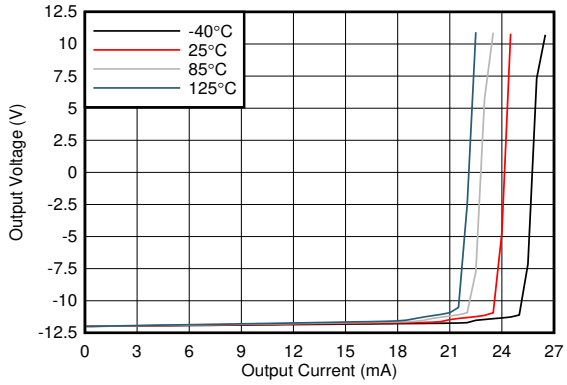


Figure 6-12. Output Voltage Swing vs Output Current (Sinking)

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6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±12 V, V_{CM} = V_S / 2, R_L = 10 kΩ (unless otherwise noted)

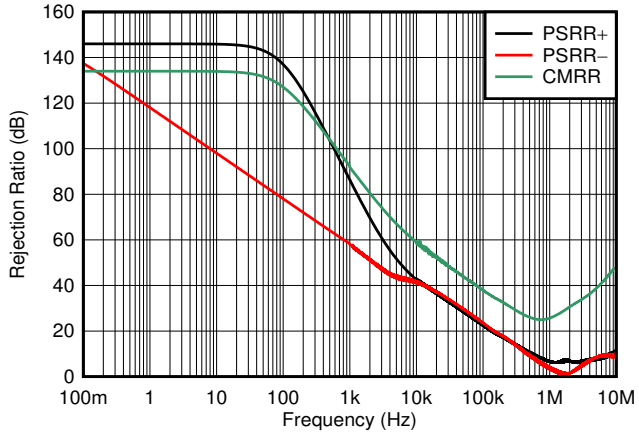


Figure 6-13. CMRR and PSRR vs Frequency

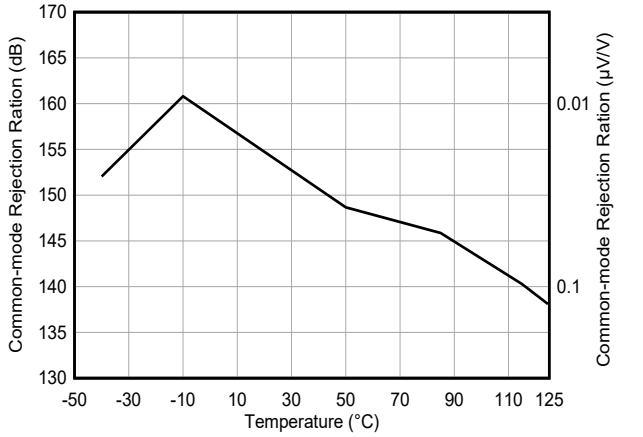


Figure 6-14. CMRR vs Temperature

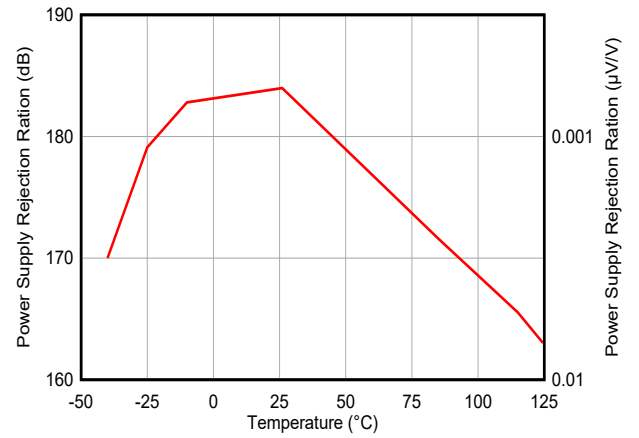


Figure 6-15. PSRR vs Temperature

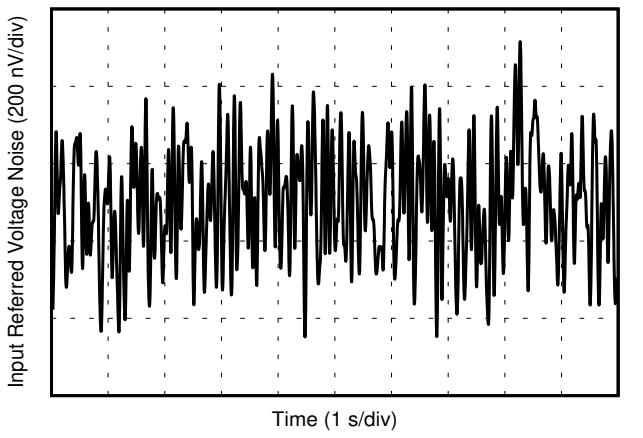


Figure 6-16. 0.1-Hz to 10-Hz Voltage Noise

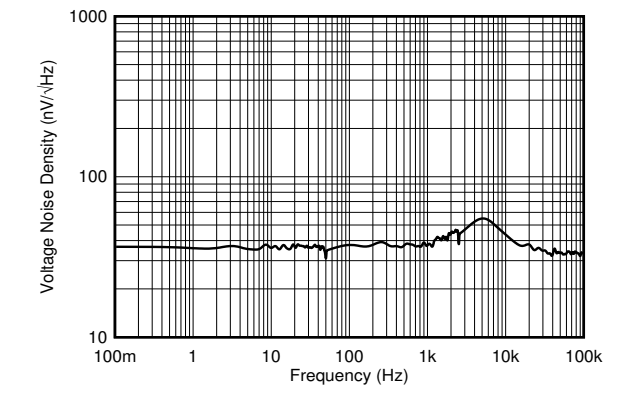


Figure 6-17. Input Voltage Noise Spectral Density vs Frequency

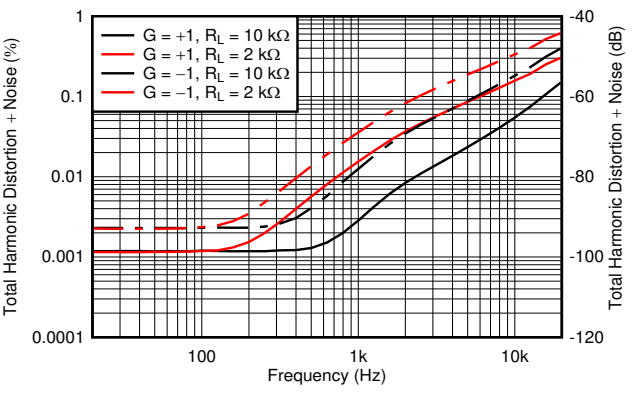


Figure 6-18. THD+N vs Frequency

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6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±12 V, V_{CM} = V_S / 2, R_L = 10 kΩ (unless otherwise noted)

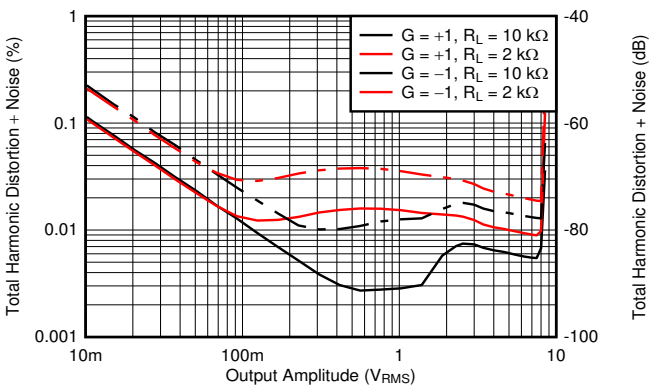


Figure 6-19. THD+N vs Output Amplitude

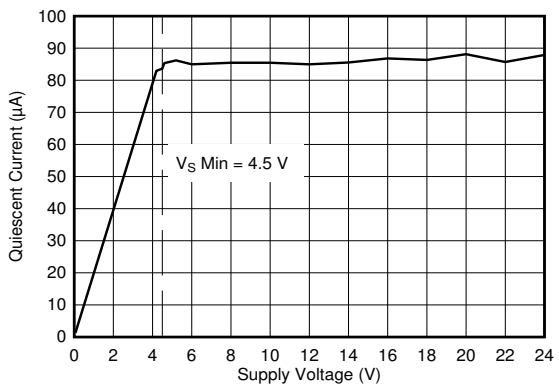


Figure 6-20. Quiescent Current vs Supply Voltage

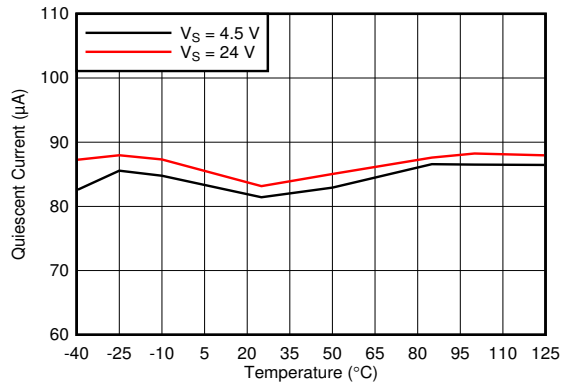


Figure 6-21. Quiescent Current vs Temperature

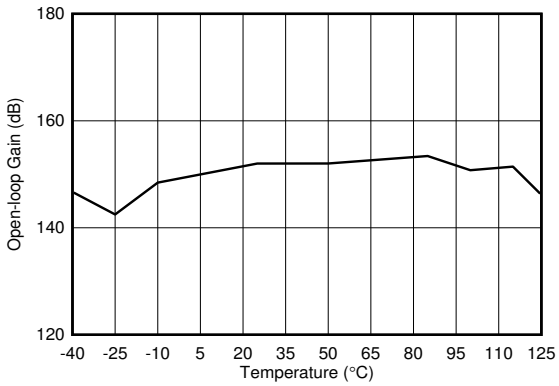
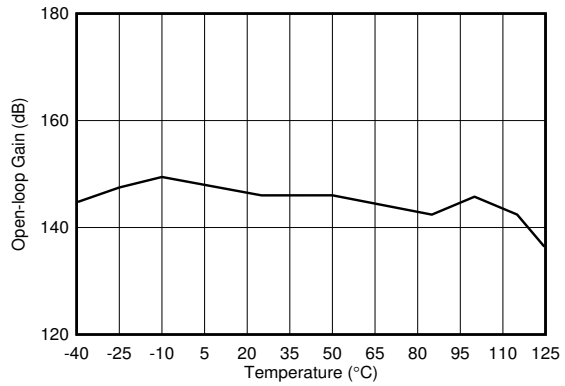


Figure 6-22. Open-Loop Gain vs Temperature



R_L = 2 kΩ

Figure 6-23. Open-Loop Gain vs Temperature

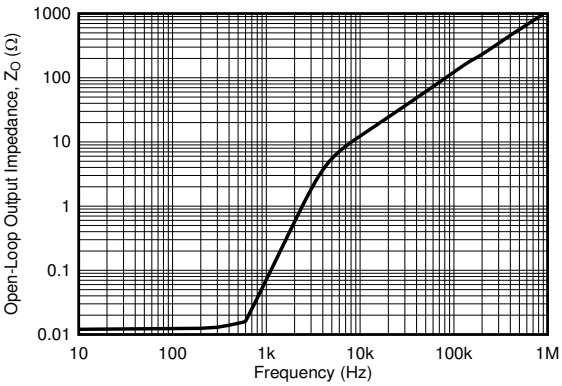
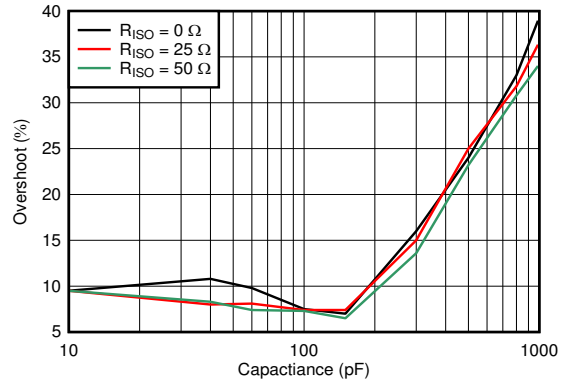


Figure 6-24. Open-Loop Output Impedance vs Frequency

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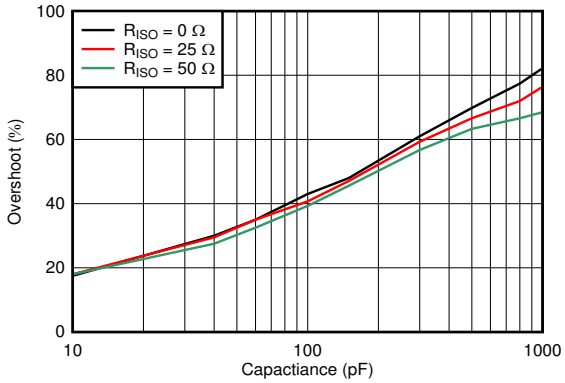
6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±12 V, V_{CM} = V_S / 2, R_L = 10 kΩ (unless otherwise noted)



Gain = –1, 10-mV step

Figure 6-25. Small-Signal Overshoot vs Capacitive Load



Gain = 1, 10-mV step

Figure 6-26. Small-Signal Overshoot vs Capacitive Load

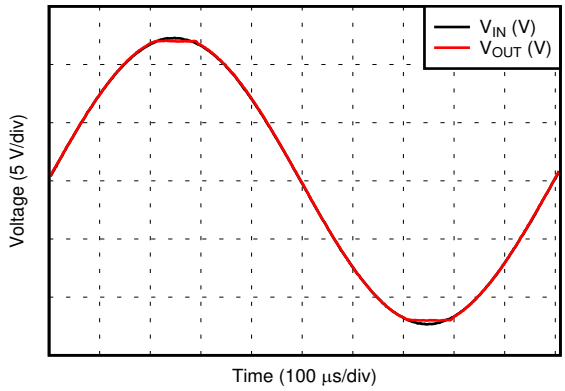


Figure 6-27. No Phase Reversal

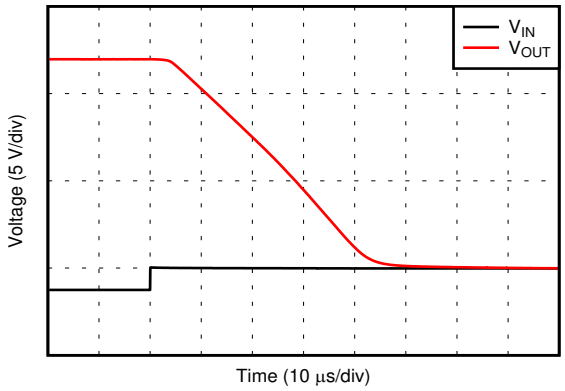


Figure 6-28. Positive Overload Recovery

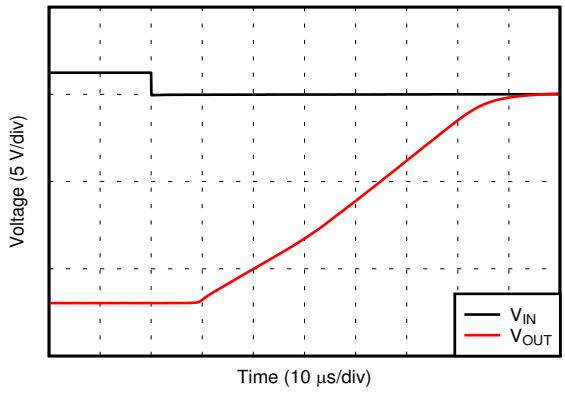
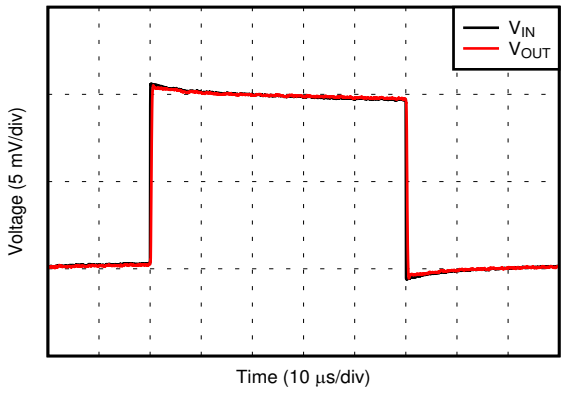


Figure 6-29. Negative Overload Recovery



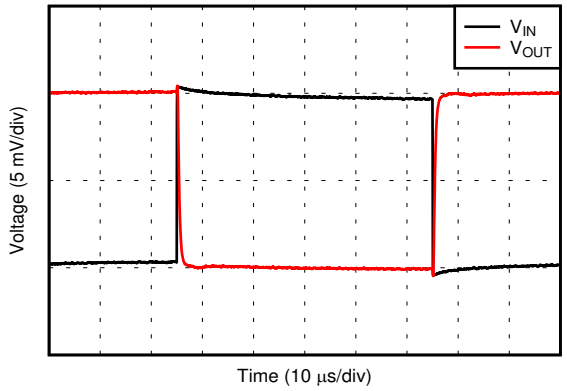
Gain = 1, 10-mV step

Figure 6-30. Small-Signal Step Response

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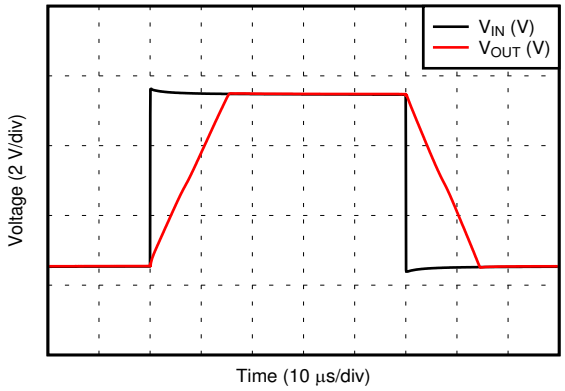
6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±12 V, V_{CM} = V_S / 2, R_L = 10 kΩ (unless otherwise noted)



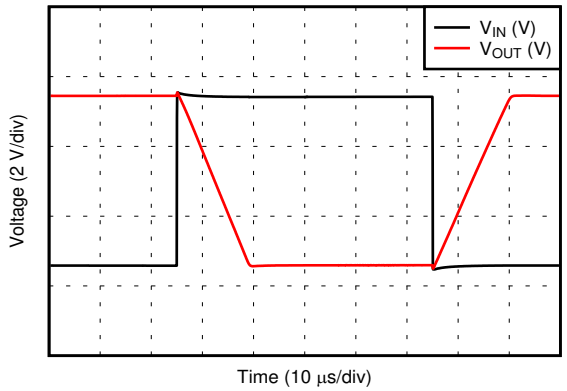
Gain = –1, 10-mV step

Figure 6-31. Small-Signal Step Response



Gain = 1, 10-V step

Figure 6-32. Large-Signal Step Response



Gain = –1, 10-V step

Figure 6-33. Large-Signal Step Response

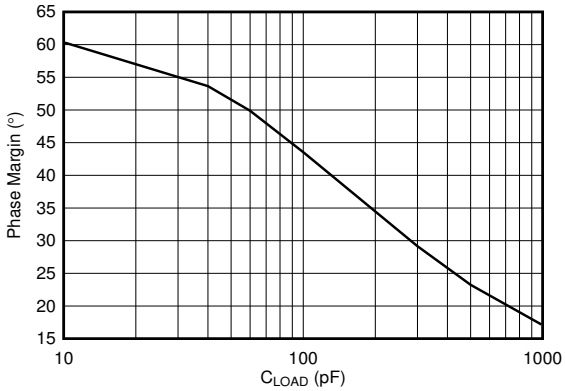
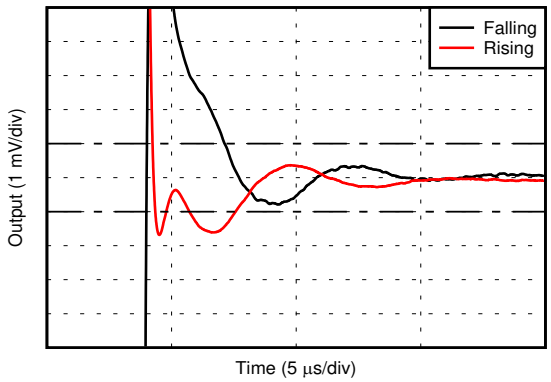


Figure 6-34. Phase Margin vs Capacitive Load



1-V step, 0.1% settling

Figure 6-35. Settling Time

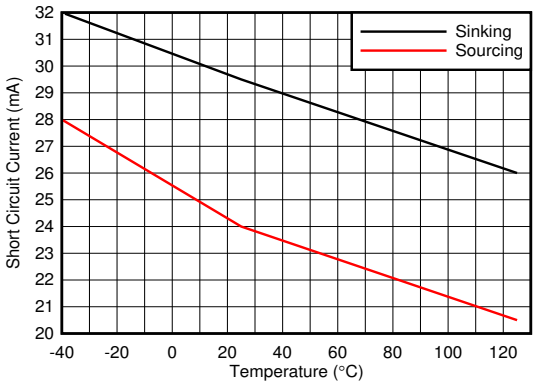


Figure 6-36. Short Circuit Current vs Temperature

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6.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±12 V, V_{CM} = V_S / 2, R_L = 10 kΩ (unless otherwise noted)

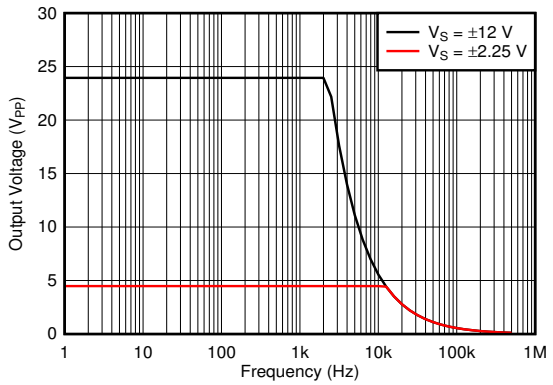


Figure 6-37. Maximum Output Voltage vs Frequency

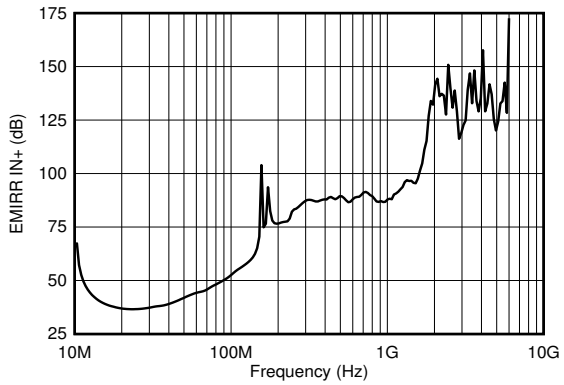


Figure 6-38. EMIRR vs Frequency

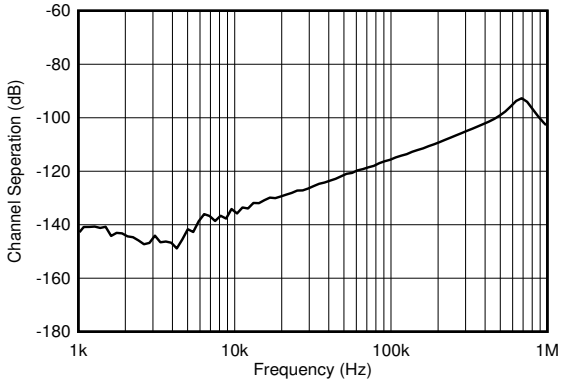


Figure 6-39. Channel Separation

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7 Detailed Description

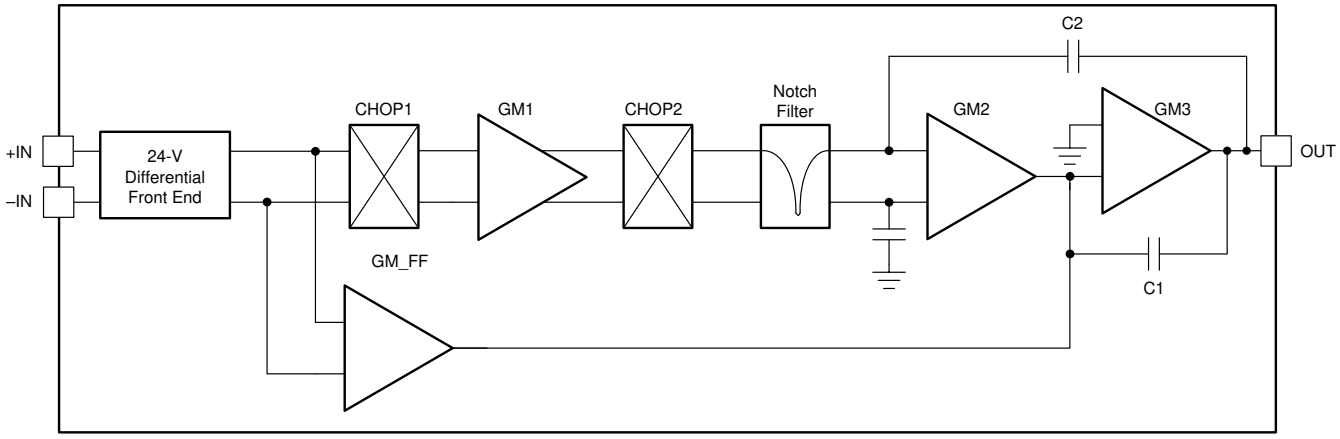
7.1 Overview

The OPAx186 operational amplifier combines precision offset and drift with excellent overall performance, making the device a great choice for a wide variety of precision applications. The precision offset drift of only 0.01 µV/°C provides stability over the entire operating temperature range of –40°C to +125°C. In addition, this device offers excellent linear performance with high CMRR, PSRR, and A_{OL}. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1-µF capacitors are adequate. For details and a layout example, see Section 8.4.

The OPAx186 is part of a family of zero-drift, MUX-friendly, rail-to-rail output operational amplifiers. This device operates from 4.5 V to 24 V, is unity-gain stable, and is designed for a wide range of general-purpose and precision applications. The zero-drift architecture provides ultra-low input offset voltage and near-zero input offset voltage drift over temperature and time. This choice of architecture also offers outstanding ac performance, such as ultra-low broadband noise, zero flicker noise, and outstanding distortion performance when operating at less than the chopper frequency.

The following section shows a representation of the proprietary OPAx186 architecture.

7.2 Functional Block Diagram



7.3 Feature Description

The OPAx186 operational amplifier has several integrated features to help maintain a high level of precision through a variety of applications. These include a rail-to-rail inputs, phase-reversal protection, input bias current clock feedthrough, EMI rejection, electrical overstress protection and MUX-friendly Inputs.

7.3.1 Rail-to-Rail Inputs

Unlike many chopper amplifiers, the OPAx186 has rail-to-rail inputs that allow the input common-mode voltage to not only reach, but exceed the supply voltages by 200 mV. This configuration simplifies power-supply requirements by not requiring headroom over the input signal range.

The OPAx186 is specified for operation from 4.5 V to 24 V (±2.25 V to ±12 V) with rail-to-rail inputs. Many specifications apply from –40°C to +125°C.

7.3.2 Phase-Reversal Protection

The OPAx186 has internal phase-reversal protection. Some op amps exhibit a phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The OPAx186 input prevents phase reversal with excessive common-mode voltage. Instead, the output limits into the appropriate rail. Figure 7-1 shows this performance.

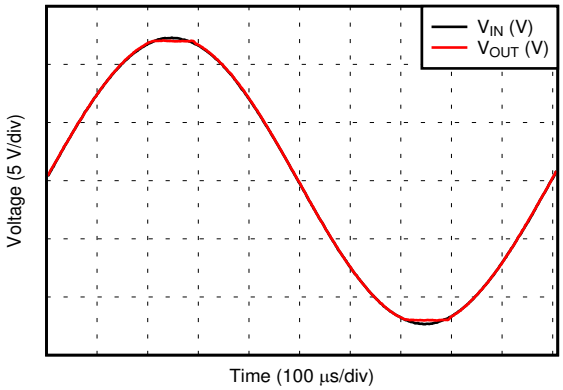


Figure 7-1. No Phase Reversal

7.3.3 Input Bias Current Clock Feedthrough

Zero-drift amplifiers such as the OPAx186 use a switching architecture on the inputs to correct for the intrinsic offset and drift of the amplifier. Charge injection from the integrated switches on the inputs can introduce short transients in the input bias current of the amplifier. The extremely short duration of these pulses prevents the pulses from amplifying; however, the pulses can be coupled to the output of the amplifier through the feedback network. The most effective method to prevent transients in the input bias current from producing additional noise at the amplifier output is to use a low-pass filter, such as an RC network.

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7.3.4 EMI Rejection

The OPAx186 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI interference from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the OPAx186 benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. Figure 7-2 shows the results of this testing on the OPAx186. Table 7-1 lists the EMIRR +IN values for the OPAx186 at particular frequencies commonly encountered in real-world applications. Table 7-1 lists applications that can be centered on or operated near the particular frequency shown. See also the *EMI Rejection Ratio of Operational Amplifiers* application report, available for download from www.ti.com.

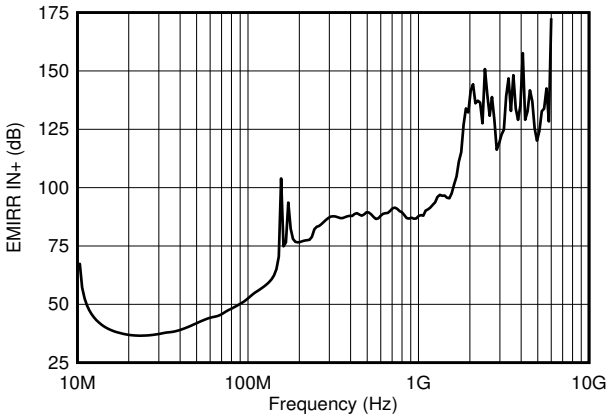


Figure 7-2. EMIRR Testing

Table 7-1. OPAx186 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION AND ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	48.4 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	52.8 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	69.1 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	88.9 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	82.5 dB
5 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	95.5 dB

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The electromagnetic interference (EMI) rejection ratio, or EMIRR, describes the EMI immunity of operational amplifiers. An adverse effect that is common to many op amps is a change in the offset voltage as a result of RF signal rectification. An op amp that is more efficient at rejecting this change in offset as a result of EMI has a higher EMIRR and is quantified by a decibel value. Measuring EMIRR can be performed in many ways, but this section provides the EMIRR +IN, which specifically describes the EMIRR performance when the RF signal is applied to the noninverting input pin of the op amp. In general, only the noninverting input is tested for EMIRR for the following three reasons:

- Op amp input pins are known to be the most sensitive to EMI, and typically rectify RF signals better than the supply or output pins.
- The noninverting and inverting op amp inputs have symmetrical physical layouts and exhibit nearly matching EMIRR performance
- EMIRR is more simple to measure on noninverting pins than on other pins because the noninverting input terminal can be isolated on a PCB. This isolation allows the RF signal to be applied directly to the noninverting input terminal with no complex interactions from other components or connecting PCB traces.

High-frequency signals conducted or radiated to any pin of the operational amplifier can result in adverse effects, as there is insufficient amplifier loop gain to correct for signals with spectral content outside the bandwidth. Conducted or radiated EMI on inputs, power supply, or output can result in unexpected dc offsets, transient voltages, or other unknown behavior. Take care to properly shield and isolate sensitive analog nodes from noisy radio signals and digital clocks and interfaces.

Figure 7-2 shows the EMIRR +IN of the OPAx186 plotted versus frequency. The OPAx186 unity-gain bandwidth is 750 kHz. EMIRR performance less than this frequency denotes interfering signals that fall within the op-amp bandwidth.

7.3.4.1 EMIRR +IN Test Configuration

Figure 7-3 shows the circuit configuration for testing the EMIRR +IN. An RF source is connected to the op-amp noninverting input pin using a transmission line. The op amp is configured in a unity-gain buffer topology with the output connected to a low-pass filter (LPF) and a digital multimeter (DMM). A large impedance mismatch at the op amp input causes a voltage reflection; however, this effect is characterized and accounted for when determining the EMIRR IN+. The multimeter samples and measures the resulting dc offset voltage. The LPF isolates the multimeter from residual RF signals that can interfere with multimeter accuracy.

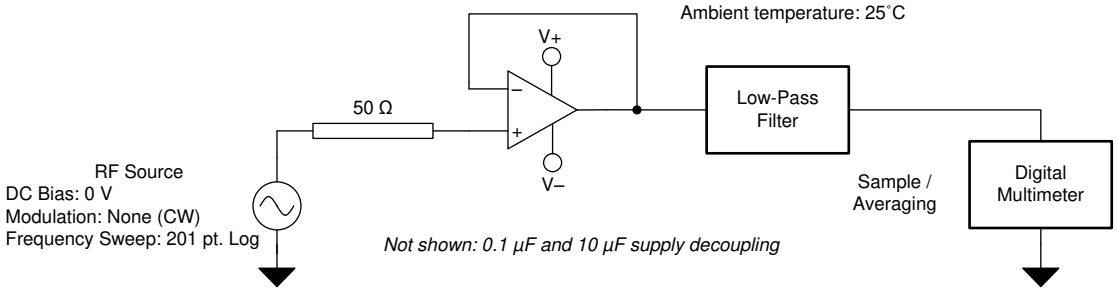


Figure 7-3. EMIRR +IN Test Configuration

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7.3.5 Electrical Overstress

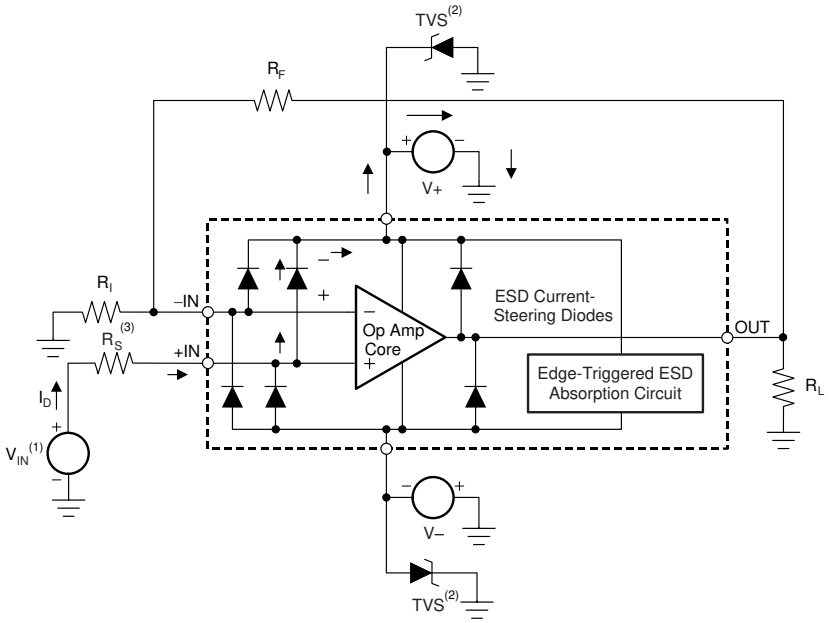
Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and the relevance to an electrical overstress event is helpful. Figure 7-4 shows an illustration of the ESD circuits contained in the OPAx186 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high-current pulse while discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more amplifier device pins, current flows through one or more steering diodes. Depending on the path that the current takes, the absorption device can activate. The absorption device has a trigger or threshold voltage that is greater than the normal operating voltage of the OPAx186, but less than the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

Figure 7-4 shows that when the operational amplifier connects into a circuit, the ESD protection components are intended to remain inactive, and do not become involved in the application circuit operation. However, circumstances can arise where an applied voltage exceeds the operating voltage range of a given pin. If this condition occurs, there is a risk that some internal ESD protection circuits are biased on and conduct current. Any such current flow occurs through steering-diode paths and rarely involves the absorption device.



(1) V_{IN} = (V+) + 500 mV

(2) TVS: 26 V > $V_{TVSBR\ (min)}$ > V+, where $V_{TVSBR\ (min)}$ is the minimum specified value for the transient voltage suppressor breakdown voltage.

(3) Suggested value is approximately 5 kΩ in example overvoltage condition.

Figure 7-4. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

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Figure 7-4 shows a specific example where the input voltage (V_{IN}) exceeds the positive supply voltage (V+) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If V+ can sink the current, one of the upper input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the data sheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, V_{IN} can begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies V+ or V– are at 0 V. Again, this question depends on the supply characteristic while at 0 V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the operational amplifier supply current can be supplied by the input source through the current-steering diodes. This state is not a normal biasing condition for the amplifier and can result in specification degradation or abnormal operation. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is any uncertainty about the ability of the supply to absorb this current, add external Zener diodes to the supply pins; see also Figure 7-4. The Zener voltage must be selected such that the diode does not turn on during normal operation. However, the Zener voltage must be low enough so that the Zener diode conducts if the supply pin begins to rise above the safe operating supply voltage level.

7.3.6 MUX-Friendly Inputs

The OPAx186 features a proprietary input stage design that allows an input differential voltage to be applied while maintaining high input impedance. Typically, high-voltage CMOS or bipolar-junction input amplifiers feature antiparallel diodes that protect input transistors from large V_{GS} voltages that can exceed the semiconductor process maximum and permanently damage the device. Large V_{GS} voltages can be forced when applying a large input step, switching between channels, or attempting to use the amplifier as a comparator.

The OPAx186 solves these problems with a switched-input technique that prevents large input bias currents when large differential voltages are applied. This input architecture addresses many issues seen in switched or multiplexed applications, where large disruptions to RC filtering networks are caused by fast switching between large potentials. The OPAx186 offers outstanding settling performance as a result of these design innovations and built-in slew-rate boost and wide bandwidth. The OPAx186 can also be used as a comparator. Differential and common-mode input ranges still apply.

7.4 Device Functional Modes

The OPAx186 has a single functional mode, and is operational when the power-supply voltage is greater than 4.5 V (±2.25 V). The maximum power supply voltage for the OPAx186 is 24 V (±12 V).

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The OPAx186 operational amplifier combines precision offset and drift with excellent overall performance, making the device an excellent choice for many precision applications. The precision offset drift of only 0.01 µV/°C provides stability over the entire temperature range. In addition, the device pairs excellent CMRR, PSRR, and A_{OL} dc performance with outstanding low-noise operation. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1-µF capacitors are adequate.

8.1.1 Basic Noise Calculations

Low-noise circuit design requires careful analysis of all noise sources. In many cases, external noise sources can dominate; consider the effect of source resistance on overall op-amp noise performance. Total noise of the circuit is the root-sum-square combination of all noise components.

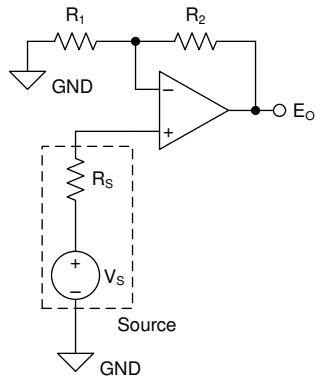
The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. The source impedance is usually fixed; consequently, select op amp and the feedback resistors that minimize the respective contributions to the total noise.

Figure 8-1 shows both noninverting *(A)* and inverting *(B)* op-amp circuit configurations with gain. In circuit configurations with gain, the feedback network resistors also contribute noise. In general, the current noise of the op amp reacts with the feedback resistors to create additional noise components. However, the extremely low current noise of the OPAx186 means that the current noise contribution can be ignored.

The feedback resistor values can generally be chosen to make these noise sources negligible. Low impedance feedback resistors load the output of the amplifier. The equations for total noise are shown for both configurations.

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(A) Noise in Noninverting Gain Configuration



Noise at the output is given as E_O, where

$$(1)\quad E_O = \left(1 + \frac{R_2}{R_1}\right) \cdot \sqrt{(e_S)^2 + (e_N)^2 + \left(e_{R_1 \| R_2}\right)^2 + (i_N \cdot R_S)^2 + \left(i_N \cdot \left[\frac{R_1 \cdot R_2}{R_1 + R_2}\right]\right)^2} \quad [\,V_{RMS}\,]$$

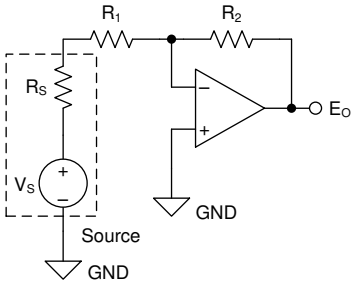
$$(2)\quad e_S = \sqrt{4 \cdot k_B \cdot T(K) \cdot R_S} \quad \left[\frac{V}{\sqrt{Hz}}\right] \quad \text{Thermal noise of } R_S$$

$$(3)\quad e_{R_1 \| R_2} = \sqrt{4 \cdot k_B \cdot T(K) \cdot \left[\frac{R_1 \cdot R_2}{R_1 + R_2}\right]} \quad \left[\frac{V}{\sqrt{Hz}}\right] \quad \text{Thermal noise of } R_1 \text{ || } R_2$$

$$(4)\quad k_B = 1.38065 \cdot 10^{-23} \quad \left[\frac{J}{K}\right] \quad \text{Boltzmann Constant}$$

$$(5)\quad T(K) = 237.15 + T(°C) \quad [\,K\,] \quad \text{Temperature in kelvins}$$

(B) Noise in Inverting Gain Configuration



Noise at the output is given as E_O, where

$$(6)\quad E_O = \left(1 + \frac{R_2}{R_S + R_1}\right) \cdot \sqrt{(e_N)^2 + \left(e_{R_1 + R_S \| R_2}\right)^2 + \left(i_N \cdot \left[\frac{(R_S + R_1) \cdot R_2}{R_S + R_1 + R_2}\right]\right)^2} \quad [\,V_{RMS}\,]$$

$$(7)\quad e_{R_1 + R_S \| R_2} = \sqrt{4 \cdot k_B \cdot T(K) \cdot \left[\frac{(R_S + R_1) \cdot R_2}{R_S + R_1 + R_2}\right]} \quad \left[\frac{V}{\sqrt{Hz}}\right] \quad \text{Thermal noise of } (R_1 + R_S) \text{ || } R_2$$

$$(8)\quad k_B = 1.38065 \cdot 10^{-23} \quad \left[\frac{J}{K}\right] \quad \text{Boltzmann Constant}$$

$$(9)\quad T(K) = 237.15 + T(°C) \quad [\,K\,] \quad \text{Temperature in kelvins}$$

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Where e_n is the voltage noise spectral density of the amplifier. For the OPAx186 operational amplifier, e_n = 38 nV/$\sqrt{\text{Hz}}$ at 1 kHz.
NOTE: For additional resources on noise calculations, visit *TI Precision Labs*.

Figure 8-1. Noise Calculation in Gain Configurations

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8.2 Typical Applications

8.2.1 High-Side Current Sensing

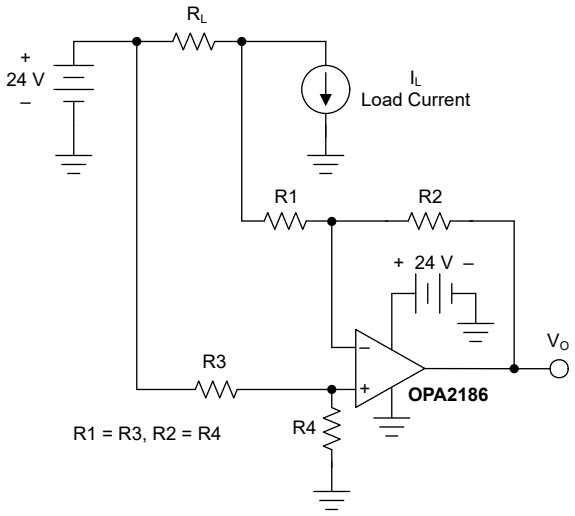


Figure 8-2. High-Side Current Monitor

8.2.1.1 Design Requirements

A common systems requirement is to monitor the current being delivered to a load. Monitoring makes sure that normal current levels are being maintained, and also provides an alert if an overcurrent condition occurs.

Fortunately, a relatively simple current monitor design can be achieved using a precision rail-to-rail input/output op amp such as the OPAx186. This device has an input common-mode voltage (V_{CM}) range that extends 200 mV beyond each power supply rail allowing for operation at the supply rail.

The OPAx186 is configured as a difference amplifier with a predetermined gain. The difference amplifier inputs are connected across a sense resistor through which the load current flows. The sense resistor can be connected to the high side or low side of the circuit through which the load current flows. Commonly, high-side current sensing is applied. Figure 8-2 shows an applicable OPAx186 configuration. Low-side current sensing can be applied as well if the sense resistor can be placed between the load and ground.

Use the following parameters for this design example:

- Single supply: 24 V
- Linear output voltage range: 0.3 V to 3.3 V
- Load current, I_L: 1 A to 11 A

The following design details and equations can be used to reconfigure this design for different output voltage ranges and current loads.

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8.2.1.2 Detailed Design Procedure

Designing a high-side current monitor circuit is straightforward, provided that the amplifier electrical characteristics are carefully considered so that linear operation is maintained. Other additional characteristics, such as the input voltage range of the analog to digital converter (ADC) that follows the current monitor stage, must also be considered when configuring the system.

For example, consider the design of a OPAx186 high-side current monitor with an output voltage range set to be compatible with the input of an ADC with an input range of 3.3 V, such as one integrated in a microcontroller. The full-scale input range of this converter is 0 V to 3.3 V. Although the OPAx186 is specified as a rail-to-rail input/output (RRIO) amplifier, the linear output operating range (like all amplifiers) does not quite extend all the way to the supply rails. This linear operating range must be considered.

In this design example, the OPAx186 is powered by 24 V; therefore, the device is easily capable of providing the 3.3-V positive level; or even more, if the ADC has a wider input range. However, because the OPAx186 output does not swing completely to 0 V, the specified lower swing limit must be observed in the design.

The best measure of an op-amp linear output voltage range comes from the open-loop voltage gain (A_{OL}) specification listed in the *Electrical Characteristics* table. The A_{OL} test conditions specify a linear swing range 300 mV from each supply rail (R_L = 10 kΩ). Therefore, the linear swing limit on the low end (V_{oMIN}) is 300 mV, and 3.3 V is the V_{oMAX} limit, thus yielding an 11:1 V_{oMAX} to V_{oMIN} ratio. This ratio proves important in determining the difference amplifier operating parameters.

A nominal load current (I_L) of 10 A is used in this example. In most applications, however, the ability to monitor current levels far less than 10 A is useful. This situation is where the 11:1 V_{oMAX} to V_{oMIN} ratio is crucial. If 11 A is set as the maximum current, this current must correspond to a 3.3-V output. Using the 11:1 ratio, the minimum current of 1 A corresponds to 300 mV.

Selection of current sense resistor R_S comes down to how much voltage drop can be tolerated at maximum current and the permissible power loss or dissipation. A good compromise for a 10-A sense application is an R_S of 10 mΩ. That value results in a power dissipation of 1 W, and a 0.1-V drop at 10 A.

Next, determine the gain of the OPAx186 difference amplifier circuit. The maximum current of 11 A flowing through a 10-mΩ sense resistor results in 110 mV across the resistor. That voltage appears as a differential voltage, V_R, that is applied across the OPAx186 difference amplifier circuit inputs:

$$V_S = I_L * R_S$$
$$V_S = 11\,A * 10\,m\Omega = 110\,mV \quad (1)$$

The OPAx186 required voltage gain is determined from:

$$G_A = \frac{V_{OMAX}}{V_S}$$
$$G_A = \frac{3.3\,V}{0.11\,V} = 30\frac{V}{V} \quad (2)$$

Now, checking the V_{oMIN} using I_L = 1 A:

$$V_{OMIN} = G_A * I_{SMIN} * R_S$$
$$V_{OMIN} = 30\frac{V}{V} * 1\,A * 10\,m\Omega = 300\,mV \quad (3)$$

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Figure 8-3 shows the complete OPAx186 high-side current monitor. The circuit is capable of monitoring a current range of < 1 A to 11 A, with a V_{CM} very close to the 24-V supply voltage.

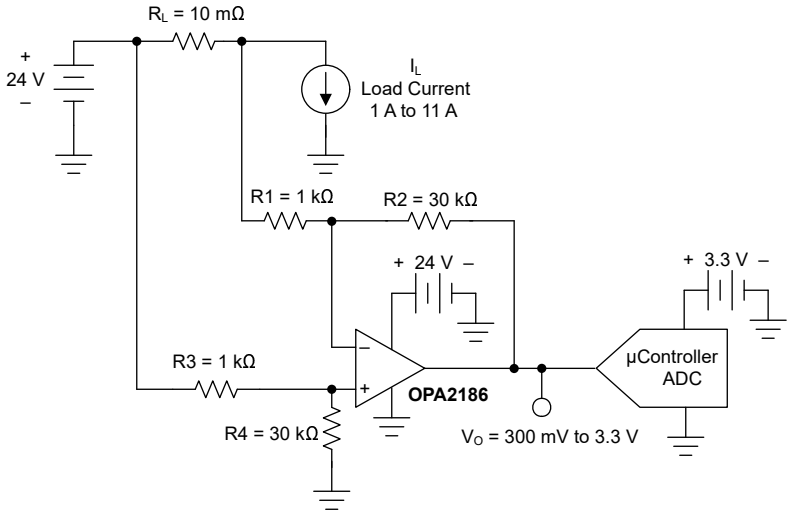


Figure 8-3. OPAx186 Configured as a High-Side Current Monitor

In this example, the OPAx186 output voltage is intentionally limited to 3.3 V. However, because of the 24-V supply, the output voltage can be much higher to allow for a higher-voltage data converter with a higher dynamic range.

The circuit in Figure 8-3 was checked using the TINA Spice circuit simulation tool to verify the correct operation of the OPAx186 high-side current monitor. The simulation results are seen in Figure 8-4. The performance is exactly as expected. Upon careful inspection of the plots, one possible surprise is that V_O continues towards zero as the sense current drops below 1 A, where V_O is 300 mV and less.

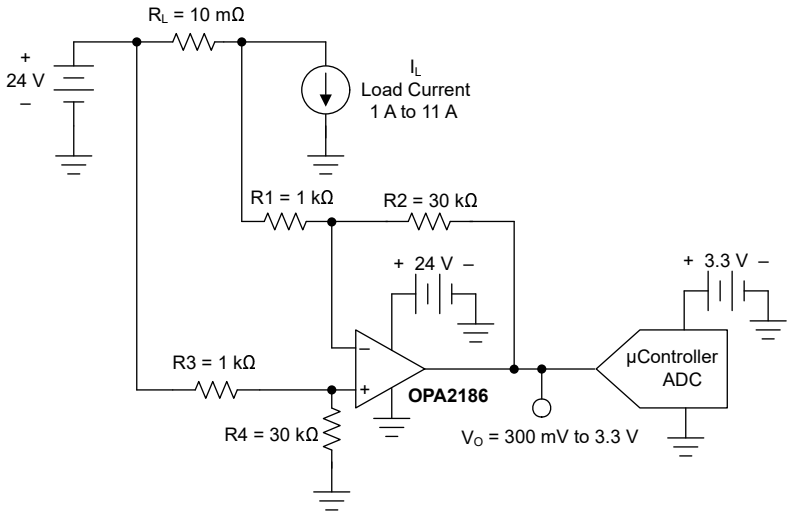


Figure 8-4. OPAx186 High-Side Current-Monitor Simulation Schematic

The OPAx186 output, as well as other CMOS output amplifiers, often swing closer to 0 V than the linear output parameters suggest. The voltage output swing, V_O (see the *Electrical Characteristics* table), is not an indication of the linear output range, but rather how close the output can move towards the supply rail. In that region, the amplifier output approaches saturation, and the amplifier ceases to operate linearly. Thus, in the current-monitor application, the current-measurement capability can continue to much less than the 300-mV output level. However, keep in mind that the linearity errors are becoming large.

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Lastly, some notes about maximizing the high-side current monitor performance:

- All resistor values are critical for accurate gain results. Match resistor pairs of [R1 and R3] and [R2 and R4] as closely as possible to minimize common-mode mismatch error. Use a 0.1% tolerance, or better. Often, selecting two adjacent resistors on a reel provides close matching compared to random selection.
- Keep the closed-loop gain, G_A, of the OPAx186 difference amplifier set to a reasonable value to reduce gain error and maximize bandwidth. A G_A of 30 V/V is used in the example.
- Although current monitoring is often used for monitoring dc supply currents, ac current can also be monitored. The –3-dB bandwidth, or upper cutoff frequency, of the circuit is:

$$f_H = \frac{GBW}{\text{Noise Gain}} \tag{4}$$

where

- GBW = the amplifier unity gain bandwidth; 750 kHz for the OPAx186.
- Noise Gain = the gain as seen going into the op-amp noninverting input, and is defined by:

$$G_{NG} = 1 + \frac{R2}{R1} \tag{5}$$

For the OPAx186 circuit in Figure 8-3, the results are:

$$G_{NG} = 1 + \frac{30\ k\Omega}{1\ k\Omega} = 31\frac{V}{V}$$
$$f_H = \frac{750\ kHz}{31} = 24.2\ kHz \tag{6}$$

Make sure that the amplifier slew rate is sufficient to support the expected output voltage swing range and waveform. Also, if a single power supply (such as 24 V) is used, the ac power source applied to the sense input must have a positive dc component to keep the V_{CM} greater than 0 V. To maintain normal operation, the input voltage cannot drop to less than 0 V.

The OPAx186 output can attain a 0-V output level if a small negative voltage is used to power the V– pin instead of ground. The LM7705 is a switched capacitor voltage inverter with a regulated, low-noise, –0.23-V fixed voltage output. Powering the OPAx186 V– pin at this level approximately matches the 300-mV linear output voltage swing lower limit, thus extending the output swing to 0 V, or very near 0 V. This configuration greatly improves the resolution at low sense current levels.

The LM7705 requires only about 78 µA of quiescent current, but be aware that the specified supply range is 3 V to 5.25 V. The 3.3-V or 5-V supply used by the ADC can be used as a power source.

For more information about amplifier-based, high-side current monitors, see the *TI Analog Engineer's Circuit Cookbook: Amplifiers*.

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8.2.1.3 Application Curve

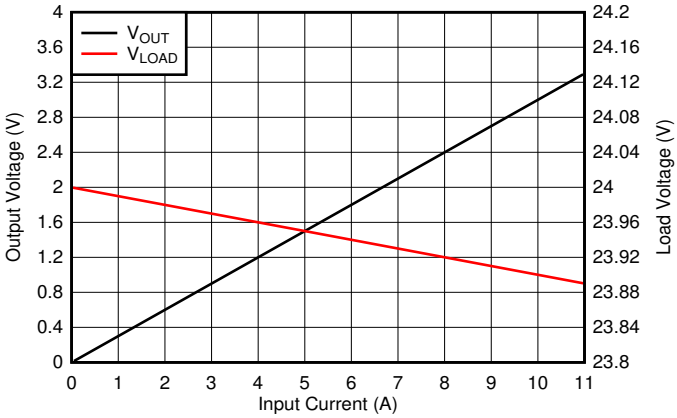
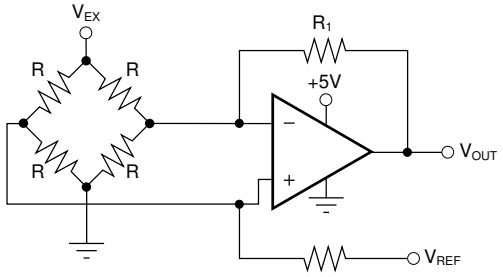


Figure 8-5. High-Side Results

8.2.2 Bridge Amplifier

Figure 8-6 shows the basic configuration for a bridge amplifier. Click the following link to download the TINA-TI file: *Bridge Amplifier Circuit*.



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Figure 8-6. Bridge Amplifier

8.3 Power Supply Recommendations

The OPAx186 is specified for operation from 4.5 V to 24 V (±2.25 V to ±12 V); many specifications apply from –40°C to +125°C.

CAUTION

Supply voltages larger than 40 V can permanently damage the device (see the *Absolute Maximum Ratings* table).

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see *Section 8.4*.

8.4 Layout

8.4.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices:

- For the lowest offset voltage, avoid temperature gradients that create thermoelectric (Seebeck) effects in the thermocouple junctions formed from connecting dissimilar conductors. Also:
  - Use low thermoelectric-coefficient conditions (avoid dissimilar metals).
  - Thermally isolate components from power supplies or other heat sources.
  - Shield operational amplifier and input circuitry from air currents, such as cooling fans.
- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the op amp itself. Bypass capacitors reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close as possible to the device. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information, see the *The PCB is a component of op amp design* analog application journal.
- To reduce parasitic coupling, run the input traces as far away as possible from the supply or output traces. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close as possible to the device. As Figure 8-7 shows, keep the feedback resistor (R3) and gain resistor (R4) close to the inverting input to minimize parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- For best performance, clean the PCB following board assembly.
- Any precision integrated circuit can experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, bake the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

8.4.2 Layout Example

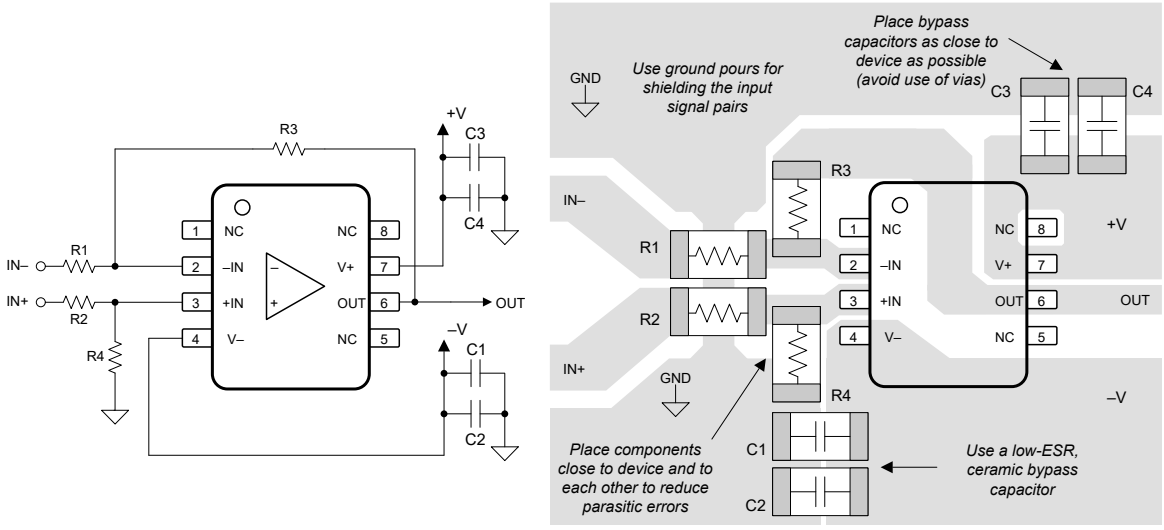


Figure 8-7. Operational Amplifier Board Layout for Difference Amplifier Configuration

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9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

9.1.1.1 PSpice® for TI

PSpice® for TI is a design and simulation environment that helps evaluate performance of analog circuits. Create subsystem designs and prototype solutions before committing to layout and fabrication, reducing development cost and time to market.

9.1.1.2 TINA-TI™ Simulation Software (Free Download)

TINA-TI™ simulation software is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI simulation software is a free, fully-functional version of the TINA™ software, preloaded with a library of macromodels, in addition to a range of both passive and active models. TINA-TI simulation software provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Design tools and simulation web page, TINA-TI simulation software offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software or TINA-TI software be installed. Download the free TINA-TI simulation software from the TINA-TI™ software folder.

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Zero-drift Amplifiers: Features and Benefits* application brief
- Texas Instruments, *The PCB is a component of op amp design* application note
- Texas Instruments, *Operational amplifier gain stability, Part 3: AC gain-error analysis*
- Texas Instruments, *Operational amplifier gain stability, Part 2: DC gain-error analysis*
- Texas Instruments, *Using infinite-gain, MFB filter topology in fully differential active filters* application note
- Texas Instruments, *Op Amp Performance Analysis*
- Texas Instruments, *Single-Supply Operation of Operational Amplifiers* application note
- Texas Instruments, *Shelf-Life Evaluation of Lead-Free Component Finishes* application note
- Texas Instruments, *Feedback Plots Define Op Amp AC Performance* application note
- Texas Instruments, *EMI Rejection Ratio of Operational Amplifiers* application note
- Texas Instruments, *Analog Linearization of Resistance Temperature Detectors* application note
- Texas Instruments, *TI Precision Design TIPD102 High-Side Voltage-to-Current (V-I) Converter*

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA186DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	31CQ
OPA186DBVR.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	31CQ
OPA186DBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	31CQ
OPA186DBVT.B	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	31CQ
OPA186DR	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O186
OPA186DR.B	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O186
OPA2186DDFR	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2MZ3
OPA2186DDFR.B	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2MZ3
OPA2186DR	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2186
OPA2186DR.B	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2186
OPA4186DR	Active	Production	SOIC (D) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4186
OPA4186DR.B	Active	Production	SOIC (D) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4186

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

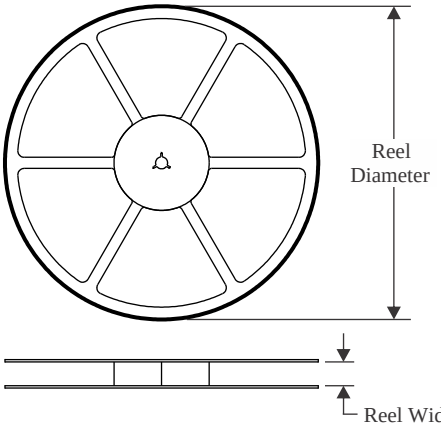
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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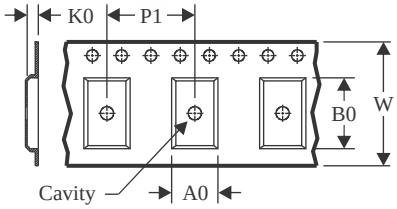
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

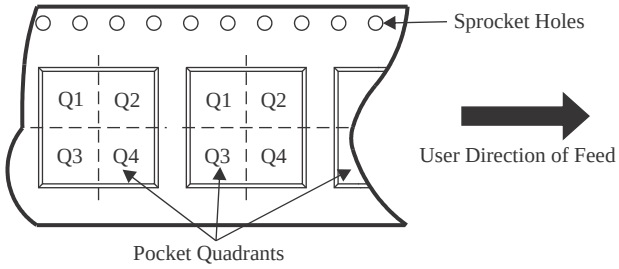


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

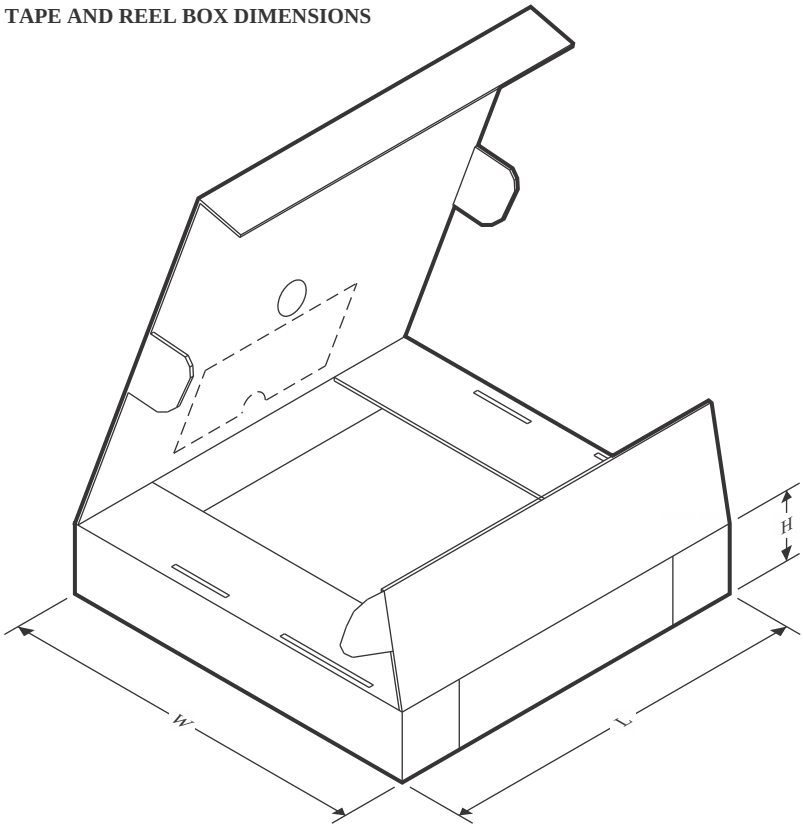
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

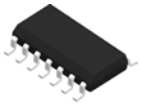
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA186DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA186DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA186DR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2186DDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA2186DR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4186DR	SOIC	D	14	3000	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA186DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
OPA186DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
OPA186DR	SOIC	D	8	3000	353.0	353.0	32.0
OPA2186DDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
OPA2186DR	SOIC	D	8	3000	353.0	353.0	32.0
OPA4186DR	SOIC	D	14	3000	353.0	353.0	32.0

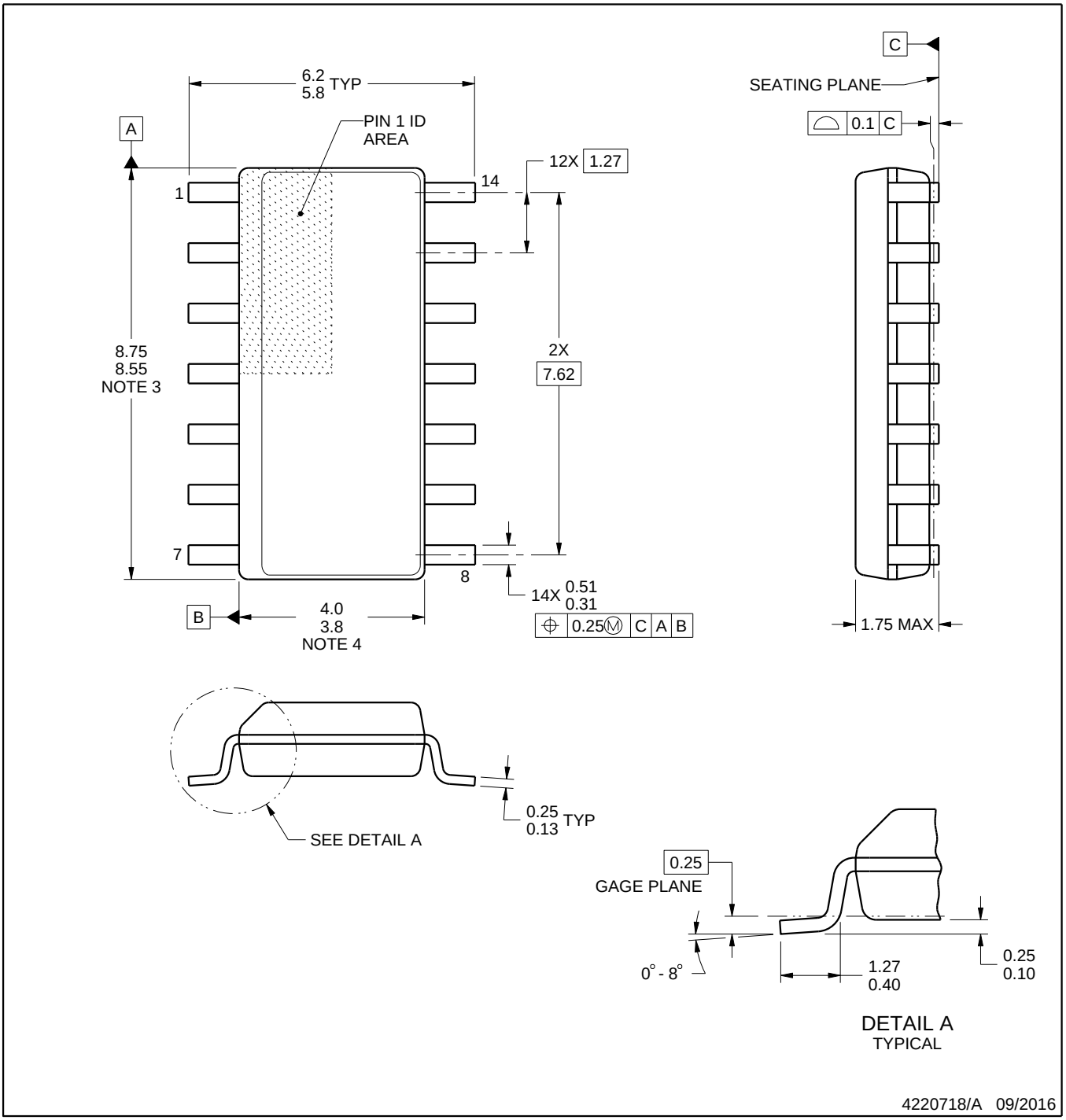


PACKAGE OUTLINE

D0014A

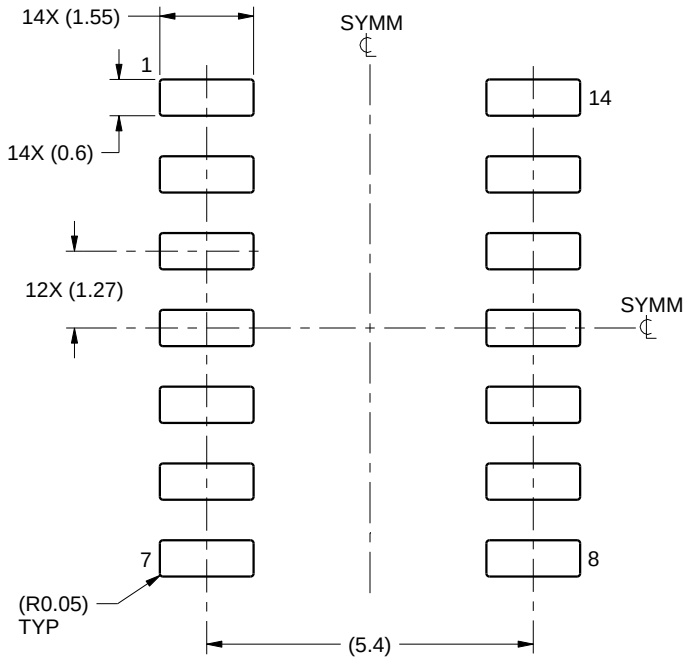
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

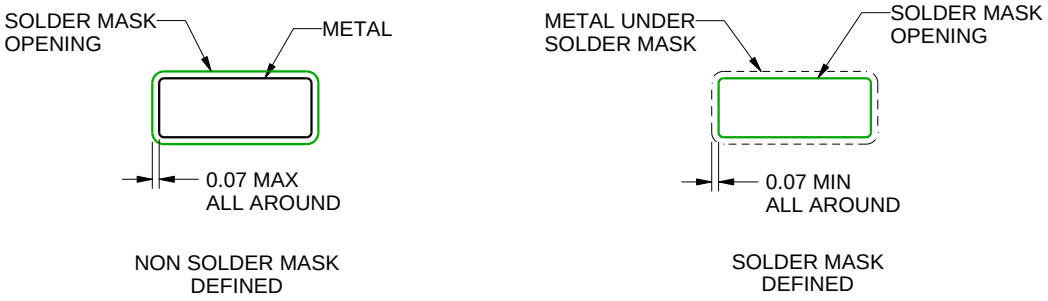


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

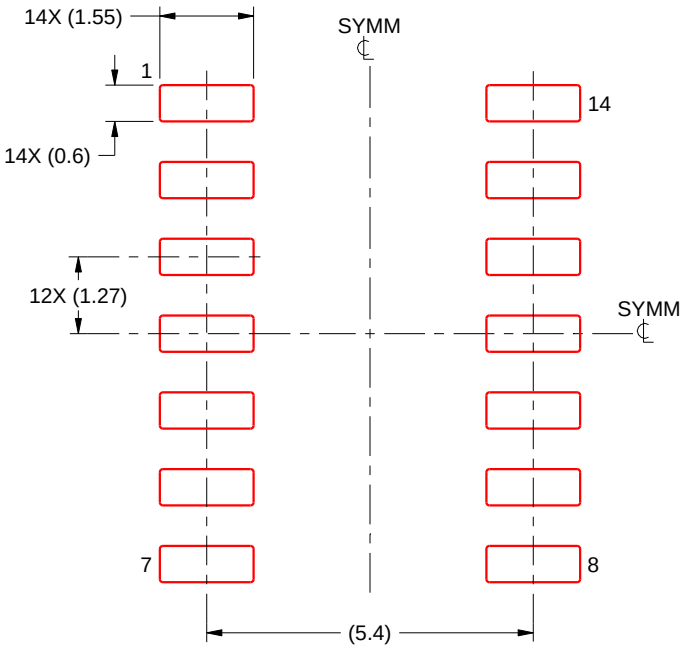
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

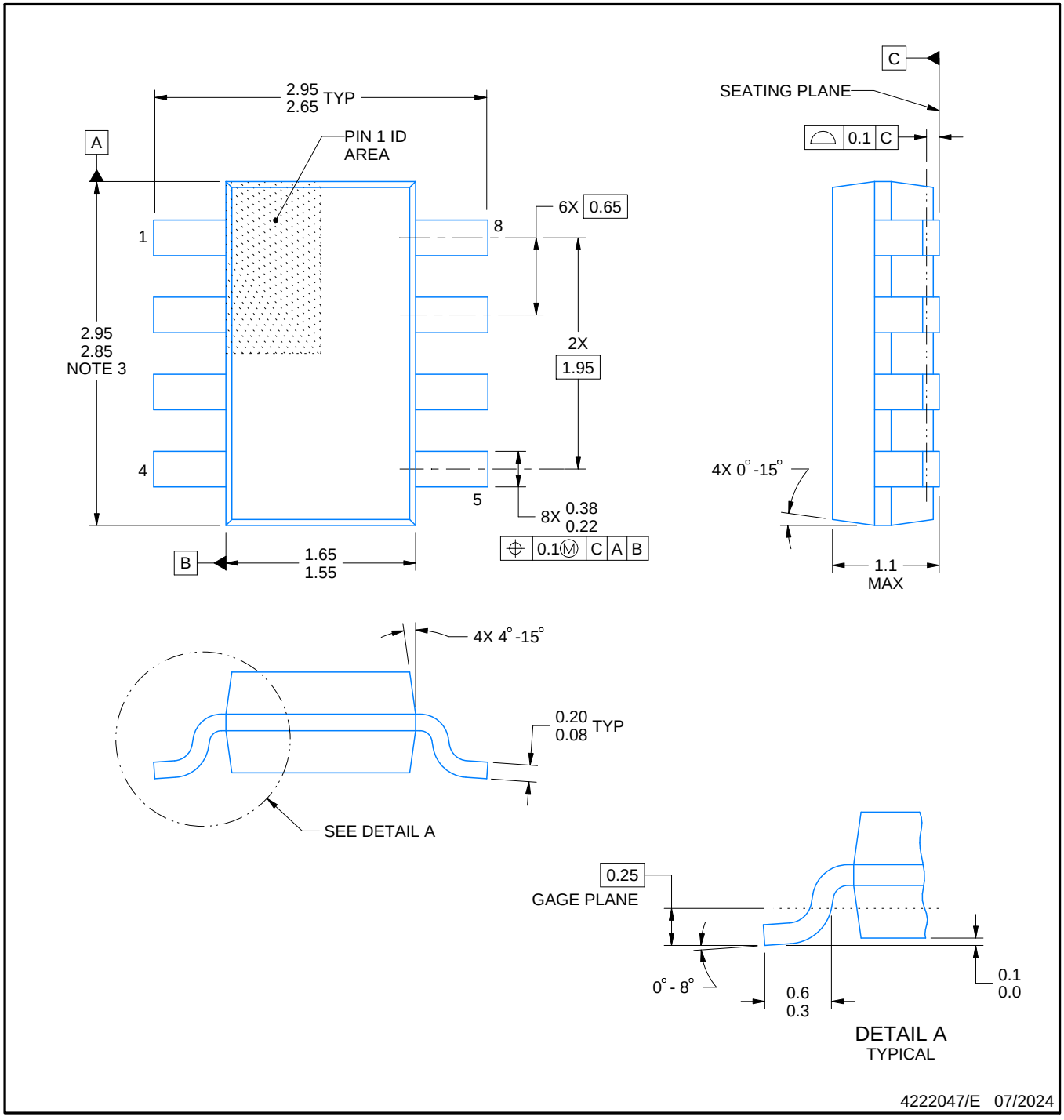
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DDF0008A

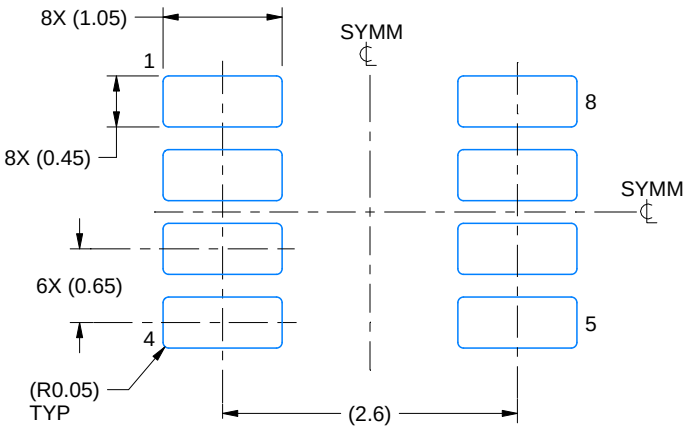
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

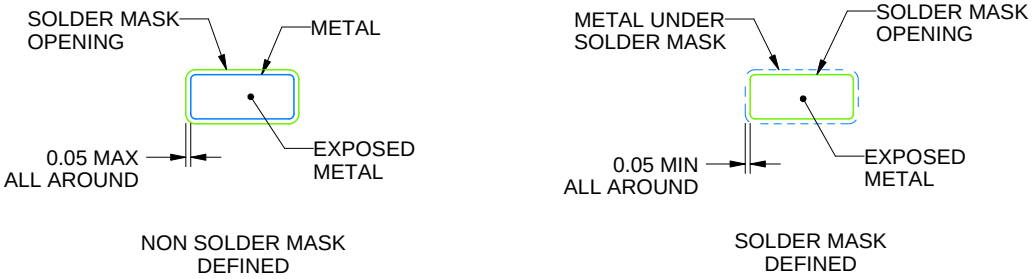


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4222047/E 07/2024

NOTES: (continued)

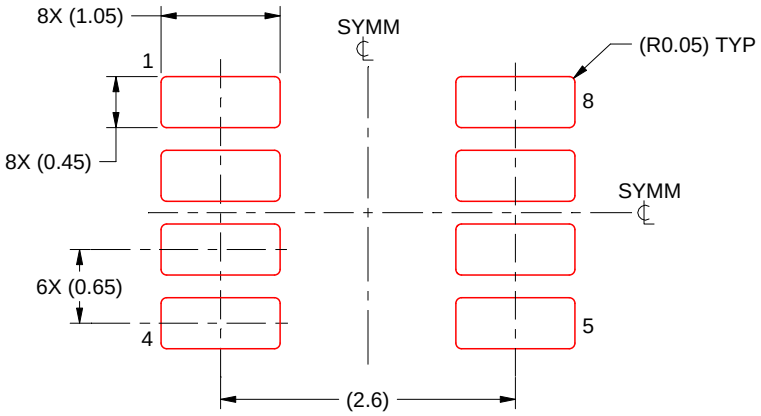
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

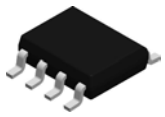


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/E 07/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

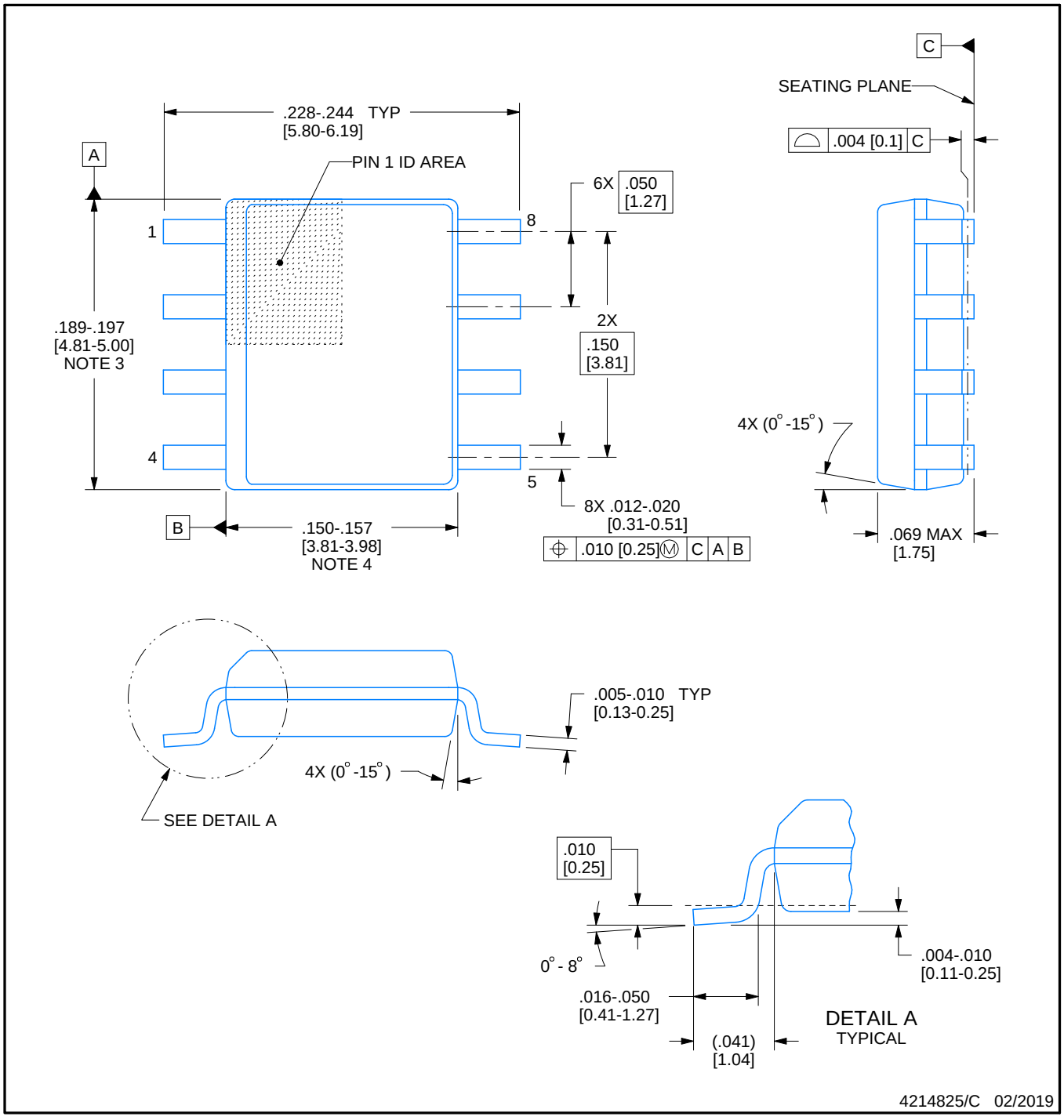


PACKAGE OUTLINE

D0008A

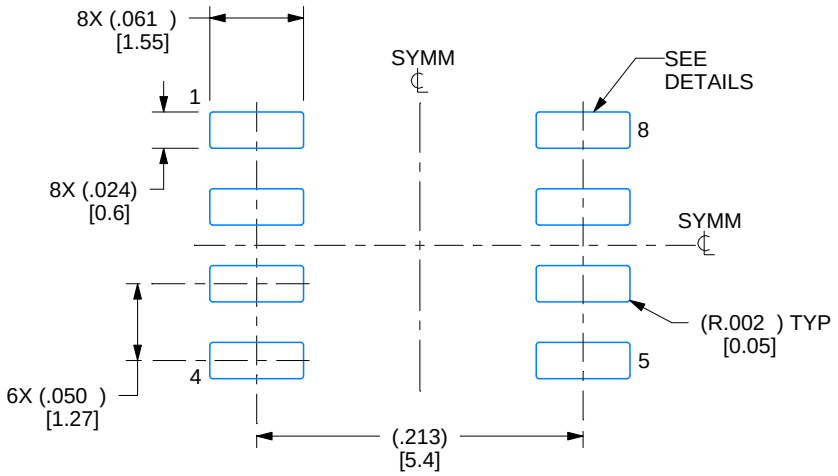
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

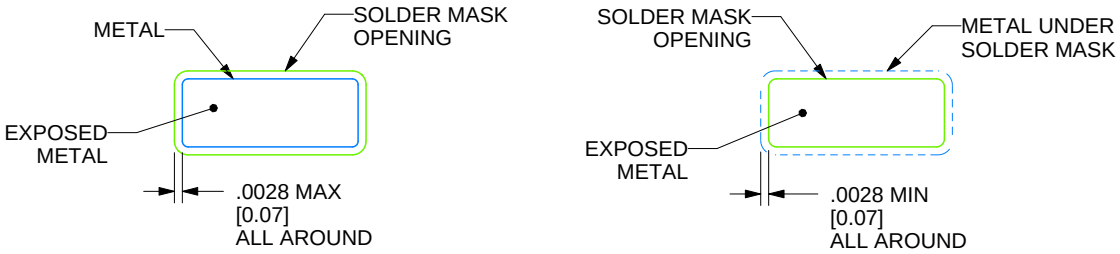


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

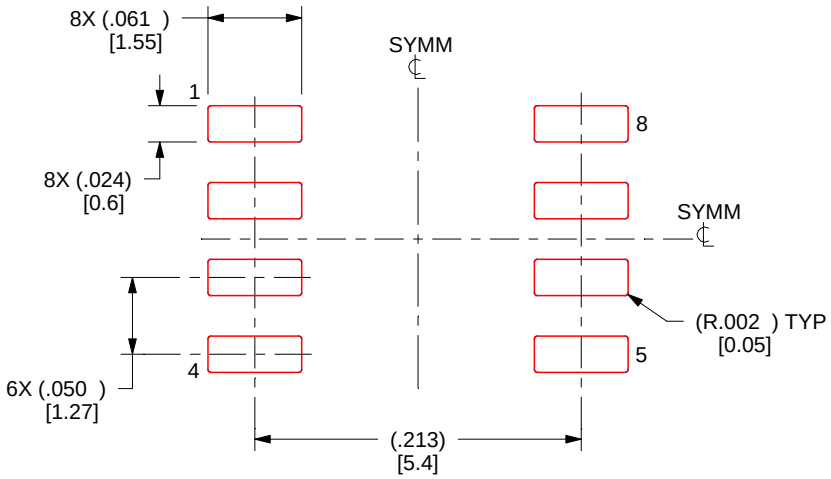
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

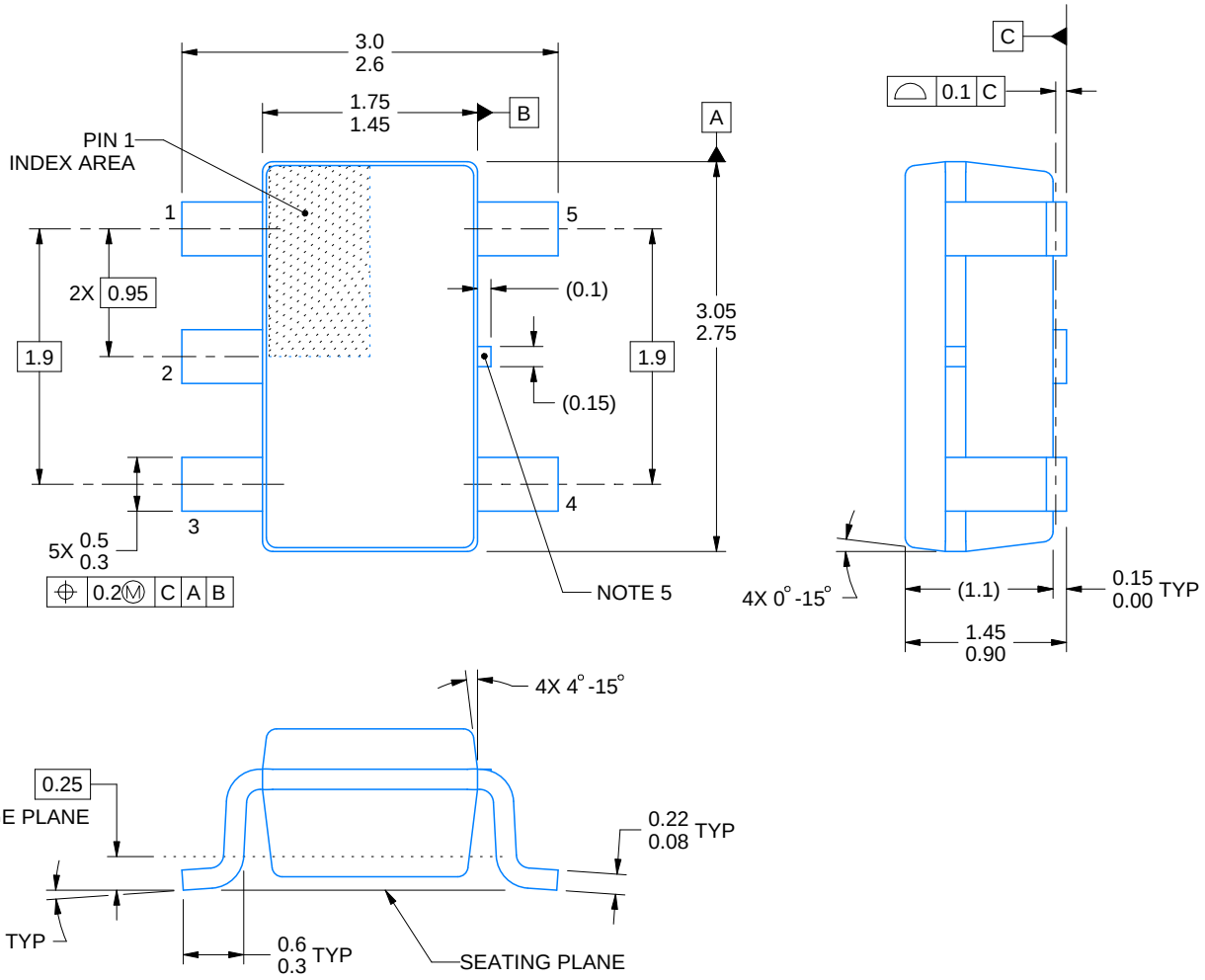
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

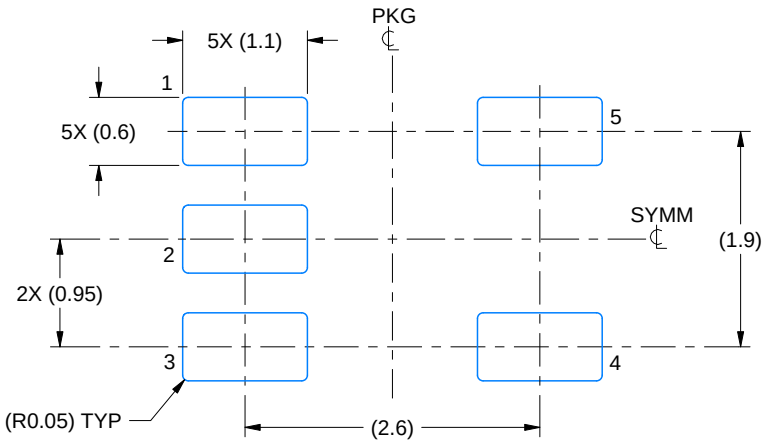
SMALL OUTLINE TRANSISTOR



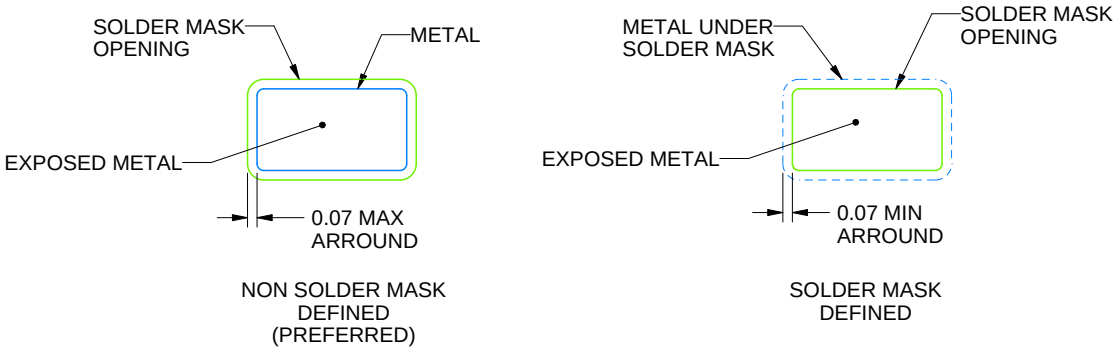
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

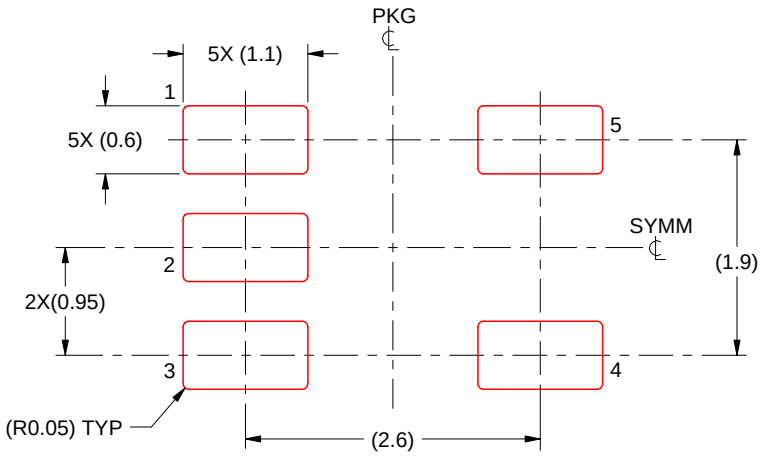


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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