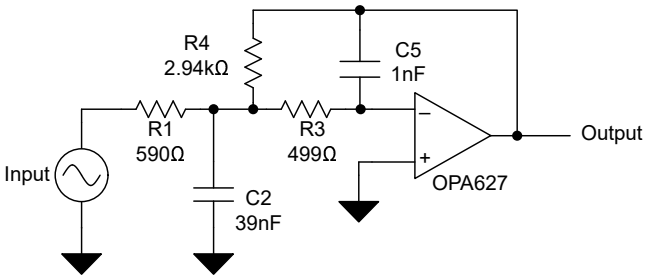
OPA6x7 Precision, High-Speed JFET Operational Amplifiers

1 Features

- Very low noise: 4.5nV/√Hz at 10kHz
- Fast settling time:
  - OPA627: 550ns to 0.01%
  - OPA637: 450ns to 0.01%
- Low V_{OS}: 100µV maximum
- Low drift: 0.8µV/°C maximum
- Low I_B: 5pA maximum
- Gain options:
  - OPA627: Unity-gain stable
  - OPA637: Stable in gain ≥ 5

2 Applications

- Precision instrumentation
- Fast data acquisition
- DAC output amplifier
- Optoelectronics
- Sonar, ultrasound
- High-impedance sensor amps
- High-performance audio circuitry
- Active filters



OPA627 Low-Pass Filter

3 Description

The OPA627 and OPA637 (OPA6x7) operational amplifiers (op amps) provide a new level of performance in a precision FET operational amplifier. When compared to the popular OPA111 op amp, the OPA6x7 have lower noise, lower offset voltage, and higher speed. The OPA6x7 are useful in a broad range of precision and high-speed analog circuitry.

The OPA6x7 is fabricated on a high-speed, dielectrically-isolated, complementary NPN/PNP process. The OPA6x7 operate over a wide power-supply voltage range of ±4.5V to ±18V. Laser-trimmed input circuitry provides high accuracy and low-noise performance comparable with the best bipolar-input op amps.

High-frequency complementary transistors allow increased circuit bandwidth, attaining dynamic performance not possible with previous precision FET op amps. The OPA627 is unity-gain stable. The OPA637 is stable in gains ≥ 5.

State-of-the-art, precision FET transistors achieve extremely low input bias currents without compromising input voltage noise performance. Low input bias current is maintained over a wide input common-mode voltage range with unique cascode circuitry.

The OPA6x7 are available in SOIC-8 and TO-99 packages. Industrial temperature range models are available.

Device Information

PART NUMBER	GAIN STABLE	PACKAGE(1)
OPA627	Unity-gain stable	D (SOIC, 8)
		LMC (TO-99, 8)
OPA637	Stable in gain ≥ 5	D (SOIC, 8)
		LMC (TO-99, 8)

(1) For more information, see Section 10.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

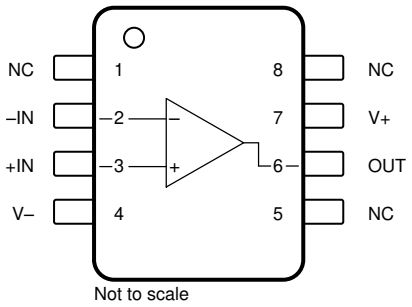


Figure 4-1. D Package, 8-Pin SOIC (Top View)

Table 4-1. Pin Functions: D (SOIC) Package

PIN		TYPE	DESCRIPTION
NO.	NAME		
1, 5, 8	NC	—	No internal connection (can be left floating)
2	–IN	Input	Inverting input
3	+IN	Input	Noninverting input
4	V–	Power	Negative (lowest) power supply
6	OUT	Output	Output
7	V+	Power	Positive (highest) power supply

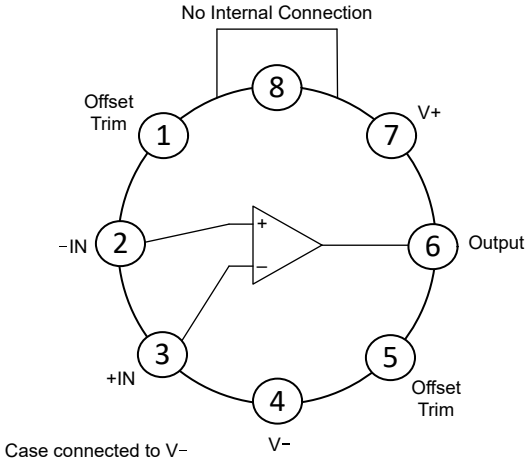


Figure 4-2. LMC Package, 8-Pin TO-99 (Top View)

Table 4-2. Pin Functions: LMC (TO-99) Package

PIN		TYPE	DESCRIPTION
NO.	NAME		
1, 5	Offset Trim	—	Input offset voltage trim (float this pin if unused)
2	–IN	Input	Inverting input
3	+IN	Input	Noninverting input
4	V–	Power	Negative (lowest) power supply
6	OUT	Output	Output
7	V+	Power	Positive (highest) power supply
8	NC	—	No internal connection (float this pin)

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)	Single supply		36	V
		Dual supply		±18	
	Input voltage	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential		(V+) – (V–)	
	Input pin current			±10	mA
	Power dissipation			1000	mW
T_A	Operating temperature	AU, BU	–40	125	°C
		AM, BM, SM	–55	125	
T_J	Junction temperature	AU, BU		150	°C
		AM, BM, SM		175	
T_{stg}	Storage temperature	AU, BU	–40	125	°C
		AM, BM, SM	–65	150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the Recommended Operating Conditions but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
OPA627AM, OPA627BM, OPA637				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	
OPA627AU, OPA627BU				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)	Single supply	9	30	36	V
		Dual supply	±4.5	±15	±18	
T_S	Specified temperature	AM, AU, BM, BU	–25	25	85	°C
		SM	–55	25	125	

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5.4 Thermal Information: OPA627

THERMAL METRIC[1]		OPA627		UNIT
		D (SOIC)	LMC (TO-99)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	121.5	200	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	64.3	N/A	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	65.0	N/A	°C/W
ψ_{JT}	Junction-to-top characterization parameter	18.0	N/A	°C/W
ψ_{JB}	Junction-to-board characterization parameter	64.3	N/A	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Thermal Information: OPA637

THERMAL METRIC[1]		OPA637		UNIT
		D (SOIC)	LMC (TO-99)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	107.9	200	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	57.3	N/A	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.7	N/A	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.7	N/A	°C/W
ψ_{JB}	Junction-to-board characterization parameter	48.9	N/A	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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5.6 Electrical Characteristics: OPA627BU, OPA627AU

at T_A = 25°C, V_S = ±15V, V_{CM} = V_{OUT} = midsupply, and R_L = 10kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage[1]	OPA627BU			±25	±125	µV
		OPA627AU			±280	±500	
dV_{OS}/dT	Input offset voltage drift[1]	T_A = –25°C to +85°C	OPA627BU		±0.3	±1.3	µV/°C
			OPA627AU		±2.5		
PSRR	Power supply rejection ratio[1]	V_S = ±4.5V to ±18V	OPA627BU	105	117		dB
			OPA627AU	100	116		
INPUT BIAS CURRENT							
I_B	Input bias current[2]	OPA627BU			±0.2	±5	pA
		OPA627AU			±2	±10	
		T_A = –25°C to +85°C	OPA627BU			±0.4	nA
			OPA627AU			±2	
		–10V < V_{CM} < +10V	OPA627BU		±1		pA
			OPA627AU		±2		
I_{OS}	Input offset current[2]	OPA627BU			±0.2	±5	pA
		OPA627AU			±1	±10	
		T_A = –25°C to +85°C	OPA627BU			±0.5	nA
			OPA627AU			±2	
NOISE							
	Input voltage noise	f = 0.1Hz to 10Hz			0.34		μV_{PP}
e_n	Input voltage noise density	f = 10Hz			7.5		$nV/\sqrt{Hz}$
		f = 100Hz			4.8		
		f = 1kHz			4		
		f = 10kHz			4		
i_n	Input current noise density	f = 100Hz			2.5		$fA/\sqrt{Hz}$
	Input current noise	f = 0.1Hz to 10Hz			48		fA_{PP}
INPUT VOLTAGE							
V_{CM}	Common-mode voltage			±11	±11.5		V
		T_A = –25°C to +85°C		±10.5	±11		
CMRR	Common-mode rejection ratio	–10.5V ≤ V_{CM} ≤ +10.5V	OPA627BU	103	110		dB
			OPA627AU	100	110		
INPUT IMPEDANCE							
Z_{ID}	Differential				10 || 8		TΩ || pF
Z_{ICM}	Common-mode				10 || 9		TΩ || pF

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5.6 Electrical Characteristics: OPA627BU, OPA627AU (continued)

at T_A = 25°C, V_S = ±15V, V_{CM} = V_{OUT} = midsupply, and R_L = 10kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	–10V < V_O < +10V, R_L = 1kΩ	OPA627BU	120	130		dB
			OPA627AU	106	116		
		–10V < V_O < +10V, R_L = 1kΩ, T_A = –25°C to +85°C	OPA627BU	117			
			OPA627AU	100	110		
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product	Gain = 1V/V, C_L = 30pF			45		MHz
SR	Slew rate	10V step, gain = –1V/V			150		V/µs
t_S	Settling time	10V step, gain = –1V/V, C_L = 30pF	To 0.01%		120		ns
			To 0.1%		110		
THD+N	Total harmonic distortion + noise	Gain = 1V/V, f = 1kHz, V_O = 3.5V_{RMS}			0.00003		%
OUTPUT							
V_O	Output voltage	R_L = 1kΩ		±11.5	±12.3		V
			T_A = –25°C to +85°C	±11	±11.5		
I_O	Current output	–10V < V_O < +10V			±30		mA
I_{SC}	Short-circuit current				±45		mA
R_O	Open-loop output impedance	f = 1MHz			13.5		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0mA			7	7.5	mA

(1) The offset voltage is measured when the device is fully warmed-up.
(2) High-speed test at T_J = 25°C. See *Typical Characteristics* for warmed-up performance.

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5.7 Electrical Characteristics: OPA627AM, OPA627BM, OPA627SM

at T_A = 25°C, V_S = ±15V, V_{CM} = V_{OUT} = midsupply, and R_L = 10kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage(1)	OPA627AM			±130	±250	µV
		OPA627BM, OPA627SM			±40	±100	
dV_{OS}/dT	Input offset voltage drift(1)	T_A = –25°C to +85°C	OPA627AM		±1.2	±2	µV/°C
			OPA627BM		±0.4	±0.8	
		T_A = –55°C to +125°C	OPA627SM		±0.4	±0.8	
PSRR	Power supply rejection ratio(1)	V_S = ±4.5V to ±18V	OPA627AM	100	116		dB
			OPA627BM, OPA627SM	106	120		
INPUT BIAS CURRENT							
I_B	Input bias current(2)	OPA627AM			±2	±10	pA
		OPA627BM, OPA627SM			±1	±5	
		T_A = –25°C to +85°C	OPA627AM			±2	nA
			OPA627BM			±1	
		T_A = –55°C to +125°C	OPA627SM			±50	
		–10V ≤ V_{CM} ≤ +10V	OPA627AM		±2		pA
			OPA627BM, OPA627SM		±1		
I_{OS}	Input offset current(2)	OPA627AM			±1	±10	pA
		OPA627BM, OPA627SM			±0.5	±5	
		T_A = –25°C to +85°C	OPA627AM			±2	nA
			OPA627BM			±1	
		T_A = –55°C to +125°C	OPA627SM			±50	
NOISE							
	Input voltage noise	f = 0.1Hz to 10Hz	OPA627AM		0.8		$µV_{PP}$
			OPA627BM, OPA627SM		0.6	1.6	
e_n	Input voltage noise density	f = 10Hz	OPA627AM		20		nV/√Hz
			OPA627BM, OPA627SM		15	40	
		f = 100Hz	OPA627AM		10		
			OPA627BM, OPA627SM		8	20	
		f = 1kHz	OPA627AM		5.6		
			OPA627BM, OPA627SM		5.2	8	
		f = 10kHz	OPA627AM		4.8		
			OPA627BM, OPA627SM		4.5	6	
i_n	Input current noise density	f = 100Hz	OPA627AM		2.5		fA/√Hz
			OPA627BM, OPA627SM		1.6	2.5	
	Input current noise	f = 0.1Hz to 10Hz	OPA627AM		48		fA_{PP}
			OPA627BM, OPA627SM		30	60	

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5.7 Electrical Characteristics: OPA627AM, OPA627BM, OPA627SM (continued)

at T_A = 25°C, V_S = ±15V, V_{CM} = V_{OUT} = midsupply, and R_L = 10kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT VOLTAGE							
V_{CM}	Common-mode voltage			±11	±11.5		V
		T_A = –25°C to +85°C	OPA627AM, OPA627BM	±10.5	±11		
		T_A = –55°C to +125°C	OPA627SM	±10.5	±11		
CMRR	Common-mode rejection ratio	–10.5V ≤ V_{CM} ≤ +10.5V	OPA627AM	100	110		dB
			OPA627BM, OPA627SM	106	116		
INPUT IMPEDANCE							
Z_{ID}	Differential				10 || 8		TΩ || pF
Z_{ICM}	Common-mode				10 || 7		TΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	–10V < V_O < +10V, R_L = 1kΩ	OPA627AM	106	116		dB
			OPA627BM, OPA627SM	112	120		
		–10V < V_O < +10V, R_L = 1kΩ, T_A = –25°C to +85°C	OPA627AM	100	110		
			OPA627BM	106	117		
		–10V < V_O < +10V, R_L = 1kΩ, T_A = –55°C to +125°C	OPA627SM	100	114		
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product	Gain = 1V/V			16		MHz
SR	Slew rate	10V step, gain = –1V/V		40	55		V/µs
t_S	Settling time	10V step, gain = –1V/V	To 0.01%		550		ns
			To 0.1%		450		
THD+N	Total harmonic distortion + noise	Gain = 1V/V, f = 1kHz			0.00003		%
OUTPUT							
V_O	Output voltage	R_L = 1kΩ		±11.5	±12.3		V
		R_L = 1kΩ, T_A = –25°C to +85°C	OPA627AM, OPA627BM	±11	±11.5		
		R_L = 1kΩ, T_A = –55°C to +125°C	OPA627SM	±11	±11.5		
I_{SC}	Current output	–10V < V_O < +10V			±45		mA
I_{SC}	Short-circuit current			±35	±70/–55	±100	mA
R_O	Open-loop output impedance	f = 1MHz			55		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0mA			7	7.5	mA

(1) The offset voltage is measured when the device is fully warmed-up.
(2) High-speed test at T_J = 25°C. See *Typical Characteristics* for warmed-up performance.

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5.8 Electrical Characteristics: OPA637

at T_A = 25°C, V_S = ±15V, V_{CM} = V_{OUT} = midsupply, and R_L = 10kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage(1)	OPA637AU			±280	±500	µV
		OPA637AM			±130	±250	
		OPA637BM, OPA637SM			±40	±100	
dV_{OS}/dT	Input offset voltage drift(1)	T_A = –25°C to +85°C	OPA637AU		±2.5		µV/°C
			OPA637AM		±1.2	±2	
			OPA637BM		±0.4	±0.8	
		T_A = –55°C to +125°C	OPA637SM		±0.4	±0.8	
PSRR	Power supply rejection ratio(1)	V_S = ±4.5V to ±18V	OPA637AU, OPA637AM	100	116		dB
			OPA637BM, OPA637SM	106	120		
INPUT BIAS CURRENT							
I_B	Input bias current(2)	OPA637AU, OPA637AM			±2	±10	pA
		OPA637BM, OPA637SM			±1	±5	
		T_A = –25°C to +85°C	OPA637AU, OPA637AM			±2	nA
			OPA637BM			±1	
		T_A = –55°C to +125°C	OPA637SM			±50	
		–10V ≤ V_{CM} ≤ +10V	OPA637AU, OPA637AM		±2		pA
			OPA637BM, OPA637SM		±1		
I_{OS}	Input offset current(2)	OPA637AU, OPA637AM			±1	±10	pA
		OPA637BM, OPA637SM			±0.5	±5	
		T_A = –25°C to +85°C	OPA637AU, OPA637AM			±2	nA
			OPA637BM			±1	
		T_A = –55°C to +125°C	OPA637SM			±50	

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5.8 Electrical Characteristics: OPA637 (continued)

at T_A = 25°C, V_S = ±15V, V_{CM} = V_{OUT} = midsupply, and R_L = 10kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
NOISE							
	Input voltage noise	f = 0.1Hz to 10Hz	OPA637AU, OPA637AM		0.8		μV_{PP}
			OPA637BM, OPA637SM		0.6	1.6	
e_n	Input voltage noise density	f = 10Hz	OPA637AU, OPA637AM		20		nV/√Hz
			OPA637BM, OPA637SM		15	40	
		f = 100Hz	OPA637AU, OPA637AM		10		
			OPA637BM, OPA637SM		8	20	
		f = 1kHz	OPA637AU, OPA637AM		5.6		
			OPA637BM, OPA637SM		5.2	8	
		f = 10kHz	OPA637AU, OPA637AM		4.8		
			OPA637BM, OPA637SM		4.5	6	
i_n	Input current noise density	f = 100Hz	OPA637AU, OPA637AM		2.5		fA/√Hz
			OPA637BM, OPA637SM		1.6	2.5	
	Input current noise	f = 0.1Hz to 10Hz	OPA637AU, OPA637AM		48		fA_{PP}
			OPA637BM, OPA637SM		30	60	
INPUT VOLTAGE							
V_{CM}	Common-mode voltage			±11	±11.5		V
		T_A = –25°C to +85°C	OPA637AU, OPA637AM, OPA637BM	±10.5	±11		
		T_A = –55°C to +125°C	OPA637SM	±10.5	±11		
CMRR	Common-mode rejection ratio	–10.5V ≤ V_{CM} ≤ +10.5V	OPA637AU, OPA637AM	100	110		dB
			OPA637BM, OPA637SM	106	116		
INPUT IMPEDANCE							
Z_{ID}	Differential				10 || 8		TΩ || pF
Z_{ICM}	Common-mode				10 || 7		TΩ || pF

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5.8 Electrical Characteristics: OPA637 (continued)

at T_A = 25°C, V_S = ±15V, V_{CM} = V_{OUT} = midsupply, and R_L = 10kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	–10V < V_O < +10V R_L = 1kΩ	OPA637AU, OPA637AM	106	116		dB
			OPA637BM, OPA637SM	112	120		
		–10V < V_O < +10V R_L = 1kΩ, T_A = –25°C to +85°C	OPA637AU, OPA637AM	100	110		
			OPA637BM	106	117		
		–10V < V_O < +10V R_L = 1kΩ, T_A = –55°C to +125°C	OPA637SM	100	114		
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product	Gain = 10V/V			80		MHz
SR	Slew rate	10V step, gain = –4V/V		100	135		V/µs
t_S	Settling time	10V step, gain = –4V/V,	To 0.01%		450		ns
			To 0.1%		300		
OUTPUT							
V_O	Output voltage	R_L = 1kΩ		±11.5	±12.3		V
		R_L = 1kΩ, T_A = –25°C to +85°C	OPA637AU, OPA637AM, OPA637BM	±11	±11.5		
		R_L = 1kΩ, T_A = –55°C to +125°C	OPA637SM	±11	±11.5		
I_{SC}	Current output	–10V < V_O < +10V			±45		mA
I_{SC}	Short-circuit current			±35	±70/–55	±100	mA
R_O	Open-loop output impedance	f = 1MHz			55		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0mA			7	7.5	mA

(1) The offset voltage is measured when the device is fully warmed-up.
(2) High-speed test at T_J = 25°C. See *Typical Characteristics* for warmed-up performance.

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5.9 Typical Characteristics

at T_A = 25°C and V_S = ±15V (unless otherwise noted)

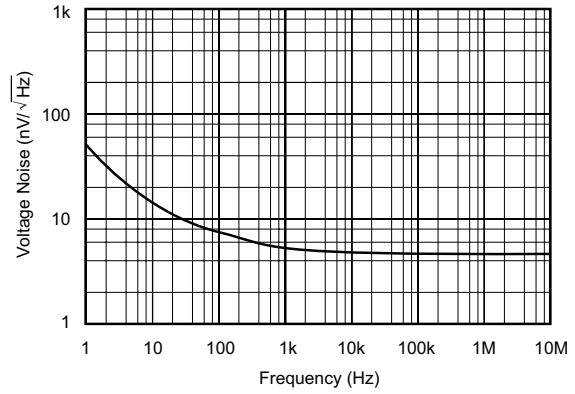


Figure 5-1. Input Voltage Noise Spectral Density vs Frequency

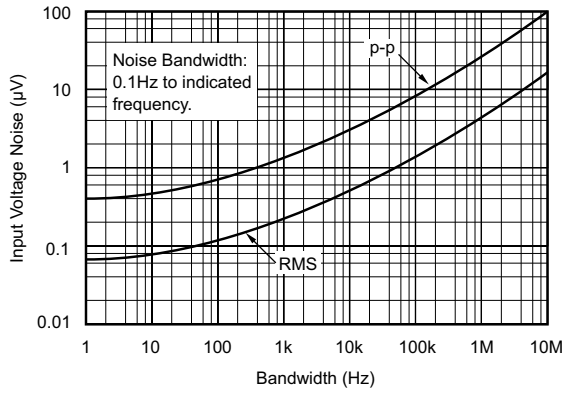


Figure 5-2. Total Input Voltage Noise vs Bandwidth

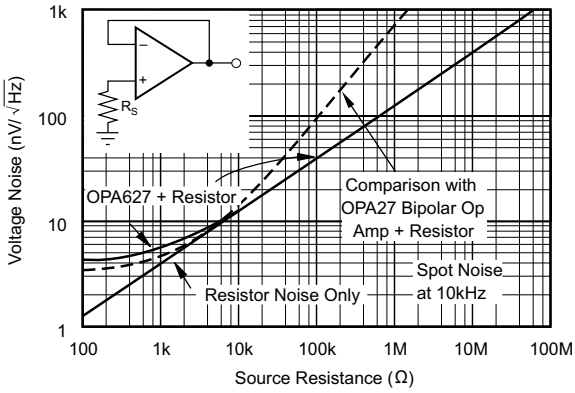


Figure 5-3. Voltage Noise vs Source Resistance

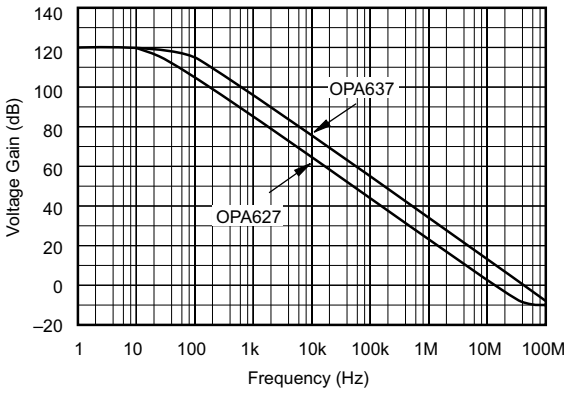


Figure 5-4. Open-Loop Gain vs Frequency

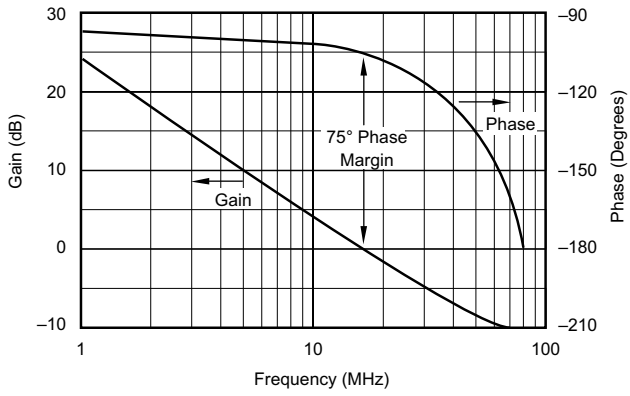


Figure 5-5. OPA627 Gain and Phase vs Frequency

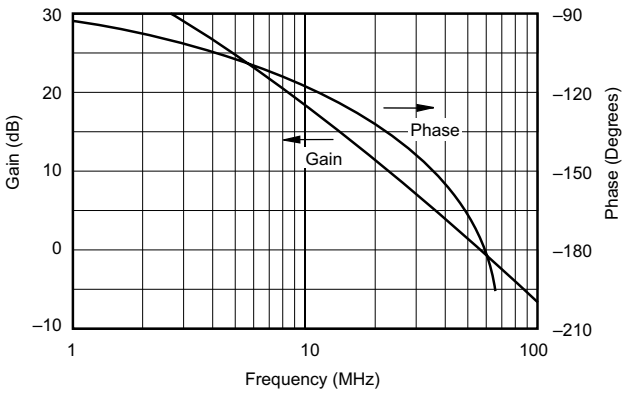


Figure 5-6. OPA637 Gain and Phase vs Frequency

5.9 Typical Characteristics (continued)

at T_A = 25°C and V_S = ±15V (unless otherwise noted)

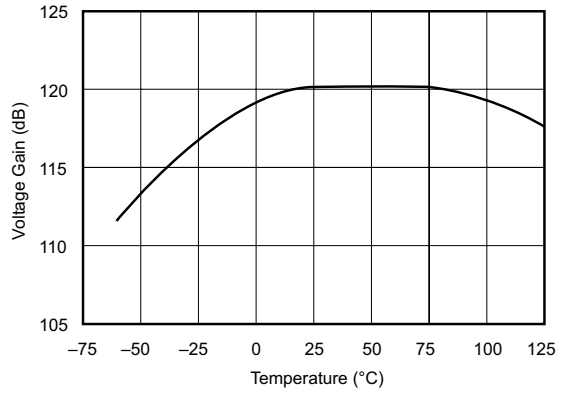


Figure 5-7. Open-Loop Gain vs Temperature

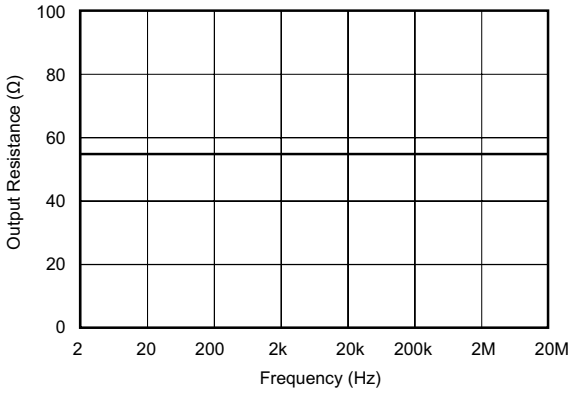


Figure 5-8. Open-Loop Output Impedance vs Frequency

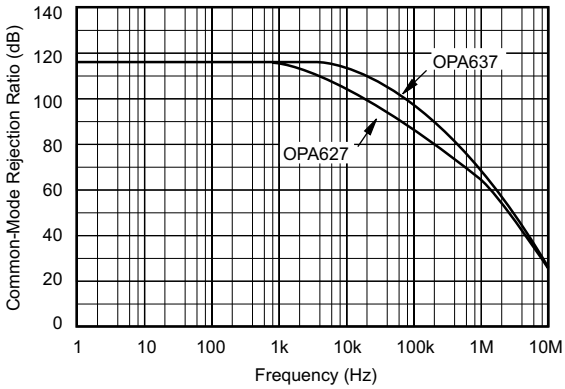


Figure 5-9. Common-Mode Rejection vs Frequency

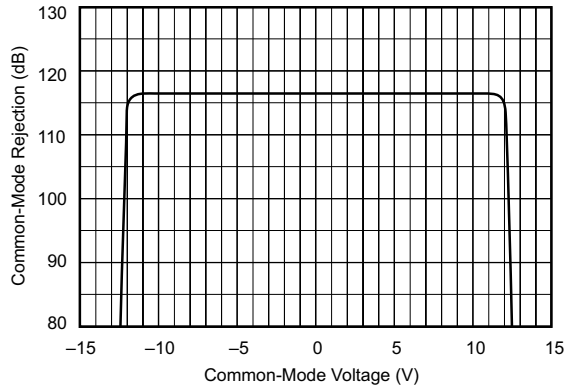


Figure 5-10. Common-Mode Rejection vs Input Common-Mode Voltage

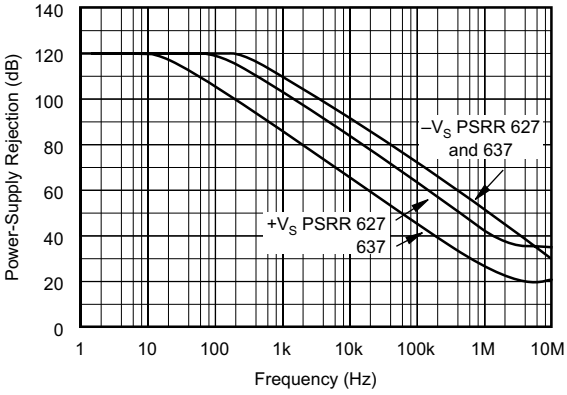


Figure 5-11. Power-Supply Rejection vs Frequency

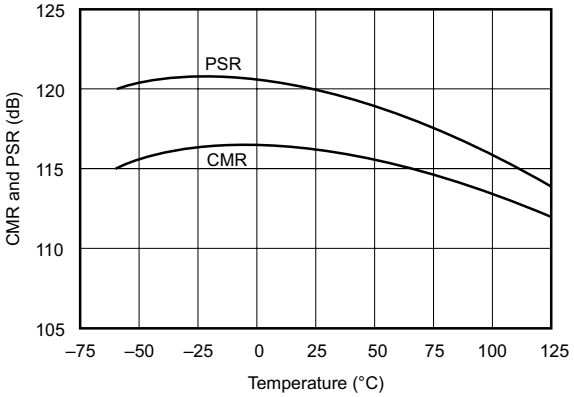


Figure 5-12. Power-Supply Rejection and Common-Mode Rejection vs Temperature

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5.9 Typical Characteristics (continued)

at T_A = 25°C and V_S = ±15V (unless otherwise noted)

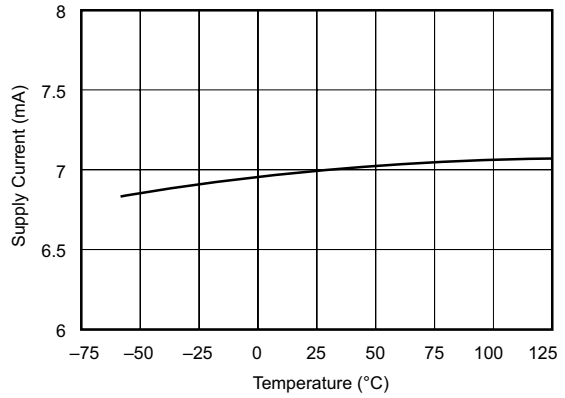


Figure 5-13. Supply Current vs Temperature

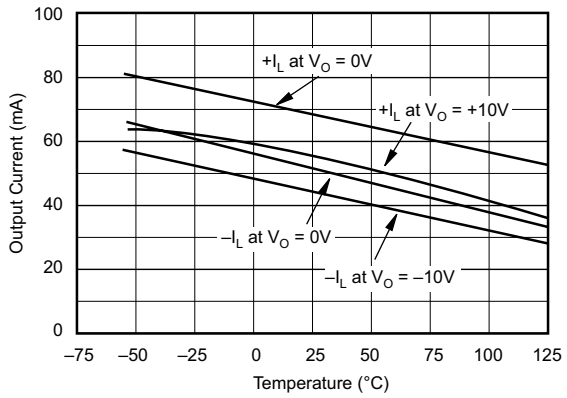


Figure 5-14. Output Current Limit vs Temperature

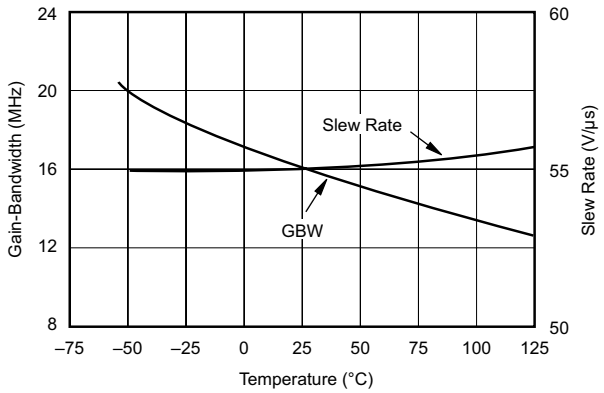


Figure 5-15. OPA627 Gain-Bandwidth and Slew Rate vs Temperature

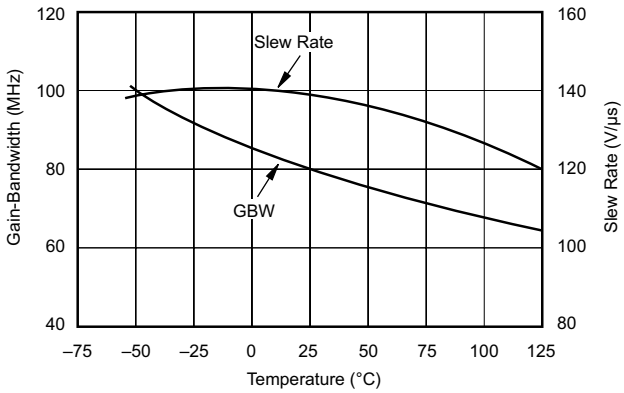


Figure 5-16. OPA637 Gain-Bandwidth and Slew Rate vs Temperature

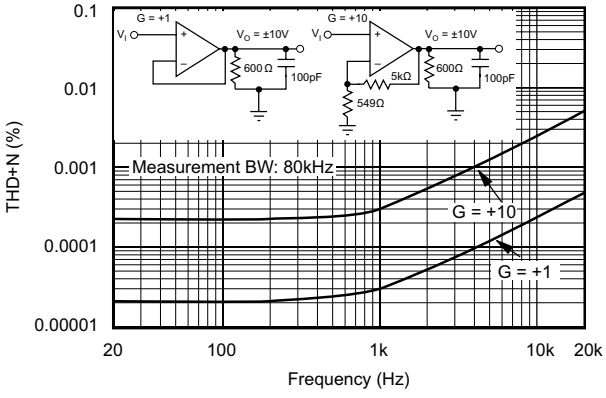


Figure 5-17. OPA627 Total Harmonic Distortion + Noise vs Frequency

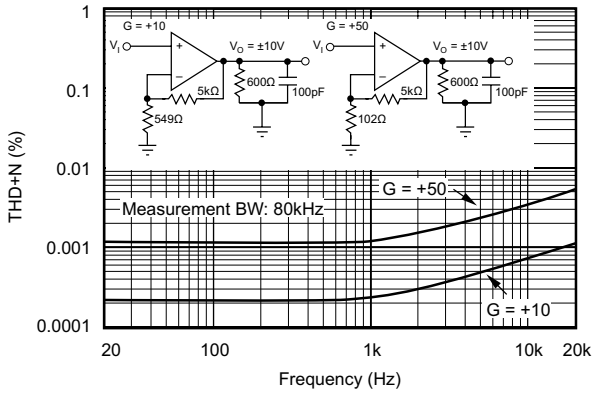


Figure 5-18. OPA637 Total Harmonic Distortion + Noise vs Frequency

5.9 Typical Characteristics (continued)

at T_A = 25°C and V_S = ±15V (unless otherwise noted)

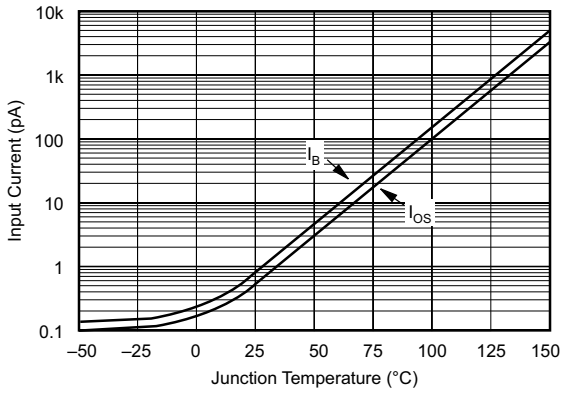


Figure 5-19. Input Bias and Offset Current vs Junction Temperature

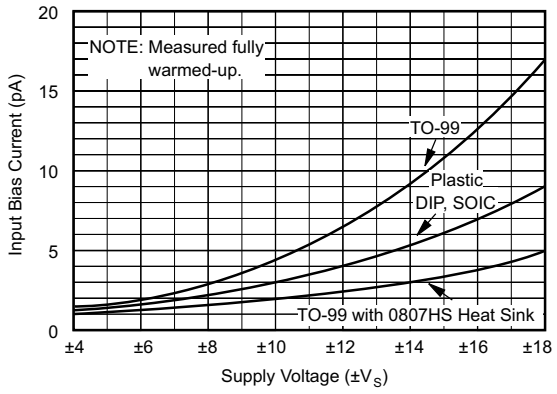


Figure 5-20. Input Bias Current vs Power Supply Voltage

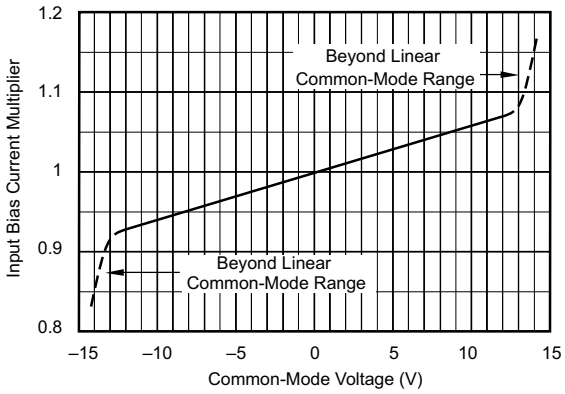


Figure 5-21. Input Bias Current vs Common-Mode Voltage

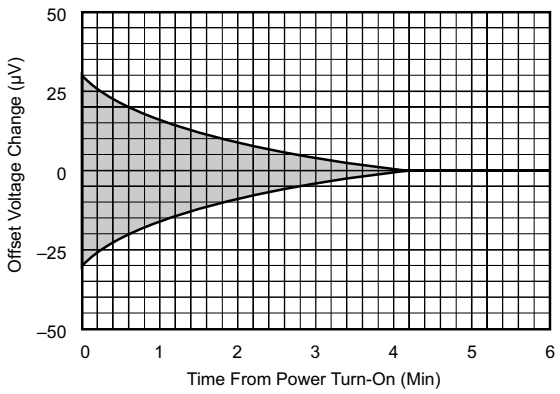


Figure 5-22. Input Offset Voltage Warm-up vs Time

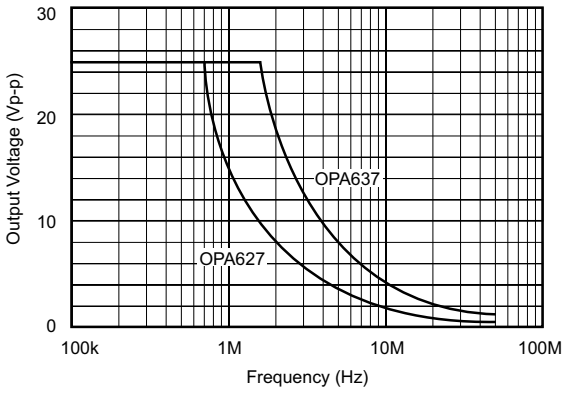


Figure 5-23. Maximum Output Voltage vs Frequency

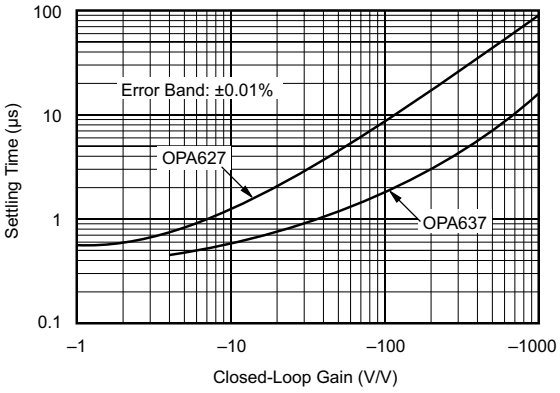


Figure 5-24. Settling Time vs Closed-Loop Gain

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5.9 Typical Characteristics (continued)

at T_A = 25°C and V_S = ±15V (unless otherwise noted)

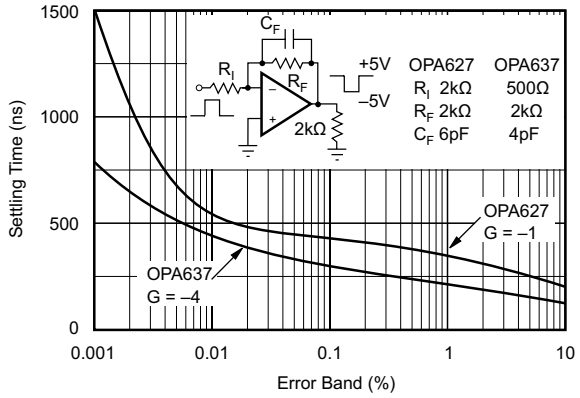


Figure 5-25. Settling Time vs Error Band

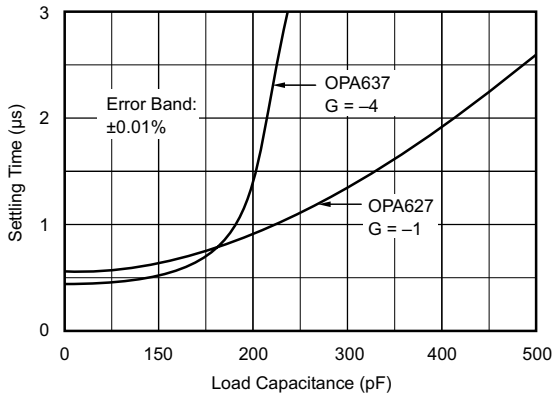


Figure 5-26. Settling Time vs Load Capacitance

6 Detailed Description

6.1 Overview

The OPA6x7 op amps provide a new level of performance in a precision FET operational amplifier. When compared to the popular OPA111 operational amplifier, the OPA6x7 have lower noise, lower offset voltage, and higher speed. The OPA6x7 are useful in a broad range of precision and high-speed analog circuitry.

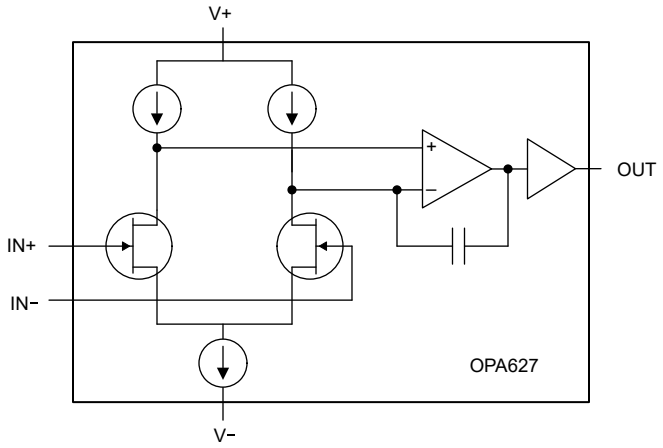
The OPA6x7 operate over the wide power-supply voltage range of ±4.5V to ±18V. Laser-trimmed input circuitry provides high accuracy and low-noise performance comparable with the best bipolar-input operational amplifiers.

High-frequency transistors allow increased circuit bandwidth, attaining dynamic performance not possible with previous precision FET operational amplifiers. The OPA627 is unity-gain stable. The OPA637 is stable in gains equal to or greater than 5.

The OPA6x7 achieve extremely low input bias currents without compromising input voltage noise performance. Low input bias current is maintained over a wide input common-mode voltage range with unique cascode circuitry.

The OPA6x7 are available in SOIC-8 and metal TO-99 packages. Industrial temperature-range models are available.

6.2 Functional Block Diagram



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6.3 Feature Description

The OPA627 is unity-gain stable. The OPA637 achieves higher speed and bandwidth in circuits with noise gain greater than 5. Noise gain refers to the closed-loop gain of a circuit, as if the noninverting operational amplifier (op amp) input were being driven. For example, the OPA637 can be used in a noninverting amplifier with gain greater than 5, or an inverting amplifier of gain greater than 4.

When choosing between the OPA627 or OPA637, consider the high frequency noise gain of the circuit configuration. Circuits with a feedback capacitor (see Figure 6-1) place the operational amplifier in unity noise-gain at high frequency. These applications must use the OPA627 for proper stability. An exception is the circuit in Figure 6-2, where a small feedback capacitance is used to compensate for the input capacitance at the inverting input of the operational amplifier. In this case, the closed-loop noise gain remains constant with frequency, so if the closed-loop gain is equal to 5 or greater, the OPA637 can be used.

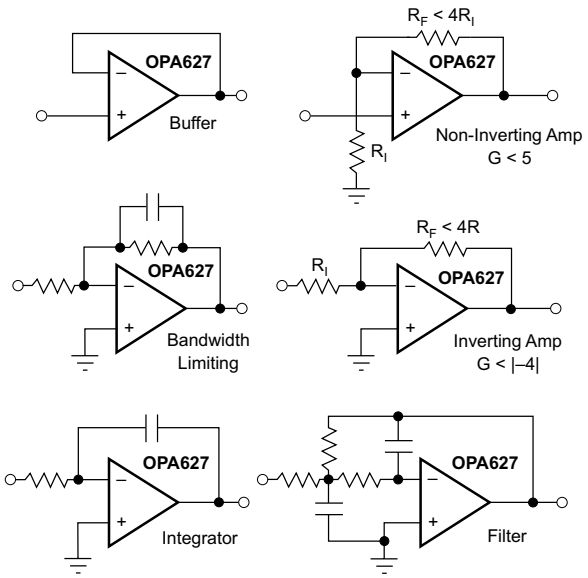


Figure 6-1. Circuits With Noise Gain Less Than 5 Require the OPA627 for Proper Stability

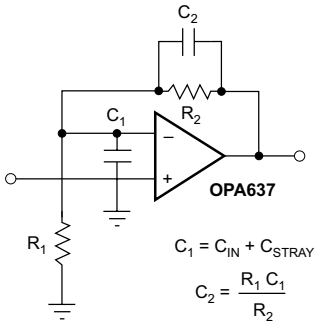


Figure 6-2. Circuits With Noise Gain Equal to or Greater Than 5 Can Use the OPA637

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6.3.1 Offset Voltage Adjustment

The OPA6x7 are laser-trimmed for low offset voltage and drift, so many circuits do not require external adjustment. The OPA6x7 offer input offset voltage as low as ±125µV and drift as low as ±0.3µV/°C, enabling applications operating over the entire industrial temperature range.

Figure 6-3 shows the optional connection of an external potentiometer to adjust offset voltage. This circuit is applicable to TO-99 packages only. Do not use this adjustment to compensate for offsets created elsewhere in a system, such as in later amplification stages or in an analog-to-digital converter (ADC).

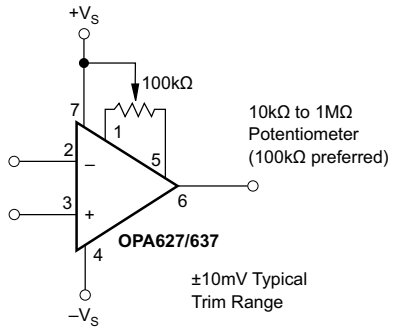


Figure 6-3. Optional Offset Voltage Trim Circuit

6.3.2 Noise Performance

Some bipolar op amps provide lower voltage noise performance, but both voltage noise and bias current noise contribute to the total noise of a system. The OPA6x7 provide both low voltage noise and low current noise. These features provide excellent noise performance over a wide range of sources, including a reactive-source impedance. The excellent noise performance can be seen in the performance curve showing the noise of a source resistor combined with the noise of an OPA627. Greater than a 2kΩ source resistance, the op amp contributes little additional noise. Less than 1kΩ, op-amp noise dominates over the resistor noise, but compares favorably with precision bipolar op amps.

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6.3.3 Input Bias Current

The OPA6x7 provide low input bias current. Because the gate current of a FET doubles approximately every 10°C, to achieve lowest input bias current, keep the die temperature as low as possible. The high speed, and therefore higher quiescent current, of the OPA6x7 can lead to higher chip temperature. Proper layout techniques help dissipate heat and reduce chip temperature, thereby lowering I_B.

A simple press-on heat sink such as the Burr-Brown model 807HS (TO-99 metal package) can reduce chip temperature by approximately 15°C, lowering the I_B to one-third of the warmed-up value. The 807HS heat sink can also reduce low-frequency voltage noise caused by air currents and thermoelectric effects.

Temperature rise in the SOIC packages can be minimized by soldering the device to the circuit board. Wide copper traces also help dissipate heat.

The OPA6x7 can also operate at reduced power supply voltage, to minimize power dissipation and temperature rise. Using ±5V power supplies reduces power dissipation to one-third of that at ±15V.

Leakage currents between printed circuit board (PCB) traces can easily exceed the input bias current of the OPA6x7. A circuit board *guard* pattern reduces leakage effects. By surrounding critical high impedance input circuitry with a low impedance circuit connection at the same potential, leakage current can flow harmlessly to the low-impedance node (see Figure 6-4). The case (TO-99 metal package only) is internally connected to $-V_S$.

Input bias current can also be degraded by improper handling or cleaning. Contamination from handling parts and circuit boards can be removed with cleaning solvents and deionized water. Follow each rinsing operation by a 30-minute bake at 85°C.

Many FET input operational amplifiers exhibit large changes in input bias current with changes in input voltage. Input stage cascode circuitry makes the input bias current of the OPA6x7 virtually constant with wide common-mode voltage changes. The OPA6x7 are a great choice for accurate, high input-impedance buffer applications.

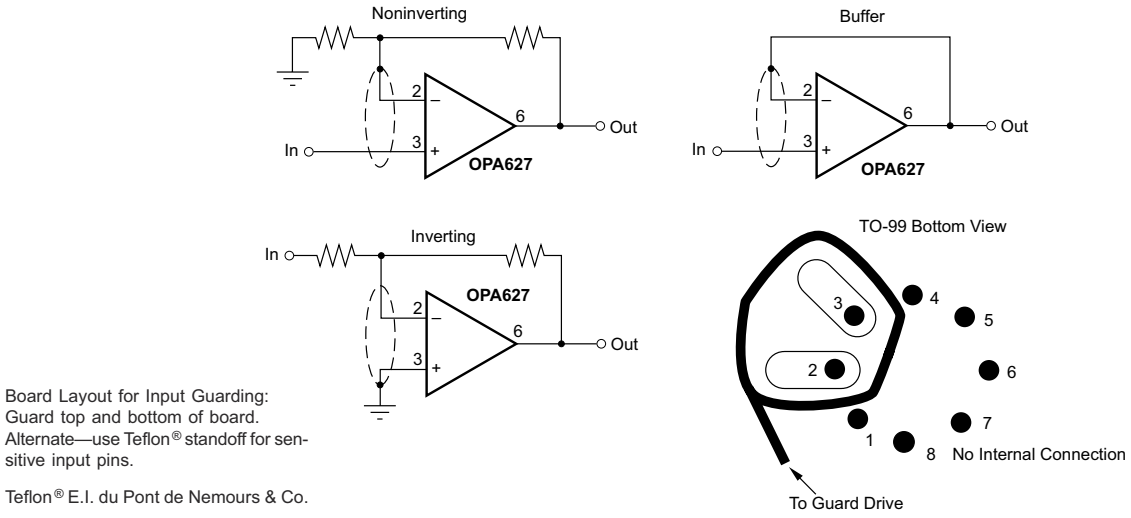


Figure 6-4. Connection of Input Guard for Lowest I_B

6.3.4 Phase-Reversal Protection

The OPA6x7 have internal phase-reversal protection. Many FET-input op amps exhibit a phase reversal when the input is driven beyond the linear common-mode range. This issue is most often encountered in noninverting circuits when the input is driven below –12V, causing the output to reverse into the positive rail. The input circuitry of the OPA6x7 does not induce phase reversal with excessive common-mode voltage, so the output limits into the appropriate rail.

6.3.5 Output Overload

When the inputs to the OPA6x7 are overdriven, the output voltage of the OPA6x7 smoothly limits at approximately 2.5V from the positive and negative power supplies. If driven to the negative swing limit, recovery takes approximately 500ns. When the output is driven into the positive limit, recovery takes approximately 6µs. Output recovery of the OPA627 can be improved using the output clamp circuit shown in Figure 6-5. Placing diodes at the inverting input prevent degradation of input bias current.

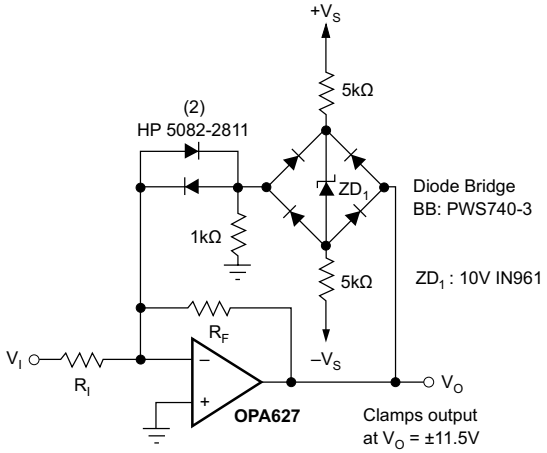


Figure 6-5. Clamp Circuit for Improved Overload Recovery

6.3.6 Capacitive Loads

As with any high-speed operational amplifier, best dynamic performance can be achieved by minimizing the capacitive load. Because a load capacitance presents a decreasing impedance at higher frequency, a load capacitance which is easily driven by a slow op amp can cause a high-speed op amp to perform poorly. See the typical curves showing settling times as a function of capacitive load. The lower bandwidth makes the OPA627 a better choice for driving large capacitive loads. Figure 6-6 shows a circuit for driving very large load capacitance. The two-pole response of this circuit can also be used to sharply limit system bandwidth, often useful in reducing the noise of systems which do not require the full bandwidth of the OPA627.

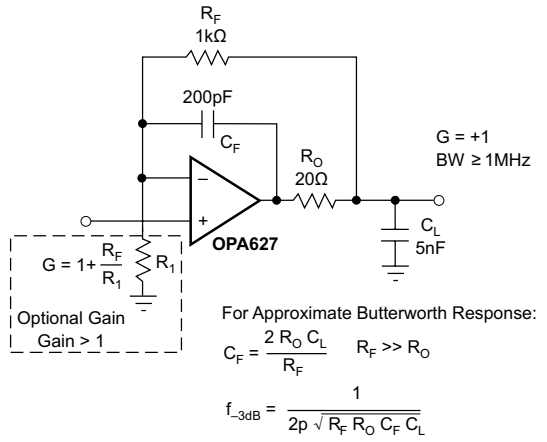


Figure 6-6. Driving Large Capacitive Loads

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6.3.7 Input Protection

The inputs of the OPA6x7 are protected for voltages from $+V_S$ + 0.5V to $–V_S$ – 0.5V. If the input voltage can exceed these limits, protect the amplifier by limiting the current into the input pins. The diode clamps shown in (a) in Figure 6-7 prevent the input voltage from exceeding one forward diode voltage drop beyond the power supplies, which is well within the safe limits. If the input source can deliver current in excess of the maximum forward current of the protection diodes, use a series resistor, R_S, to limit the current. Be aware that adding resistance to the input increases noise. The 4nV/$\sqrt{\text{Hz}}$ theoretical thermal noise of a 1kΩ resistor adds to the 4.5nV/$\sqrt{\text{Hz}}$ noise of the OPA6x7 (by the square-root of the sum of the squares), producing a total noise of 6nV/$\sqrt{\text{Hz}}$. Resistors less than 100Ω add negligible noise.

Leakage current in the protection diodes can increase the total input bias current of the circuit. The specified maximum leakage current for commonly used diodes such as the 1N4148 is approximately 25nA, more than a thousand times larger than the input bias current of the OPA6x7. Leakage current of these diodes is typically much lower and can be adequate in many applications. Light falling on the junction of the protection diodes can dramatically increase leakage current, so shield common glass-packaged diodes from ambient light. Very low leakage can be achieved by using a diode-connected FET as shown. The 2N4117A is specified at 1pA and the metal case shields the junction from light.

Sometimes input protection is required on I/V converters of inverting amplifiers; see (b) in Figure 6-7. Although in normal operation, the voltage at the summing junction is near zero (equal to the offset voltage of the amplifier), large input transients can cause this node to exceed 0.5V beyond the power supplies. In this case, protect the summing junction with diode clamps connected to ground. Even with the low voltage present at the summing junction, common signal diodes can have excessive leakage current. Because the reverse voltage on these diodes is clamped, a diode-connected signal transistor can act as an inexpensive low leakage diode; see (b) in Figure 6-7.

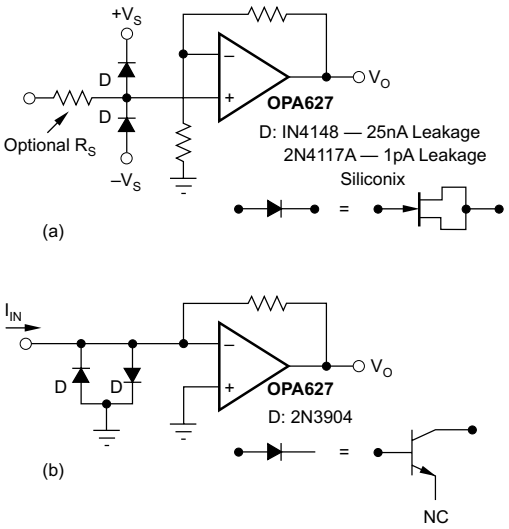


Figure 6-7. Input Protection Circuits

6.3.8 EMI Rejection Ratio (EMIRR)

The electromagnetic interference (EMI) rejection ratio, or EMIRR, describes the EMI immunity of operational amplifiers. An adverse effect that is common to many operational amplifiers is a change in the offset voltage as a result of RF signal rectification. An operational amplifier that is more efficient at rejecting this change in offset as a result of EMI has a higher EMIRR and is quantified by a decibel value. Measuring EMIRR can be performed in many ways, but this report provides the EMIRR IN+, which specifically describes the EMIRR performance when the RF signal is applied to the noninverting input pin of the operational amplifier. In general, only the noninverting input is tested for EMIRR for the following three reasons:

- Operational amplifier input pins are known to be the most sensitive to EMI, and typically rectify RF signals better than the supply or output pins.
- The noninverting and inverting operational amplifier inputs have symmetrical physical layouts and exhibit nearly matching EMIRR performance.
- EMIRR is easier to measure on noninverting pins than on other pins because the noninverting input terminal can be isolated on a printed-circuit-board (PCB). This isolation allows the RF signal to be applied directly to the noninverting input terminal with no complex interactions from other components or connecting PCB traces.

A more formal discussion of the EMIRR IN+ definition and test method is provided in the *EMI Rejection Ratio of Operational Amplifiers* application note, available for download at www.ti.com.

The EMIRR IN+ of the OPA627 is plotted versus frequency (see Figure 6-8). If available, any dual and quad op amp device versions have nearly similar EMIRR IN+ performance. The OPA627 (SOIC package) unity-gain bandwidth is 45MHz. EMIRR performance below this frequency denotes interfering signals that fall within the operational amplifier bandwidth.

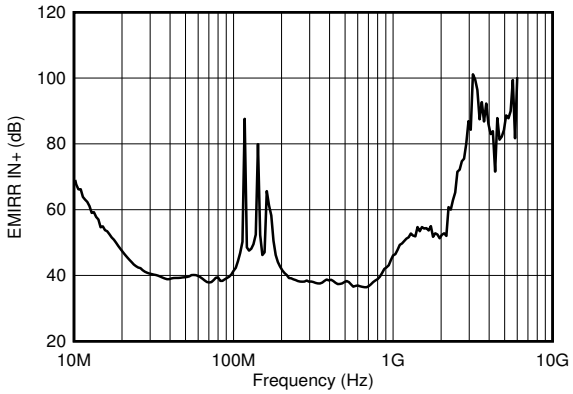


Figure 6-8. OPA627 (SOIC packages) EMIRR IN+ vs Frequency

Table 6-1 shows the EMIRR IN+ values for the OPA627 (SOIC package) at particular frequencies commonly encountered in real-world applications. Applications listed in Table 6-1 can be centered on or operated near the particular frequency shown. This information can be of special interest to designers working with these types of applications, or working in other fields likely to encounter RF interference from broad sources, such as the industrial, scientific, and medical (ISM) radio band.

Table 6-1. OPA627 (SOIC packages) EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400MHz	Mobile radio, mobile satellite and space operation, weather, radar, UHF	39dB
900MHz	GSM, radio communication/navigation/GPS (to 1.6GHz), ISM, aeronautical mobile, UHF	40dB
1.8GHz	GSM, mobile personal communication, broadband, satellite, L-band	50dB
2.4GHz	802.11b/g/n, Bluetooth™, mobile comm, ISM, amateur radio and satellite, S-band	70dB
3.6GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	85dB
5GHz	802.11a/n, aero comm and nav, mobile comm, space and satellite operation, C-band	85dB

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6.3.8.1 EMIRR IN+ Test Configuration

Figure 6-9 shows the circuit configuration for testing the EMIRR IN+. An RF source is connected to the op amp noninverting input terminal using a transmission line. The op amp is configured in a unity gain buffer topology with the output connected to a low-pass filter (LPF) and a digital multimeter (DMM). A large impedance mismatch at the op amp input causes a voltage reflection; however, this effect is characterized and accounted for when determining the EMIRR IN+. The resulting DC offset voltage is sampled and measured by the multimeter. The LPF isolates the multimeter from residual RF signals that can interfere with multimeter accuracy. See also the *EMI Rejection Ratio of Operational Amplifiers* application note.

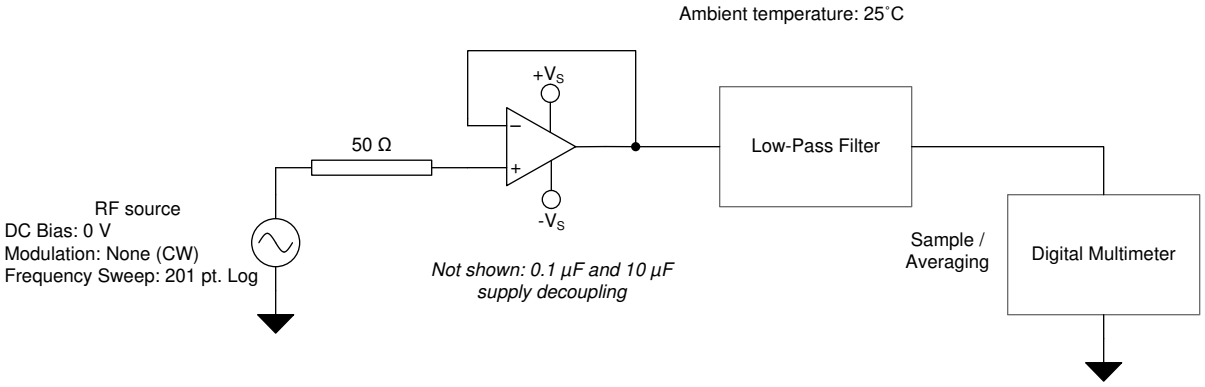
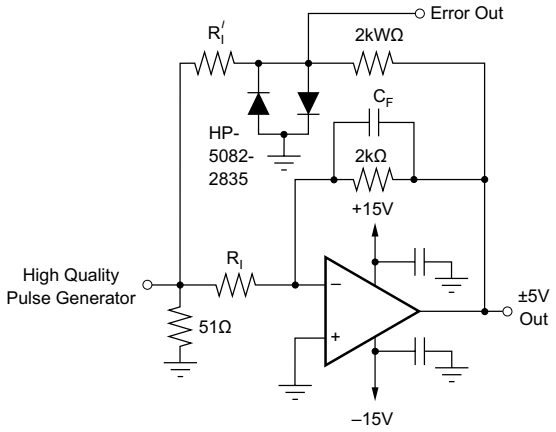


Figure 6-9. EMIRR IN+ Test Configuration Schematic

6.3.9 Settling Time

The OPA627 and OPA637 have fast settling times, as low as 110ns. Figure 6-10 illustrates the circuit used to measure settling time for the OPA627 and OPA637.



	OPA627	OPA637
R_I, R'_1	2kΩ	500Ω
C_F	6pF	4pF
Error Band (0.01%)	±0.5mV	±0.2mV

NOTE: C_F is selected for best settling time performance depending on test fixture layout. Once optimum value is determined, a fixed capacitor may be used.

Figure 6-10. Settling Time and Slew Rate Test Circuit

6.4 Device Functional Modes

The OPA627 and OPA637 have a single functional mode and are operational when the power-supply voltage is greater than 9V (±4.5V). The maximum power supply voltage for the OPA627 and OPA637 are 36V (±18V).

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The OPA627 and OPA637 are an excellent choice to use as input amplifiers in instrumentation amplifier configurations requiring high speed, fast settling and high input impedance.

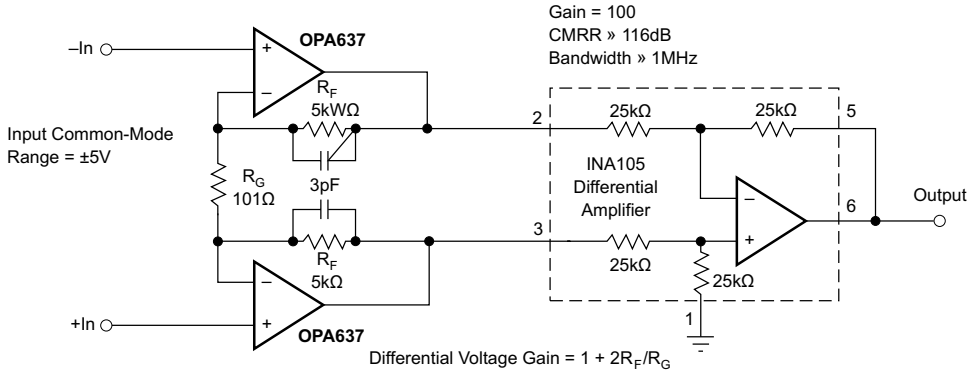


Figure 7-1. High Speed Instrumentation Amplifier, Gain = 100

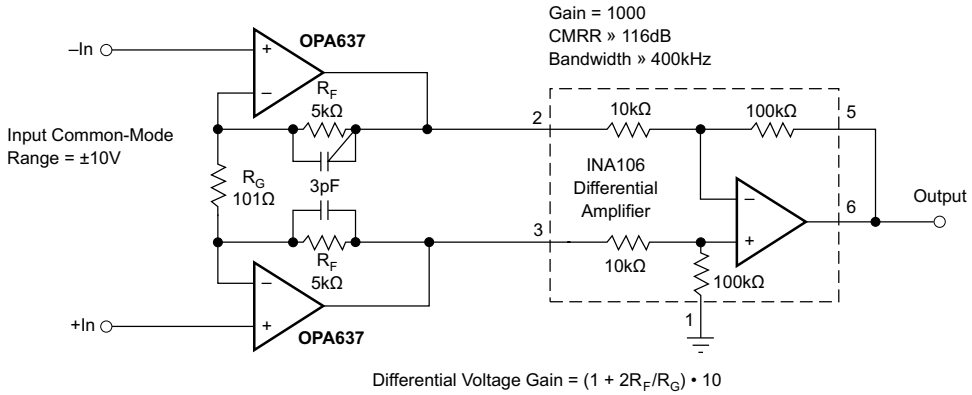
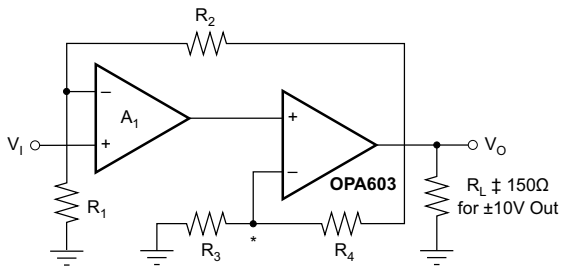


Figure 7-2. High Speed Instrumentation Amplifier, Gain = 1000



This composite amplifier uses the OPA603 current-feedback op amp to provide extended bandwidth and slew rate at high closed-loop gain. The feedback loop is closed around the composite amp, preserving the precision input characteristics of the OPA627/637. Use separate power supply bypass capacitors for each op amp.

∗Minimize capacitance at this node.

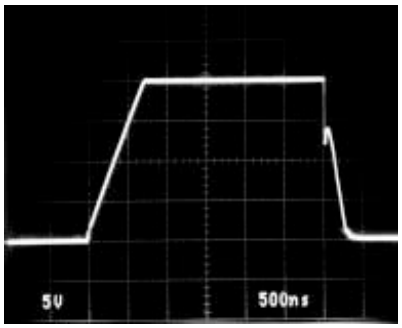
GAIN (V/V)	A_1 OP AMP	R_1 (Ω)	R_2 (kΩ)	R_3 (Ω)	R_4 (kΩ)	–3dB (MHz)	SLEW RATE (V/µs)
100	OPA627	50.5(1)	4.99	20	1	15	700
1000	OPA637	49.9	4.99	12	1	11	500

NOTE: (1) Closest 1/2% value.

Figure 7-3. Composite Amplifier for Wide Bandwidth

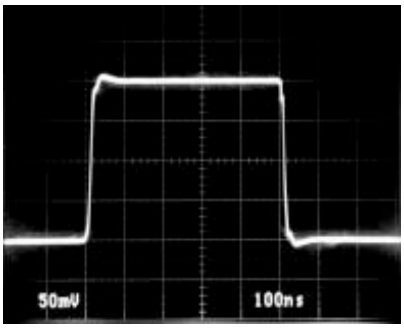
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LARGE SIGNAL RESPONSE



(A)

SMALL SIGNAL RESPONSE



(B)

When used as a unity-gain buffer, large common-mode input voltage steps produce transient variations in input-stage currents. This causes the rising edge to be slower and falling edges to be faster than nominal slew rates observed in higher-gain circuits.

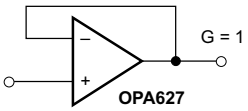
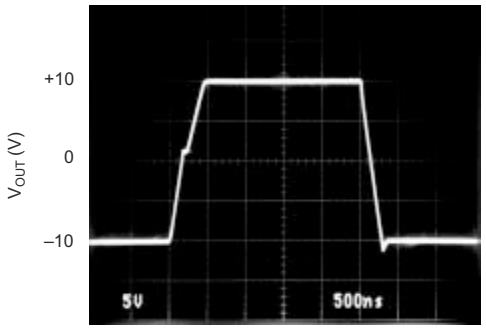
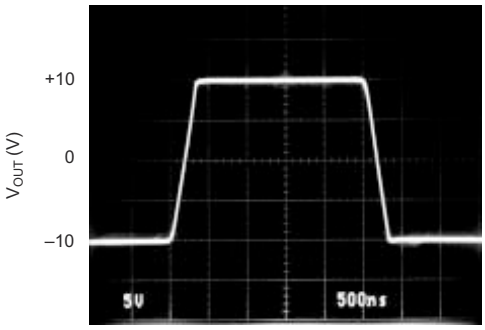


Figure 7-4. OPA627 Dynamic Performance, G = 1

LARGE SIGNAL RESPONSE



(C)



(D)

When driven with a very fast input step (left), common-mode transients cause a slight variation in input stage currents which will reduce output slew rate. If the input step slew rate is reduced (right), output slew rate will increase slightly.

NOTE: (1) Optimum value will depend on circuit board lay-out and stray capacitance at the inverting input.

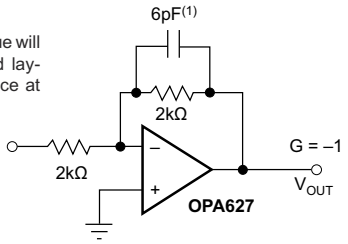


Figure 7-5. OPA627 Dynamic Performance, G = –1

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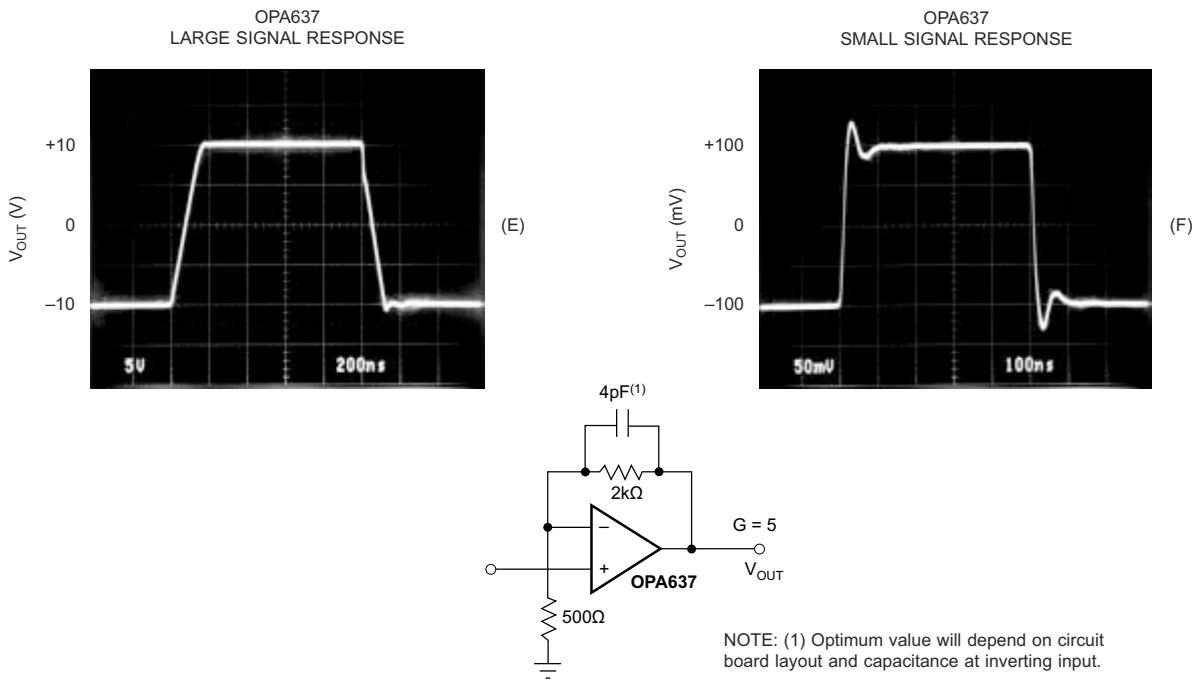


Figure 7-6. OPA637 Dynamic Response, G = 5

7.2 Typical Application

Low-pass filters are commonly employed in signal processing applications to reduce noise and prevent aliasing. The OPA627 and OPA637 are an excellent choice to construct high speed, high precision active filters. Figure 7-7 illustrates a second order low pass filter commonly encountered in signal processing applications.

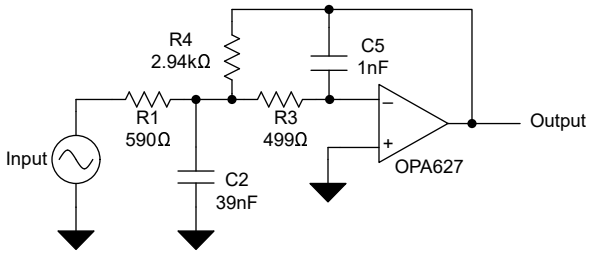


Figure 7-7. Second Order Low Pass Filter

7.2.1 Design Requirements

Use the following parameters for this design example:

- Gain = 5V/V (inverting gain)
- Low pass cutoff frequency = 25kHz
- Second order Chebyshev filter response with 3dB gain peaking in the pass band

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7.2.2 Detailed Design Procedure

The infinite-gain multiple-feedback circuit for a low-pass network function is shown in Figure 7-7. Use Equation 1 to calculate the voltage transfer function.

$$\frac{\text{Output}}{\text{Input}}(s) = \frac{-1/R_1R_3C_2C_5}{s^2 + (s/C_2)(1/R_1 + 1/R_3 + 1/R_4) + 1/R_3R_4C_2C_5} \quad (1)$$

This circuit produces a signal inversion. For this circuit the gain at DC and the low pass cutoff frequency can be calculated using Equation 2.

$$\text{Gain} = \frac{R_4}{R_1}$$
$$f_C = \frac{1}{2\pi}\sqrt{(1/R_3R_4C_2C_5)} \quad (2)$$

Software tools are readily available to simplify filter design. Available as a web-based tool from the Design tools and simulation web page, the Analog Filter Designer allows the user to design, optimize, and simulate complete multistage active filter solutions within minutes.

7.2.3 Application Curve

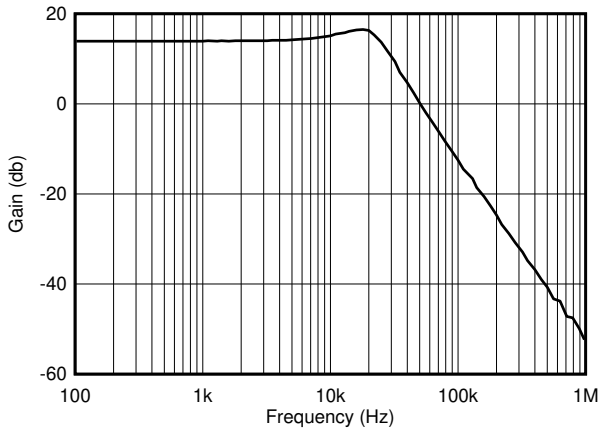


Figure 7-8. OPA627 2nd Order 25kHz, Chebyshev, Low-Pass Filter

7.3 Power Supply Recommendations

The OPA6x7 are specified for operation from 9V to 36V (±4.5V to ±18V); many specifications apply from –25°C to +85°C (OPA6x7AU, OPA627BU, OPA6x7AM, and OPA6x7BM) and –55°C to +125°C (OPA6x7SM). Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Section 5.9*.

7.4 Layout

7.4.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit and directly through the operational amplifier. Bypass capacitors help to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
  - The OPA6x7 is capable of high-output current (in excess of 45mA). Applications with low impedance loads or capacitive loads with fast transient signals demand large currents from the power supplies. Larger bypass capacitors such as 1µF solid tantalum capacitors can improve dynamic performance in these applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in Figure 7-10, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- The case (TO-99 metal package only) is internally connected to the negative power supply, as with most common operational amplifiers.
- Pin 1, 5, and 8 of the SOIC packages have no internal connection. Pin 8 of the TO-99 packages has no internal connection.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit can experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

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7.4.2 Layout Example

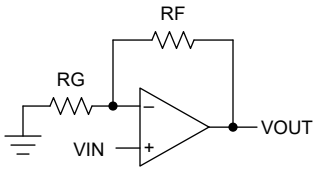


Figure 7-9. OPA627 Layout Example for the Noninverting Configuration (Schematic Representation)

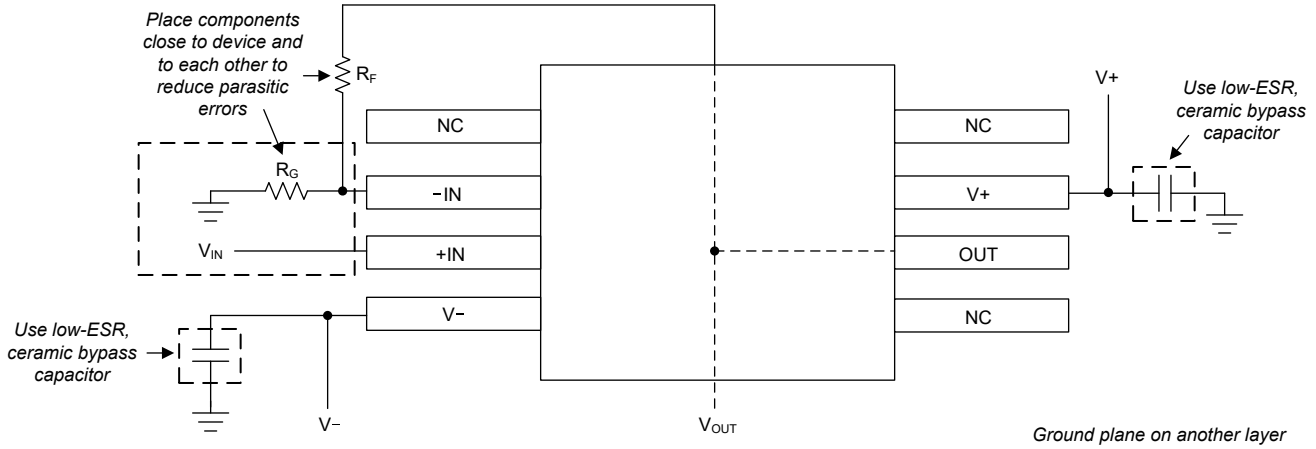


Figure 7-10. OPA627 Layout Example for the Noninverting Configuration

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 TINA-TI™ Simulation Software (Free Download)

TINA-TI™ simulation software is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI simulation software is a free, fully-functional version of the TINA™ software, preloaded with a library of macromodels, in addition to a range of both passive and active models. TINA-TI simulation software provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Design and simulation tools web page, TINA-TI simulation software offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software or TINA-TI software be installed. Download the free TINA-TI simulation software from the TINA-TI™ software folder.

8.1.1.2 Analog Filter Designer

Available as a web-based tool from the Design and simulation tool web page, the Analog Filter Designer allows the user to design, optimize, and simulate complete multistage active filter solutions within minutes.

8.1.1.3 TI Reference Designs

TI reference designs are analog solutions created by TI's precision analog applications experts. TI reference designs offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits. TI reference designs are available online at https://www.ti.com/reference-designs.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Compensate Transimpedance Amplifiers Intuitively*
- Texas Instruments, *Noise Analysis for High Speed op Amps*

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (April 2024) to Revision C (January 2025) — **Page**

- Changed OPA627BU status from preview to production data (active) ... 1

Changes from Revision A (April 2015) to Revision B (April 2024) — **Page**

- Added OPA627BU preview device and related information to data sheet ... 1
- Deleted Difet references throughout the data sheet ... 1
- Changed *OPA627 Simplified Schematic* to *OPA627 Low-Pass Filter* ... 1
- Deleted P package (PDIP, 8) from data sheet ... 1
- Updated text in *Description* ... 1
- Updated pin configuration diagrams and functions tables in *Pin Configuration and Functions* ... 3
- Changed signal input pin voltage common-mode from "(V–) – 2V to (V+) + 2V" to "(V–) – 0.5V to (V+) + 0.5V" and differential from total V_S + 4 to (V+) – (V–) in *Absolute Maximum Ratings* ... 4
- Added input pin current range row to *Absolute Maximum Ratings* ... 4
- Updated OPA627AU *ESD Ratings* ... 4
- Updated specified temperature range to fix typo in *Recommended Operating Conditions* ... 4
- Updated OPA627AU *Thermal Information* ... 5
- Updated *Electrical Characteristics* to individual tables ... 6
- Updated parameter abbreviations and names in all *Electrial Characteristics* ... 6
- Added nominal conditions to the header of all *Electrical Characteristics* ... 6
- Added ± to input offset voltage, input offset voltage drift, input bias current, and input offset current values to all *Electrical Characteristics* ... 6
- Changed OPA627AU input voltage noise from $0.8V_{PP}$ to $0.34V_{PP}$ ... 6
- Updated OPA627AU input voltage noise density values ... 6
- Changed OPA627AU common-mode input impedance from 7pF to 9pF ... 6
- Changed OPA627AU gain-bandwidth product from 16MHz to 45MHz ... 6
- Added OPA627AU capacitive load test condition to gain-bandwidth product and settling time ... 6
- Changed OPA627AU slew rate TYP value from 55V/µs to 150V/µs and deleted MIN value ... 6
- Changed OPA627AU settling time from 550ns to 120ns for 0.01%, and from 450ns to 110ns for 0.1% ... 6
- Added OPA627AU THD+N V_O test condition ... 6
- Changed OPA627AU current output from ±45 to ±30mA ... 6
- Changed OPA627AU short-circuit current TYP value from ±70mA/–50mA to ±45mA and deleted MIN and MAX values ... 6
- Changed OPA627AU open-loop output impedance from 55Ω to 13.5Ω ... 6
- Updated *Functional Block Diagram* ... 18
- Updated text in *Offset Voltage Adjustment* ... 20
- Changed protection range from "+V_S + 2V to –V_S – 2V" to "+V_S + 0.5V to –V_S – 0.5V" in *Input Protection* ... 23
- Updated Figure 6-8, *OPA627 EMIRR IN+ vs Frequency*, Table 6-1, *OPA627 EMIRR IN+ Frequencies of Interest*, and related description in *EMI Rejection Ratio (EMIRR)* ... 24

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- Deleted duplicate Figure 46; see Figure 6-4, *Connection of Input Guard for Lower I_B* 31
- Updated Figure 45, and moved to Figure 7-9 and Figure 7-10..... 31

Changes from Revision * (September 2000) to Revision A (April 2015) **Page**

- Added *ESD Ratings*, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections.....1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA627AM	Last Time Buy	Production	TO-99 (LMC) | 8	20 | TUBE	Yes	Call TI	N/A for Pkg Type	-	OPA627AM
OPA627AM.A	NRND	Production	TO-99 (LMC) | 8	20 | TUBE	Yes	Call TI	N/A for Pkg Type	-25 to 85	OPA627AM
OPA627AU	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-25 to 85	OPA 627AU
OPA627AU.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-25 to 85	OPA 627AU
OPA627AU/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-25 to 85	OPA 627AU
OPA627AU/2K5.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-25 to 85	OPA 627AU
OPA627AU/2K5E4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-25 to 85	OPA 627AU
OPA627AUE4	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-25 to 85	OPA 627AU
OPA627AUG4	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-25 to 85	OPA 627AU
OPA627BU	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-25 to 85	OPA 627BU
OPA627BU.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-25 to 85	OPA 627BU
OPA627BU/2K5	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-25 to 85	OPA 627BU
OPA627BU/2K5.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-25 to 85	OPA 627BU
OPA627SM	Last Time Buy	Production	TO-99 (LMC) | 8	20 | TUBE	Yes	AU	N/A for Pkg Type	-	OPA627SM
OPA627SM.A	NRND	Production	TO-99 (LMC) | 8	20 | TUBE	Yes	AU	N/A for Pkg Type	-25 to 85	OPA627SM
OPA637AM	Last Time Buy	Production	TO-99 (LMC) | 8	20 | TUBE	Yes	Call TI	N/A for Pkg Type	-	OPA637AM
OPA637AM.A	NRND	Production	TO-99 (LMC) | 8	20 | TUBE	Yes	Call TI	N/A for Pkg Type	-25 to 85	OPA637AM
OPA637AU	Last Time Buy	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-25 to 85	OPA 637AU

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA637AU.A	NRND	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-25 to 85	OPA 637AU
OPA637AU/2K5	Last Time Buy	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-25 to 85	OPA 637AU
OPA637AU/2K5.A	NRND	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-25 to 85	OPA 637AU
OPA637BM	Last Time Buy	Production	TO-99 (LMC) | 8	20 | TUBE	Yes	Call TI	N/A for Pkg Type	-	OPA637BM
OPA637BM.A	NRND	Production	TO-99 (LMC) | 8	20 | TUBE	Yes	Call TI	N/A for Pkg Type	-25 to 85	OPA637BM
OPA637SM	Last Time Buy	Production	TO-99 (LMC) | 8	20 | TUBE	Yes	AU	N/A for Pkg Type	-	OPA637SM
OPA637SM.A	NRND	Production	TO-99 (LMC) | 8	20 | TUBE	Yes	AU	N/A for Pkg Type	-25 to 85	OPA637SM

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

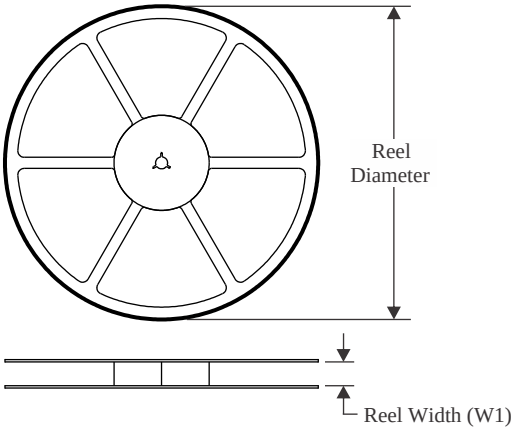
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and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

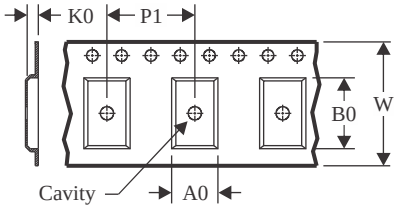
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

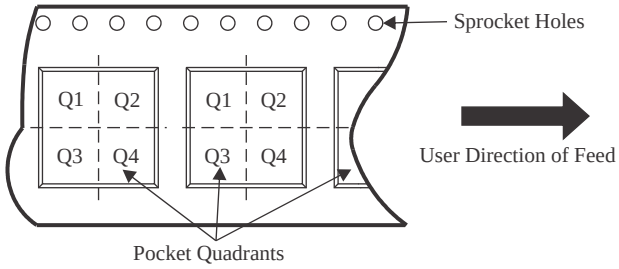


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

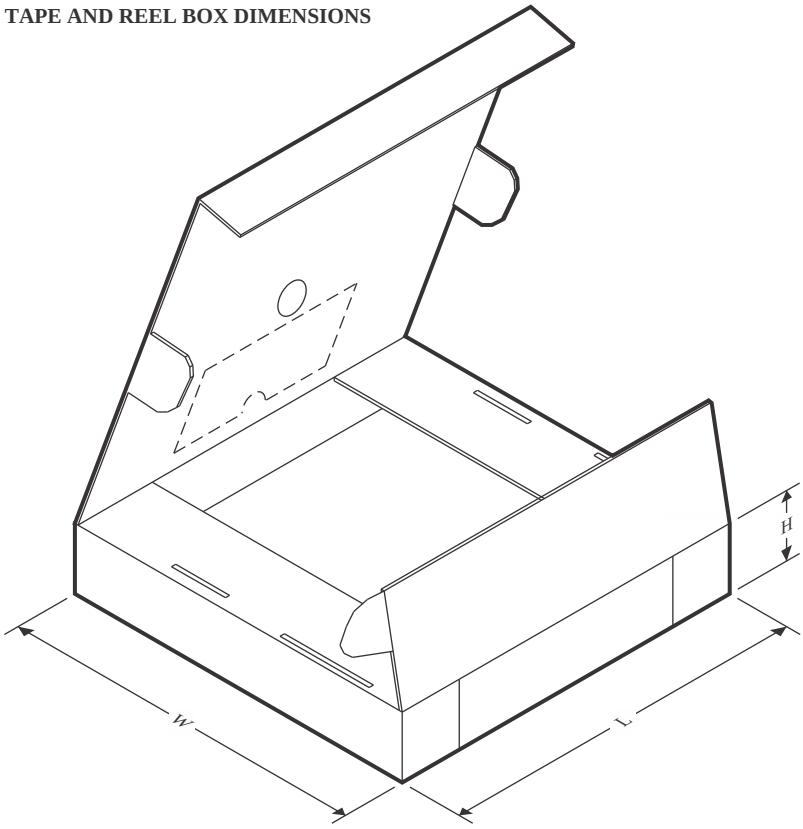
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA627AU/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA627BU/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA637AU/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

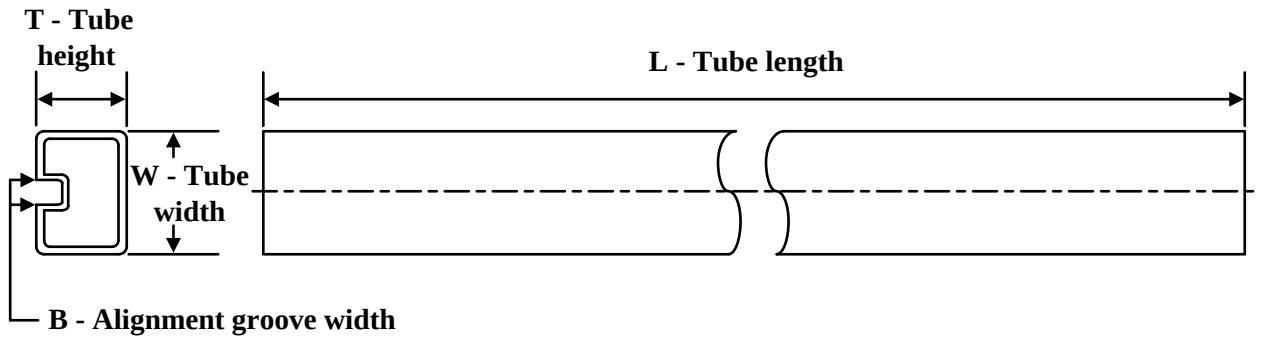
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA627AU/2K5	SOIC	D	8	2500	353.0	353.0	32.0
OPA627BU/2K5	SOIC	D	8	2500	353.0	353.0	32.0
OPA637AU/2K5	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

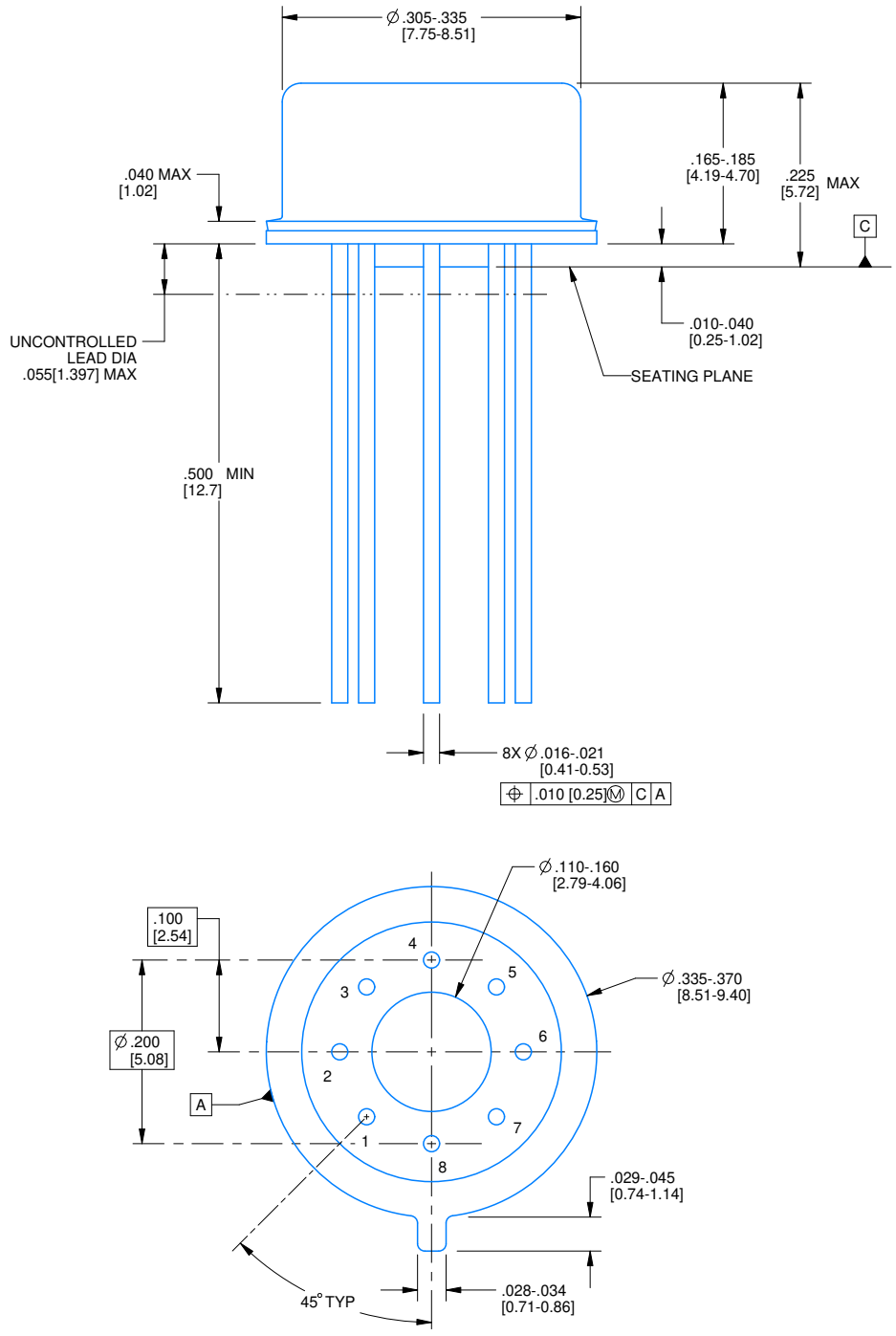
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA627AM	LMC	TO-CAN	8	20	532.13	21.59	889	NA
OPA627AM.A	LMC	TO-CAN	8	20	532.13	21.59	889	NA
OPA627AU	D	SOIC	8	75	506.6	8	3940	4.32
OPA627AU.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA627AUE4	D	SOIC	8	75	506.6	8	3940	4.32
OPA627AUG4	D	SOIC	8	75	506.6	8	3940	4.32
OPA627BU	D	SOIC	8	75	506.6	8	3940	4.32
OPA627BU.B	D	SOIC	8	75	506.6	8	3940	4.32
OPA627SM	LMC	TO-CAN	8	20	532.13	21.59	889	NA
OPA627SM.A	LMC	TO-CAN	8	20	532.13	21.59	889	NA
OPA637AM	LMC	TO-CAN	8	20	532.13	21.59	889	NA
OPA637AM.A	LMC	TO-CAN	8	20	532.13	21.59	889	NA
OPA637AU	D	SOIC	8	75	506.6	8	3940	4.32
OPA637AU.A	D	SOIC	8	75	506.6	8	3940	4.32
OPA637BM	LMC	TO-CAN	8	20	532.13	21.59	889	NA
OPA637BM.A	LMC	TO-CAN	8	20	532.13	21.59	889	NA
OPA637SM	LMC	TO-CAN	8	20	532.13	21.59	889	NA
OPA637SM.A	LMC	TO-CAN	8	20	532.13	21.59	889	NA

PACKAGE OUTLINE

LMC0008A

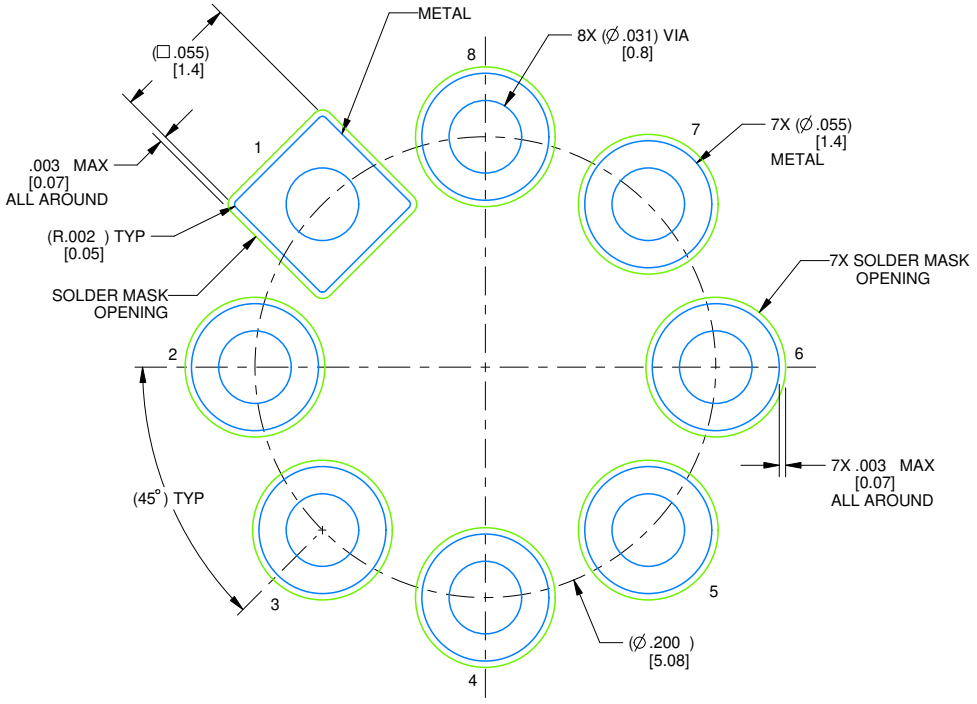
TO-CAN - 5.72 mm max height

TRANSISTOR OUTLINE



NOTES:

1. All linear dimensions are in inches [millimeters]. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Pin numbers shown for reference only. Numbers may not be marked on package.
4. Reference JEDEC registration MO-002/TO-99.



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 12X

4220610/B 09/2024

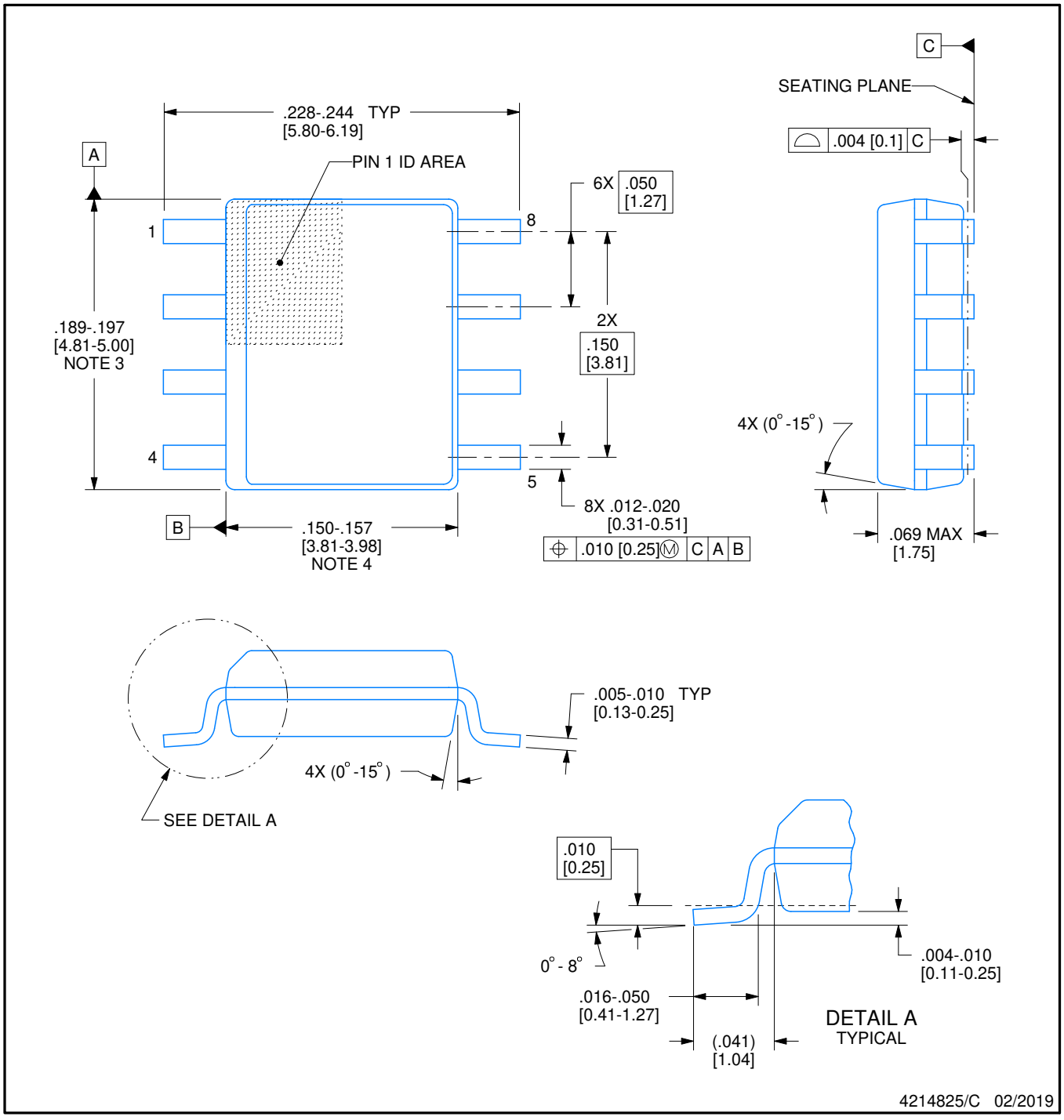


PACKAGE OUTLINE

D0008A

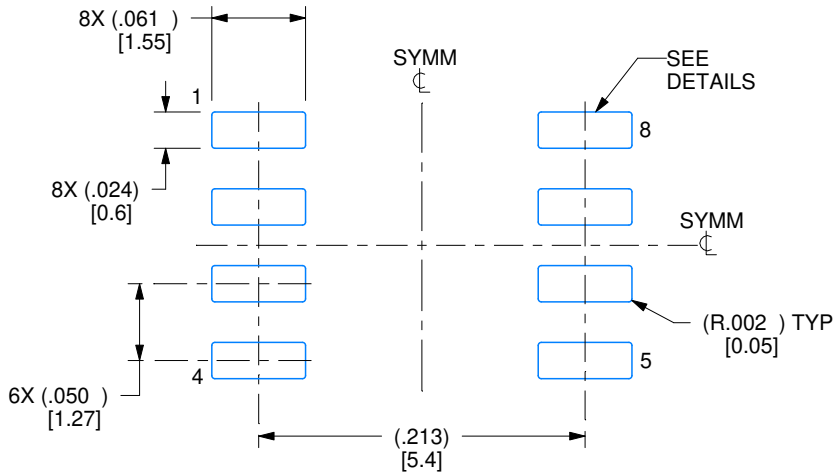
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

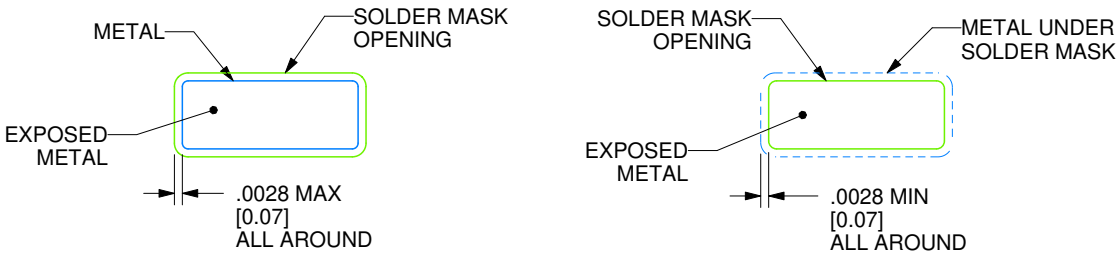


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

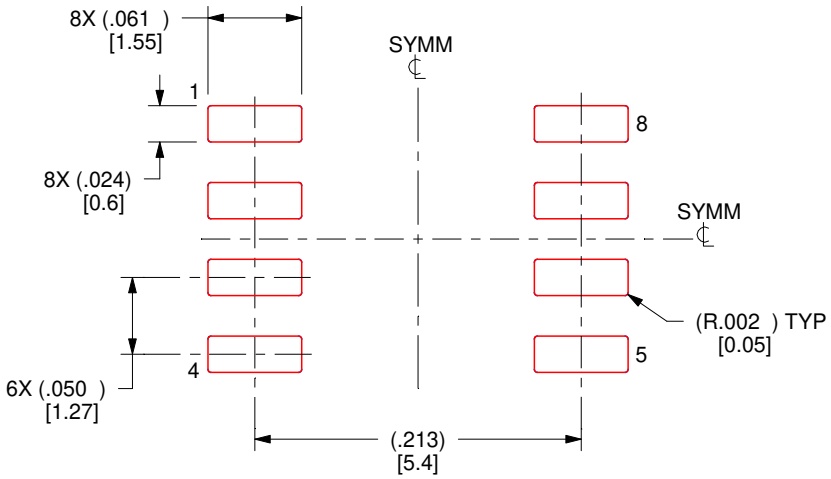
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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