OPA659 Wideband, Unity-Gain Stable, JFET-Input Operational Amplifier

1 Features

- High Bandwidth: 650 MHz (G = 1 V/V)
- High Slew Rate: 2550 V/µs (4-V Step)
- Excellent THD: –78 dBc at 10 MHz
- Low Input Voltage Noise: 8.9 nV/√Hz
- Fast Overdrive Recovery: 8 ns
- Fast Settling time (1% 4-V Step): 8 ns
- Low Input Offset Voltage: ±1 mV
- Low Input Bias Current: ±10 pA
- High Output Current: 70 mA

2 Applications

- High-Impedance Data Acquisition Input Amplifiers
- High-Impedance Oscilloscope Input Amplifiers
- Wideband Photodiode Transimpedance Amplifiers
- Wafer Scanning Equipment
- Optical Time-Domain Reflectometry (OTDR)
- High-Speed Time-of-Flight (TOF) Sensing

3 Description

The OPA659 combines a very wideband, unity-gain stable, voltage-feedback operational amplifier with a JFET-input stage to offer an ultra-high dynamic range amplifier for high impedance buffering in data acquisition applications such as oscilloscope front-end amplifiers and machine vision applications such as photodiode transimpedance amplifiers used in wafer inspection.

The wide 650-MHz unity-gain bandwidth is complemented by a very high 2550-V/µs slew rate.

The high input impedance and low bias current provided by the JFET input are supported by the low 8.9-nV/√Hz input voltage noise to achieve a very low integrated noise in wideband photodiode transimpedance applications.

Broad transimpedance bandwidths are possible with the high 350-MHz gain bandwidth product of this device.

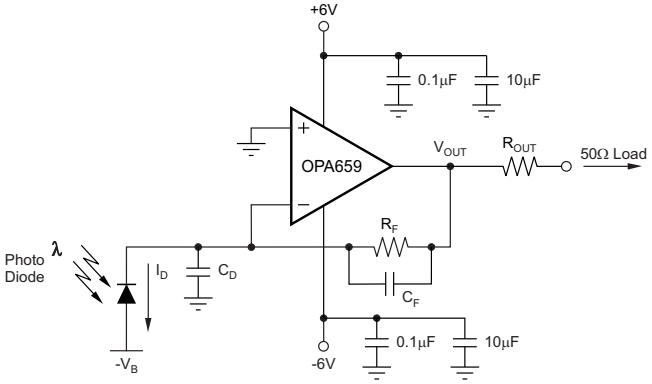
Where lower speed with lower quiescent current is required, consider the OPA656. Where unity-gain stability is not required, consider the OPA657.

Device Information(1)

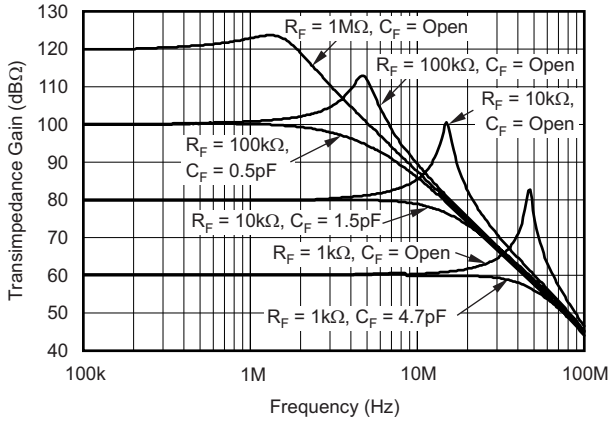
PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA659	SOT-23 (5)	2.90 mm × 1.60 mm
	SON (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



Transimpedance Gain vs Frequency



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (August 2009) to Revision C — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted THERMAL CHARACTERISTICS row from *Electrical Characteristics* ... 5

Changes from Revision A (March, 2009) to Revision B — **Page**

- Removed lead temperature specification from *Absolute Maximum Ratings* table ... 3
- Added *DRB package* to test condition for Input Offset Voltage parameter, T_A = –40°C to 85°C ... 5
- Added performance specifications for Input Offset Voltage parameter, DBV package ... 5
- Added performance specifications for Average Offset Voltage Drift parameter, DBV package ... 5
- Added footnote (2) to *Electrical Characteristics (V_S = ±6V)* table ... 5
- Added paragraph (f) to the *Board Layout* section ... 22

Changes from Original (December, 2008) to Revision A — **Page**

- Changed Changed ordering information for SOTS23-5 (DBV) package and added footnote; availability expected 2Q 2009 ... 3

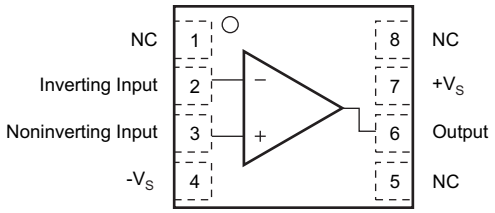
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5 Related Operational Amplifier Products

DEVICE	V_S (V)	BW (MHz)	SLEW RATE (V/µs)	VOLTAGE NOISE (nV/√Hz)	AMPLIFIER DESCRIPTION
OPA659	±6	350	2550	8.9	Unity-Gain Stable FET-Input
OPA656	±5	230	290	7	Unity-Gain Stable FET-Input
OPA657	±5	1600	700	4.8	Gain of +7 stable FET Input
LMH6629	5	4000	1600	0.69	Gain of +10 stable Bipolar Input
THS4631	±15	210	1000	7	Unity-Gain Stable FET-Input
OPA857	5	4750	220	—	Programmable Gain (5 kΩ / 20 kΩ) Transimpedance Amplifier

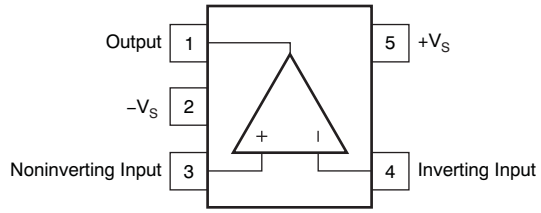
6 Pin Configuration and Functions

DRB Package
8-Pin VSON With Exposed Thermal Pad
Top View



NC: Not connected.

DRV Package
5-Pin SOT23
Top View



Pin Functions

PIN			TYPE	DESCRIPTION
NAME	SOIC	SOT-23		
NC	1	—	—	No Connection
	5			
	8			
$V_{IN–}$	2	4	I	Inverting Input
V_{IN+}	3	3	I	Noninverting Input
V_{OUT}	6	1	O	Output of amplifier
$–V_S$	4	2	POW	Negative Power Supply
$+V_S$	7	5	POW	Positive Power Supply

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted).

	MIN	MAX	UNIT
Power Supply Voltage V_{S+} to $V_{S–}$		±6.5	V
Input Voltage		$±V_S$	V
Input Current		100	mA
Output Current		100	mA
Continuous Power Dissipation	See *Thermal Information*		
Operating Free Air Temperature, T_A	–40	85	°C
Maximum Junction Temperature, T_J		150	°C
Maximum Junction Temperature, T_J (continuous operation for long term reliability)		125	°C
Storage Temperature, T_{stg}	–65	150	°C

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7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	
		Machine model (MM)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Total supply voltage	7	12	13	V
T_A	Ambient temperature	–40	25	85	°C

7.4 Thermal Information

THERMAL METRIC (1)		OPA659		UNIT
		DRB (VSON)	DRV (SOT23)	
		8 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	56.3	209	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	63.7	124	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	31.9	38.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.2	15	°C/W
ψ_{JB}	Junction-to-board characterization parameter	32.1	37.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	15.3	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

At R_F = 0 Ω, G = 1 V/V, and R_L = 100 Ω, T_A = 25°C, V_S = ±6 V unless otherwise noted.

PARAMETER	TEST CONDITIONS	TEST LEVEL (1)	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
Small-Signal Bandwidth	V_O = 200 mV_{PP}, G = 1 V/V	C		650		MHz
	V_O = 200 mV_{PP}, G = 2 V/V	C		335		MHz
	V_O = 200 mV_{PP}, G = 5 V/V	C		75		MHz
	V_O = 200 mV_{PP}, G = 10 V/V	C		35		MHz
Gain Bandwidth Product	G > 10 V/V	C		350		MHz
Bandwidth for 0.1dB Flatness	G = 2 V/V, V_O = 2V_{PP}	C		55		MHz
Large-Signal Bandwidth	V_O = 2 V_{PP}, G = 1 V/V	B		575		MHz
Slew Rate	V_O = 4-V Step, G = 1 V/V	B		2550		V/µs
Rise and Fall Time	V_O = 4-V Step, G = 1 V/V	C		1.3		ns
Settling Time to 1%	V_O = 4-V Step, G = 1 V/V	C		8		ns
Pulse Response Overshoot	V_O = 4-V Step, G = 1 V/V	C		12%		
Harmonic Distortion, 2nd harmonic	V_O = 2 V_{PP}, G = 1 V/V, f = 10 MHz	C		–79		dBc
Harmonic Distortion, 3rd harmonic	V_O = 2 V_{PP}, G = 1 V/V, f = 10 MHz	C		–100		dBc
Intermodulation Distortion, 2nd intermodulation	V_O= 2 V_{PP} Envelope (each tone 1 V_{PP}), G = 2 V/V, f_1 = 10 MHz, f_2 = 11 MHz	C		–72		dBc
Intermodulation Distortion, 3rd intermodulation	V_O= 2 V_{PP} Envelope (each tone 1 V_{PP}), G = 2 V/V, f_1 = 10 MHz, f_2 = 11 MHz	C		–96		dBc

(1) Test levels: **(A)** 100% tested at 25°C. Over temperature limits set by characterization and simulation. **(B)** Limits set by characterization and simulation. **(C)** Typical value only for information.

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Electrical Characteristics (continued)

At R_F = 0 Ω, G = 1 V/V, and R_L = 100 Ω, T_A = 25°C, V_S = ±6 V unless otherwise noted.

PARAMETER	TEST CONDITIONS		TEST LEVEL(1)	MIN	TYP	MAX	UNIT
Input Voltage Noise	f > 100 kHz		C		8.9		nV/√Hz
Input Current Noise	f < 10 MHz		C		1.8		fA/√Hz
DC PERFORMANCE							
Open-Loop Voltage Gain (A_{OL})	T_A = 25°C, V_{CM} = 0 V, R_L = 100 Ω		A	52	58		dB
	T_A = –40°C to 85°C, V_{CM} = 0 V, R_L = 100 Ω		B	49	55		dB
Input Offset Voltage	T_A = 25°C, V_{CM} = 0 V		A		±1	±5	mV
	T_A = –40°C to 85°C, V_{CM} = 0 V DRB package	DRB package	B		±1.5	±7.6	mV
		DBV package	B		±1.5	±8.9	mV
Average input-offset voltage drift(2)	T_A = –40°C to 85°C, V_{CM} = 0 V	DRB package	B		±10	±40	µV/°C
		DBV package	B		±10	±60	µV/°C
Input Bias Current	T_A = 25°C, V_{CM} = 0 V		A		±10	±50	pA
	T_A = 0°C to 70°C, V_{CM} = 0 V		B		±240	±1200	pA
	T_A = –40°C to 85°C, V_{CM} = 0 V		B		±640	±3200	pA
Average input bias current drift	T_A = 0°C to 70°C, V_{CM} = 0 V		B		±5	±26	pA/°C
	T_A = –40°C to 85°C, V_{CM} = 0 V		B		±7	±34	pA/°C
Input Offset Current	T_A = 25°C, V_{CM} = 0 V		A		±5	±25	pA
	T_A = 0°C to 70°C, V_{CM} = 0 V		B		±120	±600	pA
	T_A = –40°C to 85°C, V_{CM} = 0 V		B		±320	±1600	pA
INPUT							
Common-Mode Input Range(3)	T_A = 25°C		A	±3	±3.5		V
	T_A = –40°C to 85°C		B	±2.87	±3.37		V
Common-Mode Rejection Ratio	T_A = 25°C, V_{CM} = ±0.5 V		A	68	70		dB
	T_A = –40°C to 85°C, V_{CM} = ±0.5 V		B	64	66		dB
Input Impedance							
Input impedance, differential			C		$10^{12} \parallel 1$		Ω ‖ pF
Input impedance, common-mode			C		$10^{12} \parallel 2.5$		Ω ‖ pF
OUTPUT							
Output Voltage Swing	T_A = 25°C,	No Load	A	±4.6	±4.8		V
		R_L = 100 Ω	A	±3.8	±4		V
	T_A = –40°C to 85°C	No Load	B	±4.45	±4.65		V
		R_L = 100 Ω	B	±3.65	±3.85		V
Output Current, Sourcing, Sinking	T_A = 25°C		A	±60	±70		mA
	T_A = –40°C to 85°C		B	±56	±65		mA
Closed-Loop Output Impedance	G = 1 V/V, f = 100 kHz		C		0.04		Ω
POWER SUPPLY							
Operating Voltage			B	±3.5	±6	±6.5	V
Quiescent Current	T_A = 25°C		A	30.5	32	33.5	mA
	T_A = –40°C to 85°C		B	28.3		35.7	mA
Power-Supply Rejection Ratio (PSRR)	T_A = 25°C, V_S = ±5.5 V to ±6.5 V		A	58	62		dB
	T_A = –40°C to 85°C, V_S = ±5.5 V to ±6.5 V		A	56	60		dB

(2) DRB package only.
(3) Tested <6dB below minimum specified CMRR at ±CMIR limits.

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7.6 Typical Characteristics

At V_S = ±6 V, R_F = 0 Ω, G = 1 V/V, and R_L = 100 Ω, unless otherwise noted.

Table 1. Table of Graphs

TITLE		FIGURE
Noninverting Small-Signal Frequency Response	V_O = 200 mV_{PP}	Figure 1
Noninverting Large-Signal Frequency Response	V_O = 2 V_{PP}	Figure 2
Noninverting Large-Signal Frequency Response	V_O = 6 V_{PP}	Figure 3
Inverting Small-Signal Frequency Response	V_O = 200 mV_{PP}	Figure 4
Inverting Large-Signal Frequency Response	V_O = 2 V_{PP}	Figure 5
Inverting Large-Signal Frequency Response	V_O = 6 V_{PP}	Figure 6
Noninverting Transient Response	0.5-V Step	Figure 7
Noninverting Transient Response	2-V Step	Figure 8
Noninverting Transient Response	5-V Step	Figure 9
Inverting Transient Response	0.5-V Step	Figure 10
Inverting Transient Response	2-V Step	Figure 11
Inverting Transient Response	5-V Step	Figure 12
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Transimpedance Gain vs Frequency	C_D = 47 pF	Figure 30
Transimpedance Gain vs Frequency	C_D = 100 pF	Figure 31
Maximum/Minimum ±V_{OUT} vs R_{LOAD}		Figure 32
Slew Rate vs V_{OUT} Step		Figure 33

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At V_S = ±6 V, R_F = 0 Ω, G = 1 V/V, and R_L = 100 Ω, unless otherwise noted.

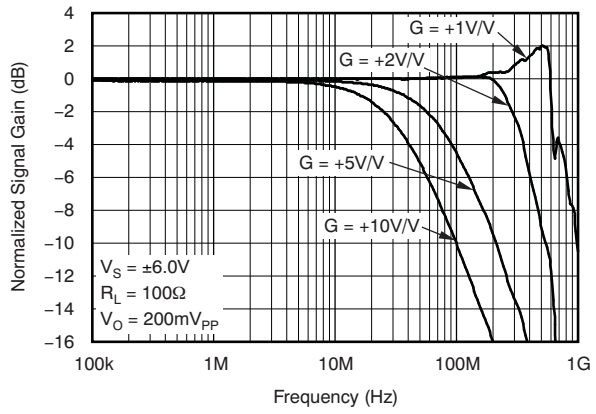


Figure 1. Noninverting Small-Signal Frequency Response (V_O = 200 mV_{PP})

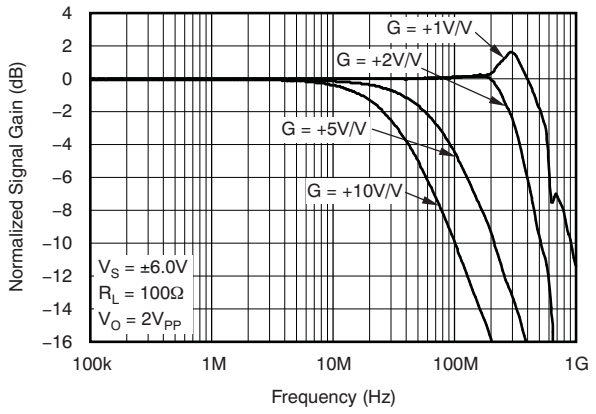


Figure 2. Noninverting Large-Signal Frequency Response (V_O = 2 V_{PP})

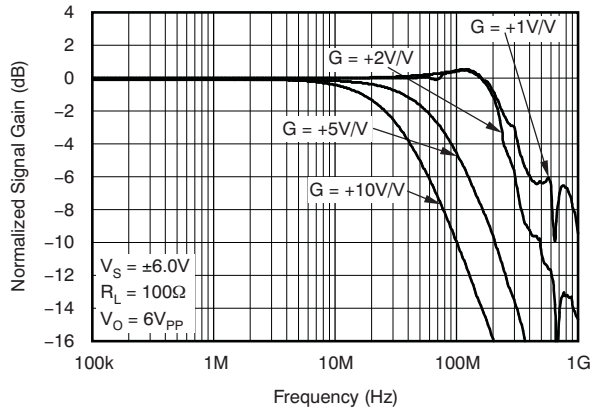


Figure 3. Noninverting Large-Signal Frequency Response (V_O = 6 V_{PP})

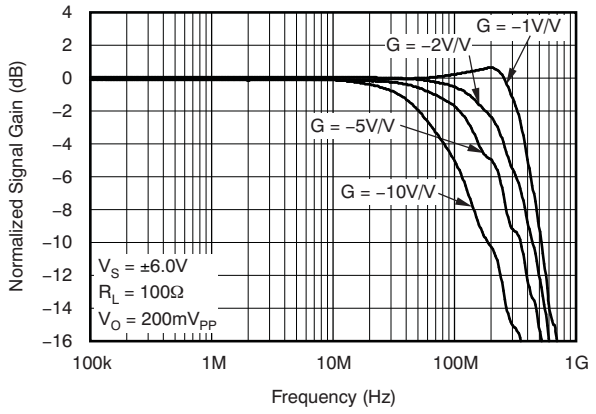


Figure 4. Inverting Small-Signal Frequency Response (V_O = 200 mV_{PP})

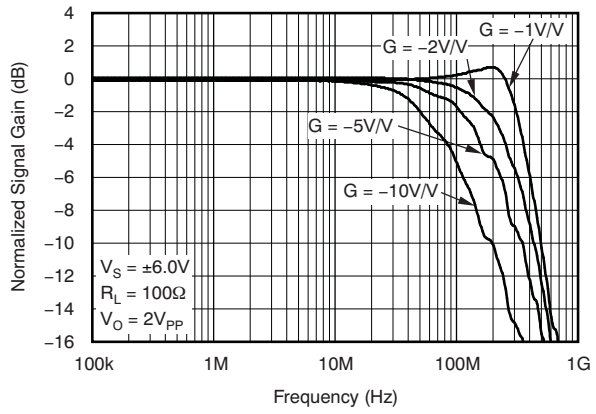


Figure 5. Inverting Large-Signal Frequency Response (V_O = 2 V_{PP})

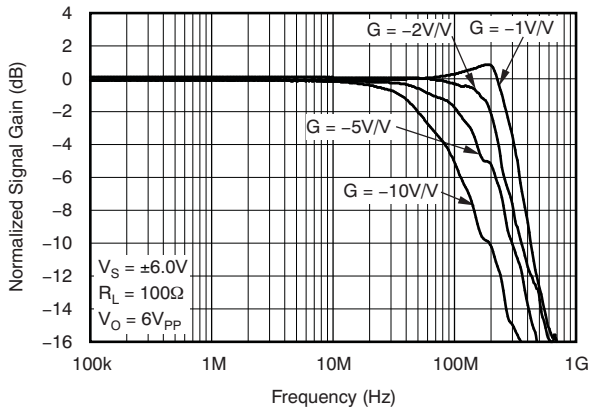


Figure 6. Inverting Large-Signal Frequency Response (V_O = 6 V_{PP})

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At V_S = ±6 V, R_F = 0 Ω, G = 1 V/V, and R_L = 100 Ω, unless otherwise noted.

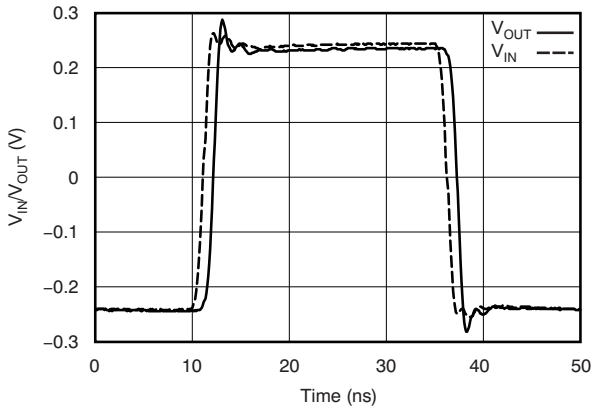


Figure 7. Noninverting Transient Response (0.5-V Step)

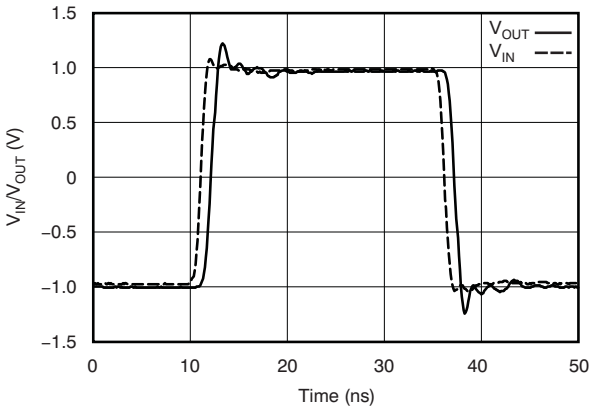


Figure 8. Noninverting Transient Response (2-V Step)

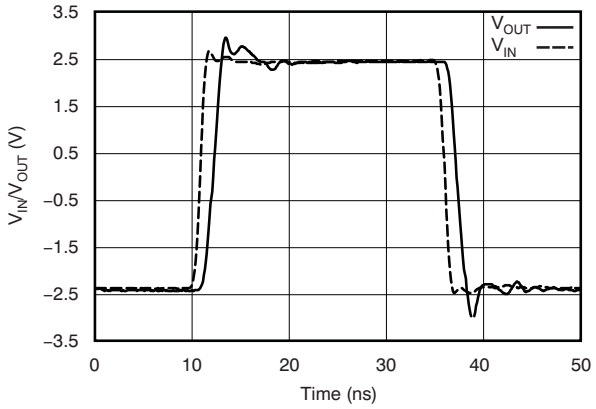


Figure 9. Noninverting Transient Response (5-V Step)

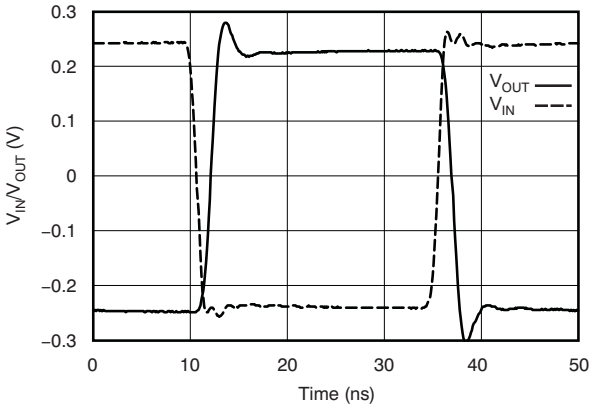


Figure 10. Inverting Transient Response (0.5-V Step)

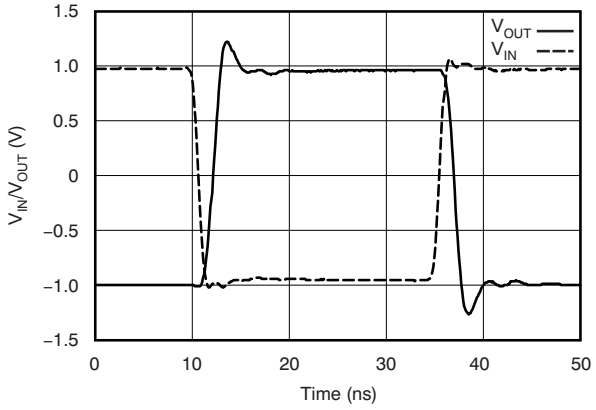


Figure 11. Inverting Transient Response (2-V Step)

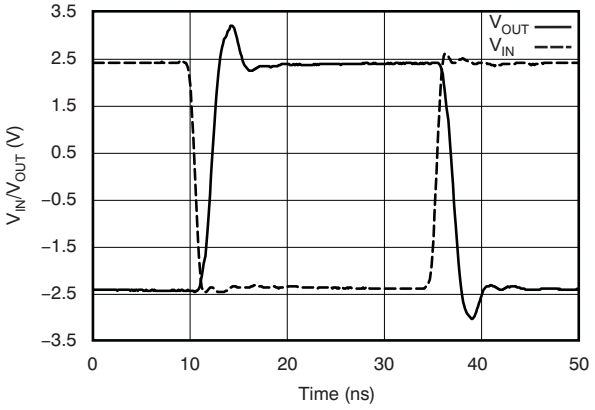


Figure 12. Inverting Transient Response (5-V Step)

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At V_S = ±6 V, R_F = 0 Ω, G = 1 V/V, and R_L = 100 Ω, unless otherwise noted.

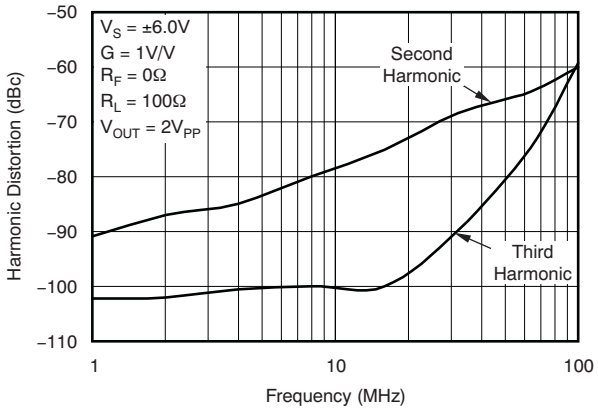


Figure 13. Harmonic Distortion vs Frequency

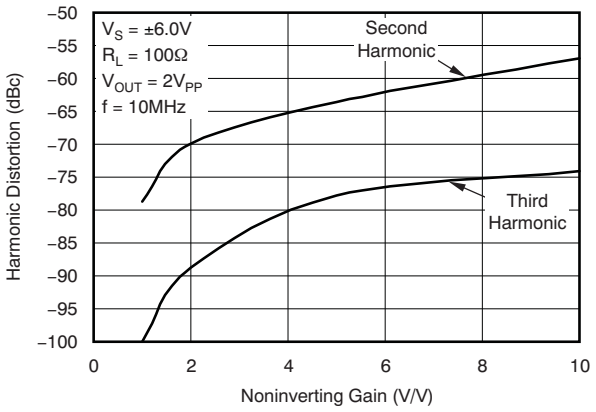


Figure 14. Harmonic Distortion vs Noninverting Gain at 10 MHz

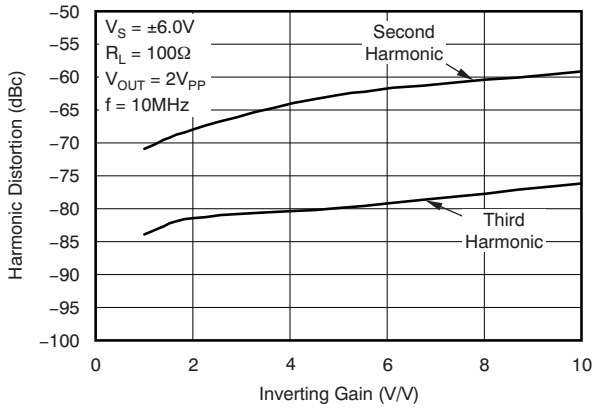


Figure 15. Harmonic Distortion vs Inverting Gain at 10 MHz

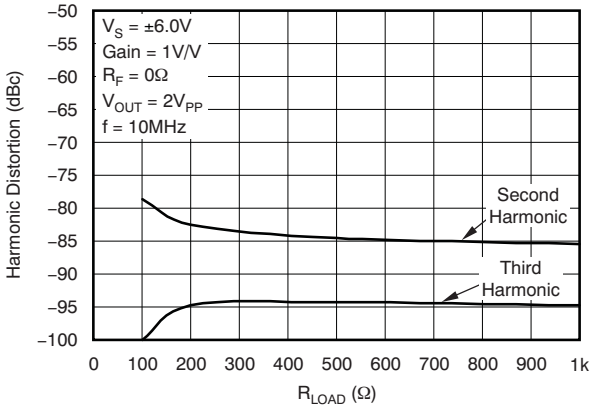


Figure 16. Harmonic Distortion vs Load Resistance at 10 MHz

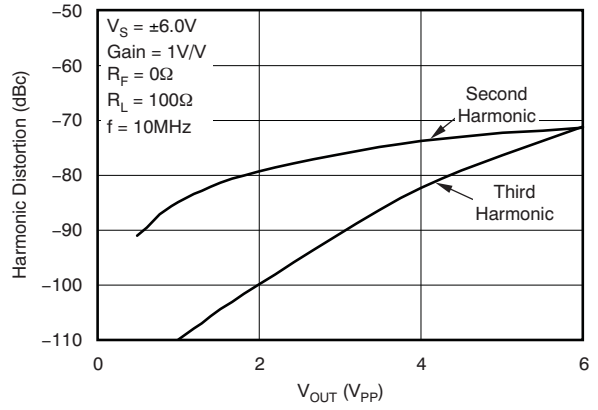


Figure 17. Harmonic Distortion vs Output Voltage

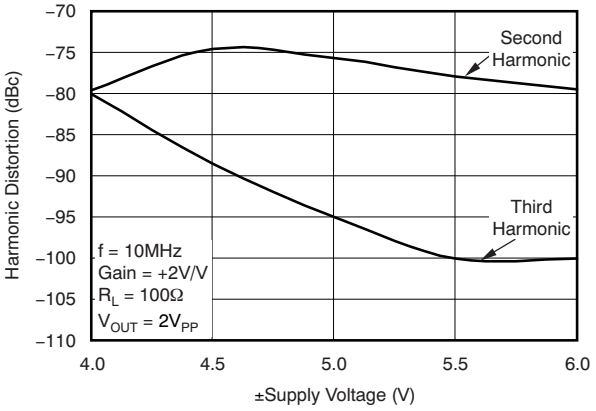


Figure 18. Harmonic Distortion vs ±Supply Voltage

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At V_S = ±6 V, R_F = 0 Ω, G = 1 V/V, and R_L = 100 Ω, unless otherwise noted.

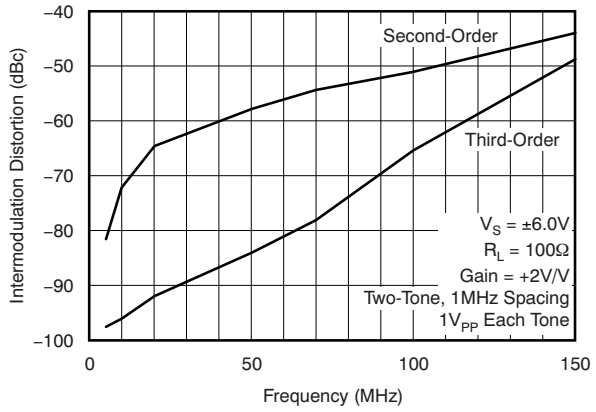


Figure 19. Two-Tone, Second- and Third-Order IMD vs Frequency

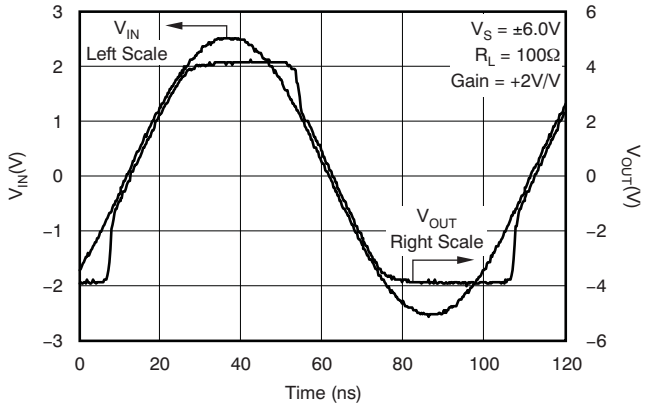


Figure 20. Overdrive Recovery (Gain = 2 V/V)

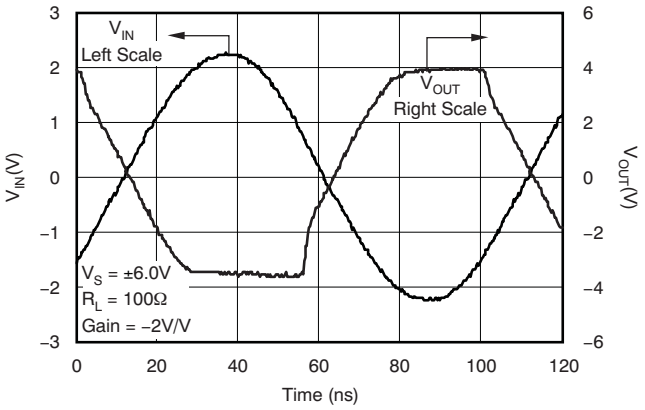


Figure 21. Overdrive Recovery (Gain = –2 V/V)

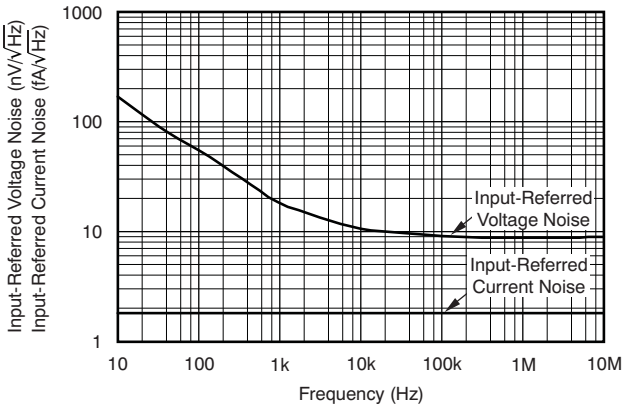


Figure 22. Input-Referred Voltage and Current Noise Density

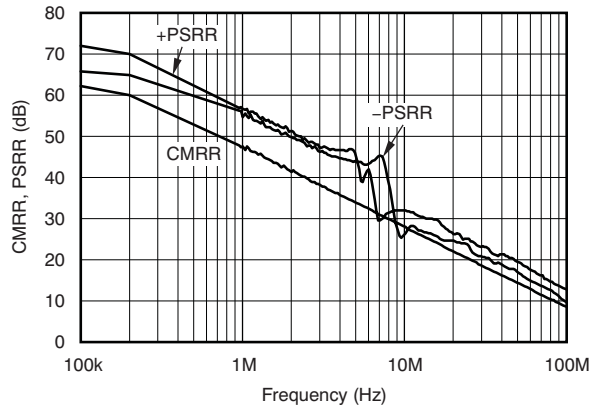


Figure 23. Common-Mode Rejection Ratio and Power-Supply Rejection Ratio vs Frequency

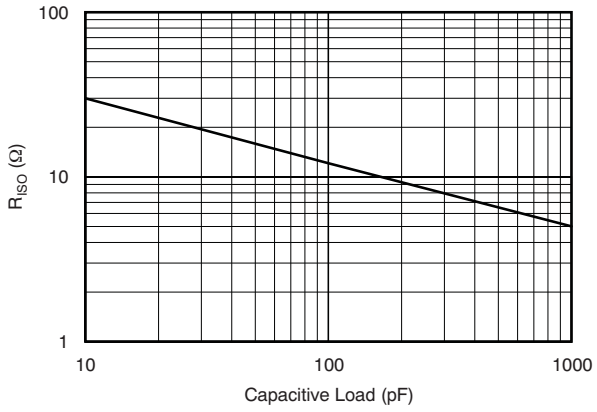


Figure 24. Recommended R_{ISO} vs Capacitive Load (R_{LOAD} = 1 kΩ)

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At V_S = ±6 V, R_F = 0 Ω, G = 1 V/V, and R_L = 100 Ω, unless otherwise noted.

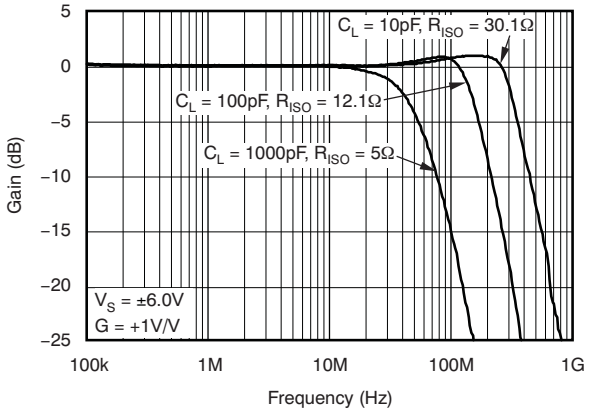


Figure 25. Frequency Response vs Capacitive Load (R_{LOAD} = 1 kΩ)

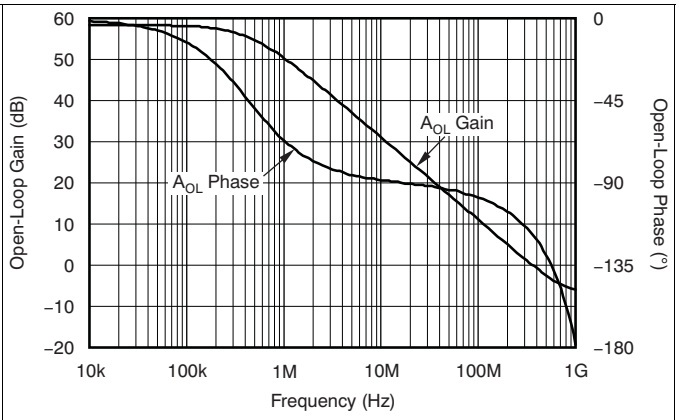


Figure 26. Open-Loop Gain and Phase

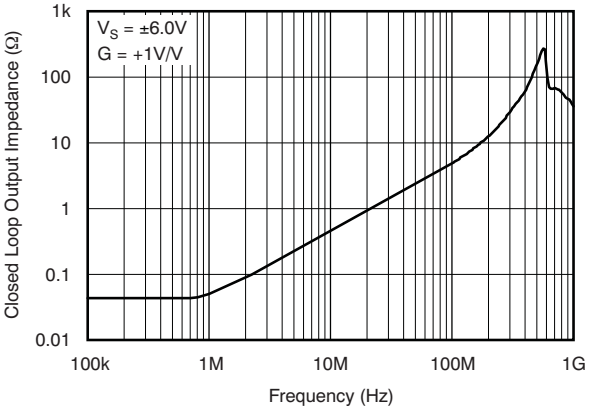


Figure 27. Closed-Loop Output Impedance vs Frequency

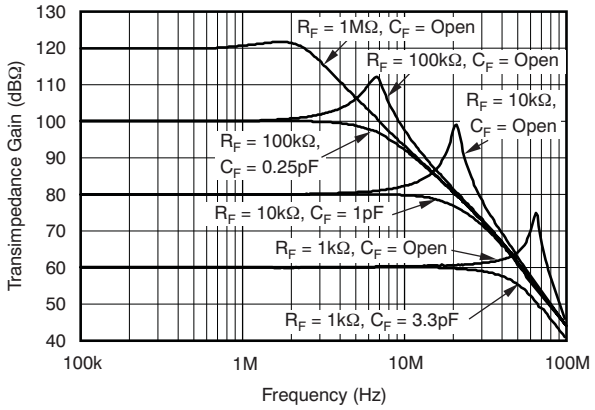


Figure 28. Transimpedance Gain vs Frequency (C_D = 10 pF)

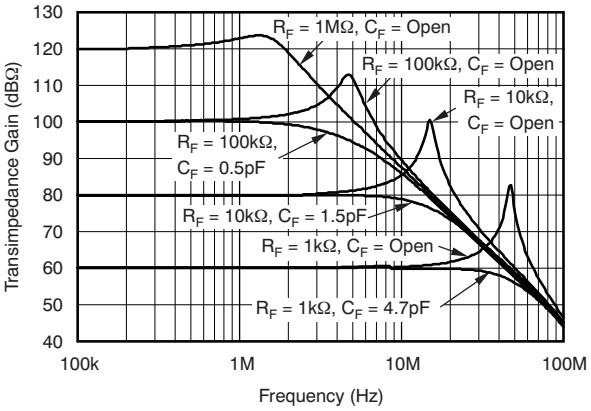


Figure 29. Transimpedance Gain vs Frequency (C_D = 22 pF)

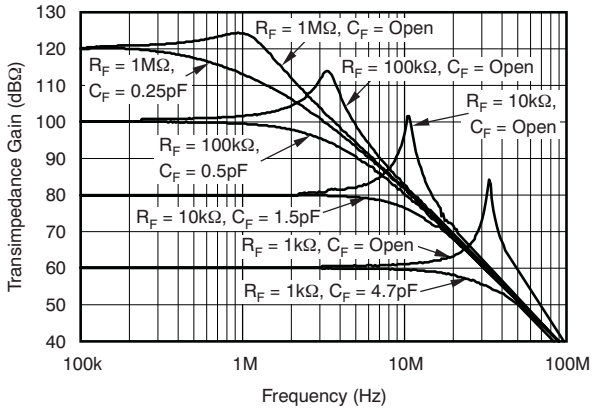


Figure 30. Transimpedance Gain vs Frequency (C_D = 47 pF)

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At V_S = ±6 V, R_F = 0 Ω, G = 1 V/V, and R_L = 100 Ω, unless otherwise noted.

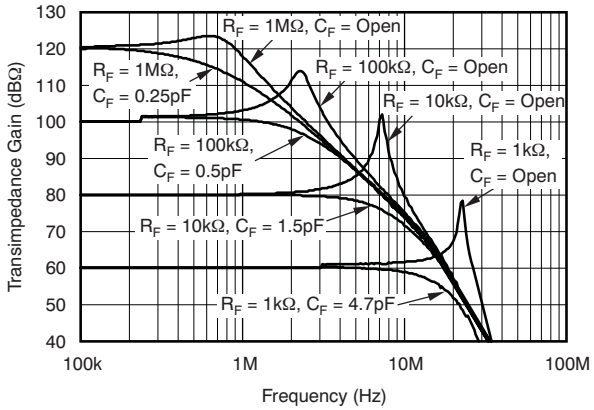


Figure 31. Transimpedance Gain vs Frequency (C_D = 100 pF)

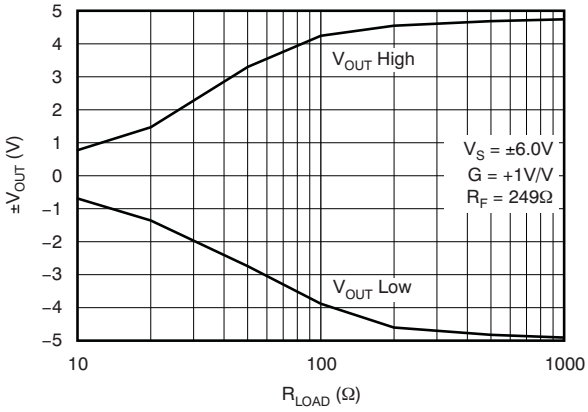


Figure 32. Maximum/Minimum ±V_{OUT} vs R_{LOAD}

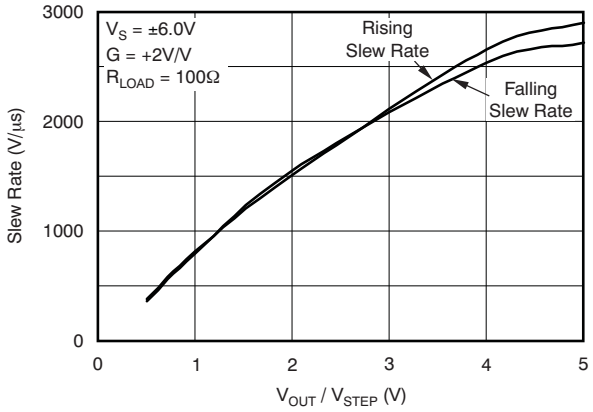


Figure 33. Slew Rate vs V_{OUT} Step

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8 Detailed Description

8.1 Overview

The OPA659 is high gain-bandwidth, voltage feedback operational amplifier featuring a low noise JFET input stage. The OPA659 is compensated to be unity gain stable. The OPA659 finds wide use in optical front-end applications and in test and measurement systems that require high input impedance.

8.2 Feature Description

8.2.1 Input and ESD Protection

The OPA659 is built using a very high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the *Absolute Maximum Ratings* table. All device pins are protected with internal ESD protection diodes to the power supplies, as Figure 34 shows.

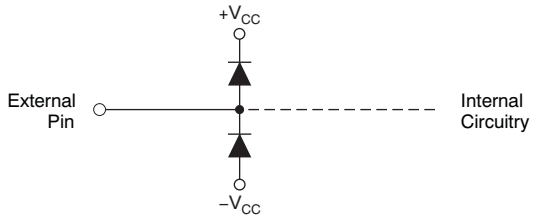


Figure 34. Internal ESD Protection

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30-mA continuous current. Where higher currents are possible (for example, in systems with ±12-V supply parts driving into the OPA659), current limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible because high values degrade both noise performance and frequency response.

8.3 Device Functional Modes

8.3.1 Split-Supply Operation (±3.5 V to ±6.5 V)

To facilitate testing with common lab equipment, the OPA659 may be configured to allow for split-supply operation. This configuration eases lab testing because the mid-point between the power rails is ground, and most signal generators, network analyzers, oscilloscopes, spectrum analyzers and other lab equipment reference their inputs and outputs to ground. Figure 36 and Figure 37 show the OPA659 configured in a simple noninverting and inverting configuration respectively with ±6-V supplies. The input and output will swing symmetrically around ground. Due to its ease of use, split-supply operation is preferred in systems where signals swing around ground, but it requires generation of two supply rails.

8.3.2 Single-Supply Operation (7 V to 13 V)

Many newer systems use single power supply to improve efficiency and reduce the cost of the extra power supply. The OPA659 is designed for use with split-supply configuration; however, it can be used with a single-supply with no change in performance, as long as the input and output are biased within the linear operation of the device. To change the circuit from split supply to single supply, level shift all the voltages by 1/2 the difference between the power supply rails. An additional advantage of configuring an amplifier for single-supply operation is that the effects of –PSRR will be minimized because the low supply rail has been grounded.

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9 Application Information

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Wideband, Noninverting Operation

The OPA659 is a very broadband, unity-gain stable, voltage-feedback amplifier with a high impedance JFET-input stage. Its very high gain bandwidth product (GBP) of 350 MHz can be used to either deliver high signal bandwidths for low-gain buffers, or to deliver broadband, low-noise, transimpedance bandwidth to photodiode-detector applications. The OPA659 is designed to provide very low distortion and accurate pulse response with low overshoot and ringing. To achieve the full performance of the OPA659, careful attention to printed-circuit board (PCB) layout and component selection are required, as discussed in the remaining sections of this data sheet.

Figure 35 shows the noninverting gain of +1 circuit; Figure 36 shows the more general circuit used for other noninverting gains. These circuits are used as the basis for most of the noninverting gain *Typical Characteristics* graphs. Most of the graphs were characterized using signal sources with 50-Ω driving impedance, and with measurement equipment presenting a 50-Ω load impedance. In Figure 35, the shunt resistor R_T at V_{IN} should be set to 50 Ω to match the source impedance of the test generator and cable, while the series output resistor, R_{OUT}, at V_{OUT} should also be set to 50 Ω to provide matching impedance for the measurement equipment load and cable. Generally, data sheet voltage swing specifications are measured at the output pin, V_{OUT}, in Figure 35 and Figure 36.

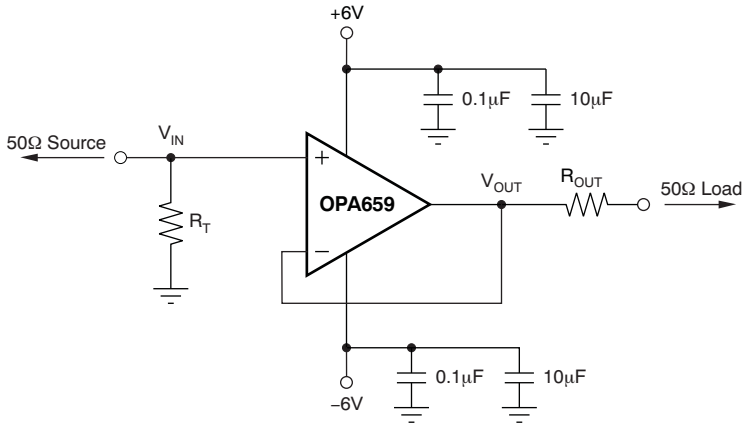


Figure 35. Noninverting Gain of +1 Test Circuit

Voltage-feedback op amps can use a wide range of resistor values to set the gain. To retain a controlled frequency response for the noninverting voltage amplifier of Figure 36, the parallel combination of R_F || R_G should always be less than 200 Ω. In the noninverting configuration, the parallel combination of R_F || R_G forms a pole with the parasitic input and board layout capacitance at the inverting input of the OPA659. For best performance, this pole should be at a frequency greater than the closed-loop bandwidth for the OPA659. For this reason, TI recommends a direct short from the output to the inverting input for the unity-gain follower application. Table 2 lists several recommended resistor values for noninverting gains with a 50-Ω input and output match.

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Application Information (continued)

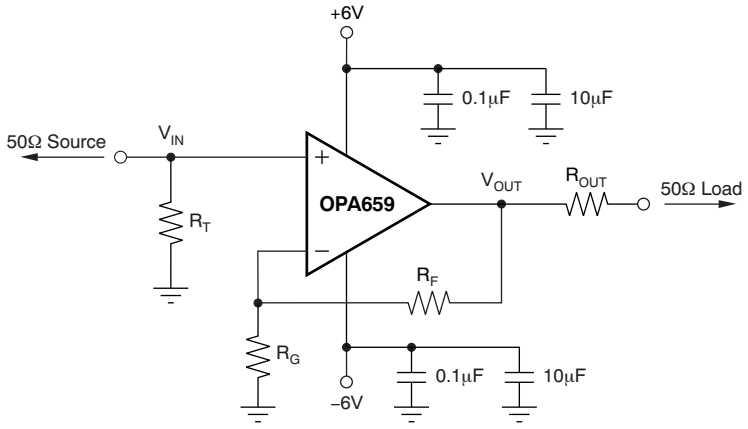


Figure 36. General Noninverting Test Circuit

Table 2. Resistor Values for Noninverting Gains With 50-Ω Input/Output Match

NONINVERTING GAIN	R_F	R_G	R_T	R_{OUT}
+1	0	Open	49.9	49.9
+2	249	249	49.9	49.9
+5	249	61.9	49.9	49.9
+10	249	27.4	49.9	49.9

9.1.2 Wideband, Inverting Gain Operation

The circuit of Figure 37 shows the inverting gain test circuit used for most of the inverting *Typical Characteristics* graphs. As with the noninverting applications, most of the curves were characterized using signal sources with 50-Ω driving impedance, and with measurement equipment that presents a 50-Ω load impedance. In Figure 37, the shunt resistor R_T at V_{IN} should be set so the parallel combination of the shunt resistor and R_G equals 50 Ω to match the source impedance of the test generator and cable, while the series output resistor R_{OUT} at V_{OUT} should also be set to 50 Ω to provide matching impedance for the measurement equipment load and cable. Generally, data sheet voltage swing specifications are measured at the output pin, V_{OUT}, in Figure 37.

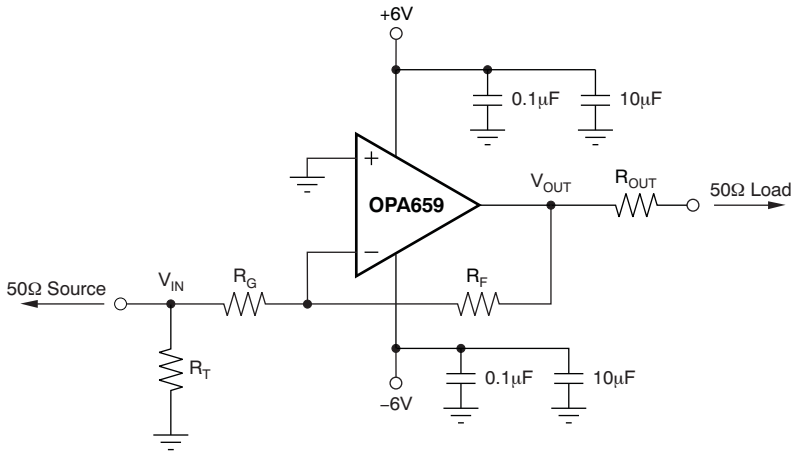


Figure 37. General Inverting Test Circuit

The inverting circuit can also use a wide range of resistor values to set the gain; Table 3 lists several recommended resistor values for inverting gains with a 50-Ω input and output match.

Table 3. Resistor Values For Inverting Gains With 50-Ω Input/Output Match

INVERTING GAIN	R_F	R_G	R_T	R_{OUT}
–1	249	249	61.9	49.9
–2	249	124	84.5	49.9
–5	249	49.9	Open	49.9
–10	499	49.9	Open	49.9

Figure 37 shows the noninverting input tied directly to ground. Often, a bias current-cancelling resistor to ground is included here to nullify the DC errors caused by input bias current effects. For a JFET input op amp such as the OPA659, the input bias currents are so low that dc errors caused by input bias currents are negligible. Thus, TI does not recommend a bias current-cancelling resistor at the noninverting input.

9.1.3 Operating Suggestions

9.1.3.1 Setting Resistor Values To Minimize Noise

The OPA659 provides a very low input noise voltage. To take full advantage of this low input noise, designers must pay careful attention to other possible noise contributors. Figure 38 shows the op amp noise analysis model with all the noise terms included. In this model, all the noise terms are taken to be noise voltage or current density terms in either nV/√Hz or pA/√Hz.

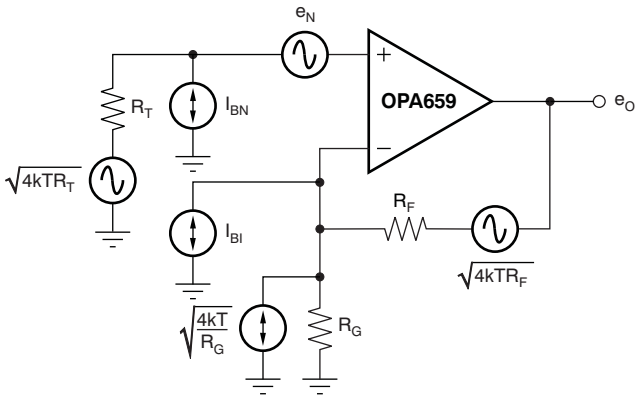


Figure 38. Op Amp Noise Analysis Model

The total output spot noise voltage can be computed as the square root of the squared contributing terms to the output noise voltage. This computation adds all the contributing noise powers at the output by superposition, then takes the square root to arrive at a spot noise voltage. Equation 1 shows the general form for this output noise voltage using the terms shown in Figure 38.

$$e_O = \sqrt{\left[4kTR_T + (I_{BN}R_T)^2 + e_N^2\right]\left(1 + \frac{R_F}{R_G}\right)^2 + (I_{BI}R_F)^2 + 4kTR_F\left(1 + \frac{R_F}{R_G}\right)} \quad (1)$$

Dividing this expression by the noise gain ($G_N = 1 + R_F/R_G$) gives the equivalent input-referred spot noise voltage at the noninverting input, as Equation 2 shows.

$$e_{NI} = \sqrt{4kTR_T + (I_{BN}R_T)^2 + e_N^2 + \left(\frac{I_{BI}R_F}{\text{Noise Gain}}\right)^2 + \left(\frac{4kTR_F}{\text{Noise Gain}}\right)} \quad (2)$$

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Putting high resistor values into Equation 2 can quickly dominate the total equivalent input-referred noise. A source impedance on the noninverting input of 5 kΩ adds a Johnson voltage noise term equal to that of the amplifier alone (8.9 nV/$\sqrt{Hz}$). While the JFET input of the OPA659 is ideal for high source impedance applications in the noninverting configuration of Figure 35 or Figure 36, both the overall bandwidth and noise are limited by high source impedances.

9.1.3.2 Frequency Response Control

Voltage-feedback op amps such as the OPA659 exhibit decreasing signal bandwidth as the signal gain increases. In theory, this relationship is described by the gain bandwidth product (GBP) shown in the *Electrical Characteristics.* Ideally, dividing the GBP by the noninverting signal gain (also called the Noise Gain, or NG) can predict the closed-loop bandwidth. In practice, this guideline is valid only when the phase margin approaches 90 degrees, as it does in high gain configurations. At low gains (with increased feedback factors), most high-speed amplifiers exhibit a more complex response with lower phase margins. The OPA659 is compensated to give a maximally-flat frequency response at a noninverting gain of +1 (see Figure 35). This compensation results in a typical gain of +1 bandwidth of 650 MHz, far exceeding that predicted by dividing the 350-MHz GBP by 1. Increasing the gain causes the phase margin to approach 90° and the bandwidth to more closely approach the predicted value of (GBP/NG). At a gain of +10, the OPA659 shows the 35-MHz bandwidth predicted using the simple formula and the typical GBP of 350 MHz. Unity-gain stable op amps such as the OPA659 can also be band-limited in gains other than +1 by placing a capacitor across the feedback resistor. For the noninverting configuration of Figure 36, a capacitor across the feedback resistor decreases the gain with frequency down to a gain of +1. For instance, to band-limit a gain of +2 design to 20 MHz, a 32-pF capacitor can be placed in parallel with the 249-Ω feedback resistor. This configuration, however, only decreases the gain from 2 to 1. Using a feedback capacitor to limit the signal bandwidth is more effective in the inverting configuration of Figure 37. Adding that same capacitance to the feedback of Figure 37 sets a pole in the signal frequency response at 20 MHz, but in this case it continues to attenuate the signal gain to less than 1. Note, however, that the noise gain of the circuit is only reduced to a gain of 1 with the addition of the feedback capacitor.

9.1.3.3 Driving Capacitive Loads

One of the most demanding, and yet very common, load conditions for an op amp is capacitive loading. The OPA659 is very robust, but care should be taken with light loading scenarios so that output capacitance does not decrease stability and increase closed-loop frequency response peaking when a capacitive load is placed directly on the output pin. When the amplifier open-loop output resistance is considered, this capacitive load introduces an additional pole in the signal path that can decrease the phase margin. Several external solutions to this problem have been suggested. When the primary considerations are frequency response flatness, pulse response fidelity, and/or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor, R_{ISO}, between the amplifier output and the capacitive load. In effect, this resistor isolates the phase shift from the loop gain of the amplifier, thus increasing the phase margin and improving stability. The *Typical Characteristics* show the recommended R_{ISO} versus capacitive load and the resulting frequency response with a 1-kΩ load (see Figure 24). Note that larger R_{ISO} values are required for lower capacitive loading. In this case, a design target of a maximally-flat frequency response was used. Lower values of R_{ISO} may be used if some peaking can be tolerated. Also, operating at higher gains (instead of the +1 gain used in the *Typical Characteristics*) requires lower values of R_{ISO} for a minimally-peaked frequency response. Parasitic capacitive loads greater than 2pF can begin to degrade the performance of the OPA659. Moreover, long PCB traces, unmatched cables, and connections to multiple devices can easily cause this value to be exceeded. Always consider this effect carefully, and add the recommended series resistor as close as possible to the OPA659 output pin (see the *Layout* section).

With heavier loads (for example, the 100-Ω load presented in the test circuits and used for testing typical characteristic performance), the OPA659 is very robust; R_{ISO} can be as low as 10 Ω with capacitive loads less than 5 pF and continue to show a flat frequency response.

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9.1.3.4 Distortion Performance

The OPA659 is capable of delivering a low distortion signal at high frequencies over a wide range of gains. The distortion plots in the *Typical Characteristics* show the typical distortion under a wide variety of conditions. Generally, until the fundamental signal reaches very high frequencies or powers, the second harmonic dominates the distortion with a negligible third harmonic component. Focusing then on the second harmonic, increasing the load impedance improves distortion directly. Remember that the total load includes the feedback network: in the noninverting configuration, this network is the sum of $R_F + R_G$, while in the inverting configuration the network is only R_F (see Figure 36). Increasing the output voltage swing directly increases harmonic distortion. A 6dB increase in output swing generally increases the second harmonic by 12 dB and the third harmonic by 18 dB. Increasing the signal gain also increases the second-harmonic distortion. Again, a 6-dB increase in gain increases the second and third harmonics by about 6 dB, even with a constant output power and frequency. Finally, the distortion increases as the fundamental frequency increases because of the rolloff in the loop gain with frequency. Conversely, the distortion improves going to lower frequencies, down to the dominant open-loop pole at approximately 300 kHz.

Note that power-supply decoupling is critical for harmonic distortion performance. In particular, for optimal second-harmonic performance, the power-supply high-frequency 0.1-µF decoupling capacitors to the positive and negative supply pins should be brought to a single point ground located away from the input pins.

The OPA659 has an extremely low third-order harmonic distortion. This characteristic also shows up in the two-tone, third-order intermodulation spurious (IMD3) response curves (see Figure 19). The third-order spurious levels are extremely low (less than –100 dBc) at low output power levels and frequencies below 10 MHz. The output stage continues to hold these levels low even as the fundamental power reaches higher levels. As with most op amps, the spurious intermodulation powers do not increase as predicted by a traditional intercept model. As the fundamental power level increases, the dynamic range does not decrease significantly. For two tones centered at 10 MHz, with –2 dBm/tone into a matched 50-Ω load (that is, 0.5 V_{PP} for each tone at the load, which requires 2 V_{PP} for the overall two-tone envelope at the output pin), the *Typical Characteristics* show a 96-dBc difference between the test tones and the third-order intermodulation spurious levels. This exceptional performance improves further when operating at lower frequencies and/or higher load impedances.

9.2 Typical Application

The high GBP and low input voltage and current noise for the OPA659 make it an ideal wideband, transimpedance amplifier for low to moderate transimpedance gains. Higher transimpedance gains (above 100 kΩ) can benefit from the low input noise current of a JFET input op amp such as the OPA659. Designs that require high bandwidth from a large area detector can benefit from the low input voltage noise for the OPA659.

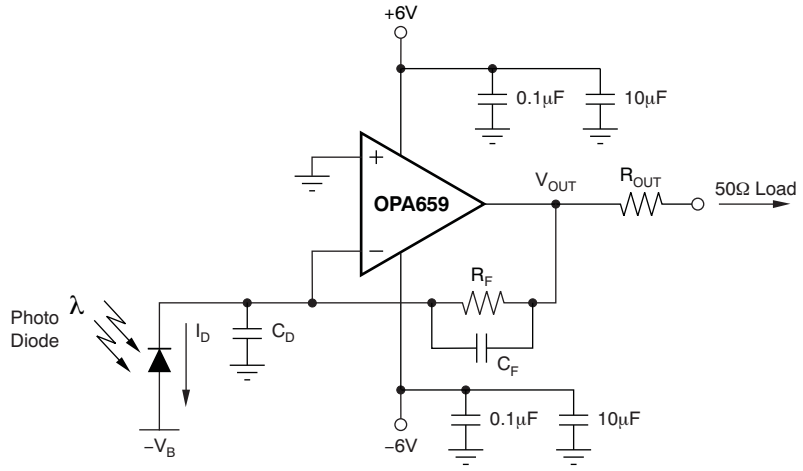


Figure 39. Wideband, Low-Noise, Transimpedance Amplifier (TIA)

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Typical Application (continued)

9.2.1 Design Requirements

Design a high-gain transimpedance amplifier with the specifications shown in Table 4.

Table 4. Design Parameters

PARAMETER	VALUE
Closed loop bandwidth (MHz)	7.5 MHz
Transimpedance gain	10 KΩ
Photodiode capacitance	100 pF

9.2.2 Detailed Design Procedure

The input voltage noise of a transimpedance amplifier is peaked up over frequency by the diode source capacitance, and in many cases, may become the limiting factor to input sensitivity. The key elements to the design are the expected diode capacitance (C_D) with the reverse bias voltage ($-V_B$) applied, the desired transimpedance gain, R_F, and the GBP for the OPA659 (350 MHz). Figure 39 shows a general transimpedance amplifier circuit, or TIA, using the OPA659. Given the source diode capacitance plus parasitic input capacitance for the OPA659, the transimpedance gain, and known GBP, the feedback capacitor value, C_F, may be calculated to avoid excessive peaking in the frequency response.

To achieve a maximally flat second-order Butterworth frequency response, the feedback pole should be set to:

$$\frac{1}{2\pi R_F C_F} = \sqrt{\frac{GBP}{4\pi R_F C_D}} \tag{3}$$

For example, adding the common mode and differential mode input capacitance (0.7 + 2.8 = 3.5)pF to the diode source with the 20-pF capacitance, and targeting a 100-kΩ transimpedance gain using the 350-MHz GBP for the OPA659, requires a feedback pole set to 3.44 MHz. This pole in turn requires a total feedback capacitance of 0.46 pF. Typical surface mount resistors have a parasitic capacitance of 0.2 pF, leaving the required 0.26 pF value to achieve the required feedback pole. This calculation gives an approximate 4.9 MHz, –3-dB bandwidth computed by:

$$f_{-3dB} = \sqrt{\frac{GBP}{2\pi R_F C_D}} \tag{4}$$

Table 5 lists the calculated component values and –3-dB bandwidths for various TIA gains and diode capacitance.

Table 5. OPA659 TIA Component Values and Bandwidth for Various Diode Capacitance and Gains

C_D	R_F	C_F	f_{-3dB}
C_{DIODE} = 10 pF			
13.5 pF	1 kΩ	3.50 pF	64.24 MHz
13.5 pF	10 kΩ	1.11 pF	20.31 MHz
13.5 pF	100 kΩ	0.35 pF	6.42 MHz
13.5 pF	1 MΩ	0.11 pF	2.03 MHz
C_{DIODE} = 20 pF			
23.5 pF	1 kΩ	4.62 pF	48.69 MHz
23.5 pF	10 kΩ	1.46 pF	15.40 MHz
23.5 pF	100 kΩ	0.46 pF	4.87 MHz
23.5 pF	1 MΩ	0.15 pF	1.54 MHz
C_{DIODE} = 50 pF			
53.5 pF	1 kΩ	6.98 pF	32.27 MHz
53.5 pF	10 kΩ	2.21 pF	10.20 MHz
53.5 pF	100 kΩ	0.70 pF	3.23 MHz
53.5 pF	1 MΩ	0.22 pF	1.02 MHz

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Table 5. OPA659 TIA Component Values and Bandwidth for Various Diode Capacitance and Gains (continued)

C_D	R_F	C_F	f_{-3dB}
C_{DIODE} = 100 pF			
103.5 pF	1kΩ	9.70pF	23.20MHz
103.5 pF	10kΩ	3.07pF	7.34MHz
103.5 pF	100kΩ	0.97pF	2.32MHz
103.5 pF	1MΩ	0.31pF	0.73MHz

9.2.3 Application Curves

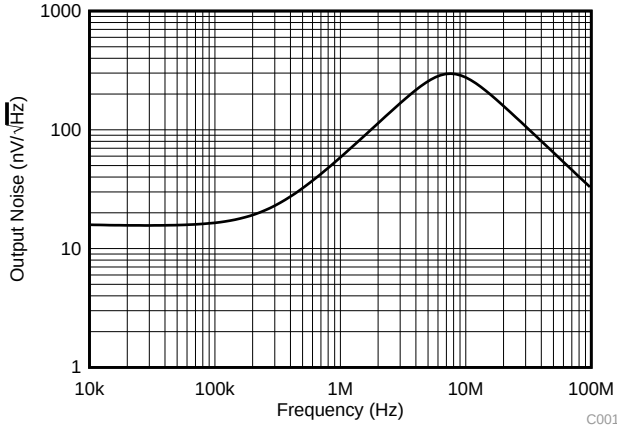


Figure 40. Simulated Total Output Noise

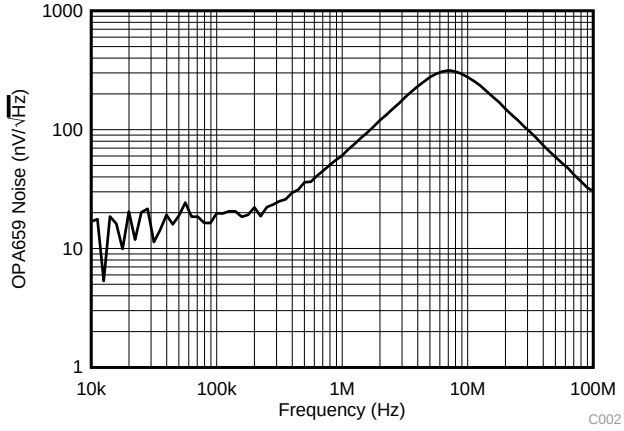


Figure 41. Measured Total Output Noise

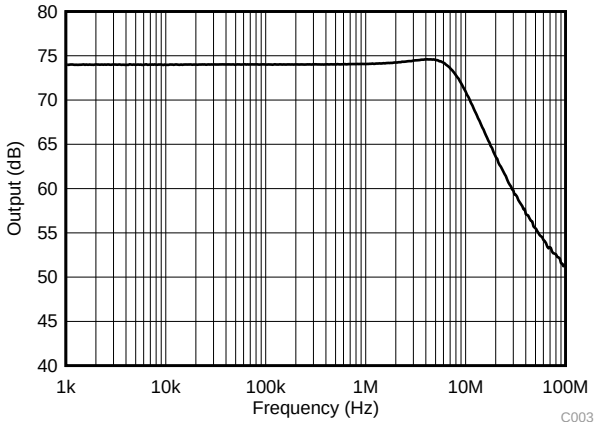


Figure 42. Measured Transimpedance Bandwidth

10 Power Supply Recommendations

The OPA659 is intended for operation on ±6-V supplies. Single-supply operation is allowed with minimal change from the stated specifications and performance from a single supply of 7 V to 13 V maximum. The limit to lower supply voltage operation is the useable input voltage range for the JFET-input stage. Operating from a single supply can have numerous advantages. With the negative supply at ground, the DC errors due to the –PSRR term can be minimized. Typically, AC performance improves slightly at 13-V operation with minimal increase in supply current.

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11 Layout

11.1 Layout Guidelines

Achieving optimum performance with a high-frequency amplifier such as the OPA659 requires careful attention to PCB layout parasitics and external component types. Recommendations that can optimize device performance include the following

1. **Minimize parasitic capacitance** to any AC ground for all of the signal input/output (I/O) pins. Parasitic capacitance on the output and inverting input pins can cause instability: on the noninverting input, it can react with the source impedance to cause unintentional band-limiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.
2. **Minimize the distance** (less than 0.25 inches, or 6.35 mm) from the power-supply pins to the high-frequency, 0.1-µF decoupling capacitors. At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Use a single point ground, located away from the input pins, for the positive and negative supply high-frequency, 0.1-µF decoupling capacitors. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections should always be decoupled with these capacitors. Larger (2.2 µF to 10 µF) decoupling capacitors, effective at lower frequencies, should also be used on the supply pins. These larger capacitors may be placed somewhat farther from the device and may be shared among several devices in the same area of the PCB.
3. **Careful selection and placement of external components preserves the high-frequency performance of the OPA659.** Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal film and carbon composition, axially-leaded resistors can also provide good high-frequency performance. Again, keep the leads and PCB trace length as short as possible. Never use wirewound-type resistors in a high-frequency application. The inverting input pin is the most sensitive to parasitic capacitance; consequently, always position the feedback resistor as close to the negative input as possible. The output is also sensitive to parasitic capacitance; therefore, position a series output resistor (in this case, R_{ISO}) as close to the output pin as possible. Other network components, such as noninverting input termination resistors, should also be placed close to the package. Even with a low parasitic capacitance, excessively high resistor values can create significant time constants that can degrade device performance. Good axial metal film or surface-mount resistors have approximately 0.2 pF in shunt with the resistor. For resistor values greater than 1.5 kΩ, this parasitic capacitance can add a pole and/or zero below 500 MHz that can affect circuit operation. Keep resistor values as low as possible, consistent with load driving considerations. TI recommends keeping $R_F \parallel R_G$ less than 250 Ω. This low value ensures that the resistor noise terms remain low, and minimizes the effects of the parasitic capacitance. Transimpedance applications (for example, see Figure 39) can use the feedback resistor required by the application as long as the feedback compensation capacitor is set given consideration to all parasitic capacitance terms on the inverting node.
4. **Connections to other wideband devices** on the board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50 mils to 100 mils, or 1.27 cm to 2.54 cm) should be used. Estimate the total capacitive load and set R_{ISO} from Figure 24. Low parasitic capacitive loads (less than 5 pF) may not need an R_{ISO} because the OPA659 is nominally compensated to operate with a 2-pF parasitic load. Higher parasitic capacitive loads without an R_{ISO} are allowed as the signal gain increases (increasing the unloaded phase margin). If a long trace is required, and the 6-dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50-Ω environment is normally not necessary onboard, and in fact a higher impedance environment improves distortion as shown in the distortion versus load plots. With a characteristic board trace impedance defined based on board material and trace dimensions, a matching series resistor into the trace from the output of the OPA659 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance is the parallel combination of the shunt resistor and the input impedance of the destination device: this total effective impedance should be set to match the trace impedance. If the 6-dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case, and set the series resistor value as shown in Figure 24. This configuration does not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there will be some signal

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Layout Guidelines (continued)

attenuation as a result of the voltage divider formed by the series output into the terminating impedance.

5. **Socketing a high-speed part such as the OPA659 is not recommended.** The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network that can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA659 directly onto the board.
6. **The thermal slug on bottom of OPA659 DRB package must be tied to the most negative supply.** The DRB package is a thermally-enhanced package. Best results are obtained by soldering the exposed metal tab on the bottom of the OPA659 DRB directly to a metal plane on the PCB that is connected to the most negative supply voltage of the operational amplifier. For general layout guidelines, refer to the EVM layout in the *Schematic and PCB Layout* section.

11.2 Layout Example

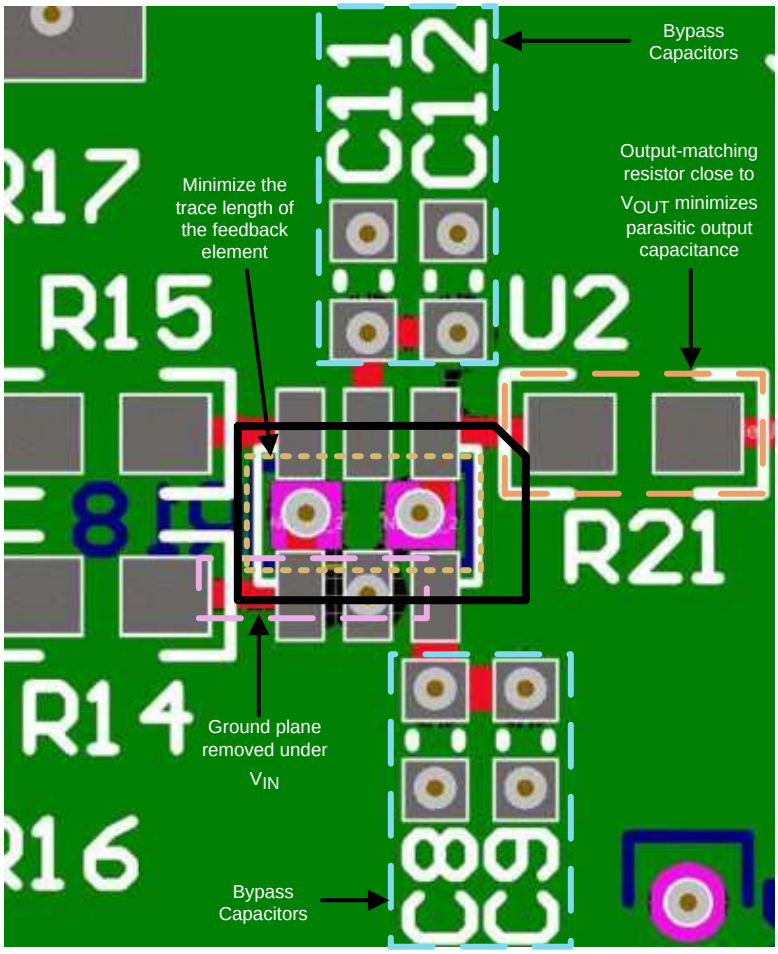


Figure 43. Layout Recommendation

11.3 Thermal Pad Information

The DRB package includes an exposed thermal pad for increased thermal performance. When using this package, TI recommends to distribute the negative supply as a power plane, and tie the thermal pad to this supply with multiple vias for proper power dissipation. For proper operation, the thermal pad must be tied to the most negative supply voltage. TI recommends using five evenly-spaced vias under the device as shown in the EVM layer views (see Figure 45). For more general data and detailed information about the exposed thermal pad, go to www.ti.com/thermal.

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11.4 Schematic and PCB Layout

Figure 44 is the OPA659EVM schematic. Layers 1 through 4 of the PCB are shown in Figure 45. TI recommends following the layout of the external components near to the amplifier, ground plane construction, and power routing as closely as possible.

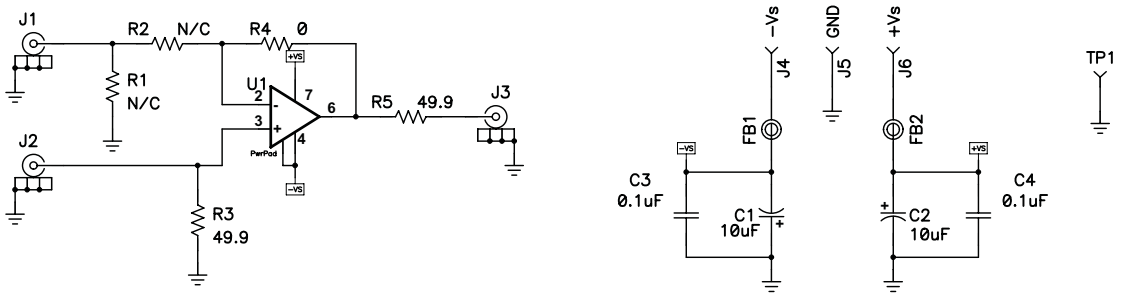


Figure 44. OPA659EVM Schematic

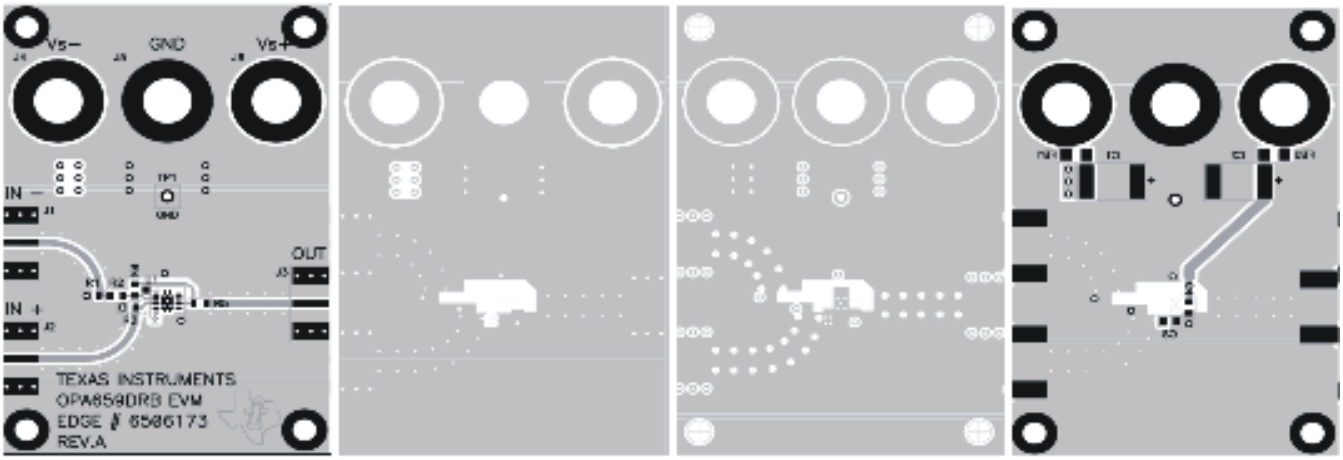


Figure 45. OPA659EVM Layers 1 Through 4

11.5 Evaluation Module

11.5.1 Bill of Materials

Table 6 lists the bill of material for the OPA659EVM as supplied from TI.

Table 6. OPA659EVM Parts List

ITEM	DESCRIPTION	SMD SIZE	REFERENCE DESIGNATOR	QUANTITY	MANUFACTURER PART NUMBER
1	Cap, 10 µF, Tantalum, 10%, 35V	D	C1, C2	2	(AVX) TAJ106K035R
2	Cap, 0.1 µF, Ceramic, X7R, 16V	0603	C3, C4	2	(AVX) 0603YC104KAT2A
3	Open	0603	R1, R2	2	
4	Resistor, 0 Ω	0603	R4	1	(ROHM) MCR03EZPJ000
5	Resistor, 49.9 Ω, 1/10 W, 1%	0603	R3, R5	2	(ROHM) MCR03EZPFX49R9
6	Jack, Banana Receptance, 0.25 inch diameter hole		J4, J5, J8	3	(SPC) 813
7	Connector, Edge, SMA PCB Jack		J1, J2, J3	3	(JOHNSON) 142-0701-801
8	Test Point, Black		TP1	1	(KEYSTONE) 5001
9	IC, OPA659		U1	1	(TI) OPA659DRB
10	Standoff, 4-40 HEX, 0.625 inch length			4	(KEYSTONE) 1808
11	Screw, Phillips, 4-40, 0.25 inch			4	SHR-0440-016-SN
12	Board, Printed Circuit			1	(TI) EDGE# 6506173
13	Bead, Ferrite, 3 A, 80 Ω	1206	FB1, FB2	2	(STEWARD) HI1206N800R-00

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12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

For thermal information go to www.ti.com/thermal.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA659IDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BZX
OPA659IDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BZX
OPA659IDBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BZX
OPA659IDBVT.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BZX
OPA659IDRBR	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OBFI
OPA659IDRBR.A	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OBFI
OPA659IDRBT	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OBFI
OPA659IDRBT.A	Active	Production	SON (DRB) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OBFI

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

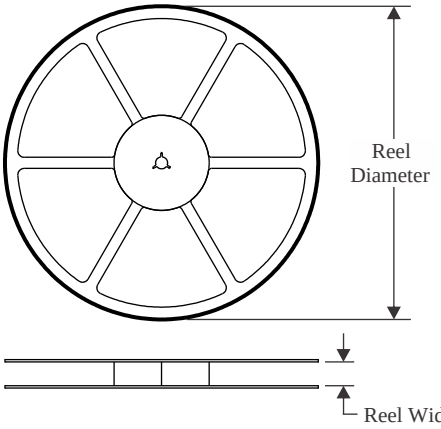
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

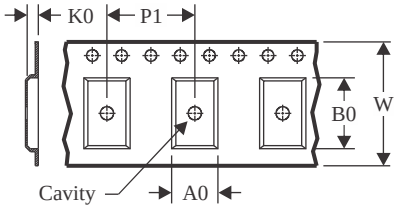
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

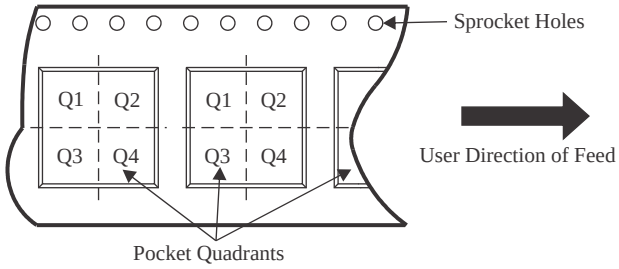


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

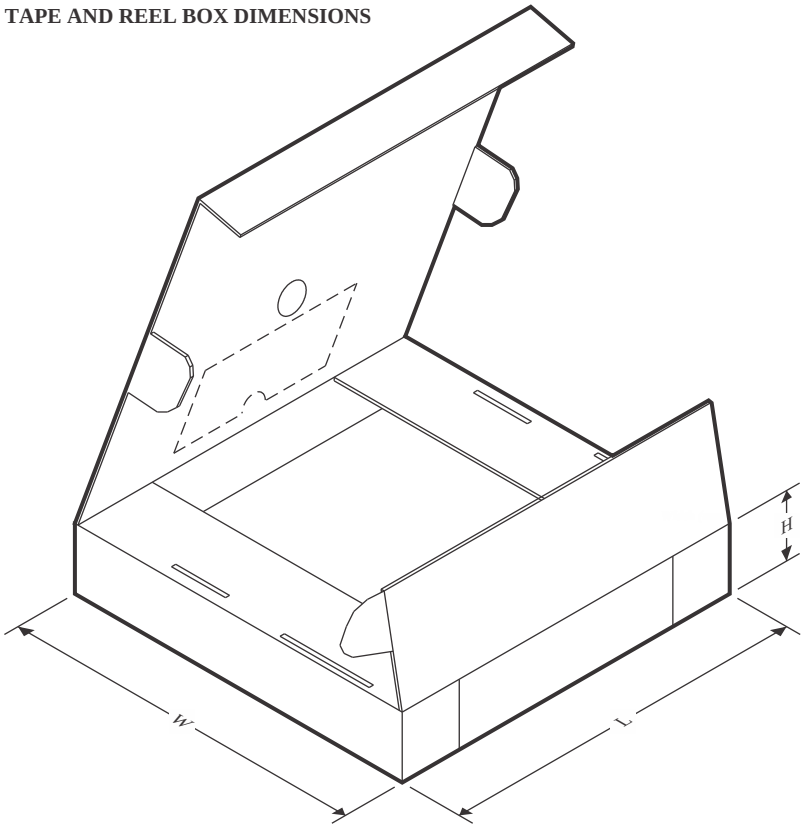
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA659IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.15	3.1	1.55	4.0	8.0	Q3
OPA659IDBVT	SOT-23	DBV	5	250	180.0	8.4	3.15	3.1	1.55	4.0	8.0	Q3
OPA659IDRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA659IDRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

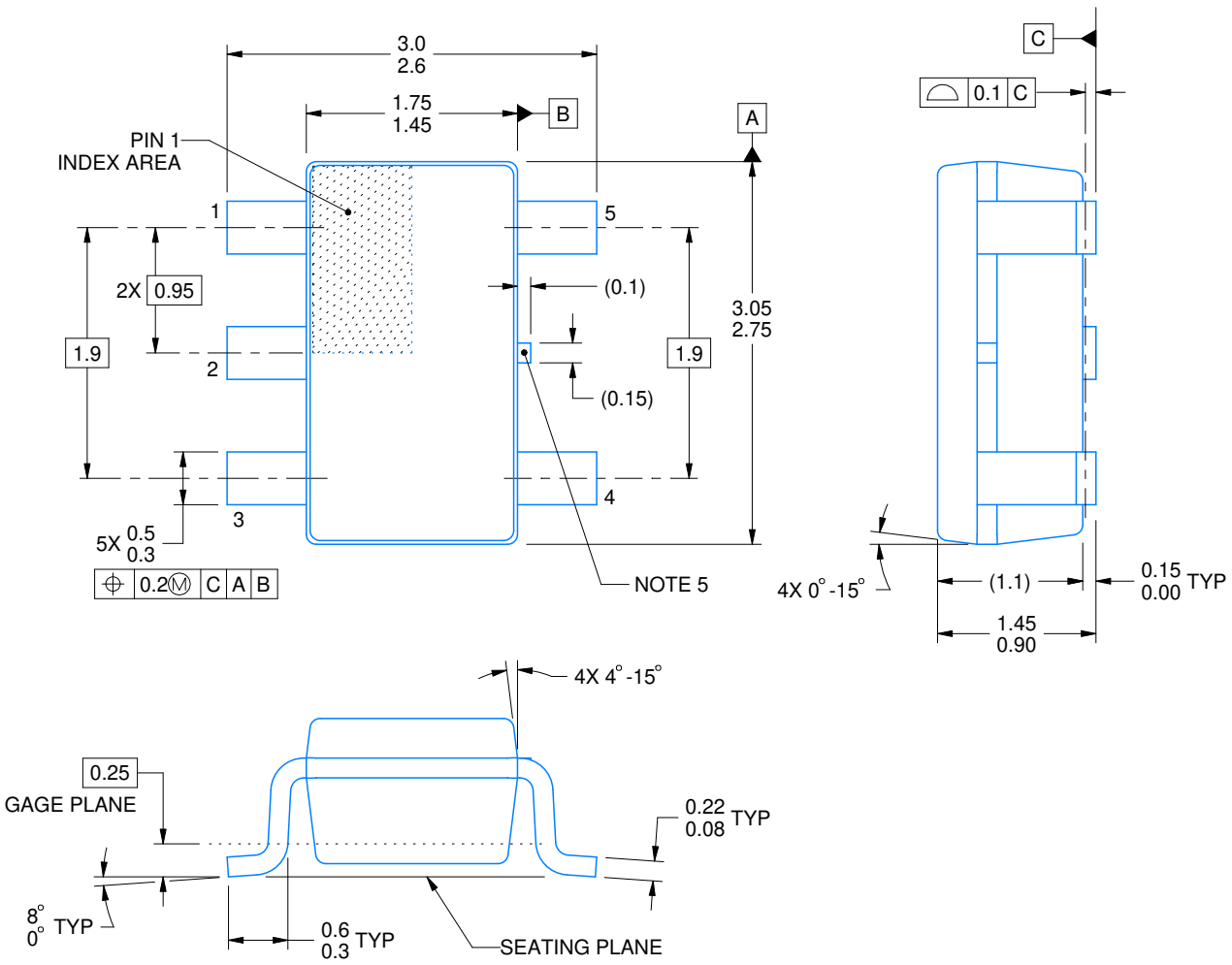
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA659IDBVR	SOT-23	DBV	5	3000	213.0	191.0	35.0
OPA659IDBVT	SOT-23	DBV	5	250	213.0	191.0	35.0
OPA659IDRBR	SON	DRB	8	3000	353.0	353.0	32.0
OPA659IDRBT	SON	DRB	8	250	213.0	191.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

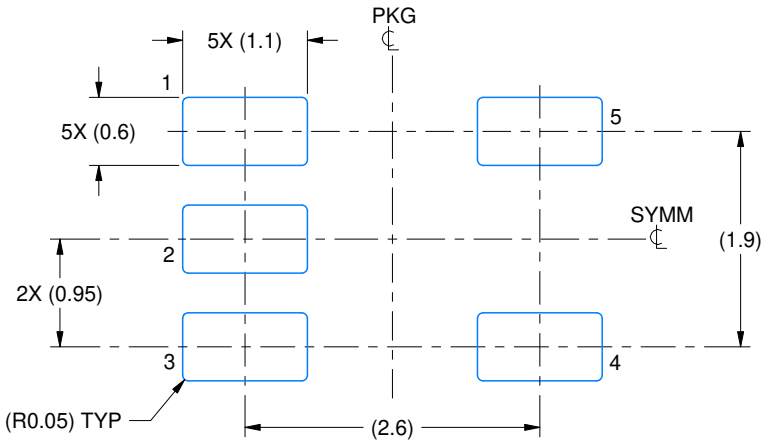
SMALL OUTLINE TRANSISTOR



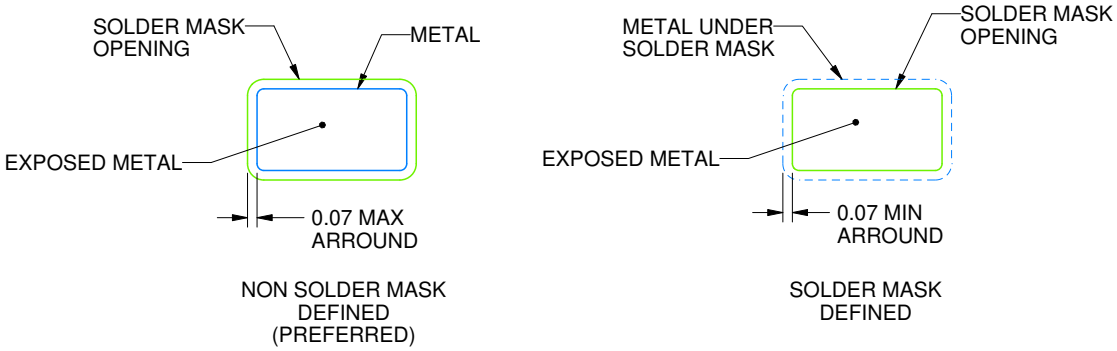
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

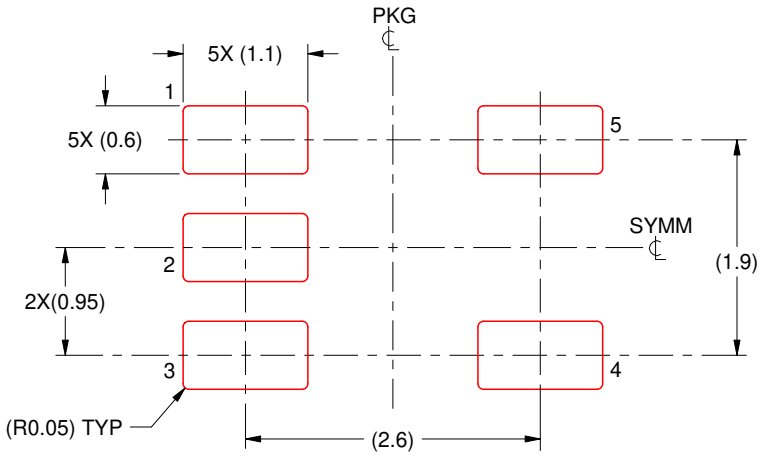


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DRB 8

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

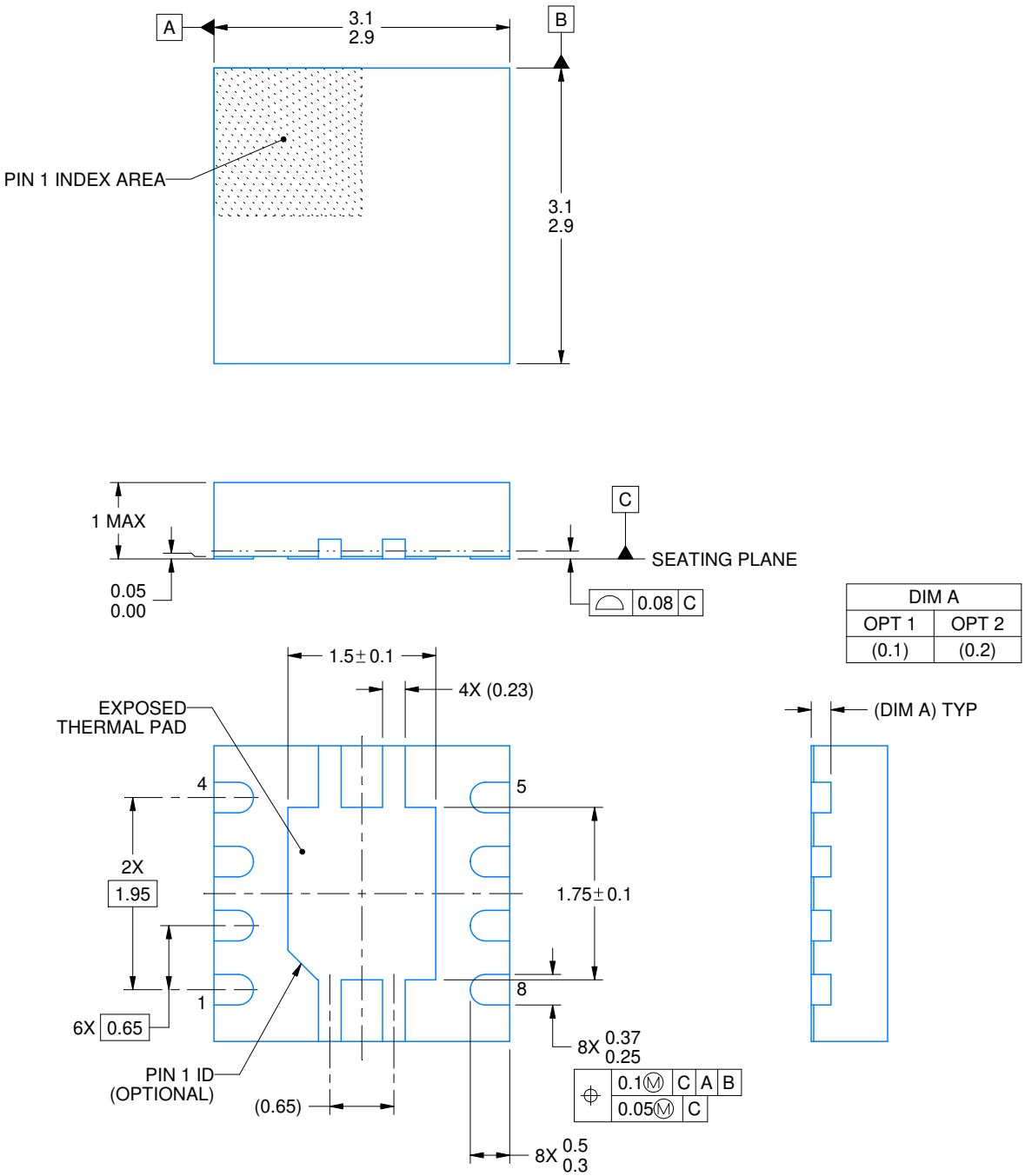
4203482/L

PACKAGE OUTLINE

DRB0008A

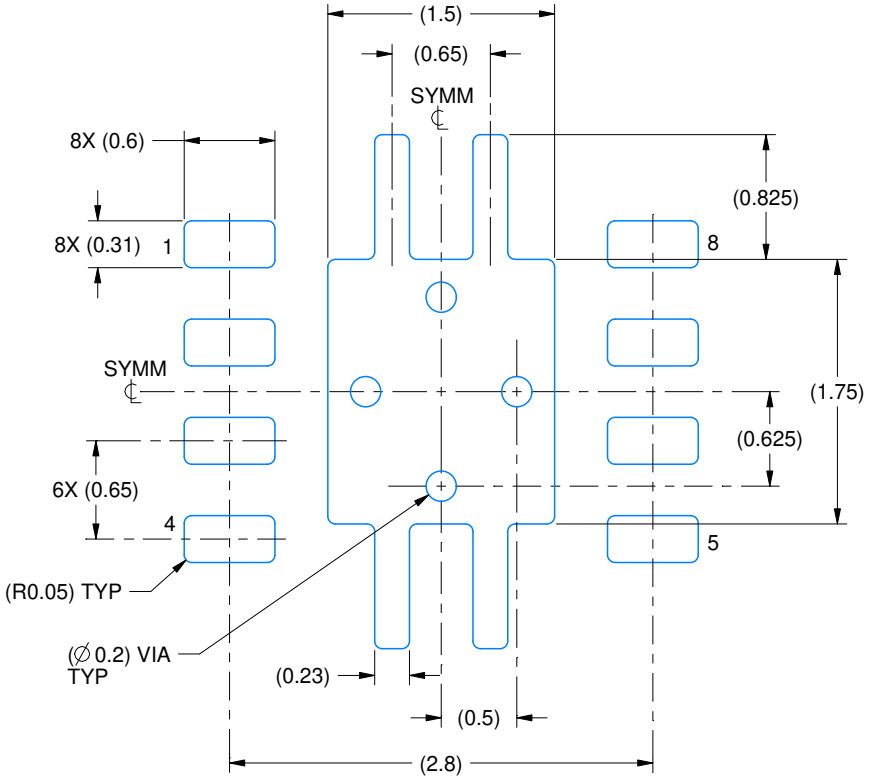
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

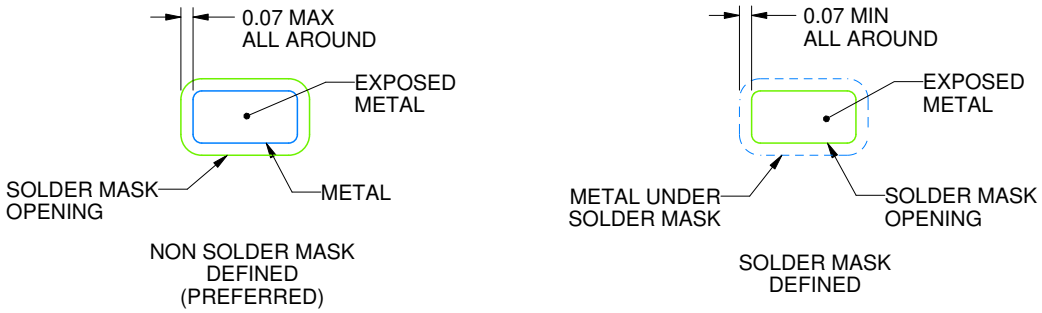


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

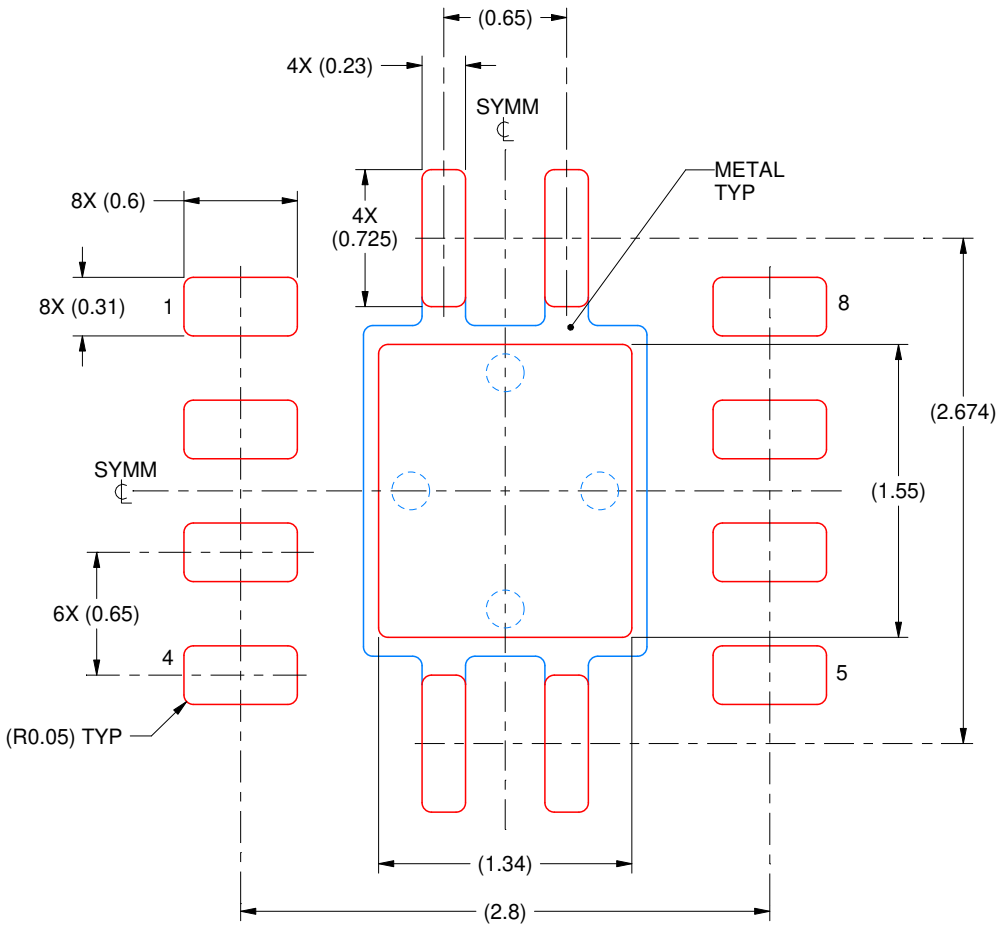


SOLDER MASK DETAILS

4218875/A 01/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218875/A 01/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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