Wide Bandwidth Operational Transconductance Amplifier (OTA)

Check for Samples: OPA861

FEATURES

- **Wide Bandwidth (80MHz, Open-Loop, G = +5)**
- **High Slew Rate (900V/µs)**
- **High Transconductance (95mA/V)**
- **External I_Q-Control**
- **Low Quiescent Current (5.4mA)**

APPLICATIONS

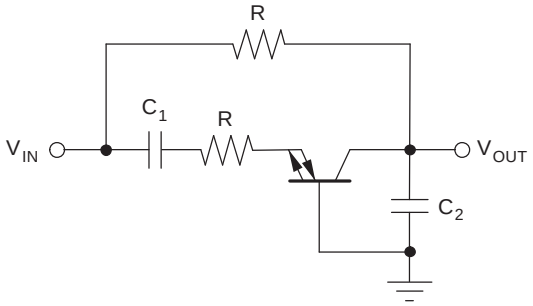
- **Video/Broadcast Equipment**
- **Communications Equipment**
- **High-Speed Data Acquisition**
- **Wideband LED Drivers**
- **Control Loop Amplifiers**
- **Wideband Active Filters**
- **Line Drivers**

DESCRIPTION

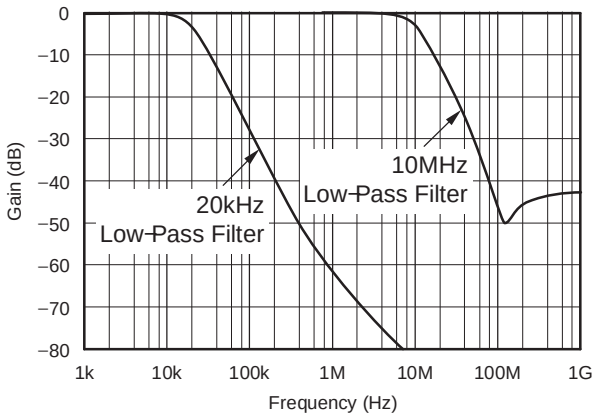
The OPA861 is a versatile monolithic component designed for wide-bandwidth systems, including high performance video, RF and IF circuitry. The OPA861 is a wideband, bipolar operational transconductance amplifier (OTA).

The OTA or voltage-controlled current source can be viewed as an *ideal transistor*. Like a transistor, it has three terminals—a high impedance input (base), a low-impedance input/output (emitter), and the current output (collector). The OPA861, however, is self-biased and bipolar. The output collector current is zero for a zero base-emitter voltage. AC inputs centered about zero produce an output current, which is bipolar and centered about zero. The transconductance of the OPA861 can be adjusted with an external resistor, allowing bandwidth, quiescent current, and gain trade-offs to be optimized.

Used as a basic building block, the OPA861 simplifies the design of AGC amplifiers, LED driver circuits for fiber optic transmission, integrators for fast pulses, fast control loop amplifiers and control amplifiers for capacitive sensors, and active filters. The OPA861 is available in SO-8 and SOT23-6 surface-mount packages.



Low-Pass Negative Impedance Converter (NIC) Filter



Frequency Response of 20kHz and 10MHz Low-Pass NIC Filters

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA861	SO-8	D	–45°C to +85°C	OPA861	OPA861ID	Rails, 75
					OPA861IDR	Tape and Reel, 2500
OPA861	SOT23-6	DBV	–45°C to +85°C	N5R	OPA861IDBVT	Tape and Reel, 250
					OPA861IDBVR	Tape and Reel, 3000

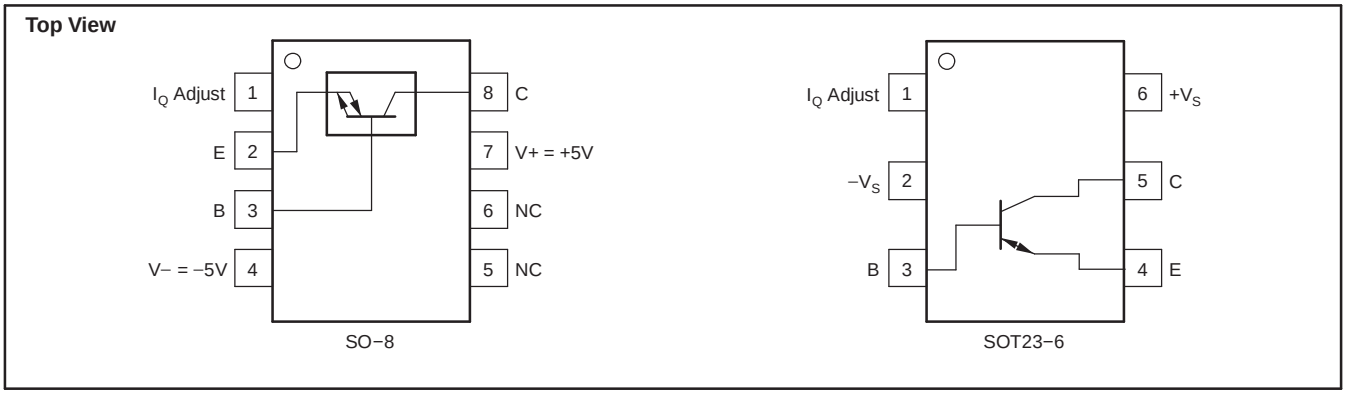
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Power Supply	±6.5V_{DC}
Internal Power Dissipation	See Thermal Information
Differential Input Voltage	±1.2V
Input Common-Mode Voltage Range	±V_S
Storage Temperature Range: D	–65°C to +125°C
Lead Temperature (soldering, 10s)	+260°C
Junction Temperature (T_J)	+150°C
ESD Rating:	
Human Body Model (HBM)(2)	1500V
Charge Device Model (CDM)	1000V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operations of the device at these and any other conditions beyond those specified is not supported.
(2) Pin 2 for the SO-8 package > 500V HBM. Pin 4 for the SOT23-6 package > 500V HBM.

Figure 1. PIN CONFIGURATION



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ELECTRICAL CHARACTERISTICS: V_S = ±5V

R_L = 500Ω and R_{ADJ} = 250Ω, unless otherwise noted.

PARAMETER	CONDITIONS	OPA861ID, IDBV				UNITS	MIN/ MAX	TEST LEVEL(1)
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C(2)	0°C to 70°C(3)	–40°C to +85°C(3)			
OTA—Open-Loop (see Figure 33)								
AC PERFORMANCE								
Bandwidth	G = +5, V_O = 200mV$_{PP}$, R_L = 500Ω	80	77	75	74	MHz	min	B
	G = +5, V_O = 1V$_{PP}$	80				MHz	typ	C
	G = +5, V_O = 5V$_{PP}$	80				MHz	typ	C
Slew Rate	G = +5, V_O = 5V Step	900	860	850	840	V/µs	min	B
Rise Time and Fall Time	V_O = 1V Step	4.4				ns	typ	C
Harmonic Distortion	G = +5, V_O = 2V$_{PP}$, 5MHz							
2nd-Harmonic	R_L = 500Ω	–68	–55	–54	–53	dB	max	B
3rd-Harmonic	R_L = 500Ω	–57	–52	–51	–49	dB	max	B
Base Input Voltage Noise	f > 100kHz	2.4	3.0	3.3	3.4	nV/√Hz	max	B
Base Input Current Noise	f > 100kHz	1.7	2.4	2.45	2.5	pA/√Hz	max	B
Emitter Input Current Noise	f > 100kHz	5.2	15.3	16.6	17.5	pA/√Hz	max	B
OTA DC PERFORMANCE(4) (see Figure 33)								
Minimum OTA Transconductance (g_m)	V_O = ±10mV, R_C = 50Ω, R_E = 0Ω	95	**80**	77	75	mA/V	min	A
Maximum OTA Transconductance (g_m)	V_O = ±10mV, R_C = 50Ω, R_E = 0Ω	95	**150**	155	160	mA/V	max	A
B-Input Offset Voltage	V_B = 0V, R_C = 0Ω, R_E = 100Ω	±3	**±12**	±15	±20	mV	max	A
Average B-Input Offset Voltage Drift	V_B = 0V, R_C = 0Ω, R_E = 100Ω			±67	±120	µV/°C	max	B
B-Input Bias Current	V_B = 0V, R_C = 0Ω, R_E = 100Ω	±1	**±5**	±6	±6.6	µA	max	A
Average B-Input Bias Current Drift	V_B = 0V, R_C = 0Ω, R_E = 100Ω			±20	±25	nA/°C	max	B
E-Input Bias Current	V_B = 0V, V_C = 0V	±30	**±100**	±125	±140	µA	max	A
Average E-Input Bias Current Drift	V_B = 0V, V_C = 0V			±500	±600	nA/°C	max	B
C-Output Bias Current	V_B = 0V, V_C = 0V	±5	**±18**	±30	±38	µA	max	A
Average C-Output Bias Current Drift	V_B = 0V, V_C = 0V			±250	±300	nA/°C	max	B
OTA INPUT (see Figure 33)								
B-Input Voltage Range		±4.2	±3.7	±3.6	±3.6	V	min	B
B-Input Impedance		455 || 2.1				kΩ || pF	typ	C
Min E-Input Resistance		10.5	12.5	13.0	13.3	Ω	max	B
Max E-Input Resistance		10.5	6.7	6.5	6.3	Ω	min	B
OTA OUTPUT								
E-Output Voltage Compliance	I_E = ±1mA	±4.2	**±3.7**	±3.6	±3.6	V	min	A
E-Output Current, Sinking/Sourcing	V_E = 0	±15	**±10**	±9	±9	mA	min	A
C-Output Voltage Compliance	I_C = ±1mA	±4.7	**±4.0**	±3.9	±3.9	V	min	A
C-Output Current, Sinking/Sourcing	V_C = 0	±15	**±10**	±9	±9	mA	min	A
C-Output Impedance		54 || 2				kΩ || pF	typ	C

(1) Test levels: (A) 100% tested at +25°C. Over temperature limits set by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(2) Junction temperature = ambient for +25°C specifications.
(3) Junction temperature = ambient at low temperature limit; junction temperature = ambient + 7°C at high temperature limit for over temperature specifications.
(4) Current is considered positive out of node.

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ELECTRICAL CHARACTERISTICS: V_S = ±5V (continued)

R_L = 500Ω and R_{ADJ} = 250Ω, unless otherwise noted.

PARAMETER	CONDITIONS	OPA861ID, IDBV				UNITS	MIN/ MAX	TEST LEVEL[1]
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C[2]	0°C to 70°C[3]	–40°C to +85°C[3]			
POWER SUPPLY								
Specified Operating Voltage		±5				V	typ	C
Maximum Operating Voltage			**±6.3**	±6.3	±6.3	V	max	A
Minimum Operating Voltage			±2.0	±2.0	±2.0	V	min	B
Maximum Quiescent Current	R_{ADJ} = 250Ω	5.4	**5.9**	7.0	7.4	mA	max	A
Minimum Quiescent Current	R_{ADJ} = 250Ω	5.4	**4.9**	4.3	3.4	mA	min	A
OTA Power-Supply Rejection Ratio (+PSRR)	$\Delta I_C/\Delta V_S$	±20	**±50**	±60	±65	µA/V	max	A
THERMAL CHARACTERISTICS								
Specification: ID, IDBV		–40 to +85				°C	typ	C
Thermal Resistance θ_{JA}								
D SO-8	Junction-to-Ambient	+125				°C/W	typ	C
DBV SOT23-6	Junction-to-Ambient	+150				°C/W	typ	C

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ELECTRICAL CHARACTERISTICS: V_S = +5V

R_L = 500Ω to V_S/2 and R_{ADJ} = 250Ω, unless otherwise noted.

PARAMETER	CONDITIONS	OPA861ID, IDBV				UNITS	MIN/ MAX	TEST LEVEL(1)
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C(2)	0°C to 70°C(3)	–40°C to +85°C(3)			
OTA—Open-Loop (see Figure 33)								
AC PERFORMANCE								
Bandwidth	G = +5, V_O = 200mV$_{PP}$, R_L = 500Ω	73	72	72	70	MHz	min	B
	G = +5, V_O = 1V$_{PP}$	73				MHz	typ	C
Slew Rate	G = +5, V_O = 2.5V Step	410	395	390	390	V/µs	min	B
Rise Time and Fall Time	V_O = 1V Step	4.4				ns	typ	C
Harmonic Distortion	G = +5, V_O = 2V$_{PP}$, 5MHz							
2nd-Harmonic	R_L = 500Ω	–67	–55	–54	–54	dB	max	B
3rd-Harmonic	R_L = 500Ω	–57	–50	–49	–48	dB	max	B
Base Input Voltage Noise	f > 100kHz	2.4	3.0	3.3	3.4	nV/√Hz	max	B
Base Input Current Noise	f > 100kHz	1.7	2.4	2.45	2.5	pA/√Hz	max	B
Emitter Input Current Noise	f > 100kHz	5.2	15.3	16.6	17.5	pA/√Hz	max	B
OTA DC PERFORMANCE(4) (see Figure 33)								
Minimum OTA Transconductance (g_m)	V_O = ±10mV, R_C = 50Ω, R_E = 0Ω	85	**70**	67	65	mA/V	min	A
Maximum OTA Transconductance (g_m)	V_O = ±10mV, R_C = 50Ω, R_E = 0Ω	85	**140**	145	150	mA/V	max	A
B-Input Offset Voltage	V_B = 0V, R_C = 0Ω, R_E = 100Ω	±3	**±12**	±15	±20	mV	max	A
Average B-Input Offset Voltage Drift	V_B = 0V, R_C = 0Ω, R_E = 100Ω			±67	±120	µV/°C	max	B
B-Input Bias Current	V_B = 0V, R_C = 0Ω, R_E = 100Ω	±1	**±5**	±6	±6.6	µA	max	A
Average B-Input Bias Current Drift	V_B = 0V, R_C = 0Ω, R_E = 100Ω			±20	±25	nA/°C	max	B
E-Input Bias Current	V_B = 0V, V_C = 0V	±30	**±100**	±125	±140	µA	max	A
Average E-Input Bias Current Drift	V_B = 0V, V_C = 0V			±500	±600	nA/°C	max	B
C-Output Bias Current	V_B = 0V, V_C = 0V	±15				µA	typ	C
OTA INPUT (see Figure 33)								
Most Positive B-Input Voltage		4.2	3.7	3.6	3.6	V	min	B
Least Positive B-Input Voltage		0.8	1.3	1.4	1.4	V	max	B
B-Input Impedance		455 || 2.1				kΩ || pF	typ	C
Min E-Input Resistance		11.8	14.4	14.9	15.4	Ω	max	B
Max E-Input Resistance		11.8	7.1	6.9	6.7	Ω	min	B
OTA OUTPUT								
Maximum E-Output Voltage Compliance	I_E = ±1mA	4.2	**3.7**	3.6	3.6	V	min	A
Minimum E-Output Voltage Compliance	I_E = ±1mA	0.8	**1.3**	1.4	1.4	V	max	A
E-Output Current, Sinking/Sourcing	V_E = 0	±8	**±7**	±6.5	±6.5	mA	min	A
Maximum C-Output Voltage Compliance	I_C = ±1mA	4.7	**4.0**	3.9	3.9	V	min	A
Minimum C-Output Voltage Compliance	I_C = ±1mA	0.3	**1.0**	1.1	1.1	V	max	A
C-Output Current, Sinking/Sourcing	V_C = 0	±8	**±7**	±6.5	±6.5	mA	min	A
C-Output Impedance		54 || 2				kΩ || pF	typ	C

(1) Test levels: (A) 100% tested at +25°C. Over temperature limits set by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(2) Junction temperature = ambient for +25°C specifications.
(3) Junction temperature = ambient at low temperature limit; junction temperature = ambient + 3°C at high temperature limit for over temperature specifications.
(4) Current is considered positive out of node.

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ELECTRICAL CHARACTERISTICS: V_S = +5V (continued)

R_L = 500Ω to V_S/2 and R_{ADJ} = 250Ω, unless otherwise noted.

PARAMETER	CONDITIONS	OPA861ID, IDBV				UNITS	MIN/ MAX	TEST LEVEL[1]
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C[2]	0°C to 70°C[3]	–40°C to +85°C[3]			
POWER SUPPLY								
Specified Operating Voltage		5				V	typ	C
Maximum Operating Voltage			**12.6**	12.6	12.6	V	max	A
Minimum Operating Voltage			4	4	4	V	min	B
Maximum Quiescent Current	R_{ADJ} = 250Ω	4.7	**5.2**	6.0	6.4	mA	max	A
Minimum Quiescent Current	R_{ADJ} = 250Ω	4.7	**4.2**	3.4	3.0	mA	min	A
OTA Power-Supply Rejection Ratio (+PSRR)	$\Delta I_C/\Delta V_S$	±20	**±50**	±60	±65	µA/V	max	A
THERMAL CHARACTERISTICS								
Specification: ID, IDBV		–40 to +85				°C	typ	C
Thermal Resistance θ_{JA}								
D SO-8	Junction-to-Ambient	+125				°C/W	typ	C
DBV SOT23-6	Junction-to-Ambient	+150				°C/W	typ	C

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TYPICAL CHARACTERISTICS: V_S = ±5V

At T_A = +25°C, I_Q = 5.4mA, and R_L = 500Ω, unless otherwise noted.

OTA TRANSCONDUCTANCE vs FREQUENCY

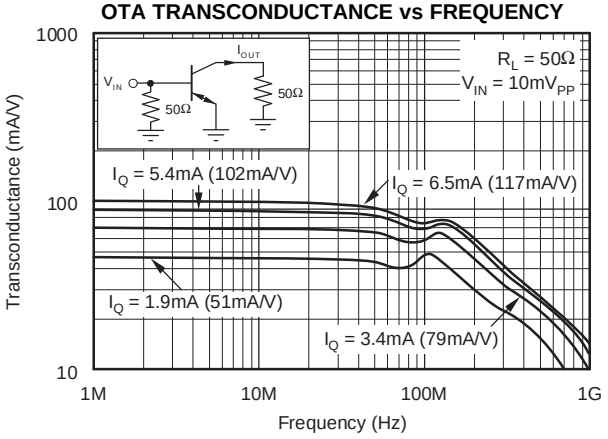


Figure 2.

OTA TRANSCONDUCTANCE vs QUIESCENT CURRENT

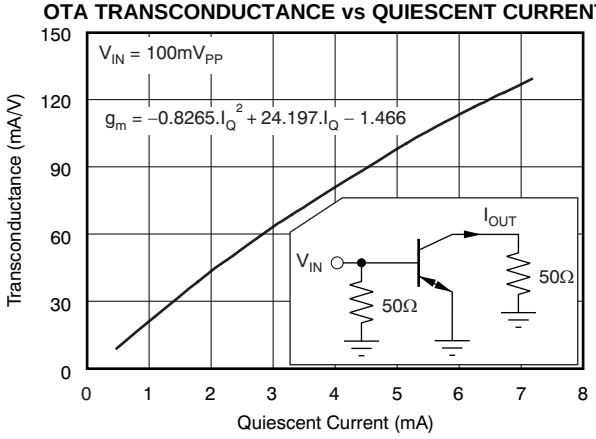


Figure 3.

OTA TRANSCONDUCTANCE vs INPUT VOLTAGE

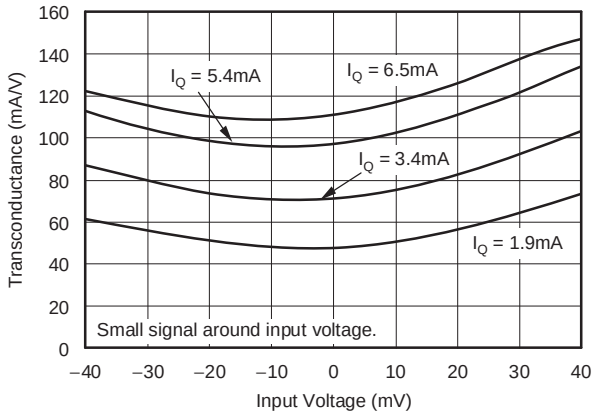


Figure 4.

OTA TRANSFER CHARACTERISTICS

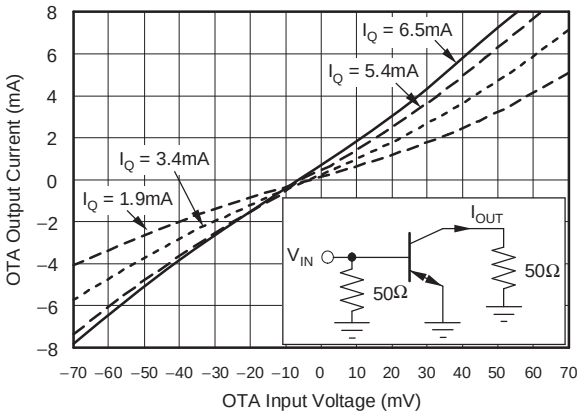


Figure 5.

OTA SMALL-SIGNAL PULSE RESPONSE

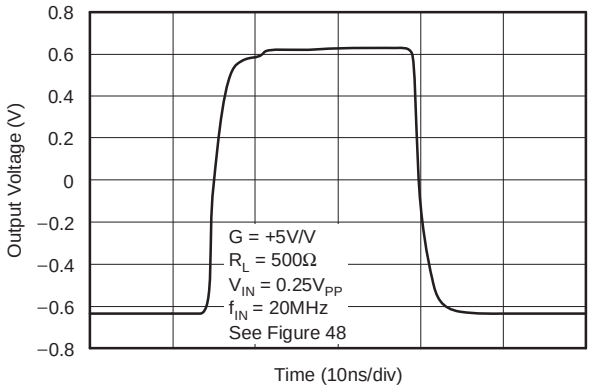


Figure 6.

OTA LARGE-SIGNAL PULSE RESPONSE

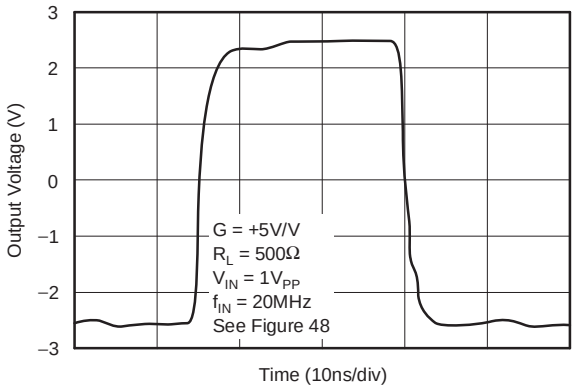


Figure 7.

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TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

At T_A = +25°C, I_Q = 5.4mA, and R_L = 500Ω, unless otherwise noted.

B-INPUT RESISTANCE vs QUIESCENT CURRENT

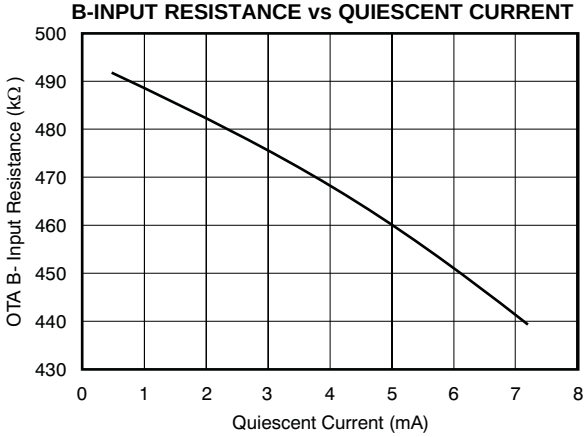


Figure 8.

C-OUTPUT RESISTANCE vs QUIESCENT CURRENT

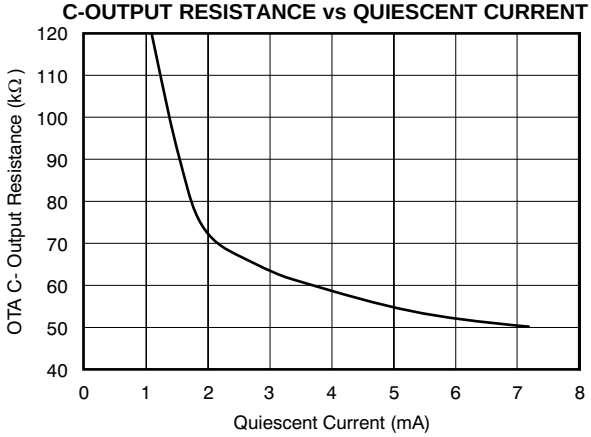


Figure 9.

E-OUTPUT RESISTANCE vs QUIESCENT CURRENT

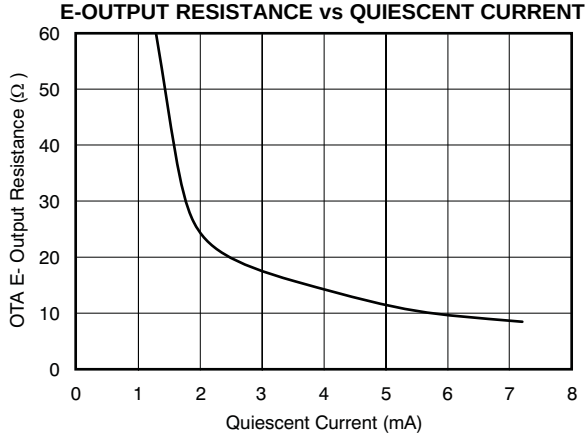


Figure 10.

INPUT VOLTAGE AND CURRENT NOISE DENSITY

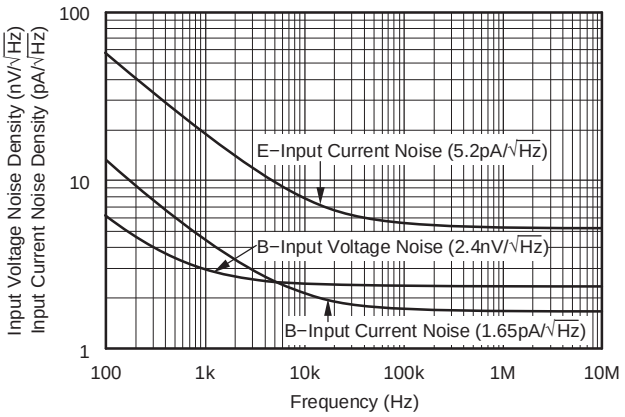


Figure 11.

QUIESCENT CURRENT vs R_{ADJ}

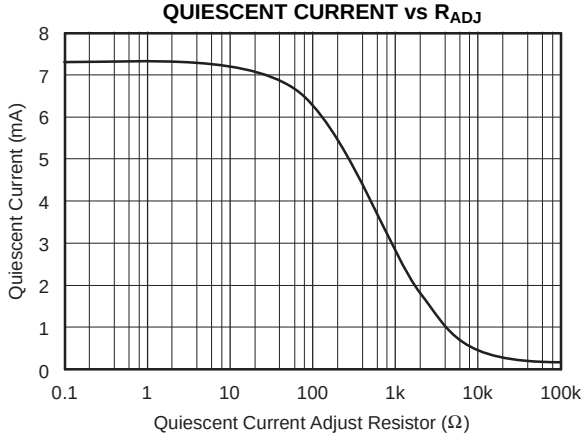


Figure 12.

1MHz OTA VOLTAGE AND CURRENT NOISE DENSITY vs QUIESCENT CURRENT ADJUST RESISTOR

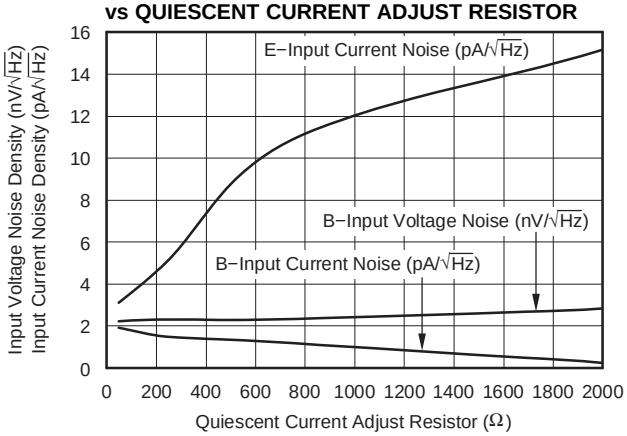


Figure 13.

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TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

At T_A = +25°C, I_Q = 5.4mA, and R_L = 500Ω, unless otherwise noted.

B-INPUT OFFSET VOLTAGE AND BIAS CURRENT vs TEMPERATURE

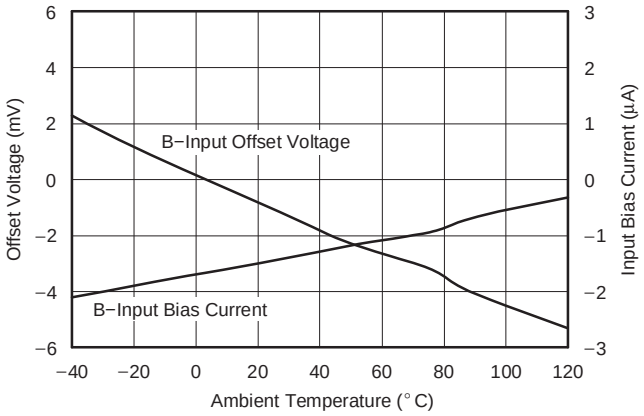


Figure 14.

QUIESCENT CURRENT vs TEMPERATURE

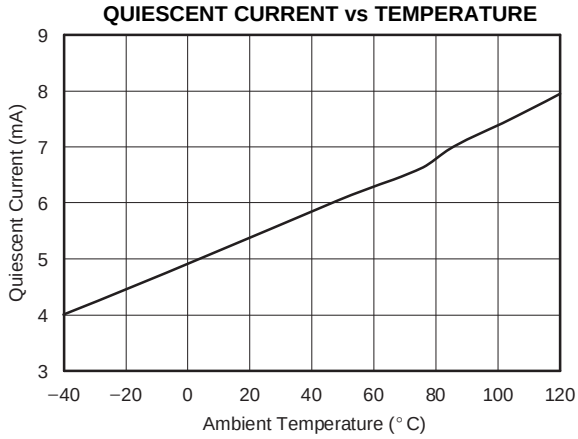


Figure 15.

C-OUTPUT BIAS CURRENT vs TEMPERATURE

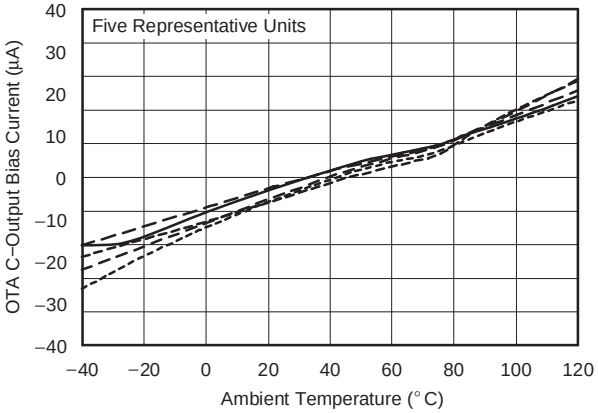


Figure 16.

I_Q/I_{ADS} Ratio vs R_{ADJ}

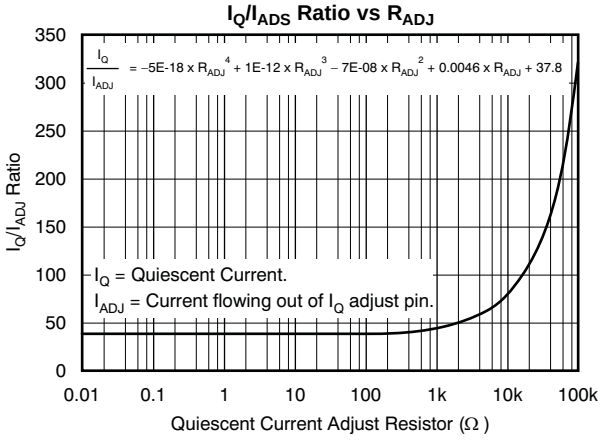


Figure 17.

QUIESCENT CURRENT vs ADJUST PIN BIAS CURRENT

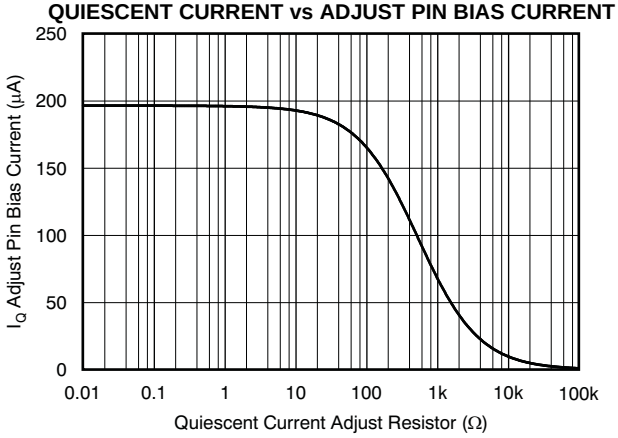


Figure 18.

TYPICAL CHARACTERISTICS: V_S = +5V

At T_A = +25°C, I_Q = 4.7mA, and R_L = 500Ω to V_S/2, unless otherwise noted.

OTA TRANSCONDUCTANCE vs FREQUENCY

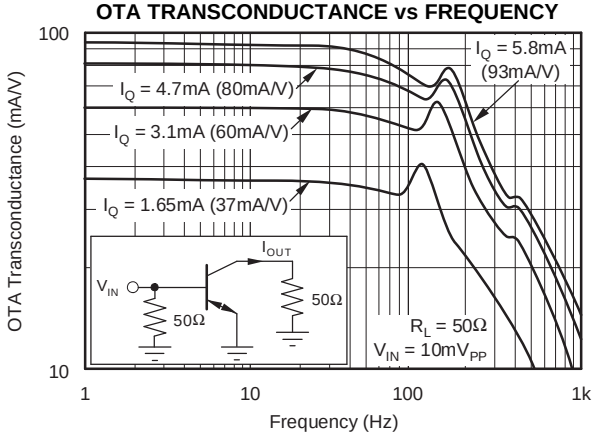


Figure 19.

OTA TRANSCONDUCTANCE vs I_Q

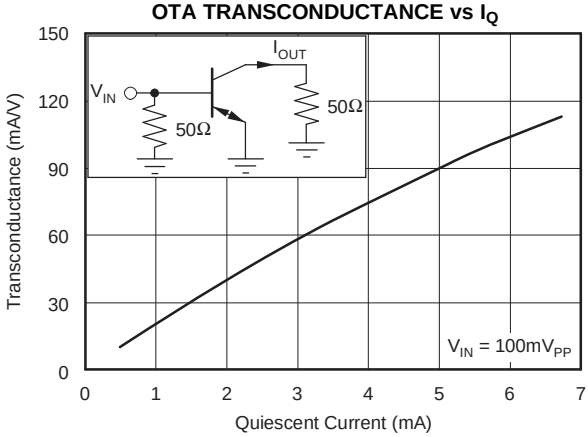


Figure 20.

OTA TRANSCONDUCTANCE vs INPUT VOLTAGE

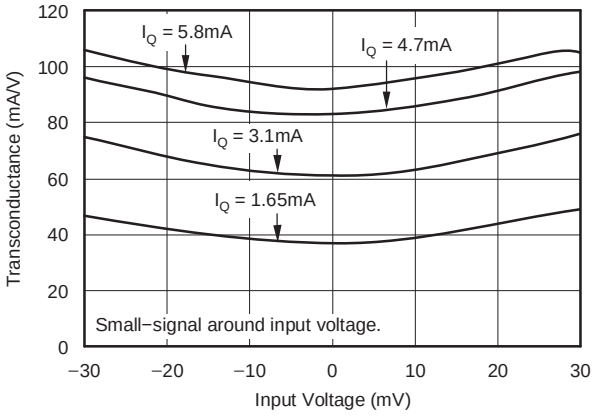


Figure 21.

OTA TRANSFER CHARACTERISTICS

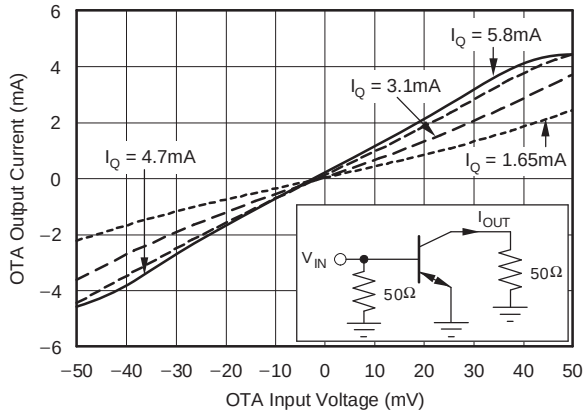


Figure 22.

OTA SMALL-SIGNAL PULSE RESPONSE

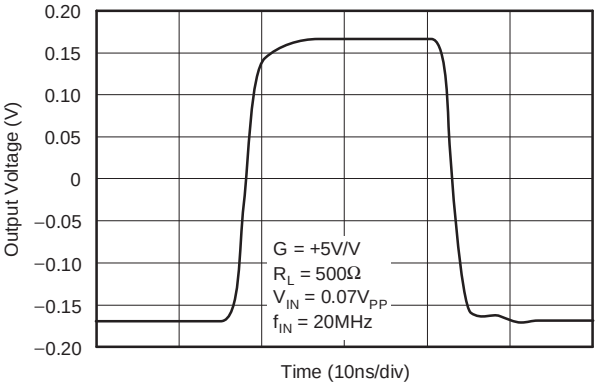


Figure 23.

OTA LARGE-SIGNAL PULSE RESPONSE

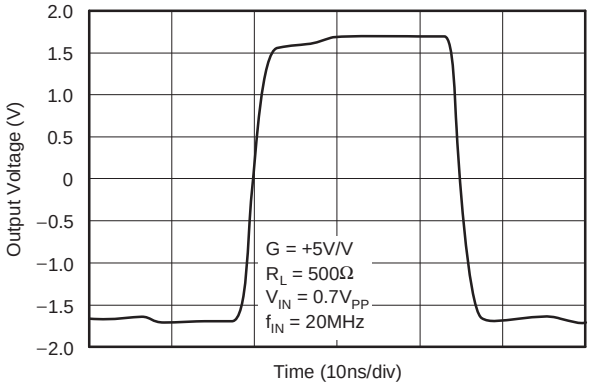


Figure 24.

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TYPICAL CHARACTERISTICS: V_S = +5V (continued)

At T_A = +25°C, I_Q = 4.7mA, and R_L = 500Ω to V_S/2, unless otherwise noted.

B-INPUT RESISTANCE vs QUIESCENT CURRENT

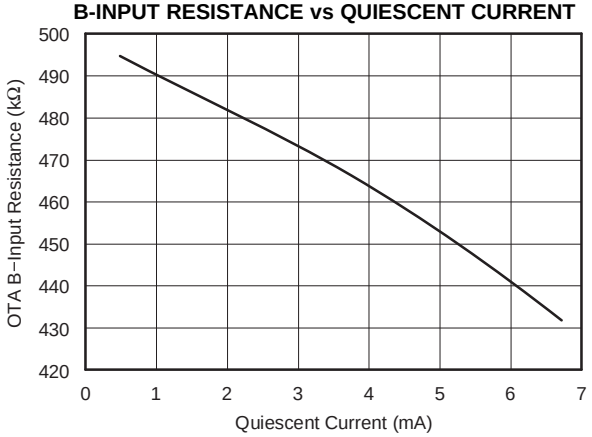


Figure 25.

C-OUTPUT RESISTANCE vs QUIESCENT CURRENT

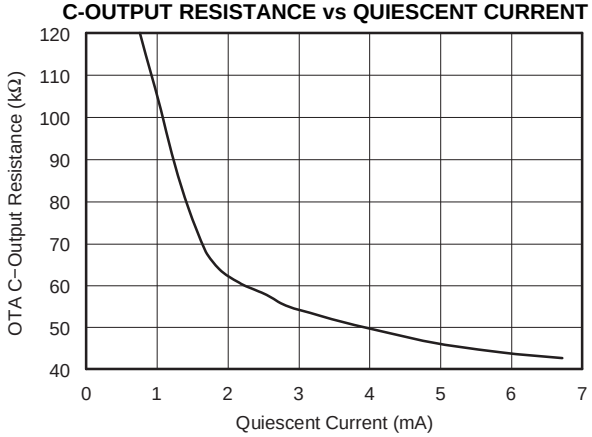


Figure 26.

E-OUTPUT RESISTANCE vs QUIESCENT CURRENT

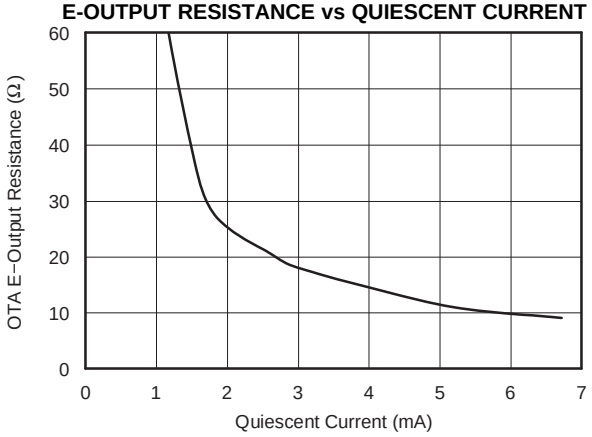


Figure 27.

QUIESCENT CURRENT vs R_{ADJ}

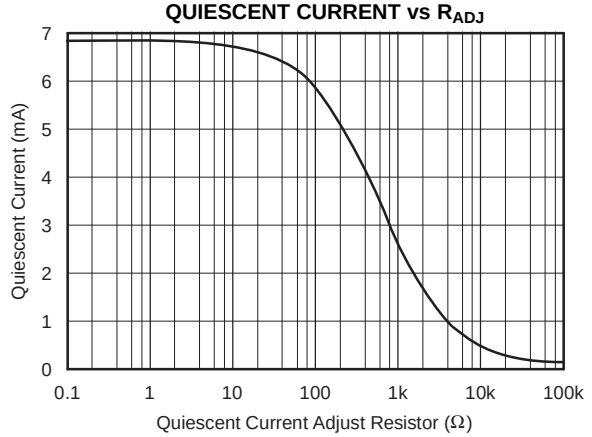


Figure 28.

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APPLICATION INFORMATION

The OPA861 is a versatile monolithic transconductance amplifier designed for wide-bandwidth systems, including high-performance video, RF, and IF circuitry. The operation of the OPA861 is discussed in the *OTA (Operational Transconductance Amplifier)* section of this data sheet. Over the years and depending on the writer, the OTA section of an op amp has been referred to as a Diamond Transistor, Voltage-Controlled Current source, Transconductor, Macro Transistor, or positive second-generation current conveyor (CCII+). Corresponding symbols for these terms are shown in Figure 29.

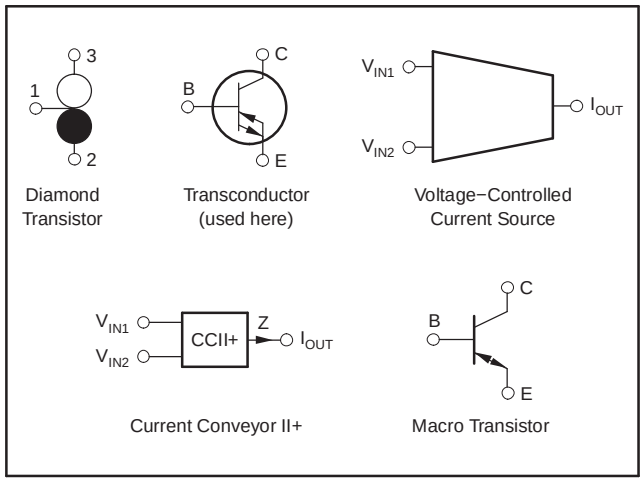


Figure 29. Symbols and Terms

Regardless of its depiction, the OTA section has a high-input impedance (B-input), a low-input/output impedance (E-input), and a high-impedance current source output (C-output).

TRANSCONDUCTANCE (OTA) SECTION—AN OVERVIEW

The symbol for the OTA section is similar to a transistor (see Figure 29). Applications circuits for the OTA look and operate much like transistor circuits—the transistor is also a voltage-controlled current source. Not only does this characteristic simplify the understanding of application circuits, it aids the circuit optimization process as well. Many of the same intuitive techniques used with transistor designs apply to OTA circuits. The three terminals of the OTA are labeled B, E, and C. This labeling calls attention to its similarity to a transistor, yet draws distinction for clarity. While the OTA is similar to a transistor, one essential difference is the sense of the C-output current: it flows out the C terminal for positive B-to-E input voltage and in the C terminal for negative B-to-E input voltage. The OTA offers many advantages over a discrete transistor. The OTA is self-biased, simplifying the design process and reducing component count. In addition, the OTA is far more linear than a transistor. Transconductance of the OTA is constant over a wide range of collector currents—this feature implies a fundamental improvement of linearity.

BASIC CONNECTIONS

Figure 30 shows basic connections required for operation. These connections are not shown in subsequent circuit diagrams. Power-supply bypass capacitors should be located as close as possible to the device pins. Solid tantalum capacitors are generally best.

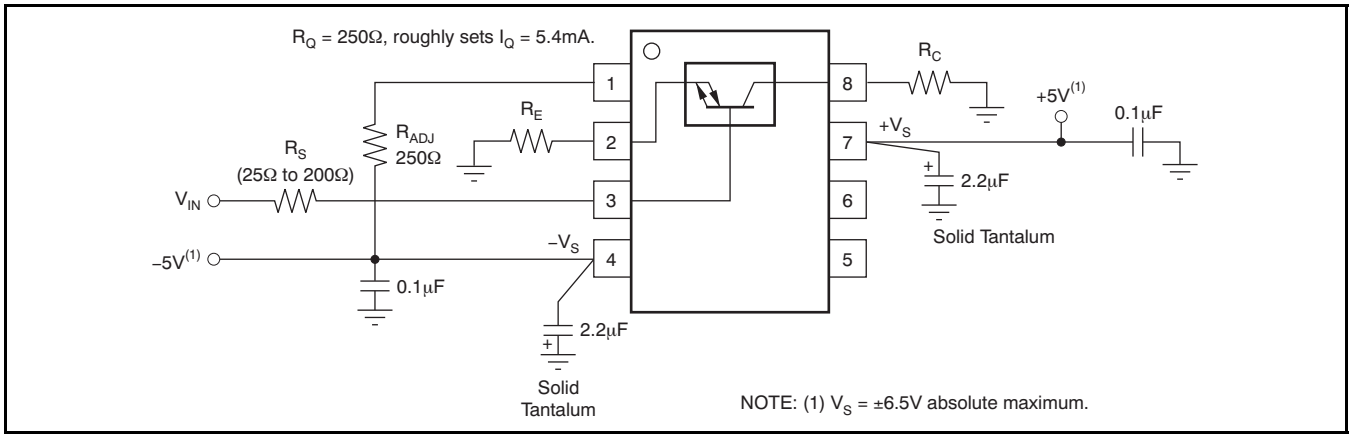


Figure 30. Basic Connections

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QUIESCENT CURRENT CONTROL PIN

The quiescent current of the transconductance portion of the OPA861 is set with a resistor, R_{ADJ}, connected from pin 1 to $-V_S$. The maximum quiescent current is 6mA. R_{ADJ} should be set between 50Ω and 1kΩ for optimal performance of the OTA section. This range corresponds to the 5mA quiescent current for R_{ADJ} = 50Ω, and 1mA for R_{ADJ} = 1kΩ. If the I_Q adjust pin is connected to the negative supply, the quiescent current will be set by the 250Ω internal resistor.

Reducing or increasing the quiescent current for the OTA section controls the bandwidth and AC behavior as well as the transconductance. With R_{ADJ} = 250Ω, this sets approximately 5.4mA total quiescent current at 25°C. It may be appropriate in some applications to trim this resistor to achieve the desired quiescent current or AC performance.

Applications circuits generally do not show the resistor R_Q, but it is required for proper operation.

With a fixed R_{ADJ} resistor, quiescent current increases with temperature (see Figure 12 in the *Typical Characteristics* section). This variation of current with temperature holds the transconductance, g_m, of the OTA relatively constant with temperature (another advantage over a transistor).

It is also possible to vary the quiescent current with a control signal. The control loop in Figure 31 shows 1/2 of a REF200 current source used to develop 100mV on R_1. The loop forces 125mV to appear on R_2. Total quiescent current of the OPA861 is approximately 37 × I_1, where I_1 is the current made to flow out of pin 1.

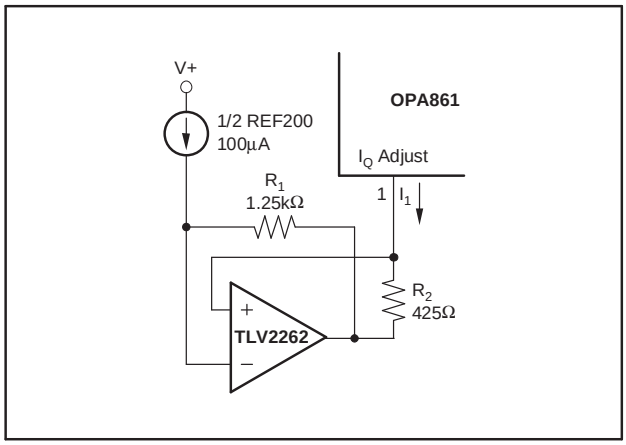


Figure 31. Optional Control Loop for Setting Quiescent Current

With this control loop, quiescent current will be nearly constant with temperature. Since this method differs from the temperature-dependent behavior of the internal current source, other temperature-dependent behavior may differ from that shown in the Typical Characteristics. The circuit of Figure 31 will control the I_Q of the OPA861 somewhat more accurately than with a fixed external resistor, R_Q. Otherwise, there is no fundamental advantage to using this more complex biasing circuitry. It does, however, demonstrate the possibility of signal-controlled quiescent current. This capability may suggest other possibilities such as AGC, dynamic control of AC behavior, or VCO.

BASIC APPLICATIONS CIRCUITS

Most applications circuits for the OTA section consist of a few basic types, which are best understood by analogy to a transistor. Used in voltage-mode, the OTA section can operate in three basic operating states—common emitter, common base, and common collector. In the current-mode, the OTA can be useful for analog computation such as current amplifier, current differentiator, current integrator, and current summer.

Common-E Amplifier or Forward Amplifier

Figure 32 compares the common-emitter configuration for a BJT with the common-E amplifier for the OTA section. There are several advantages in using the OTA section in place of a BJT in this configuration. Notably, the OTA does not require any biasing, and the transconductance gain remains constant over temperature. The output offset voltage is close to 0, compared with several volts for the common-emitter amplifier.

The gain is set in a similar manner as for the BJT equivalent with Equation 1:

$$G = \frac{R_L}{\frac{1}{g_m} + R_E} \quad (1)$$

Just as transistor circuits often use emitter degeneration, OTA circuits may also use degeneration. This option can be used to reduce the effects that offset voltage and offset current might otherwise have on the DC operating point of the OTA. The E-degeneration resistor may be bypassed with a large capacitor to maintain high AC gain. Other circumstances may suggest a smaller value capacitor used to extend or optimize high-frequency performance.

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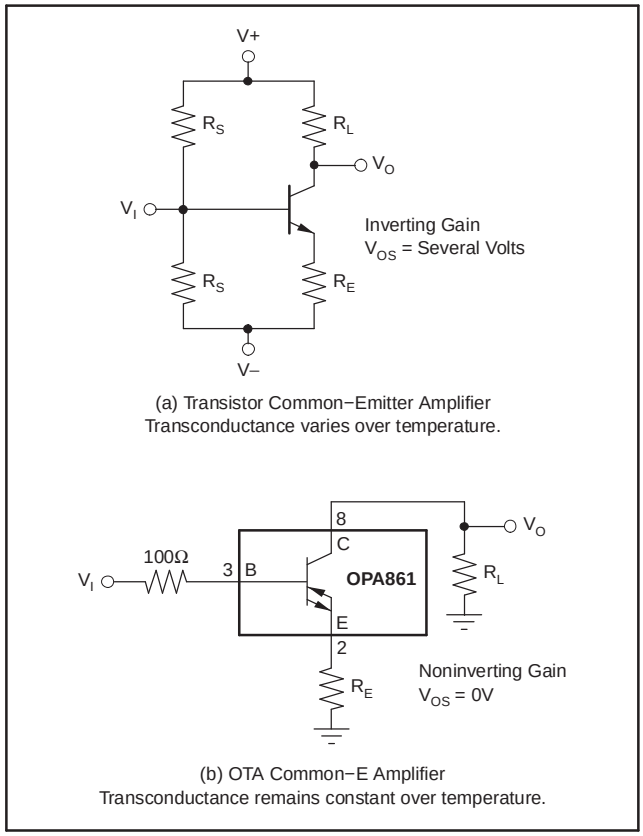


Figure 32. Common-Emitter vs Common-E Amplifier

The transconductance of the OTA with degeneration can be calculated by Equation 2:

$$g_{m_deg} = \frac{1}{\frac{1}{g_m} + R_E} \quad (2)$$

A positive voltage at the B-input, pin 3, causes a positive current to flow out of the C-input, pin 8. This gives a noninverting gain where the circuit of Figure 32a is inverting. Figure 32b shows an amplifier connection of the OPA861, the equivalent of a common-emitter transistor amplifier. Input and output can be ground-referenced without any biasing. The amplifier is non-inverting because of the sense of the output current.

The forward amplifier shown in Figure 33 and Figure 34 corresponds to one of the basic circuits used to characterize the OPA861. Extended characterization of this topology appears in the *Typical Characteristics* section of this datasheet.

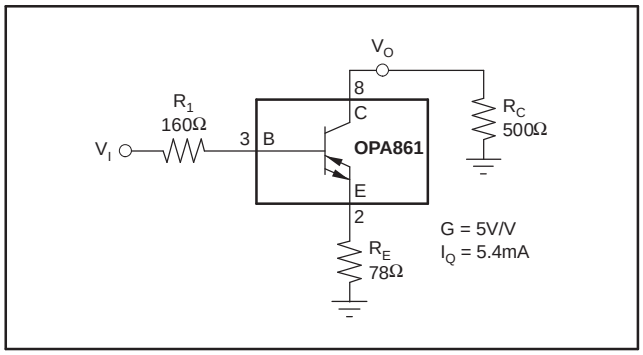


Figure 33. Forward Amplifier Configuration and Test Circuit

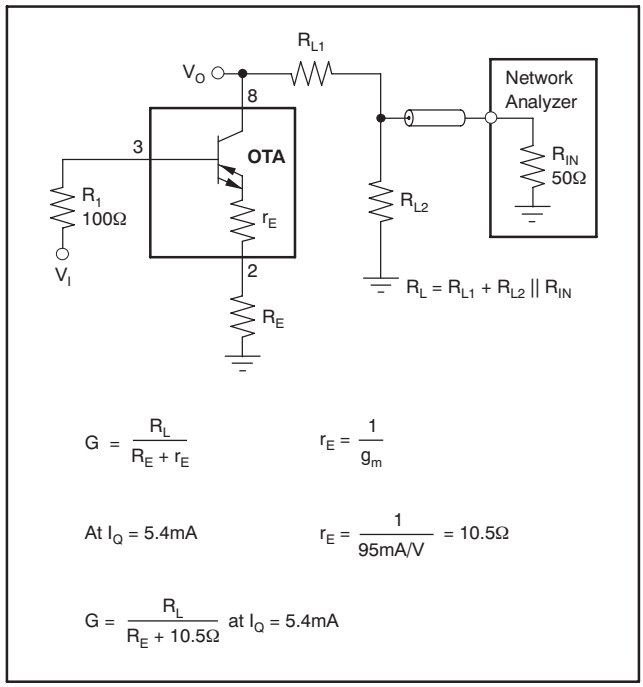


Figure 34. Forward Amplifier Design Equations

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Common-C Amplifier

Figure 35b shows the OPA861 connected as an E-follower—a voltage buffer. It is interesting to notice that the larger the R_E resistor, the closer to unity gain the buffer will be. If the OPA861 is to be used as a buffer, use $R_E \geq 500\Omega$ for best results. For the OPA861 used as a buffer, the gain is given by Equation 3:

$$G = \frac{1}{1 + \frac{1}{g_m \times R_E}} \approx 1 \quad (3)$$

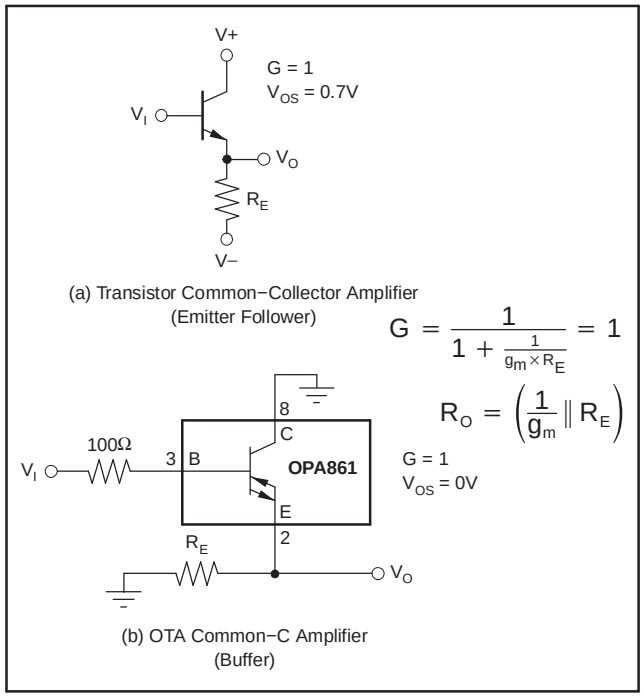


Figure 35. Common-Collector vs Common-C Amplifier

A low value resistor in series with the B-input is recommended. This resistor helps isolate trace parasitic from the inputs, reduces any tendency to oscillate, and controls frequency response peaking. Typical resistor values are from 25Ω to 200Ω.

Common-B Amplifier

Figure 36 shows the Common-B amplifier. This configuration produces an inverting gain and a low impedance input. Equation 4 shows the gain for this configuration.

$$G = \frac{R_L}{R_E + \frac{1}{g_m}} \approx -\frac{R_L}{R_E} \quad (4)$$

This low impedance can be converted to a high impedance by inserting the buffer amplifier in series.

Current-Mode Analog Computations

As mentioned earlier, the OPA861 can be used advantageously for analog computation. Among the application possibilities are functionality as a current amplifier, current differentiator, current integrator, current summer, and weighted current summer. Table 1 lists these different uses with the associated transfer functions.

These functions can easily be combined to form active filters. Some examples using these current-mode functions are shown later in this document.

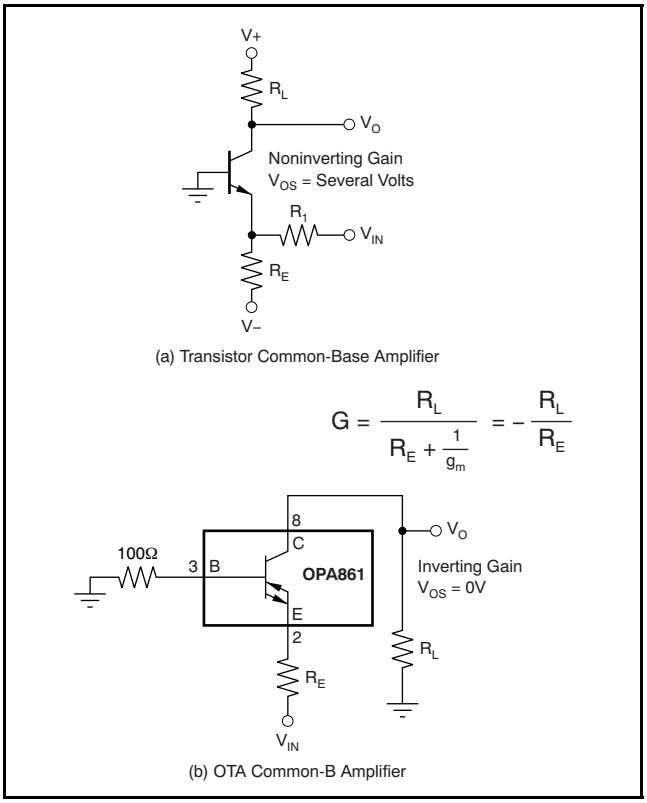
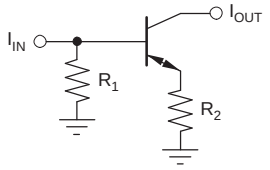
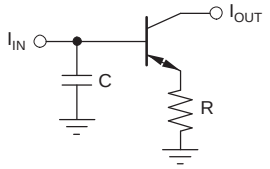
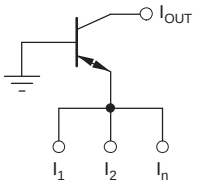
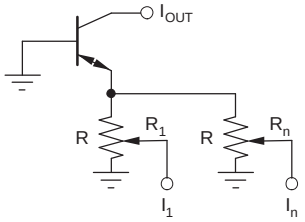


Figure 36. Common-Base Transistor vs Common-B OTA

Table 1. Current-Mode Analog Computation Using the OTA Section

FUNCTIONAL ELEMENT	TRANSFER FUNCTION	IMPLEMENTATION WITH THE OTA SECTION
Current Amplifier	$I_{OUT} = \frac{R_1}{R_2} \times I_{IN}$	
Current Integrator	$I_{OUT} = \frac{1}{C \times R \times \int I_{IN} dt}$	
Current Summer	$I_{OUT} = 1 \sum_{j=1}^{n} I_j$	
Weighted Current Summer	$I_{OUT} = 1 \sum_{j=1}^{n} I_j \times \frac{R_j}{R}$	

OPA861 APPLICATIONS

Control-Loop Amplifier

A new type of control loop amplifier for fast and precise control circuits can be designed with the OPA861. The circuit of Figure 37 illustrates a series connection of two voltage control current sources that have an integral (and at higher frequencies, a proportional) behavior versus frequency. The control loop amplifiers show an integrator behavior from DC to the frequency represented by the RC time constant of the network from the C-output to GND. Above this frequency, they operate as an amp with constant gain. The series connection increases the overall gain to about 110dB and thus minimizes the control loop deviation. The differential configuration at the inputs enables one to apply the measured output signal and the reference voltage to two identical high-impedance inputs. The output buffer decouples the C-output of the second OTA in order to insure the AC performance and to drive subsequent output stages.

DC-Restore Circuit

The OPA861 can be used advantageously with an operational amplifier, here the OPA656, as a DC-restore circuit. Figure 38 illustrates this design. Depending on the collector current of the transconductance amplifier (OTA) of the OPA861, a switching function is realized with the diodes D_1 and D_2.

When the C-output is sourcing current, the capacitor C_1 is being charged. When the C-output is sinking current, D_1 is turned off and D_2 is turned on, letting the voltage across C_1 be discharged through R_2.

The condition to charge C_1 is set by the voltage difference between V_{REF} and V_{OUT}. For the OTA C-output to source current, V_{REF} has to be greater than V_{OUT}. The rate of charge of C_1 is set by both R_1 and C_1. The discharge rate is given by R_2 and C_1.

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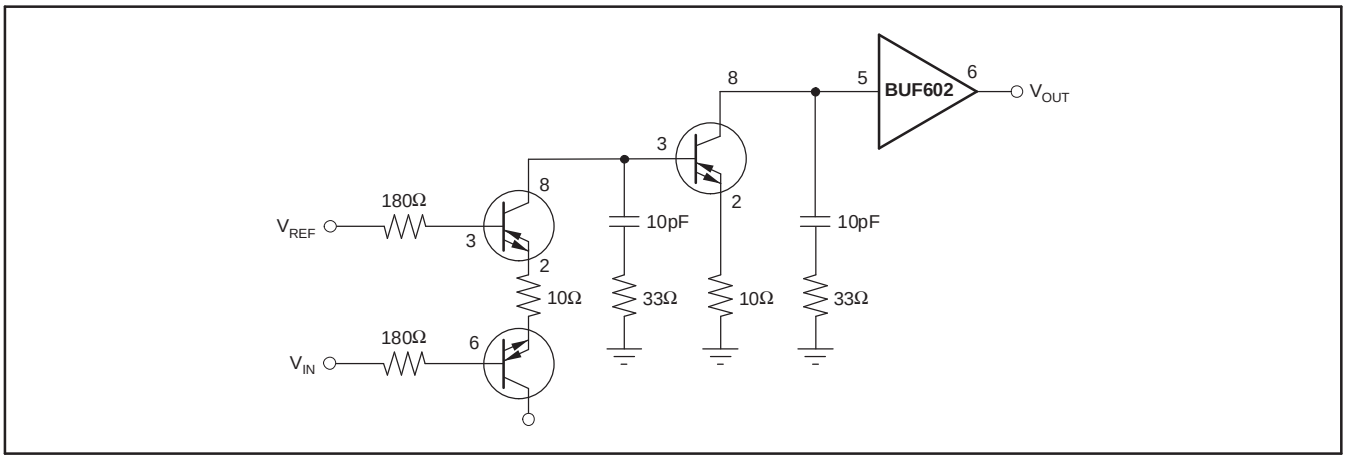


Figure 37. Control-Loop Amplifier Using Three OPA861s

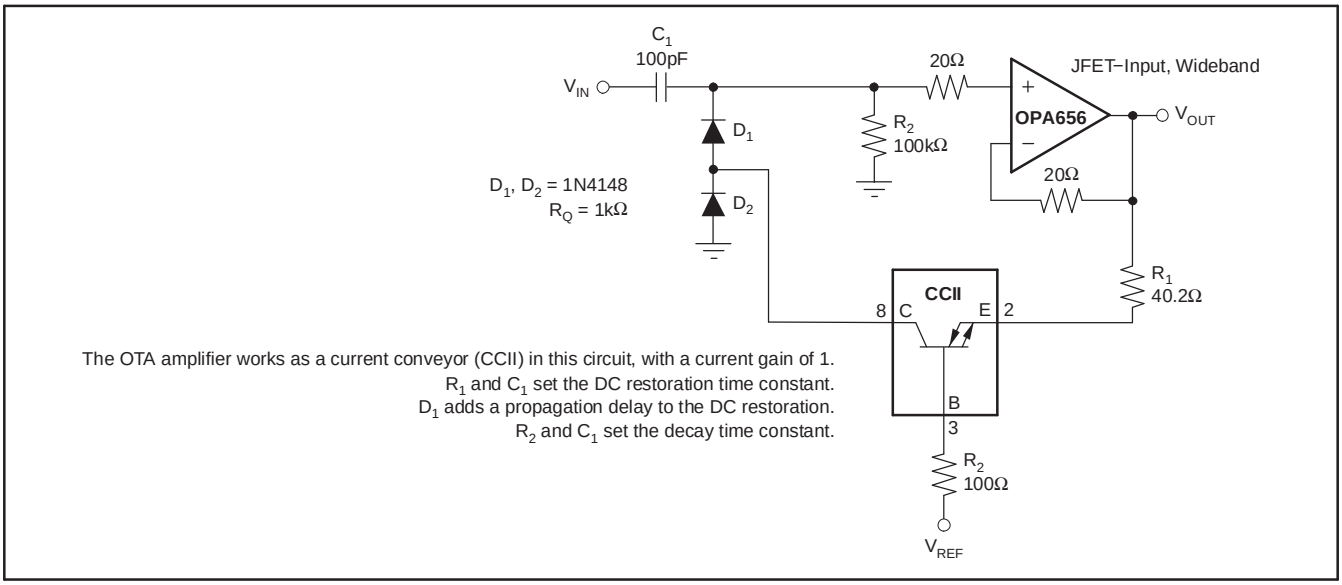


Figure 38. DC Restorer Circuit

Negative Impedance Converter Filter: Low-Pass Filter

The OPA861 can be used as a negative impedance converter to realize the low-pass filer shown in Figure 39.

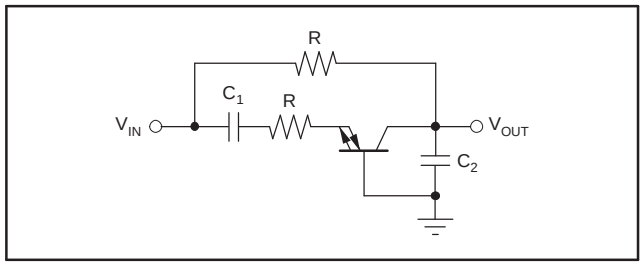


Figure 39. Low-Pass Negative Impedance Converter Filter

The transfer function is shown in Equation 5:

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{1 + sR(C_1 + C_2) + s^2C_1C_2R^2} \quad (5)$$

with:

$$\omega_0 = \frac{1}{\sqrt{C_1C_2}R}$$

$$Q = \frac{\sqrt{C_1C_2}}{C_1 + C_2}$$

The input impedance is shown in Equation 6:

$$Z_{IN} = \frac{1}{2sC} + R\frac{1 + sRC}{1 + 2sRC} \quad (6)$$

Figure 40 shows the frequency responses for low-pass, Butterworth filters set at 20kHz and 10MHz.

For the 20kHz filter, set R to 1kΩ and $C_1 = \frac{1}{2} \times C_2 = 5.6\mu F$. For the 10MHz filter, the parasitic capacitance at the output pin needs to be taken into consideration. In the example of Figure 40, the parasitic is 3pF, which gives us the settings of R = 1.13kΩ, C_1 = 10pF, and C_2 = 17pF.

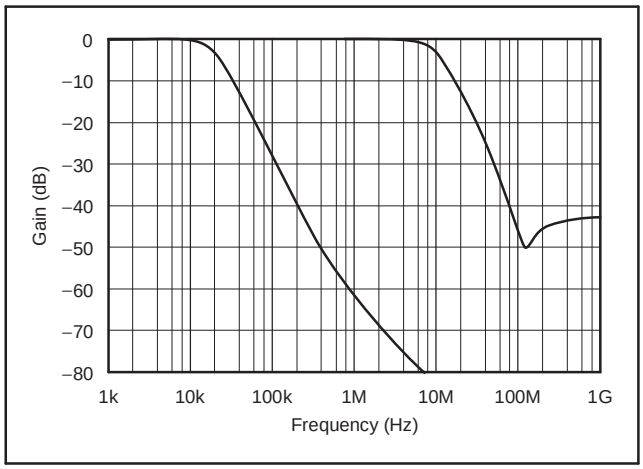


Figure 40. Small-Signal Frequency Response for a Low-Pass Negative Impedance Converter Filter

Differential Line Driver/Receiver

The wide bandwidth and high slew rate of the OPA861 current-mode amplifier make it an ideal line driver. The circuit in Figure 42 makes use of two OPA861s to realize a single-ended to differential conversion. The high-impedance current source output of the OPA861 allows it to drive low-impedance or capacitive loads without series resistances and avoids any attenuation that would have otherwise occured in the resistive network.

The OPA861 used as a differential receiver exhibits excellent common-mode rejection ratio, as can be seen in Figure 41.

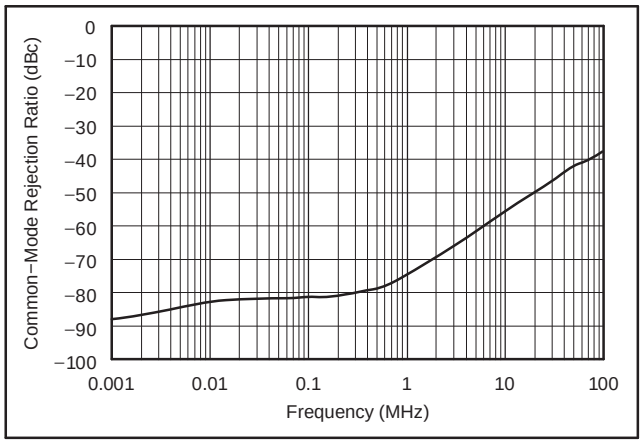


Figure 41. Differential Driver Common-Mode Rejection Ratio for $2V_{PP}$ Input Signals

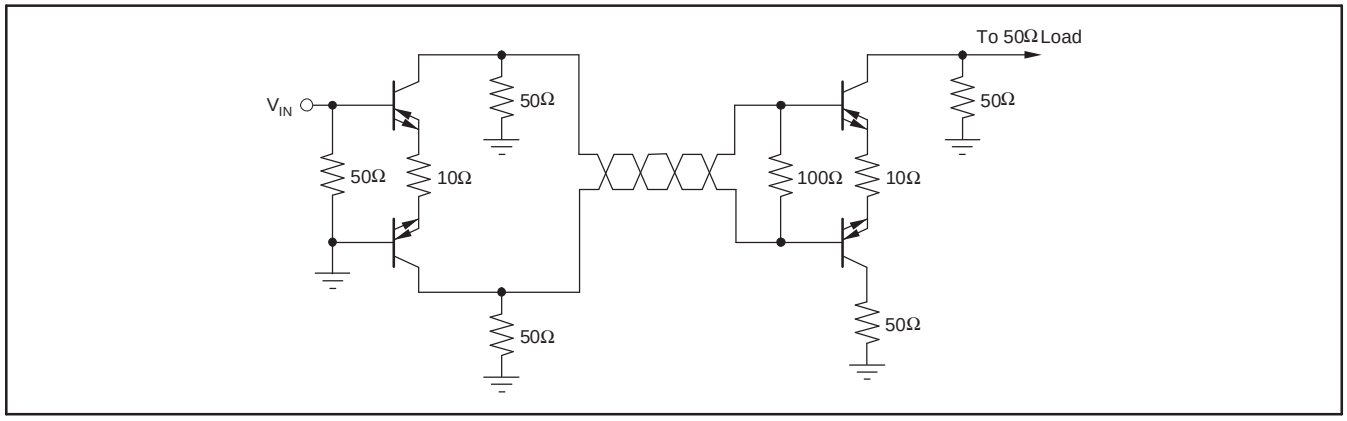


Figure 42. Twisted-Pair Differential Driver and Receiver with the OPA861

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ACTIVE FILTERS USING THE OPA861 IN CURRENT CONVEYOR STRUCTURE

One further example of the versatility of the Diamond Transistor and Buffer is the construction of high-frequency (> 10MHz) active filters. Here, the Current Conveyor structure, shown in Figure 43, is used with the Diamond Transistor as a Current Conveyor.

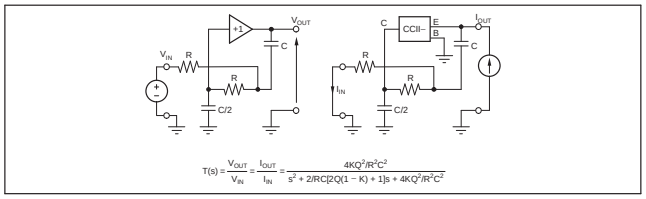


Figure 43. Current Conveyor

The method of converting RC circuit loops with operational amplifiers in Current Conveyor structures is based upon the adjoint network concept. A network is reversible or reciprocal when the transfer function does not change even when the input and output have been exchanged. Most networks, of course, are nonreciprocal. The networks of Figure 44, perform interreciprocally when the input and output are exchanged, while the original network, N, is exchanged for a new network N_A. In this case, the transfer function remains the same, and N_A is the adjoing network. It is easy to construct an adjoint network for any given circuit, and these networks are the base for circuits in Current-Conveyor structure. Individual elements can be interchanged according to the list in Figure 45. Voltage sources at the input become short circuits, and the current flowing there becomes the output variable. In contrast, the voltage output becomes the input, which is excitated by a current source. The following equation describes the interreciprocal features of the circuit: $V_{OUT}/V_{IN} = I_{OUT}/I_{IN}$. Resistances and capacitances remain unchanged. In the final step, the operational amplifier with infinite input impedance and 0Ω output impedance is transformed into a current amplifier with 0Ω input impedance and infinite output impedance. A Diamond Transistor with the base at ground comes quite close to an ideal current amplifier. The well-known Sallen-Key low-pass filter with positive feedback, is an example of conversion into Current-Conveyor structure, see Figure 46. The positive gain of the operational amplifier becomes a negative second type of Current Conveyor (CCII), as shown in Figure 43. Both arrangements have identical transfer functions and the same level of sensitivity to deviations. The most recent implementation of active filters in a Current-Conveyor structure produced a second-order Bi-Quad filter. The value of the resistance in the emitter of the Diamond Transistor controls the filter characteristic. For more information, refer to application note SBOS047, *New Ultra High-Speed Circuit Techniques with Analog ICs*.

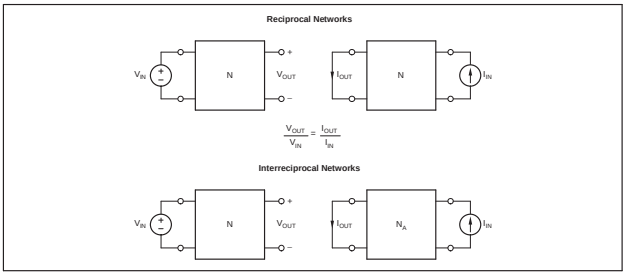


Figure 44. Networks

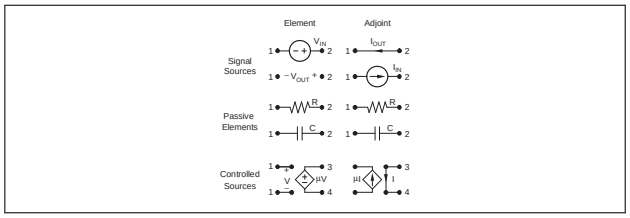


Figure 45. Individual Elements in the Current Conveyor

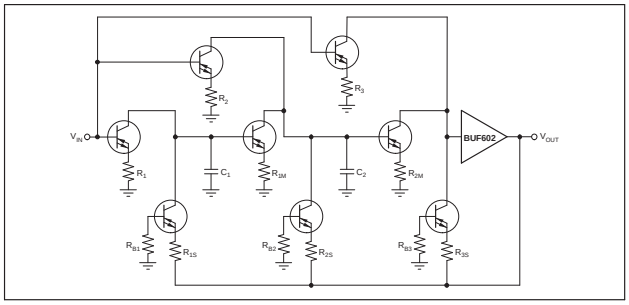


Figure 46. Universal Active Filter

Transfer Function

The transfer function of the universal active filter of Figure 46 is shown in Equation 7.

$$F(p) = \frac{V_{OUT}}{V_{IN}} = \frac{s^2C_1C_2R_{1M}\frac{R_{2M}}{R_3} + sC_1\frac{R_{1M}}{R_2} + \frac{1}{R_1}}{s^2C_1C_2R_{1M}\frac{R_{2M}}{R_{3S}} + sC_1\frac{R_{1M}}{R_{2S}} + \frac{1}{R_{1S}}} \quad (7)$$

Filter Characteristics

Five filter types can be made with this structure:

- For a low-pass filter, set $R_2 = R_3 = \infty$,
- For a high-pass filter, set $R_1 = R_2 = \infty$,
- For a bandpass filter, set $R_1 = R_3 = \infty$,
- For a band rejection filter, set $R_2 = \infty$; $R_1 = R_3$,
- For an all-pass filter, set $R_1 = R_{1S}$; $R_2 = R_{2S}$; and $R_3 = R_{3S}$.

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A few designs for a low-pass filter are shown in Figure 47 and Table 2.

Table 2. Component Values for Filters Shown In Figure 47

f_O	R	R_O	C_O
1MHz	150	100	2nF
20MHz	150	100	112.5pF
50MHz	150	100	25pF

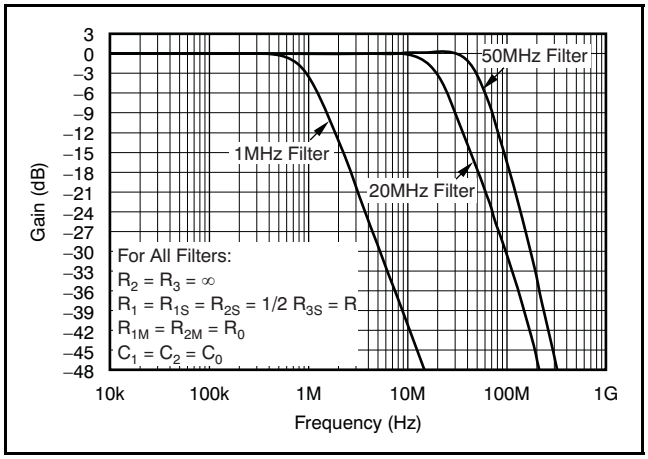


Figure 47. Butterworth Low-Pass Filter with the Universal Active Filter

The advantages of building active filters using a Current Conveyor structure are:

- The increase in output resistance of operational amplifiers at high frequencies makes it difficult to construct feedback filter structures (decrease in stop-band attenuation).
- All filter coefficients are represented by resistances, making it possible to adjust the filter frequency response without affecting the filter coefficients.
- The capacitors which determine the frequency are located between the ground and the current source outputs and are thus grounded on one side. Therefore, all parasitic capacitances can be viewed as part of these capacitors, making them easier to comprehend.
- The features which determine the frequency characteristics are currents, which charge the integration capacitors. This situation is similar to the transfer characteristic of the Diamond Transistor.

High-CMRR, Moderate Precision, Differential I/O ADC Driver

The circuit shown in Figure 48 depicts an ADC driver implemented with two OPA861s. Since the gain is set here by the ratio of the internal 600Ω resistors and R_E, its accuracy will only be as good as the input resistor of the ADS5272. The small-signal frequency response for this circuit has 150MHz at –3dB bandwidth for a gain of approximately 5.6dB, as shown in Figure 49. The advantage of this circuit lies in its high CMRR to 100kHz; see Figure 50. This circuit also has more than 10 bits of linearity.

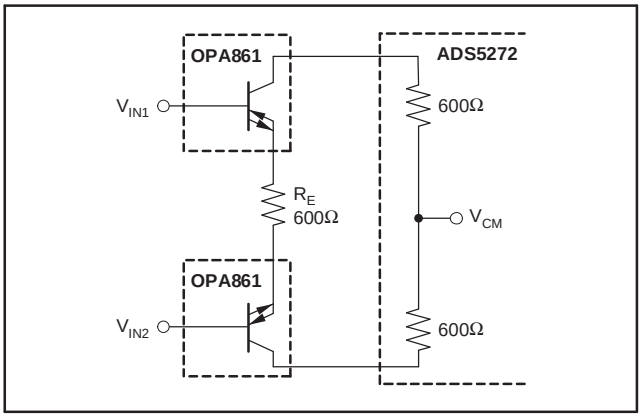


Figure 48. High CMRR, Moderate Precision, Differential I/O ADC Driver

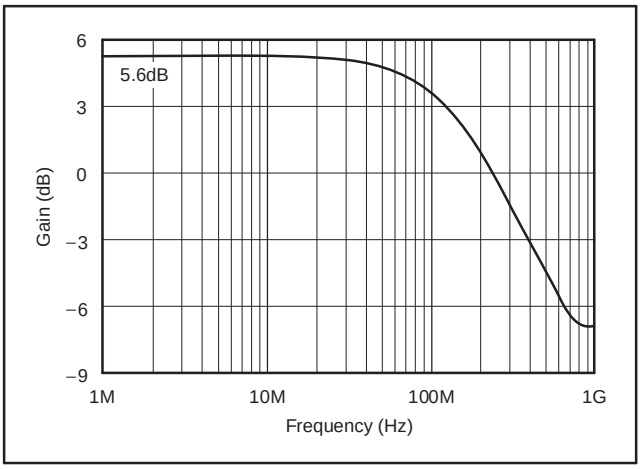


Figure 49. ADC Driver, Small-Signal Frequency Response

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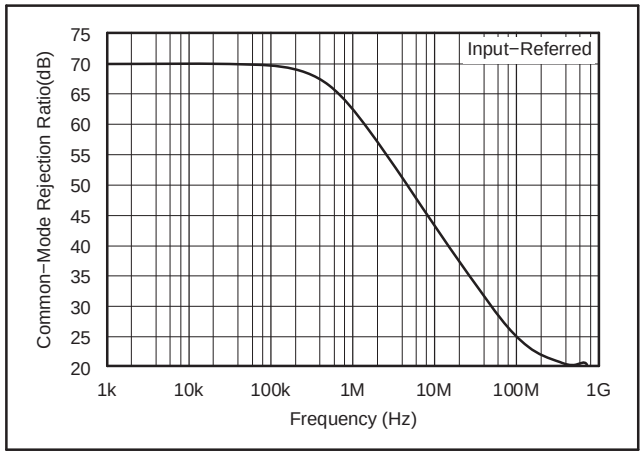


Figure 50. CMRR of the ADC Driver

DESIGN-IN TOOLS

DEMONSTRATION BOARDS

A printed circuit board (PCB) is available to assist in the initial evaluation of circuit performance using the OPA861. This module is available free, as an unpopulated PCB delivered with descriptive documentation. The summary information for the board is shown below:

PRODUCT	PACKAGE	BOARD PART NUMBER	LITERATURE REQUEST NUMBER
OPA861ID	SO-8	DEM-OTA-SO-1A	SBOU035

The board can be requested on the Texas Instruments web site (www.ti.com).

MACROMODELS AND APPLICATIONS SUPPORT

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. This principle is particularly true for Video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. A SPICE model for the OPA861 is available through the Texas Instruments web page (www.ti.com). These models do a good job of predicting small-signal AC and transient performance under a wide variety of operating conditions. They do not do as well in predicting the harmonic distortion. These models do not attempt to distinguish between the package types in their small-signal AC performance.

NOISE PERFORMANCE

The OTA noise model consists of three elements: a voltage noise on the B-input; a current noise on the B-input; and a current noise on the E-input. Figure 51 shows the OTA noise analysis model with all the noise terms included. In this model, all noise terms are taken to be noise voltage or current density terms in either nV/√Hz or pA/√Hz.

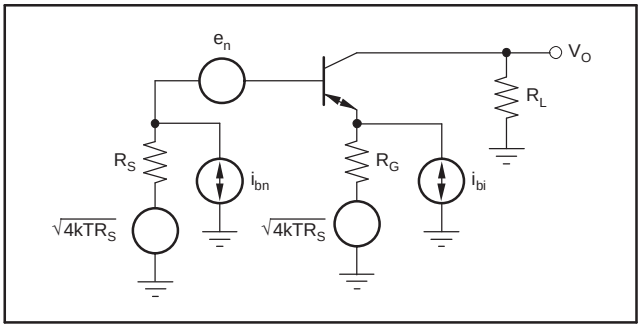


Figure 51. OTA Noise Analysis Model

The total output spot noise voltage can be computed as the square root of the sum of all squared output noise voltage contributors. Equation 8 shows the general form for the output noise voltage using the terms shown in Figure 51.

$$e_O = \sqrt{\left[e_N^2 + (R_S i_{BN})^2 + 4kTR_S + (R_G i_{BI})^2 + 4kTR_G\right]\left(\frac{R_L}{R_G + \frac{1}{g_m}}\right)^2} \quad (8)$$

THERMAL ANALYSIS

Maximum desired junction temperature will set the maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed 150°C.

Operating junction temperature (T_J) is given by $T_A + P_D \times \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver output current. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} will depend on the required output signal and load but would, for the OPA861 be at a maximum when the maximum I_O is being driven into a voltage source that puts the maximum voltage across the output stage. Maximum I_O is 15mA times a 9V maximum across the output.

Note that it is the power in the output stage and not into the load that determines internal power dissipation.

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As a worst-case example, compute the maximum T_J using an OPA861IDBV in the circuit of Figure 32b operating at the maximum specified ambient temperature of +85°C and driving a –1V voltage reference.

$P_D = 10V \times 5.4mA + (15mA \times 9V) = 185mW$

Maximum $T_J = +85°C + (0.19W \times 150°C/W) = 114°C$.

Although this is still well below the specified maximum junction temperature, system reliability considerations may require lower tested junction temperatures. The highest possible internal dissipation will occur if the load requires current to be forced into the output for positive output voltages or sourced from the output for negative output voltages. This puts a high current through a large internal voltage drop in the output transistors.

BOARD LAYOUT GUIDELINES

Achieving optimum performance with a high-frequency amplifier like the OPA861 requires careful attention to board layout parasitics and external component types. Recommendations that will optimize performance include:

a) Minimize parasitic capacitance to any AC ground for all of the signal I/O pins. Parasitic capacitance on the inverting input pin can cause instability: on the noninverting input, it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) Minimize the distance (< 0.25") from the power-supply pins to high-frequency 0.1µF decoupling capacitors. At the device pins, the ground and power-plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections should always be decoupled with these capacitors. An optional supply decoupling capacitor (0.1µF) across the two power supplies (for bipolar operation) will improve 2nd-harmonic distortion performance. Larger (2.2µF to 6.8µF) decoupling capacitors, effective at lower frequency, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board.

c) Careful selection and placement of external components will preserve the high-frequency performance of the OPA861. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal film or carbon composition, axially-leaded resistors can also provide good high-frequency performance. Again, keep their leads and PC board traces as short as possible. Never use wirewound type resistors in a high-frequency application.

d) Connections to other wideband devices on the board may be made with short, direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50mils to 100mils) should be used, preferably with ground and power planes opened up around them.

e) Socketing a high-speed part like the OPA861 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network that makes it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA861 onto the board.

INPUT AND ESD PROTECTION

The OPA861 is built using a very high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the *Absolute Maximum Ratings* table. All device pins are protected with internal ESD protection diodes to the power supplies as shown in Figure 52.

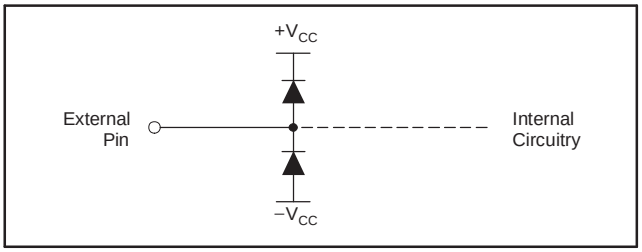


Figure 52. Internal ESD Protection

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (for example, in systems with ±15V supply parts driving into the OPA861), current-limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible since high values degrade both noise performance and frequency response.

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REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (May 2011) to Revision G **Page**

- Changed transfer function equations in *Negative Impedance Converter Filter: Low-Pass Filter* section 17

Changes from Revision E (August 2008) to Revision F **Page**

- Updated Figure 30 12
- Updated Equation 8 21

Changes from Revision D (August 2006) to Revision E **Page**

- Changed storage temperature range rating in *Absolute Maximum Ratings* table from –40°C to +125°C to –65°C to +125°C 2

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA861ID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 861
OPA861ID.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 861
OPA861IDBVT	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NSR
OPA861IDBVT.A	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NSR

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

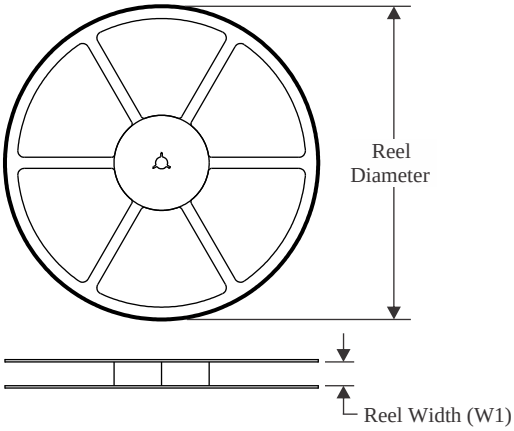
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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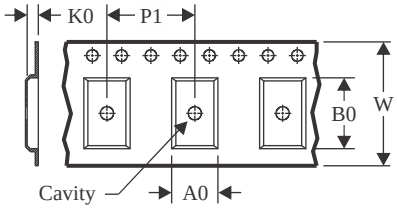
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

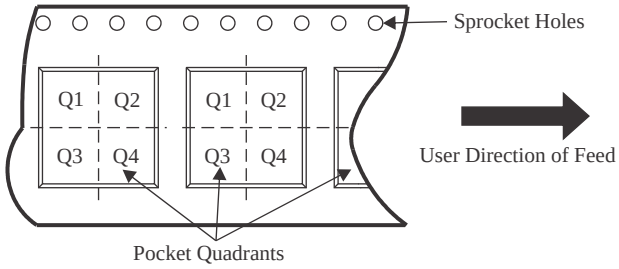


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

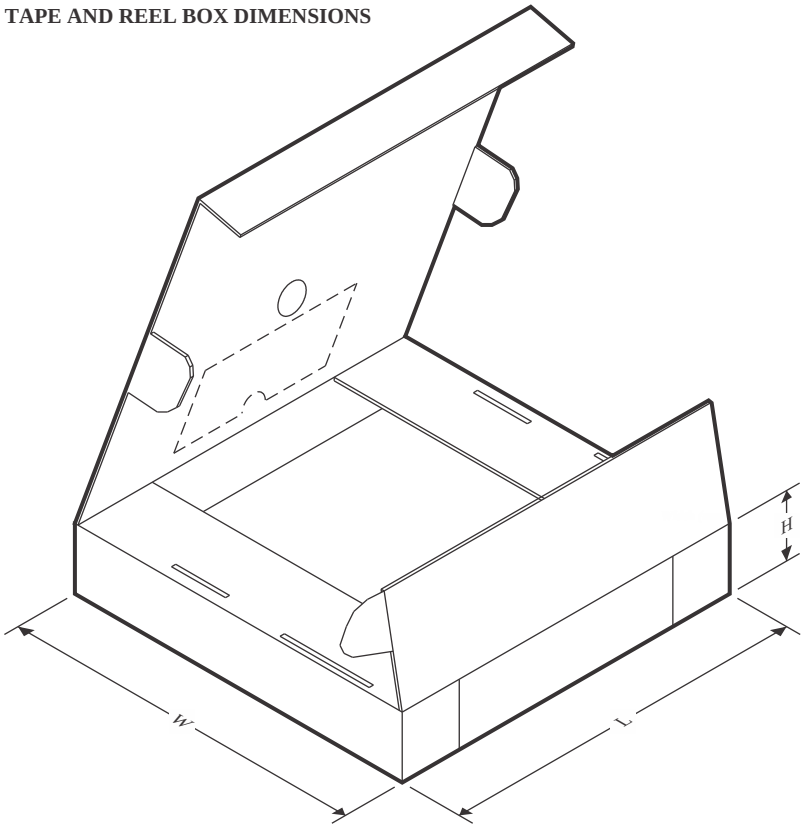
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA861IDBVT	SOT-23	DBV	6	250	180.0	8.4	3.15	3.1	1.55	4.0	8.0	Q3

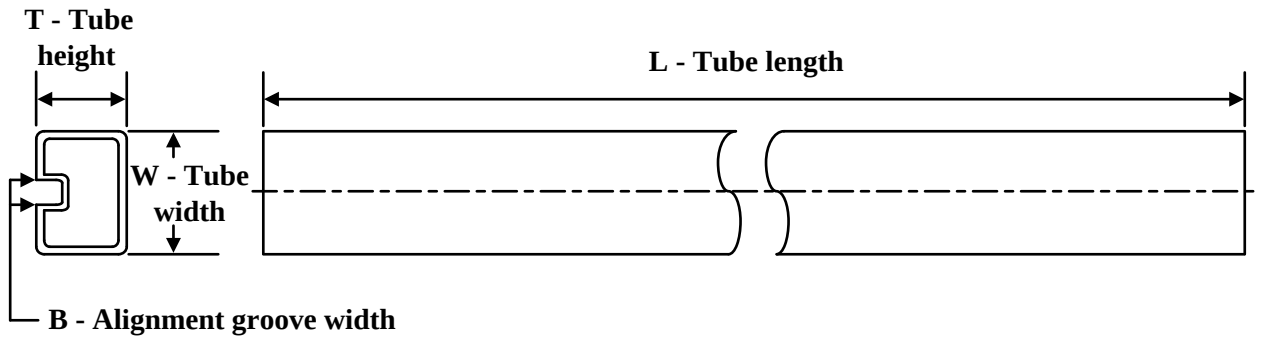
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA861IDBVT	SOT-23	DBV	6	250	213.0	191.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA861ID	D	SOIC	8	75	506.6	8	3940	4.32
OPA861ID.A	D	SOIC	8	75	506.6	8	3940	4.32

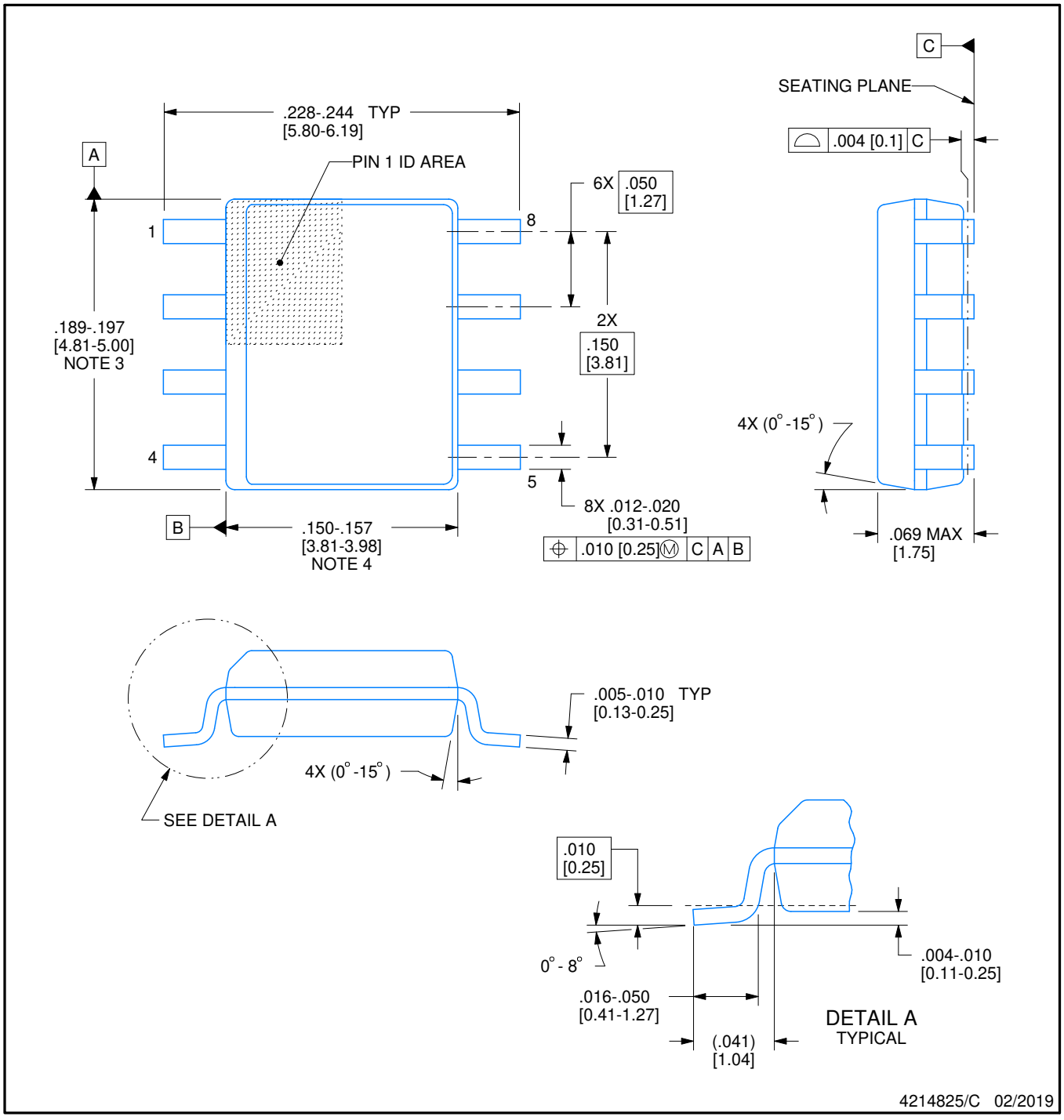


PACKAGE OUTLINE

D0008A

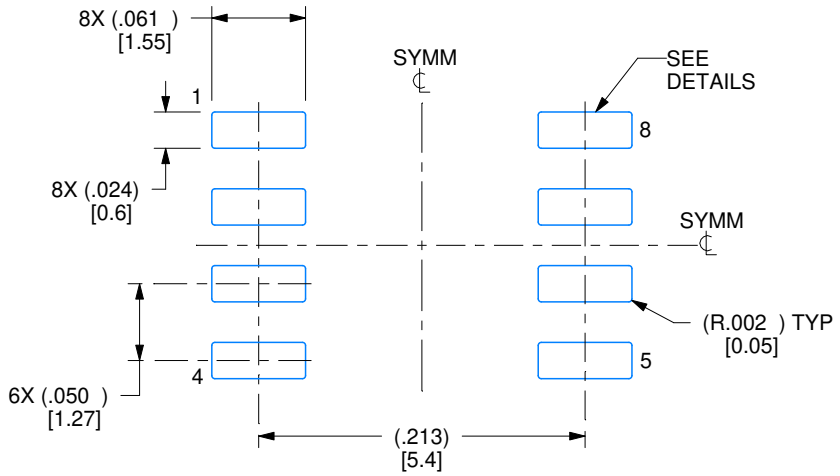
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

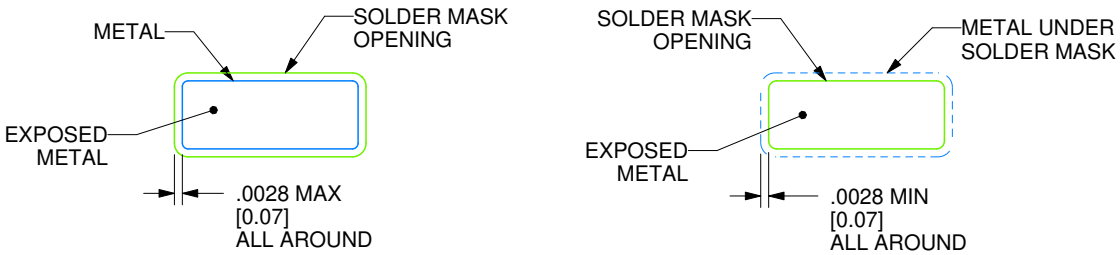


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

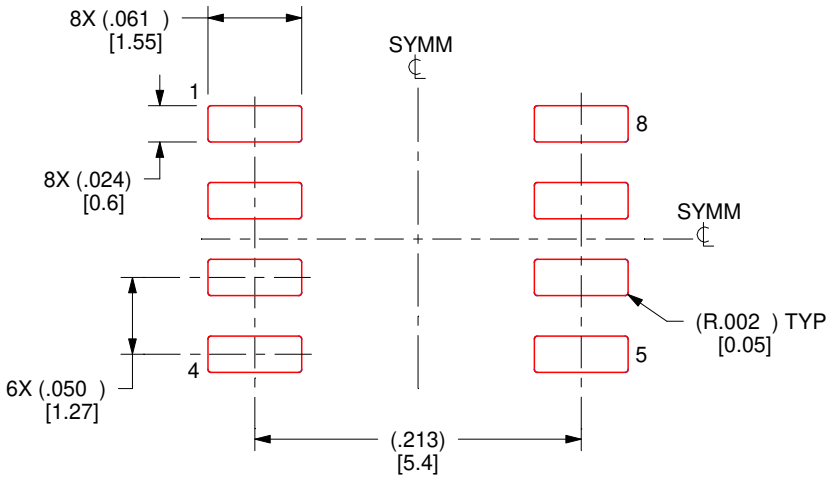
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

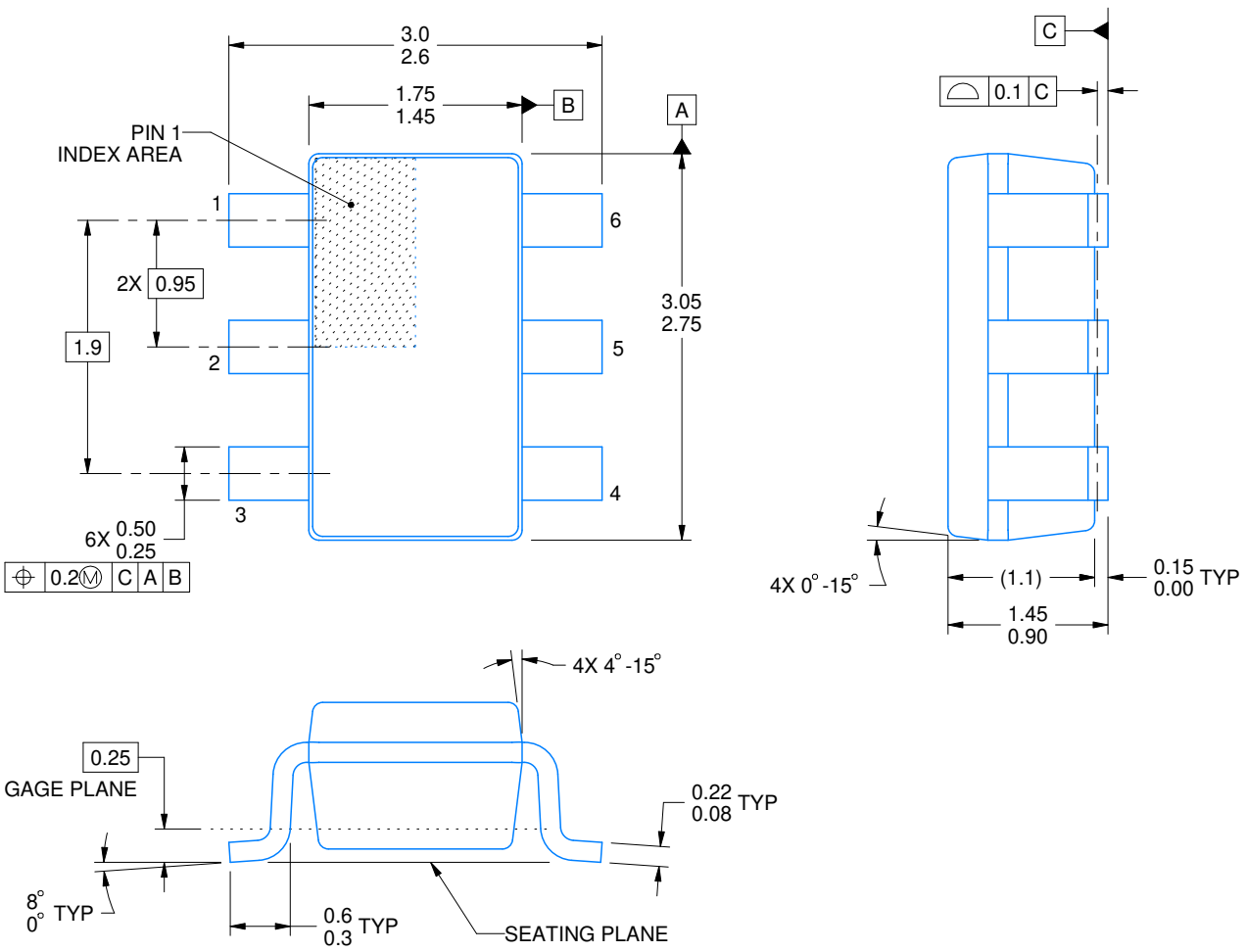
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

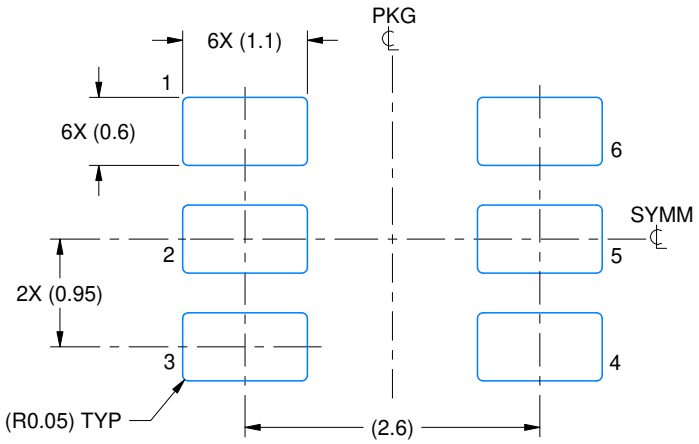
SMALL OUTLINE TRANSISTOR



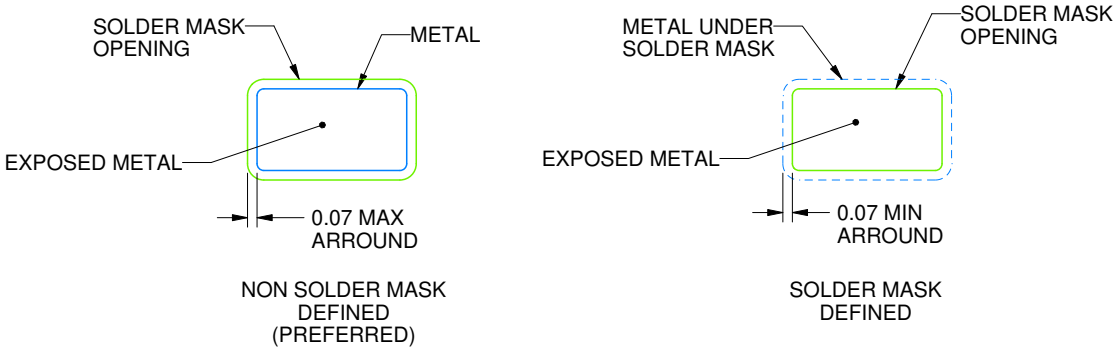
4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

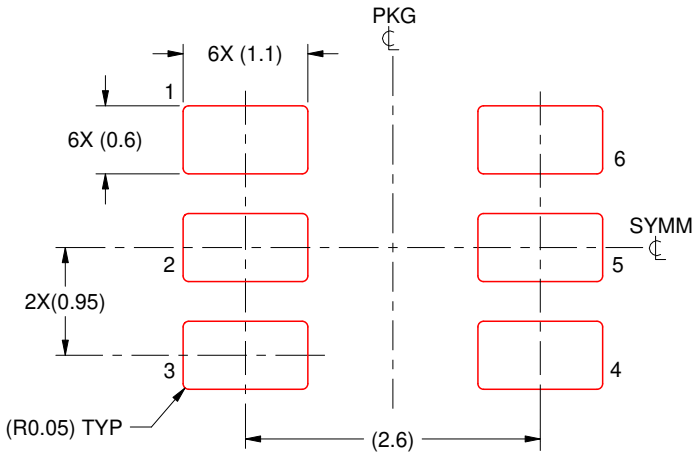


SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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