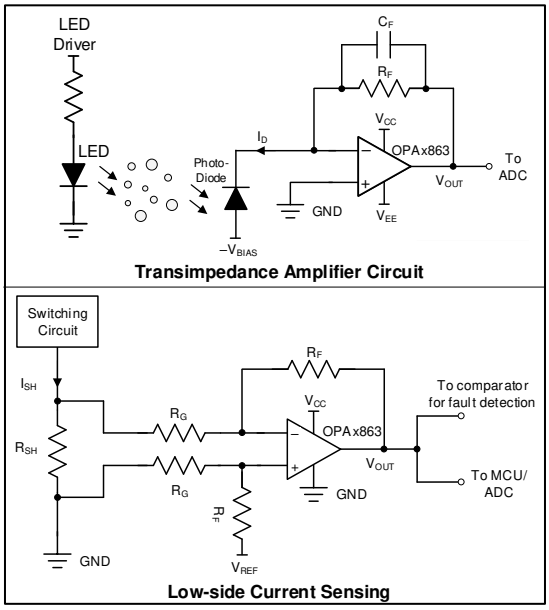
OPAx863 Low-Power, 110-MHz, Rail-to-Rail Input/Output Voltage-Feedback Op Amps

1 Features

- Wide-bandwidth
  - Unity-gain bandwidth: 110-MHz (A_V= 1 V/V)
  - Gain-bandwidth product: 50-MHz
- Low power
  - Quiescent current: 700-µA/ch (typical)
  - Power down mode: 1.5-µA (maximum, V_S= 3 V)
  - Supply voltage: 2.7-V to 12.6-V
- Input voltage noise: 5.9-nV/√Hz
- Slew rate: 105-V/µs
- Rail-to-rail input and output
- HD_2/HD_3: –129 dBc/–138 dBc at 20 kHz (2-V_{PP})
- Operating temperature range: –40°C to +125°C
- Additional features:
  - Overload power limit
  - Output short-circuit protection
- High-precision version: OPAx863A

2 Applications

- Low-power SAR and ΔΣ ADC driver
- ADC reference buffer
- Low-side current sensing
- Photodiode TIA interface
- Inductive sensing
- Ultrasonic flow meter
- Multifunction printer
- MDAC output buffer
- Gain and active filter stages



Application Circuits Using OPAx863

3 Description

The OPAx863 devices are low-power, unity-gain stable, rail-to-rail input and output, voltage-feedback operational amplifiers designed to operate over a power-supply range of 2.7 V to 12.6 V. Consuming only 700 µA per channel, the OPAx863 offers a gain-bandwidth product of 50 MHz, slew rate of 105 V/µs with a voltage noise density of 5.9 nV/√Hz.

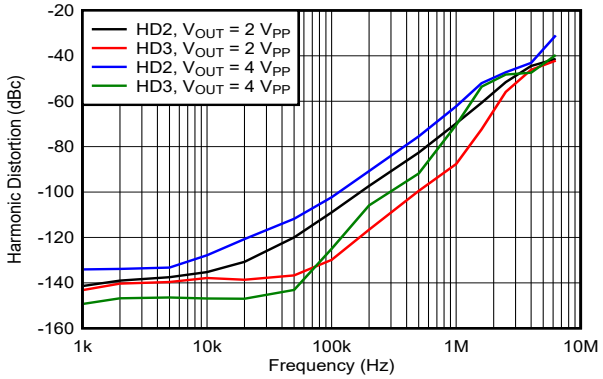
The rail-to-rail input stage with 2.7-V supply operation is useful in portable, battery-powered applications. The rail-to-rail input stage is well-matched for gain-bandwidth product and noise across the full input common-mode voltage range, enabling excellent performance with wide-input dynamic range. The OPAx863 feature a power-down (PD) mode with a PD quiescent current (I_Q) of 1.5-µA (maximum) and a turn-on or turn-off time within 6.5-µs using a 3-V supply.

The OPAx863 includes overload power limiting to limit the increase in I_Q with saturated outputs, thereby preventing excessive power dissipation in power-conscious, battery-operated systems. The output stage is short-circuit protected, making these devices conducive to ruggedized environments.

Device Information(1)(2)

PART NUMBER	CHANNEL COUNT	PACKAGE
OPA863	Single	DBV (SOT-23, 5)
		DBV (SOT-23, 6)
OPA2863	Dual	DGK (VSSOP, 8)
		RUN (WQFN, 10)
		D (SOIC, 8)
OPA4863	Quad	PW (TSSOP, 14)

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) For related products, see *Device Comparison*



Distortion Performance in G = 1 V/V

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision I (December 2022) to Revision J (June 2023)	Page
• Changed the status of OPA4863 PW package, 14-pin TSSOP from: *preview* to: *production* and added associated content	1

Changes from Revision H (August 2022) to Revision I (December 2022)	Page
• Changed the status of the DBV package, 5-pin SOT23 from: *preview* to: *production*	1

Changes from Revision G (July 2022) to Revision H (August 2022)	Page
• Changed the status of the RUN Package, from: *preview* to: *production*	3

Changes from Revision F (April 2022) to Revision G (July 2022)	Page
• Added OPAx863A information to the *Features* section	1
• Added the DBV package, 5-pin SOT23 to the data sheet	1
• Changed the status of the D Package, from: *preview* to: *production*	3
• Updated the *Output Voltage vs Load Current* and *Output Voltage vs Load Current* figures to show typical device performance	12

Changes from Revision E (November 2021) to Revision F (April 2022)	Page
• Added the D package, 8-pin SOIC and RUN package, 10-pin WQFN to the data sheet	1

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5 Device Comparison Table

DEVICE	$\pm V_S$ (V)	I_Q / CHANNEL (mA)	GBWP (MHz)	SLEW RATE (V/µs)	VOLTAGE NOISE (nV/√Hz)	AMPLIFIER DESCRIPTION
OPA2863	±6.3	0.70	50	105	5.9	Unity-gain stable RRIO Bipolar Amplifier
LMH6643	±6.4	2.7	65	130	17	Unity-gain stable NRI/RRO Bipolar Amplifier
OPAx810	±13.5	3.6	70	200	6.3	Unity-gain stable RRIO FET-Input Amplifier
OPAx837	±2.7	0.6	50	105	4.7	Unity-gain stable NRI/RRO Bipolar Amplifier
OPAx607	±2.75	0.9	50	24	3.8	Decompensated Gain of 6 V/V stable CMOS Amplifier

6 Pin Configuration and Functions

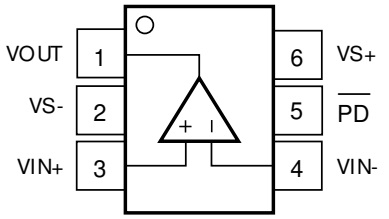


Figure 6-1. OPA863 DBV Package, 6-Pin SOT-23 (Top View)

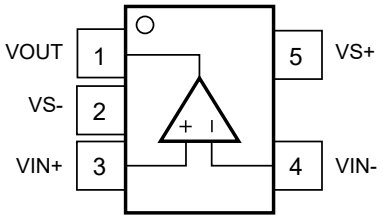


Figure 6-2. OPA863 DBV Package, 5-Pin SOT-23 (Top View)

Table 6-1. Pin Functions: OPA863

PIN			TYPE(1)	DESCRIPTION
NAME	NO.			
	DBV (SOT-23, 5)	DBV (SOT-23, 6)		
$\overline{PD}$	—	5	I	Power down. Low = disabled, high = normal operation (pin must be driven).
VIN+	3	3	I	Noninverting input pin
VIN–	4	4	I	Inverting input pin
VOUT	1	1	O	Output pin
VS–	2	2	P	Negative power-supply pin
VS+	5	6	P	Positive power-supply pin

(1) I = input, O = output, and P = power.

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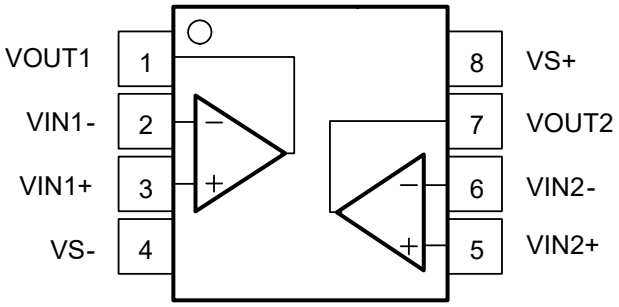


Figure 6-3. OPA2863 D Package, 8-Pin SOIC and DGK Package, 8-Pin VSSOP, (Top View)

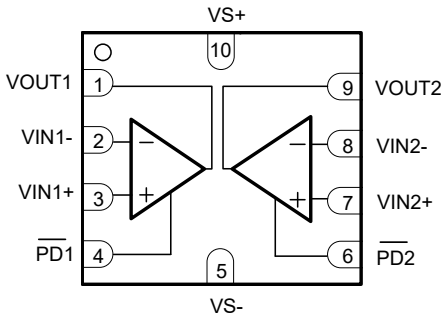


Figure 6-4. OPA2863 RUN Package, 10-Pin WQFN (Top View)

Table 6-2. Pin Functions: OPA2863

PIN			TYPE[1]	DESCRIPTION
NAME	NO.			
	D (SOIC), DGK (VSSOP)	RUN (WQFN)		
$\overline{PD1}$	—	4	I	Amplifier 1 power down. Low = disabled, high = normal operation (pin must be driven).
$\overline{PD2}$	—	6	I	Amplifier 2 power down. Low = disabled, high = normal operation (pin must be driven).
VIN1–	2	2	I	Amplifier 1 inverting input pin
VIN1+	3	3	I	Amplifier 1 noninverting input pin
VIN2–	6	8	I	Amplifier 2 inverting input pin
VIN2+	5	7	I	Amplifier 2 noninverting input pin
VOUT1	1	1	O	Amplifier 1 output pin
VOUT2	7	9	O	Amplifier 2 output pin
VS–	4	5	P	Negative power-supply pin
VS+	8	10	P	Positive power-supply pin

(1) I = input, O = output, and P = power.

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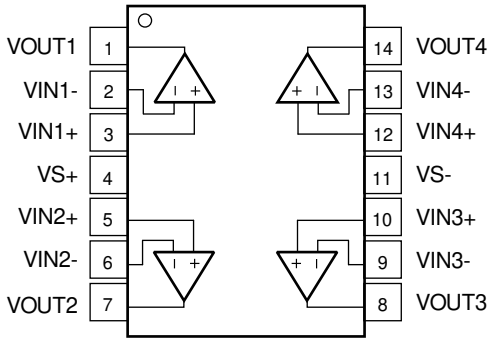


Figure 6-5. OPA4863 PW Package, 14-Pin TSSOP (Top View)

Table 6-3. Pin Functions: OPA4863

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
VIN1–	2	I	Amplifier 1 inverting input pin
VIN1+	3	I	Amplifier 1 noninverting input pin
VIN2–	6	I	Amplifier 2 inverting input pin
VIN2+	5	I	Amplifier 2 noninverting input pin
VIN3–	9	I	Amplifier 3 inverting input pin
VIN3+	10	I	Amplifier 3 noninverting input pin
VIN4–	13	I	Amplifier 4 inverting input pin
VIN4+	12	I	Amplifier 4 noninverting input pin
VOUT1	1	O	Amplifier 1 output pin
VOUT2	7	O	Amplifier 2 output pin
VOUT3	8	O	Amplifier 3 output pin
VOUT4	14	O	Amplifier 4 output pin
VS–	11	P	Negative power-supply pin
VS+	4	P	Positive power-supply pin

(1) I = input, O = output, and P = power.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
$V_{S–}$ to V_{S+}	Supply voltage		13	V
	Supply turn-on/off maximum dV/dt, DBV-6 and D packages		0.1	V/µs
V_I	Input voltage	$V_{S–}$ – 0.5	V_{S+} + 0.5	V
V_{ID}	Differential input voltage		±1	V
I_I	Continuous input current(2)		±10	mA
I_O	Continuous output current(3)		±30	mA
	Continuous power dissipation	See *Thermal Information*		
T_J	Maximum junction temperature		150	°C
T_A	Operating free-air temperature	–40	125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Continuous input current limit for both the ESD diodes to supply pins and amplifier differential input clamp diode. The differential input clamp diode limits the voltage across it to 1 V with this continuous input current flowing through it.
(3) Long-term continuous current for electromigration limits.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{S+} – V_{S–}$	Total supply voltage	2.7	10	12.6	V
T_A	Ambient temperature	–40	25	125	°C

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7.4 Thermal Information: OPA863

THERMAL METRIC[1]		OPA863		UNIT
		DBV (SOT-23)		
		5 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	168.3	161.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	64.3	73.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	40.6	42.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	14.2	21.2	°C/W
Y_{JB}	Junction-to-board characterization parameter	40.3	42.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Thermal Information: OPA2863

THERMAL METRIC[1]		OPA2863			UNIT
		DGK (VSSOP)	D (SOIC)	RUN (WQFN)	
		8 PINS	8 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	180.3	120.0	110.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	67.5	63.3	66.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	101.9	63.2	43.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	9.8	17.2	2.9	°C/W
Y_{JB}	Junction-to-board characterization parameter	100.1	62.5	43.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.6 Thermal Information: OPA4863

THERMAL METRIC[1]		OPA4863	UNIT
		PW (TSSOP)	
		14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	99.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	27.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.4	°C/W
Y_{JB}	Junction-to-board characterization parameter	55.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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7.7 Electrical Characteristics: V_S = 10 V

at V_{S+} = 5 V, $V_{S–}$ = –5 V, G = 1 V/V, R_F = 0 Ω for G = 1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ referenced to mid-supply, input and output common-mode is at mid-supply, and T_A ≅ 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
SSBW	Small-signal bandwidth	V_{OUT} = 20 mV_{PP}, G = 1, < 1 dB peaking		110		MHz
GBWP	Gain-bandwidth product			50		MHz
LSBW	Large-signal bandwidth	V_{OUT} = 2 V_{PP}		17		MHz
	Bandwidth for 0.1-dB flatness	V_{OUT} = 20 mV_{PP}		15		MHz
SR	Slew rate	V_{OUT} = 2–V step, G = –1		105		V/µs
	Rise, fall time	V_{OUT} = 200–mV step		9		ns
	Settling time to 0.1%	V_{OUT} = 2–V step		57		ns
	Settling time to 0.01%			70		
	Overshoot/undershoot	V_{OUT} = 2–V step		1		%
	Overdrive recovery time	G = –1, 0.5 V overdrive beyond supplies		70		ns
		G = 1, 0.5 V overdrive beyond supplies		100		
HD2	Second-order harmonic distortion	f = 20 kHz, V_{OUT} = 2 V_{PP}		–129		dBc
HD3	Third-order harmonic distortion			–138		
HD2	Second-order harmonic distortion	f = 100 kHz, V_{OUT} = 2 V_{PP}		–107		dBc
HD3	Third-order harmonic distortion			–125		
e_N	Input voltage noise	Flatband, 1/f corner at 25 Hz		5.9		nV/√Hz
i_N	Input current noise	Flatband, 1/f corner at 2 kHz		0.4		pA/√Hz
	Closed-loop output impedance	f = 1 MHz		0.2		Ω
	Channel-to-channel crosstalk	f = 1 MHz, V_{OUT} = 2 V_{PP}, OPA2863		–124		dBc
DC PERFORMANCE						
A_{OL}	Open-loop voltage gain	V_{OUT} = ±2.5 V	110	128		dB
V_{OS}	Input-referred offset voltage		–1.3	±0.4	1.3	mV
	Input offset voltage drift	T_A = –40°C to +125°C, D, DBV-5, RUN and DGK packages	–3.5	±1	3.5	µV/°C
		T_A = –40°C to +125°C, PW package	–4	±1	4	
		T_A = 0°C to +85°C, DBV-6 package	–4.4	±1	4.4	
		T_A = –40°C to +125°C, DBV-6 package	–4.9	±1	4.9	
	Input bias current	T_A ≅ 25°C		0.3	0.73	µA
		T_A = –40°C to +85°C			1.2	
		T_A = –40°C to +125°C			1.6	
	Input bias current drift	T_A = –40°C to +125°C		±3	7.6	nA/°C
	Input offset current		–30	±10	30	nA
INPUT						
	Input common-mode voltage range		$V_{S–}$–0.2		V_{S+}+0.2	V
CMRR	Common-mode rejection ratio	V_{CM} = $V_{S–}$ – 0.2 V to V_{S+} – 1.6 V	100	120		dB
	Input impedance common-mode			650 || 0.8		MΩ || pF
	Input impedance differential mode			200 || 0.5		kΩ || pF
OUTPUT						
V_{OL}	Output voltage, low	T_A ≅ 25°C		$V_{S–}$+0.14	$V_{S–}$+0.2	V
		T_A = –40°C to +125°C		$V_{S–}$+0.15	$V_{S–}$+0.22	
V_{OH}	Output voltage, high	T_A ≅ 25°C	V_{S+}–0.2	V_{S+}–0.14		V
		T_A = –40°C to +125°C	V_{S+}–0.2	V_{S+}–0.15		

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7.7 Electrical Characteristics: V_S = 10 V (continued)

at V_{S+} = 5 V, $V_{S–}$ = –5 V, G = 1 V/V, R_F = 0 Ω for G = 1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ referenced to mid-supply, input and output common-mode is at mid-supply, and T_A ≅ 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Linear output drive (sourcing/ sinking)	V_{OUT} = ±2.5 V, ΔV_{OS} < 1 mV OPA863 and OPA2863(1)	25	30		mA
	Short-circuit current			45		mA
POWER SUPPLY						
I_Q	Quiescent current per amplifier	T_A ≅ 25°C		700	970	µA
		T_A = –40°C to +125°C			1280	
PSRR	Power-supply rejection ratio	ΔV_S = ±2 V(2)	100	120		dB
POWER DOWN (Pin Must be Driven)						
	Enable voltage threshold	Specified *on* above V_{S+} – 0.5 V			4.5	V
	Disable voltage threshold	Specified *off* below V_{S+} – 1.5 V	3.5			V
	Power-down quiescent current per channel	$\overline{PD}$ ≤ V_{S+} – 1.5 V		2	3.3	µA
	Power-down pin bias current			2	50	nA
	Turn-on time delay			6		µs
	Turn-off time delay			4.5		µs
AUXILIARY INPUT STAGE						
	Gain-bandwidth product			50		MHz
	Input voltage noise	Flatband, 1/f corner at 25 Hz		6		nV/√Hz
	Input current noise	Flatband, 1/f corner at 100 Hz		0.4		pA/√Hz
	Input-referred offset voltage		–1.3	±0.15	1.3	mV
	Input bias current	T_A ≅ 25°C		0.2	0.6	µA
		T_A = –40°C to +125°C		0.2	1.3	
	Common-mode rejection ratio	V_{CM} = 4.1 V to 5.2 V	100	120		dB
	Power supply rejection ratio	ΔV_S = ±0.6 V	100	120		dB

(1) Change in input offset voltage from no-load condition.
(2) Change in supply voltage from the default test condition with only one of the positive or negative supplies changing corresponding to +PSRR and –PSRR.

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7.8 Electrical Characteristics: V_S = 3 V

at V_{S+} = 3 V, $V_{S–}$ = 0 V, G = 1, R_F = 0 Ω for G =1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ connected to 1 V, input and output V_{CM} = 1 V, and T_A ≅ 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
SSBW	Small-signal bandwidth	V_{OUT} = 20 mV_{PP}, G = 1		97		MHz
GBWP	Gain-bandwidth product			50		MHz
LSBW	Large-signal bandwidth	V_{OUT} = 1 V_{PP}		26		MHz
	Bandwidth for 0.1-dB flatness	V_{OUT} = 20 mV_{PP}		10		MHz
SR	Slew rate	V_{OUT} = 1–V step, Gain = –1		105		V/µs
	Rise, fall time	V_{OUT} = 200–mV step		10		ns
	Settling time to 0.1%	V_{OUT} = 1–V step		58		ns
	Settling time to 0.01%			90		
	Overshoot	V_{OUT} = 1–V step		2		%
	Undershoot			16		
	Overdrive recovery time	G = –1, 0.5V overdrive beyond supplies		95		ns
		G = 1, 0.5V overdrive beyond supplies		100		
HD2	Second-order harmonic distortion	f = 20 kHz, V_{OUT} = 1 V_{PP}		–123		dBc
HD3	Third-order harmonic distortion			–132		
HD2	Second-order harmonic distortion	f = 100 kHz, V_{OUT} = 1 V_{PP}		–109		dBc
HD3	Third-order harmonic distortion			–129		
e_N	Input voltage noise	Flatband, 1/f corner at 25 Hz		6		nV/√Hz
i_N	Input current noise	Flatband, 1/f corner at 2 kHz		0.4		pA/√Hz
	Closed-loop output impedance	f = 1 MHz		0.2		Ω
	Channel-to-channel crosstalk	f = 1 MHz, V_{OUT} = 1 V_{PP}, OPA2863		–127		dBc
DC PERFORMANCE						
A_{OL}	Open-loop voltage gain	V_{OUT} = 1 V to 2 V	104	123		dB
V_{OS}	Input-referred offset voltage		–1.3	±0.4	1.3	mV
	Input offset voltage drift	T_A = –40°C to +125°C, D, DBV-5, RUN, and DGK packages	–3.5	±1	3.5	µV/°C
		T_A = –40°C to +125°C, PW package	–4	±1	4	
		T_A = 0°C to +85°C, DBV-6 package	–4.4	±1	4.4	
		T_A = –40°C to +125°C, DBV-6 package	–5	±1	5	
	Input bias current	T_A ≅ 25°C		0.3	0.73	µA
		T_A = –40°C to +85°C			1.2	
		T_A = –40°C to +125°C			1.56	
	Input bias current drift	T_A = –40°C to +125°C		±3	7.4	nA/°C
	Input offset current		–30	±10	30	nA
INPUT						
	Input common-mode voltage range		$V_{S–}$–0.2		V_{S+}+0.2	V
CMRR	Common-mode rejection ratio	V_{CM} = $V_{S–}$ – 0.2 V to V_{S+} – 1.6 V	94	115		dB
	Input impedance common-mode			360 || 0.9		MΩ || pF
	Input impedance differential mode			200 || 0.5		kΩ || pF

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7.8 Electrical Characteristics: V_S = 3 V (continued)

at V_{S+} = 3 V, $V_{S–}$ = 0 V, G = 1, R_F = 0 Ω for G =1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ connected to 1 V, input and output V_{CM} = 1 V, and T_A ≅ 25°C (unless otherwise noted)

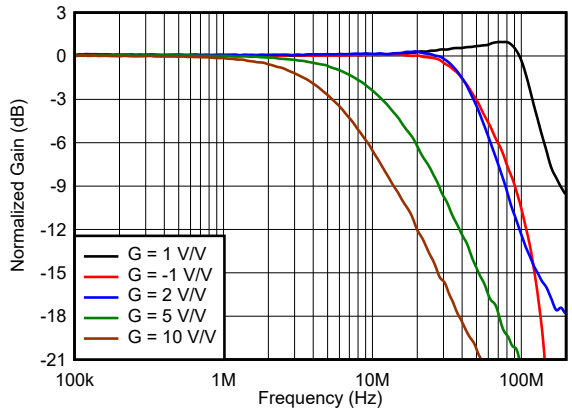
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
V_{OL}	Output voltage, low	T_A ≅ 25°C		$V_{S–}$ + 0.13	$V_{S–}$ + 0.15	V
		T_A = –40°C to +125°C		$V_{S–}$ + 0.13	$V_{S–}$ + 0.16	
V_{OH}	Output voltage, high	T_A ≅ 25°C	V_{S+}–0.15	V_{S+}–0.13		V
		T_A = –40°C to +125°C	V_{S+}–0.15	V_{S+}–0.13		
	Linear output drive (sourcing/ sinking)	V_{OUT} = ±0.7 V, ΔV_{OS} < 1 mV OPA863 and OPA2863(1)	23	33		mA
	Short-circuit current			45		mA
POWER SUPPLY						
I_Q	Quiescent current per amplifier	T_A ≅ 25°C		690	910	µA
		T_A = –40°C to +125°C			1180	
PSRR	Power-supply rejection ratio	ΔV_S = ±1 V(2)	100	120		dB
POWER DOWN (Pin Must be Driven)						
	Enable voltage threshold	Specified *on* above V_{S+} – 0.5 V			2.5	V
	Disable voltage threshold	Specified *off* below V_{S+} – 1.5 V	1.5			V
	Power-down quiescent current per channel	$\overline{PD}$ ≤ V_{S+} – 1.5 V		0.8	1.5	µA
	Power-down pin bias current			1	50	nA
	Turn-on time delay			6.5		µs
	Turn-off time delay			5		µs
AUXILIARY INPUT STAGE						
	Gain-bandwidth product			50		MHz
	Input voltage noise	Flatband, 1/f corner at 25 Hz		6		nV/√Hz
	Input current noise	Flatband, 1/f corner at 100 Hz		0.4		pA/√Hz
	Input-referred offset voltage		–1.3	±0.15	1.3	mV
	Input bias current	T_A ≅ 25°C		0.2	0.6	µA
		T_A = –40°C to +125°C		0.4	1.2	
	Common-mode rejection ratio	V_{CM} = 2.1 V to 3.2 V	100	120		dB
	Power supply rejection ratio	ΔV_S = ±0.6 V	100	115		dB

(1) Change in input offset voltage from no-load condition.
(2) Change in supply voltage from the default test condition with only one of the positive or negative supplies changing corresponding to +PSRR and –PSRR.

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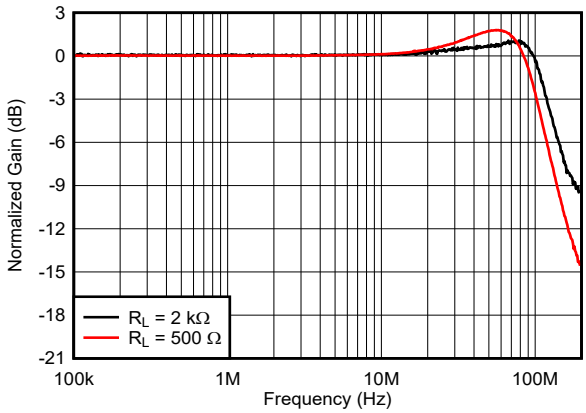
7.9 Typical Characteristics: V_S = 10 V

at V_{S+} = 5 V, $V_{S–}$ = –5 V, R_F = 0 Ω for Gain = 1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ referenced to mid-supply, G = 1 V/V, input and output referenced to mid-supply, and TA ≅ 25°C (unless otherwise noted)



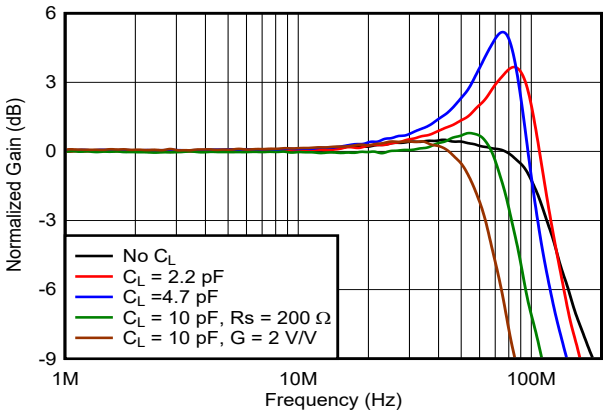
V_{OUT} = 20 mV_{PP}

Figure 7-1. Small-Signal Frequency Response vs Gain



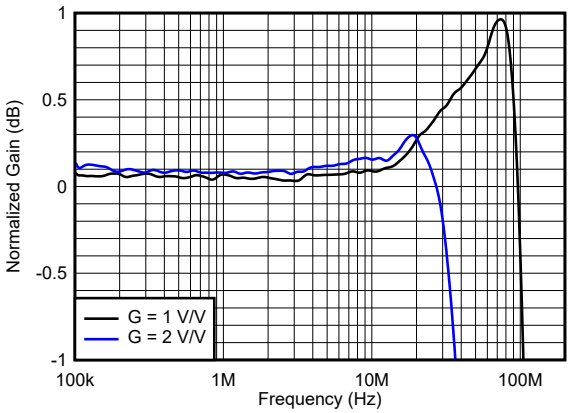
V_{OUT} = 20 mV_{PP}

Figure 7-2. Small-Signal Frequency Response vs Output Load



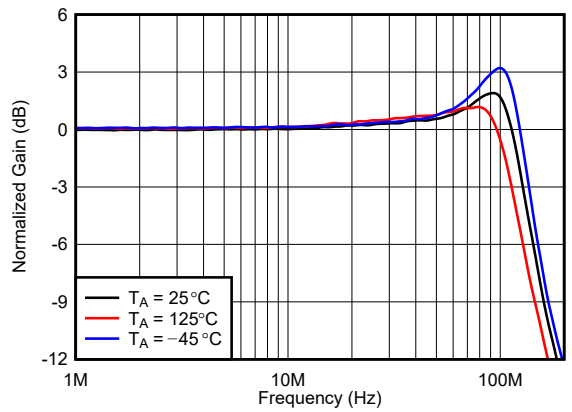
V_{OUT} = 20 mV_{PP}

Figure 7-3. Frequency Response vs Load Capacitance



V_{OUT} = 20 mV_{PP}

Figure 7-4. Small-Signal Response Flatness vs Gain



V_{OUT} = 20 mV_{PP}

Figure 7-5. Frequency Response vs Ambient Temperature

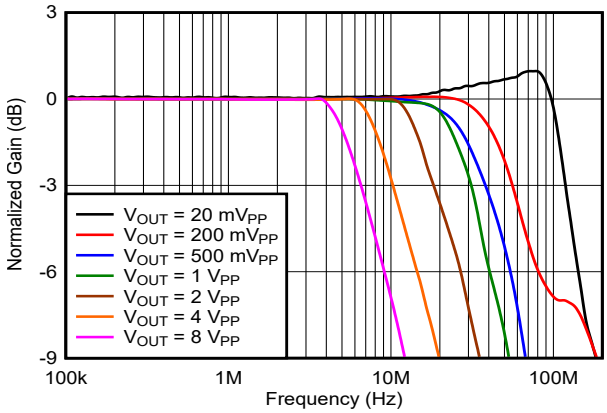
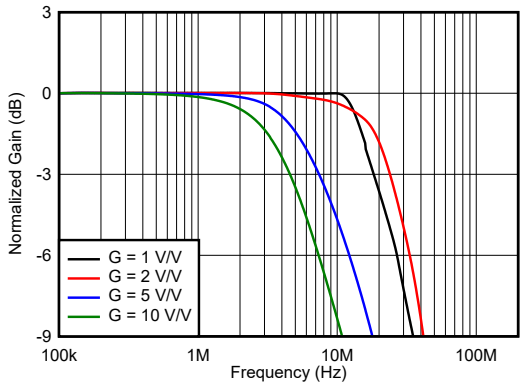


Figure 7-6. Frequency Response vs Output Voltage

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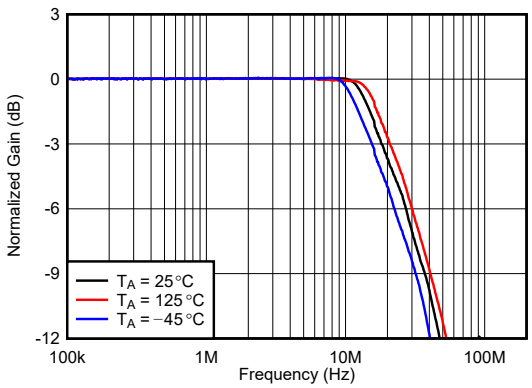
7.9 Typical Characteristics: V_S = 10 V (continued)

at V_{S+} = 5 V, $V_{S–}$ = –5 V, R_F = 0 Ω for Gain = 1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ referenced to mid-supply, G = 1 V/V, input and output referenced to mid-supply, and TA ≅ 25°C (unless otherwise noted)



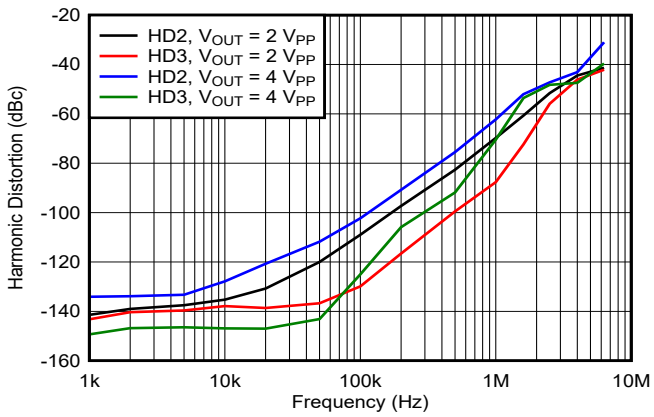
V_{OUT} = 2 V_{PP}

Figure 7-7. Large-Signal Frequency Response vs Gain



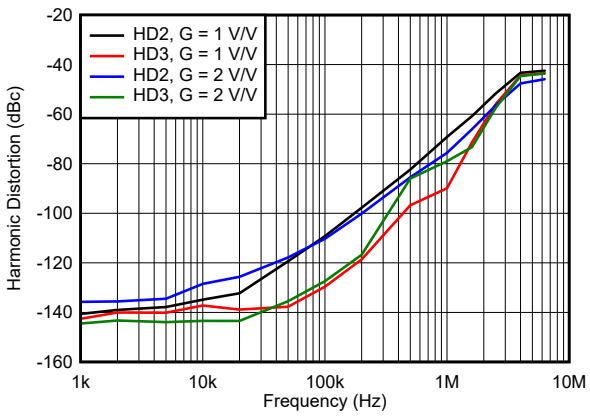
V_{OUT} = 2 V_{PP}

Figure 7-8. Frequency Response vs Ambient Temperature



G = 1 V/V

Figure 7-9. Harmonic Distortion vs Frequency



V_{OUT} = 2 V_{PP}

Figure 7-10. Harmonic Distortion vs Gain

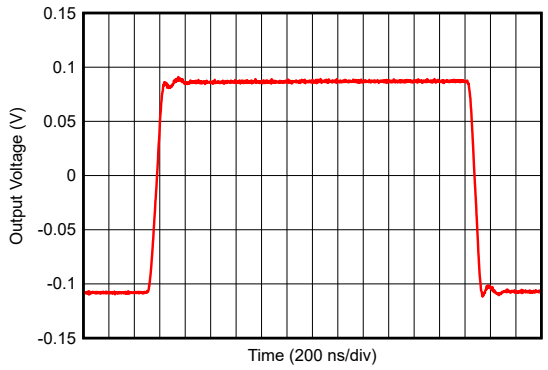


Figure 7-11. Small-Signal Transient Response

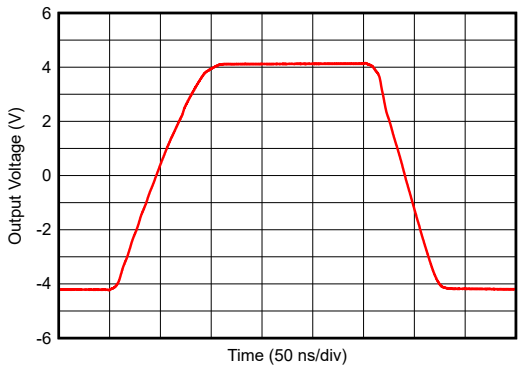
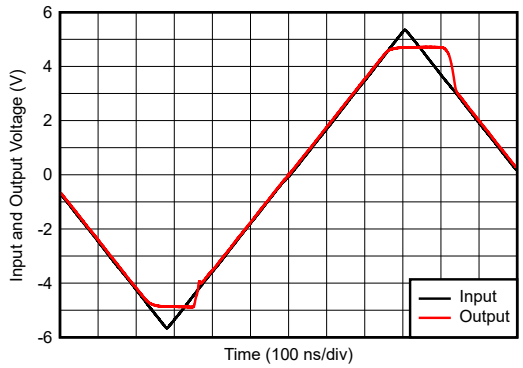


Figure 7-12. Large-Signal Transient Response

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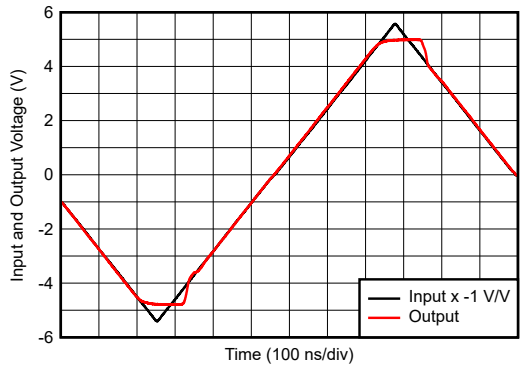
7.9 Typical Characteristics: V_S = 10 V (continued)

at V_{S+} = 5 V, $V_{S–}$ = –5 V, R_F = 0 Ω for Gain = 1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ referenced to mid-supply, G = 1 V/V, input and output referenced to mid-supply, and TA ≅ 25°C (unless otherwise noted)



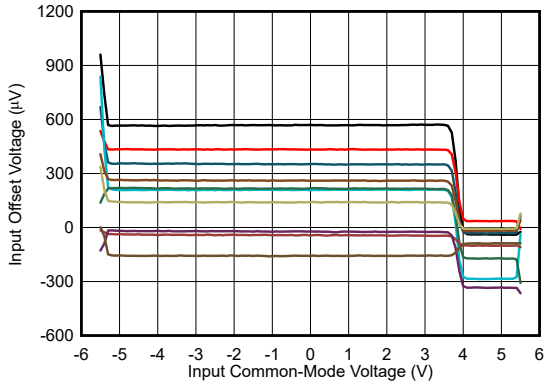
Gain = 1 V/V

Figure 7-13. Input Overdrive Recovery



Gain = –1 V/V

Figure 7-14. Output Overdrive Recovery



Measured for 10 units

Figure 7-15. Input Offset Voltage vs Input Common-Mode Voltage

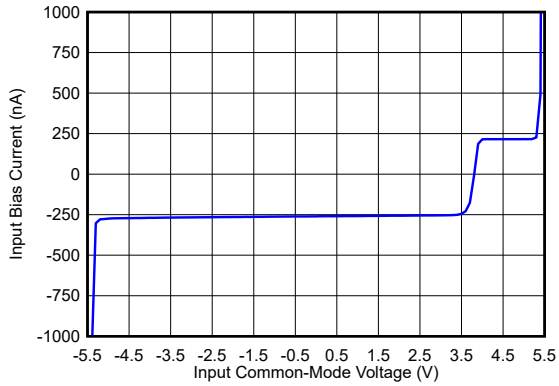


Figure 7-16. Input Bias Current vs Input Common-Mode Voltage

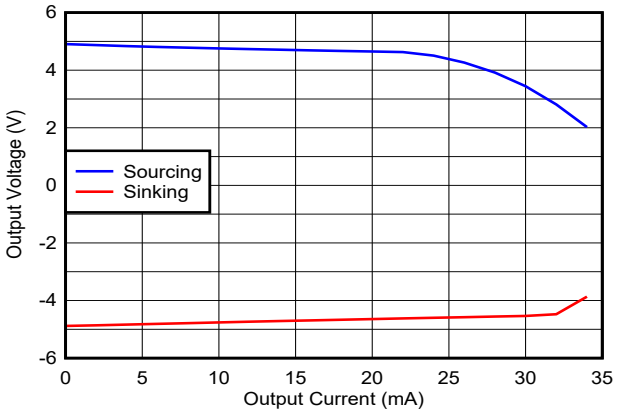
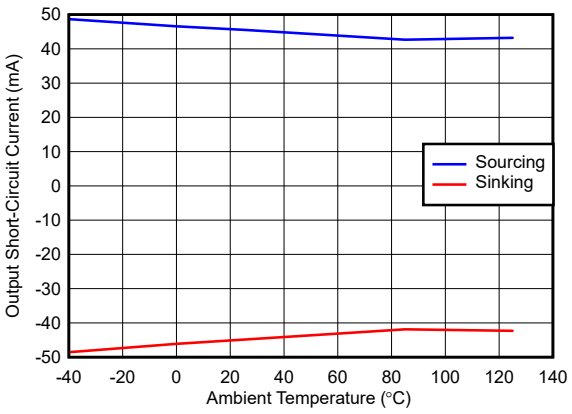


Figure 7-17. Output Voltage vs Load Current



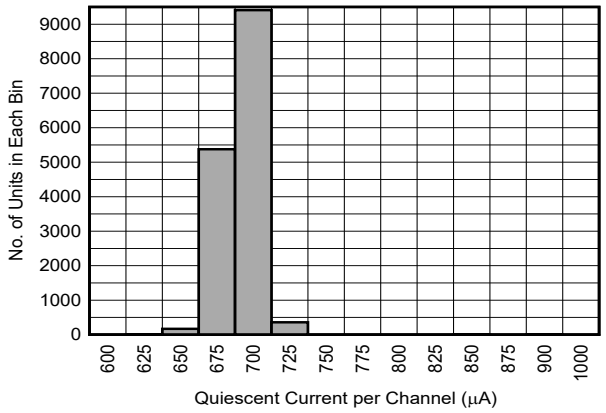
Output saturated and then short-circuited to opposite supply

Figure 7-18. Output Short-Circuit Current vs Ambient Temperature

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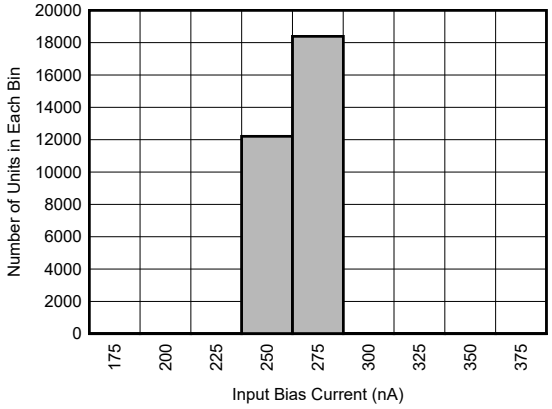
7.9 Typical Characteristics: V_S = 10 V (continued)

at V_{S+} = 5 V, $V_{S–}$ = –5 V, R_F = 0 Ω for Gain = 1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ referenced to mid-supply, G = 1 V/V, input and output referenced to mid-supply, and TA ≅ 25°C (unless otherwise noted)



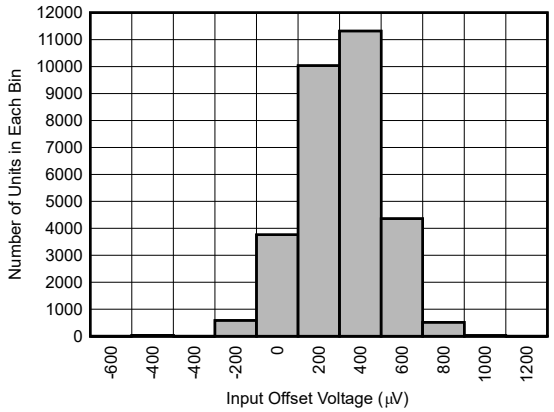
µ = 678 µA, σ = 13 µA

Figure 7-19. Quiescent Current Distribution



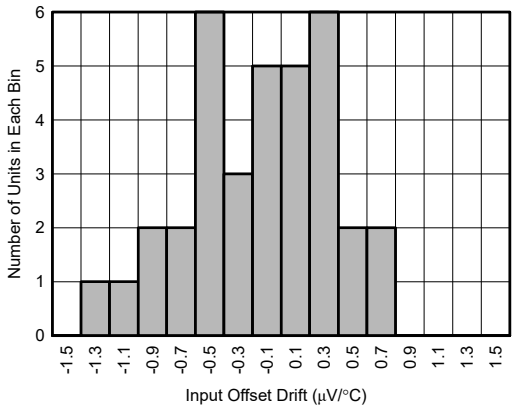
µ = 251 nA, σ = 5.6 nA

Figure 7-20. Input Bias Current Distribution



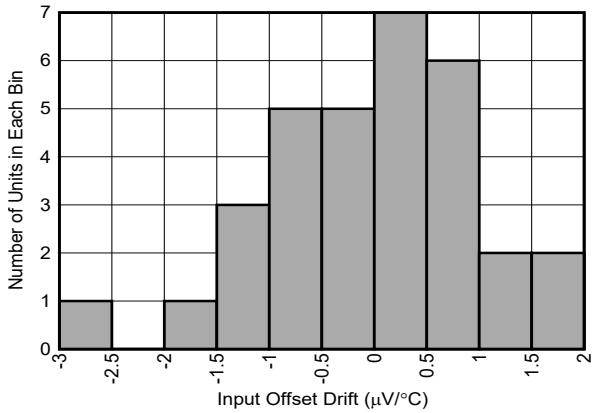
µ = 209 µV, σ = 193 µV

Figure 7-21. Input Offset Voltage Distribution



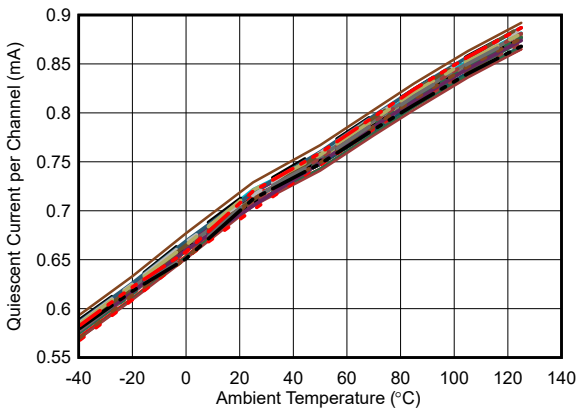
35 units, µ =-0.26 µV/°C, σ = 0.49 µV/°C, DGK package

Figure 7-22. Input Offset Voltage Drift Distribution



32 units, µ = −0.02 µV/°C, σ = 0.98 µV/°C, DBV-6 package

Figure 7-23. Input Offset Voltage Drift Distribution

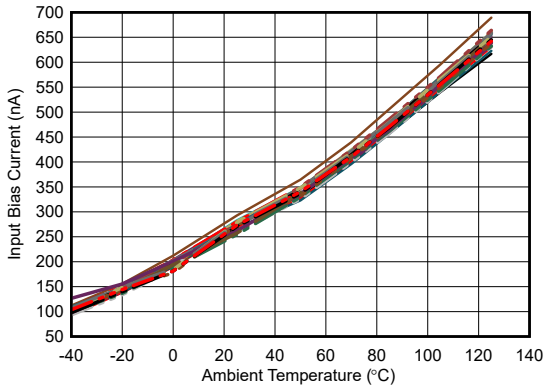


35 units

Figure 7-24. Quiescent Current vs Ambient Temperature

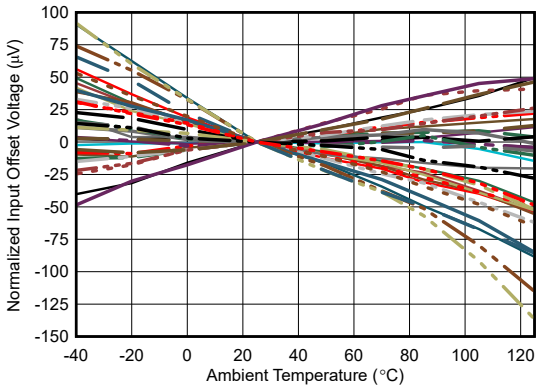
7.9 Typical Characteristics: V_S = 10 V (continued)

at V_{S+} = 5 V, $V_{S–}$ = –5 V, R_F = 0 Ω for Gain = 1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ referenced to mid-supply, G = 1 V/V, input and output referenced to mid-supply, and TA ≅ 25°C (unless otherwise noted)



35 units

Figure 7-25. Input Bias Current vs Ambient Temperature



Normalized to 25°C values, 35 units, DGK package

Figure 7-26. Input Offset Voltage vs Ambient Temperature

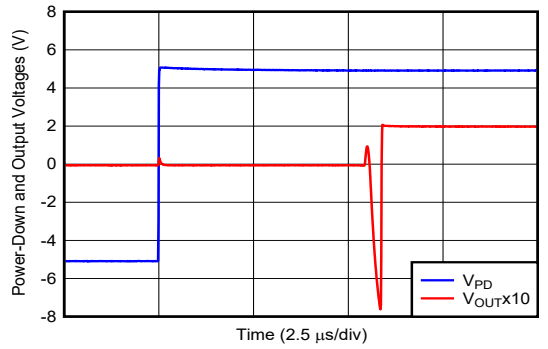


Figure 7-27. Turn-On Time to DC Input

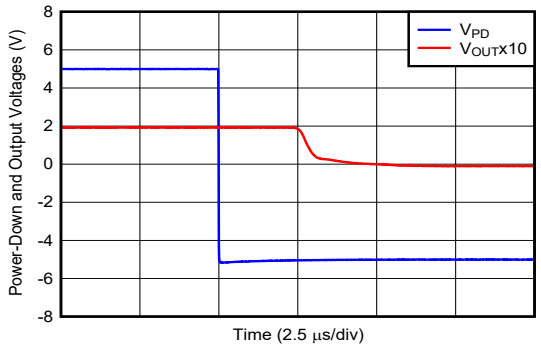
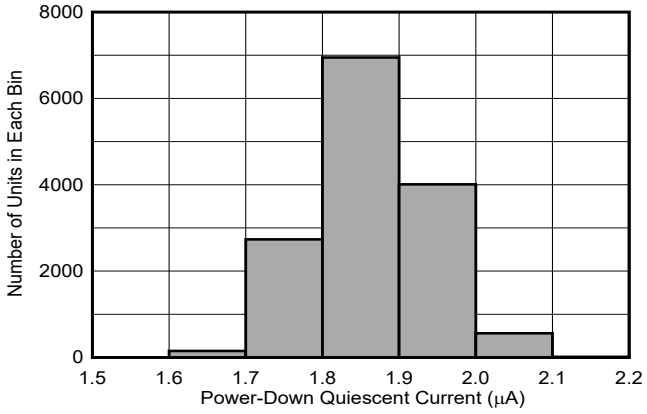


Figure 7-28. Turn-Off Time to DC Input



µ = 1.86 µA, σ = 0.076 µA

Figure 7-29. Power-Down Quiescent Current Distribution

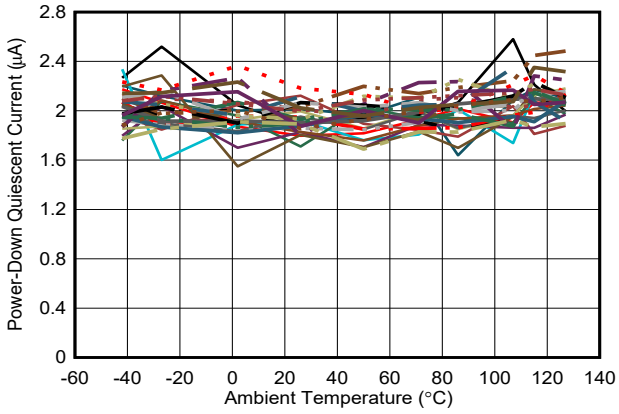
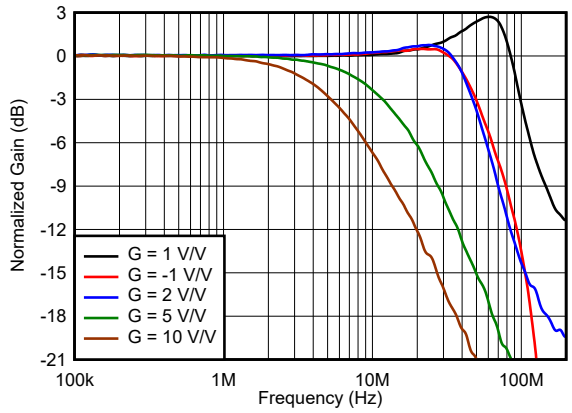


Figure 7-30. Power-Down I_Q vs Ambient Temperature

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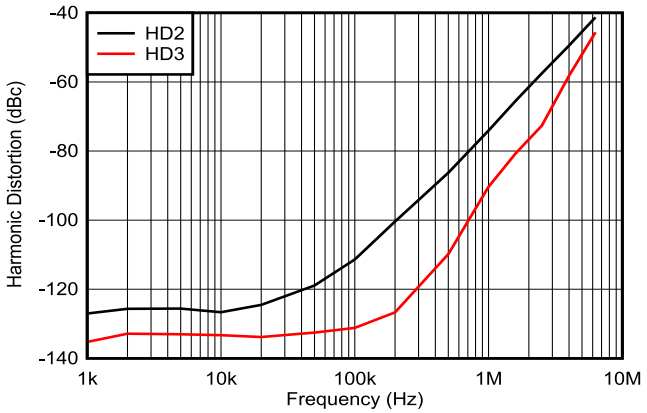
7.10 Typical Characteristics: V_S = 3 V

at V_{S+} = 3 V, $V_{S–}$ = 0 V, R_F = 0 Ω for Gain = 1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ connected to 1 V, G = 1 V/V, input and output V_{CM} = 1 V, and T_A ≅ 25°C (unless otherwise noted)



V_{OUT} = 20 mV_{PP}

Figure 7-31. Small-Signal Frequency Response vs Gain



V_{OUT} = 1 V_{PP}

Figure 7-32. Harmonic Distortion vs Frequency

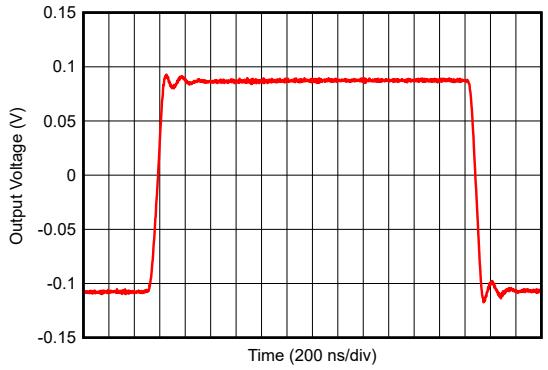


Figure 7-33. Small-Signal Transient Response

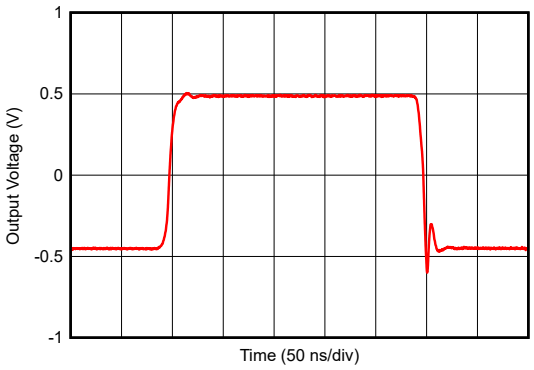
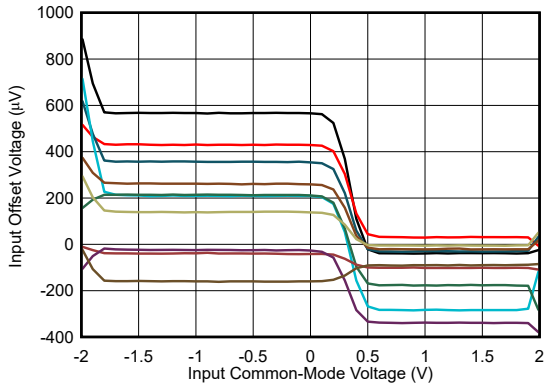


Figure 7-34. Large-Signal Transient Response



Measured for 10 units

Figure 7-35. Input Offset Voltage vs Input Common-Mode Voltage

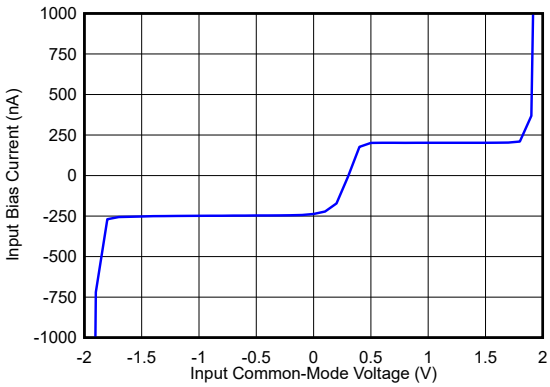


Figure 7-36. Input Bias Current vs Input Common-Mode Voltage

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7.10 Typical Characteristics: V_S = 3 V (continued)

at V_{S+} = 3 V, $V_{S–}$ = 0 V, R_F = 0 Ω for Gain = 1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ connected to 1 V, G = 1 V/V, input and output V_{CM} = 1 V, and T_A ≅ 25°C (unless otherwise noted)

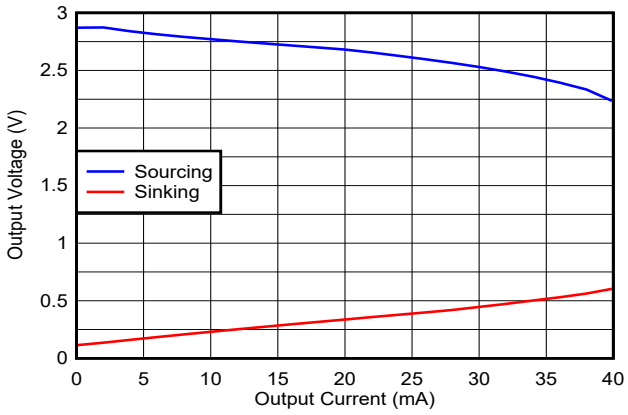
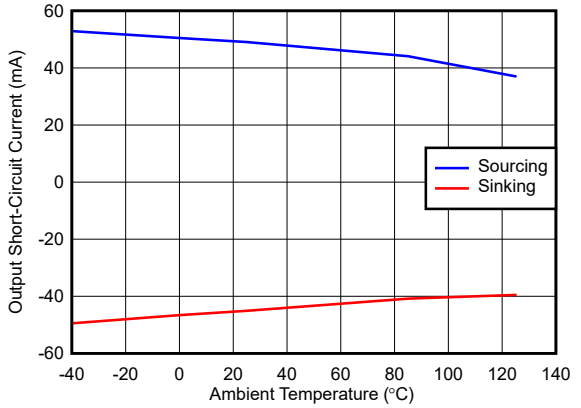


Figure 7-37. Output Voltage vs Load Current



Output saturated and then short-circuited to other supply

Figure 7-38. Output Short-Circuit Current vs Ambient Temperature

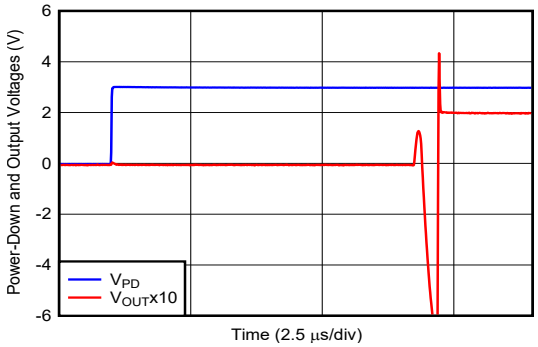


Figure 7-39. Turn-On Time to DC Input

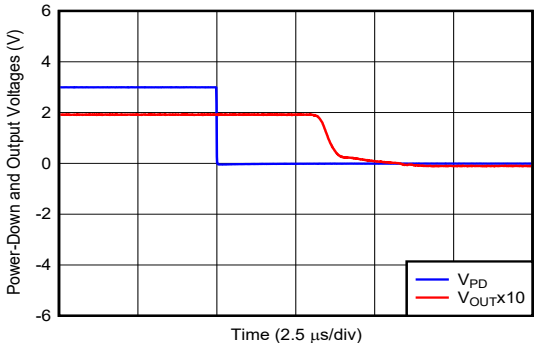
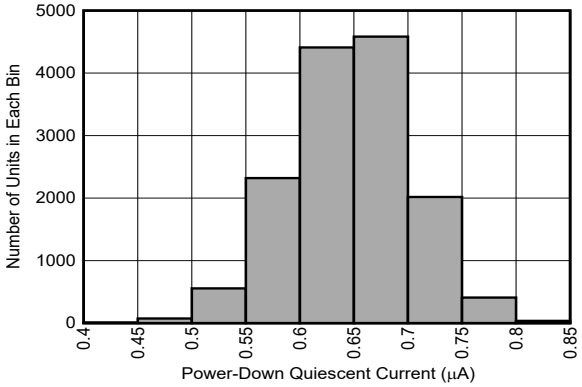


Figure 7-40. Turn-Off Time to DC Input



µ = 0.64 µA, σ = 0.056 µA

Figure 7-41. Power-Down Quiescent Current Distribution

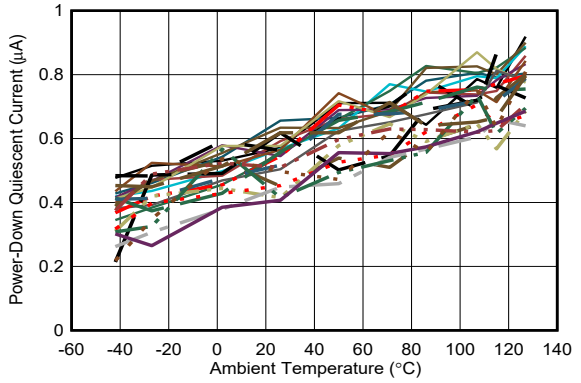
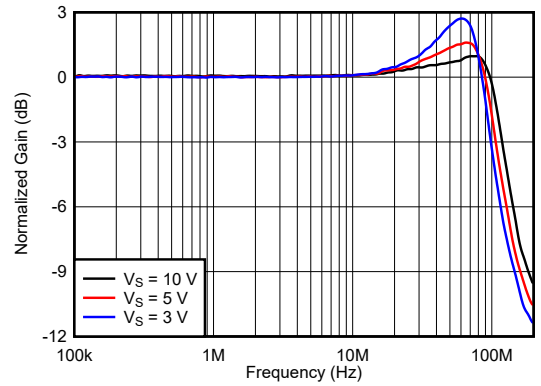


Figure 7-42. Power-Down I_Q vs Ambient Temperature

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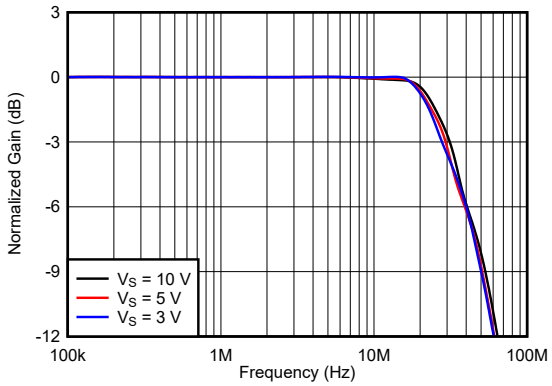
7.11 Typical Characteristics: V_S = 3 V to 10 V

at V_{OUT} = 2 V_{PP}, R_F = 0 Ω for Gain = 1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ referenced to mid-supply, G = 1 V/V, input and output referenced to mid-supply, and T_A ≅ 25°C (unless otherwise noted)



V_{OUT} = 20 mV_{PP}

Figure 7-43. Frequency Response vs Supply Voltage



V_{OUT} = 1 V_{PP}

Figure 7-44. Frequency Response vs Supply Voltage

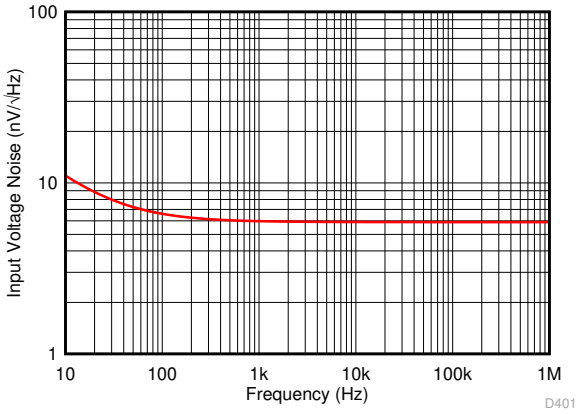


Figure 7-45. Input Voltage Noise Density vs Frequency

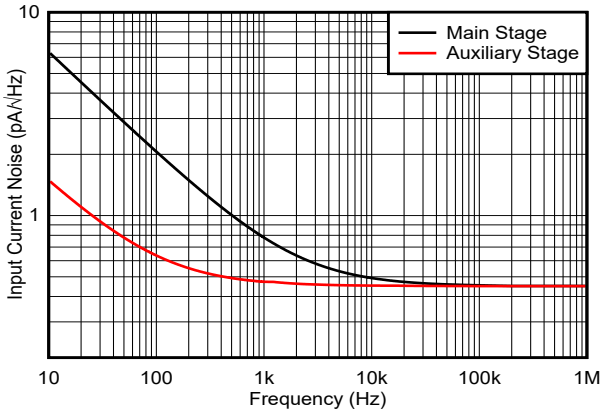


Figure 7-46. Input Current Noise Density vs Frequency

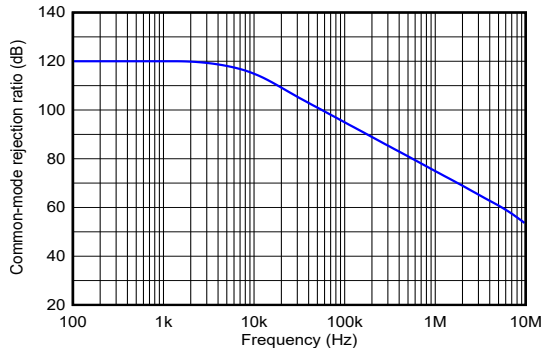


Figure 7-47. Common-Mode Rejection Ratio vs Frequency

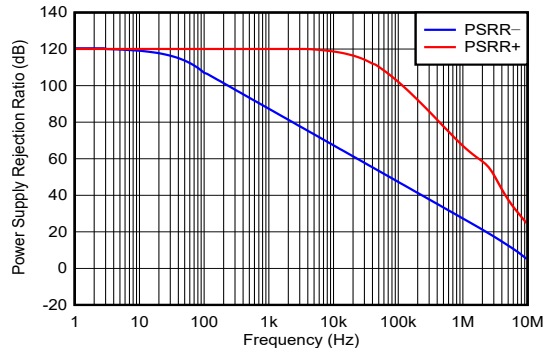


Figure 7-48. Power Supply Rejection Ratio vs Frequency

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7.11 Typical Characteristics: V_S = 3 V to 10 V (continued)

at V_{OUT} = 2 V_{PP}, R_F = 0 Ω for Gain = 1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ referenced to mid-supply, G = 1 V/V, input and output referenced to mid-supply, and T_A ≅ 25°C (unless otherwise noted)

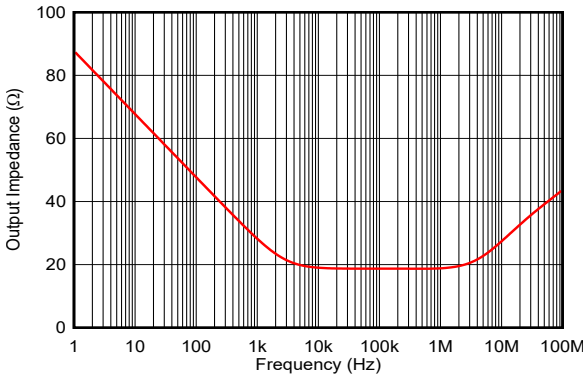
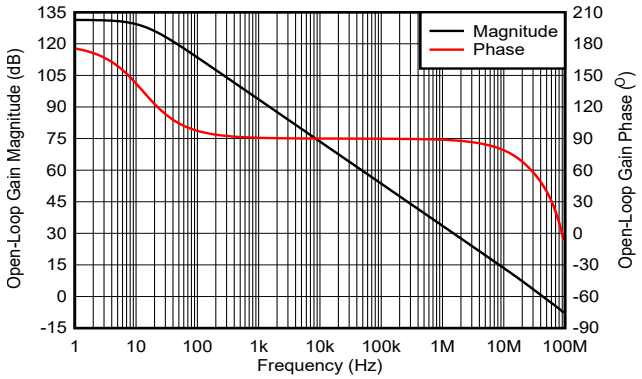
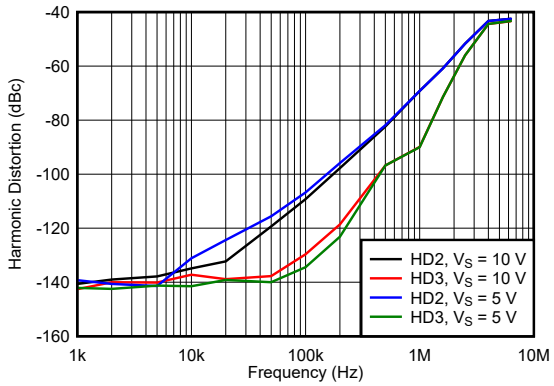


Figure 7-49. Open-Loop Output Impedance vs Frequency



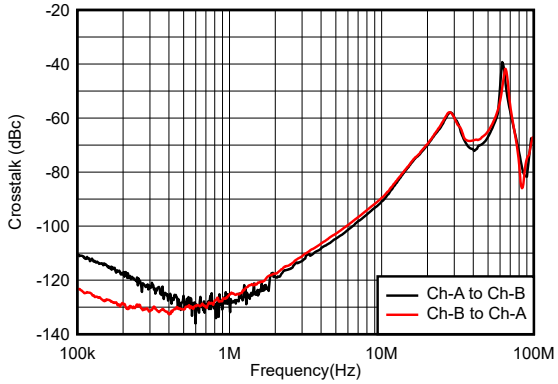
Small-signal response

Figure 7-50. Open-Loop Gain and Phase vs Frequency



V_{OUT} = 2 V_{PP}

Figure 7-51. Harmonic Distortion vs Supply Voltage



DGK package

Figure 7-52. Crosstalk vs Frequency

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8 Detailed Description

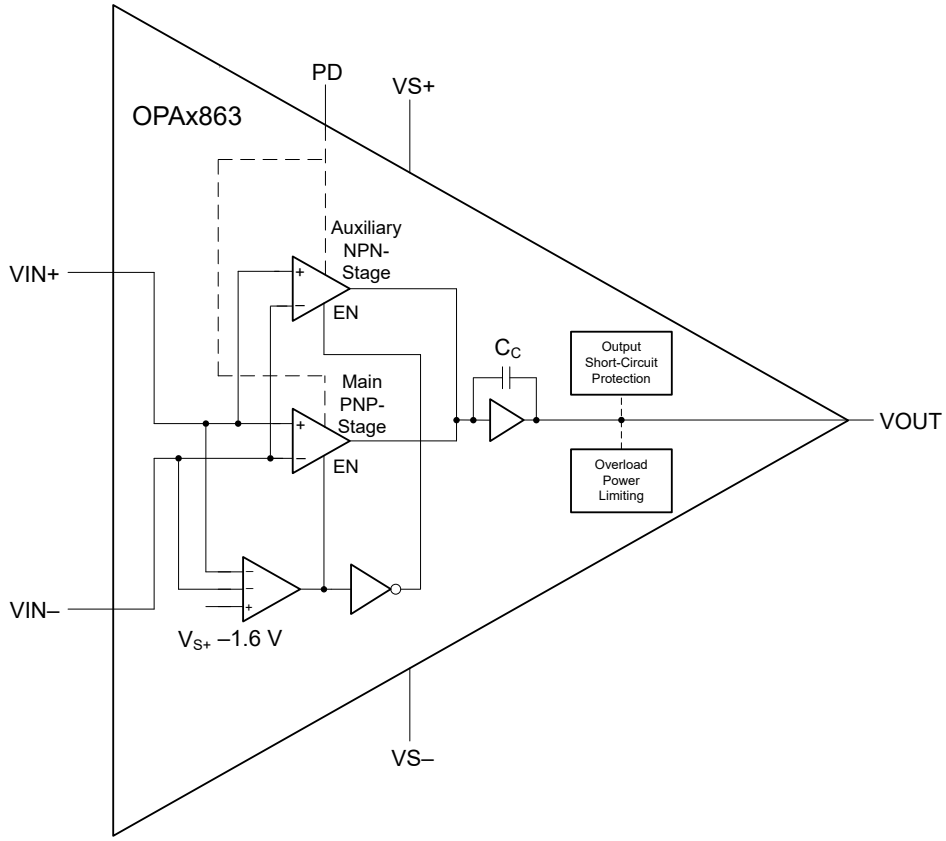
8.1 Overview

The OPAx863 devices are low-power, 50-MHz, rail-to-rail input and output (RRIO), bipolar, voltage-feedback operational amplifiers with a voltage noise density of 5.9 nV/√Hz and 1/f noise corner at 25 Hz. The OPAx863 work with a wide-supply voltage range of 2.7 V to 12.6 V, and consume only 700 µA quiescent current. The OPAx863 operate with a 2.7 V supply, are RRIO capable, consume low-power, and offer a power-down mode, which makes them great amplifiers for 3.3-V or lower-voltage applications that require excellent ac performance. The main and auxiliary input stages of the amplifier are matched for gain bandwidth product (GBW), noise, and offset voltage and designed for applications that require wide dynamic input range and good SNR.

The device includes an overload power limit feature which limits the increase in quiescent current with over-driven and saturated outputs to either of the supply rails. For more details of this overload power limit feature, see Section 8.3.2.1. The amplifier's output is protected against short-circuit fault conditions.

The OPAx863 feature a power-down mode (PD) with a PD quiescent current of 1.5 µA (maximum) with a 3-V supply, with turn-on and turn-off time within less than 6.5 µs.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Input Stage

The OPAx863 include a rail-to-rail input stage. The main stage differential pair using PNP bipolar transistors operates for common-mode input voltages from $V_{S–}$ – 0.2 V to V_{S+} – 1.6 V. The amplifier inputs transition into the auxiliary stage using NPN transistors for common-mode input voltages from V_{S+} – 1.6 V till V_{S+} + 0.2 V. The PNP and NPN input stages offer a gain-bandwidth product of 50 MHz and a voltage noise density of 6.3 nV/√Hz. The offset voltage for the two input stages is matched to lie within the device specifications. The auxiliary NPN input stage does not use the slew-boost circuit during large-signal transient response. The input bias current for the PNP and NPN input stages is opposite in polarity, which adds an additional offset based on the values of the gain-setting and feedback resistors. A common-mode input voltage transition between these input stages causes a crossover distortion that must be considered in high-frequency applications requiring excellent linearity. Limit the common-mode input voltage to V_{S+} – 1.6 V (maximum) for main-stage operation across process and ambient temperature.

The OPAx863 are bipolar amplifiers; therefore, the two inputs are protected with antiparallel back-to-back diodes between the inputs, which limits the maximum input differential voltage to 1 V. The amplifier is slew limited, and the two inputs are pulled apart up to 1 V when the antiparallel diodes begin to conduct in very fast input or output transient conditions. Make sure to use gain-setting and feedback resistors large enough to limit the current through these diodes in such conditions.

8.3.2 Output Stage

The OPAx863 feature a rail-to-rail output stage with possible signal swing from $V_{S–}$ + 0.2 V to V_{S+} – 0.2 V. Violating the output headroom of either supply causes output signal clipping and introduces distortion.

The OPAx863 integrate an output short-circuit protection circuit that makes the device rugged for use in real-world applications.

8.3.2.1 Overload Power Limit

The OPAx863 include overload power limiting that limits the increase in device quiescent current with output saturated to either of the supplies. Typically, when an amplifier output saturates, the two inputs are pulled apart, which can enable the slew-boost circuit. The input differential voltage is an error voltage in negative feedback that the amplifier core nullifies by engaging the slew-boost circuit and driving the output stage deeper into saturation. After the input to an amplifier attains a value large enough to saturate the output, any further increase in this input excitation results in a finite input differential voltage. As the output stage transistor is pushed deeper into saturation, the base-to-collector current gain (h_{FE}) drops with an increase in the base and collector current, and an increase in the device quiescent current. This increase in quiescent current can cause a catastrophic failure in multichannel, high-gain, high-density front-end designs, and reduce operating lifetime in portable, battery-powered systems.

The OPAx863 overload power limiting includes an intelligent output saturation-detection circuit that limits the device quiescent current to 2.2-mA per channel under dc overload conditions. This increase in quiescent current is smaller with ac input or output and output saturation duration for only a fraction of the overall signal time period. Table 8-1 compares the increase in quiescent current with 50-mV input overdrive for OPAx863 devices and other voltage-feedback amplifiers without overload power limit.

Table 8-1. Quiescent Current With Saturated Outputs

DEVICE	INPUT DIFFERENTIAL VOLTAGE	QUIESCENT CURRENT DURING OVERLOAD	INCREASE IN I_Q FROM STEADY-STATE CONDITION
OPAx863 with overload power limit	50 mV	1.1 mA	1.57 ×
Competitor amplifier without overload power limit	50 mV	1.96 mA	3.43 ×

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8.3.3 ESD Protection

As Figure 8-1 shows, all device pins are protected with internal ESD protection diodes to the power supplies. These diodes provide moderate protection to input overdrive voltages greater than the supplies. The protection diodes typically support 10-mA continuous input and output currents. Use series current limiting resistors if input voltages exceeding the supply voltages occur at the amplifier inputs, which makes sure that the current through the ESD diodes remains within the rated value. OPAx863 is a bipolar amplifier; therefore, the two inputs are protected with antiparallel, back-to-back diodes between the inputs that limits the maximum input differential voltage to approximately 1 V. Make sure to use gain-setting and feedback resistors large enough to limit the current through these diodes in fast slewing conditions.

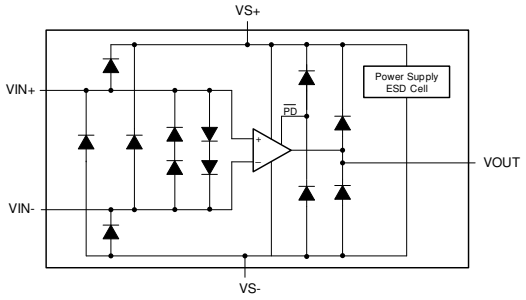


Figure 8-1. Internal ESD Protection

8.4 Device Functional Modes

8.4.1 Power-Down Mode

The OPAx863 includes a power-down mode for low-power standby operation with a quiescent current of only 1.5 µA (maximum) with a 3-V supply and high output impedance. Many low-power systems are active for only a small time interval when the parameters of interest are measured and remain in low-power standby mode for a majority of the time and an overall small average power consumption. The OPAx863 enables such a low-power operation with quick turn-on within less than 6.5 µs. See the *Electrical Characteristics* tables for power-down pin control thresholds.

Always drive $\overline{PD}$ pin to avoid false triggering and oscillations. If power-down mode is not used, then connect the $\overline{PD}$ pin to V_{S+}. For applications that need power-down mode, use an external pull-up resistor from the $\overline{PD}$ pin to V_{S+} (driven with an open-collector power-down control logic).

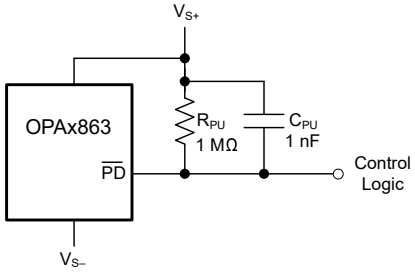


Figure 8-2. Power Down Control

Figure 8-2 shows the choice of value of the pull-up resistor R_{PU}, which impacts the current consumption in power-down mode. Using a large RPU reduces power consumption, but increases the noise at the PD pin, which can cause the amplifier to power down. A 1-nF capacitor can be used in parallel with RPU to avoid coupling of external noise and false triggering. For the case of the $\overline{PD}$ pin driven to V_{S-}, the I_{PU} current through R_{PU} is given as:

$$I_{PU} = \frac{V_{S+} - V_{S-}}{R_{PU}} \quad (1)$$

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The OPAx863 are classic voltage-feedback amplifiers with two high-impedance inputs and a low-impedance output. These devices have a GBW of 50 MHz, 5.9 nV/√Hz of noise, RRIO capability, and precision performance consuming only 700 µA quiescent current per channel These features make the OPAx863 an excellent choice for use in low-side current sensing, ADC input driver, and reference buffering with fast settling, buffers, high gain and filter circuits. The overload power limit makes the OPAx863 truly low-power in high-gain, multichannel systems limiting any increase in quiescent current during output overload conditions.

9.2 Typical Applications

9.2.1 Low-Side Current Sensing

Power converters use current-mode feedback control for excellent transient response and multiphase load sharing. Inverter stages control the phase currents for torque control in motor drives. As a result of the simplicity and low-cost, many of these topologies use difference-amplifier-based, low-side current sensing. Figure 9-1 shows the use of the OPAx863 in a difference amplifier circuit for low-side current sensing.

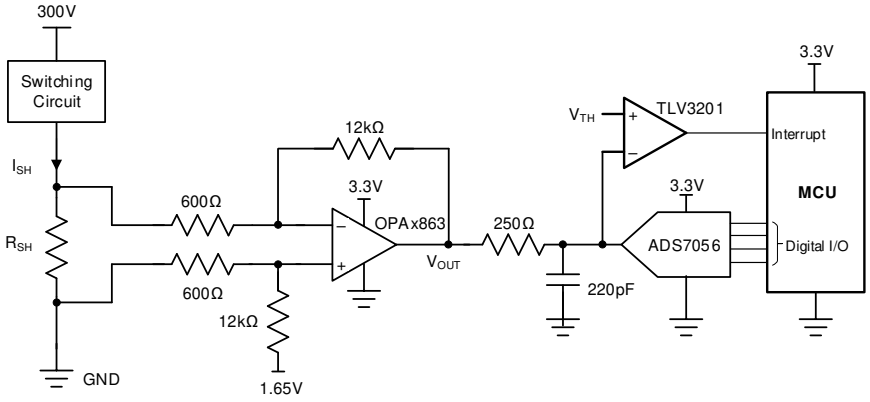


Figure 9-1. Low-Side Current Sensing in Power Converters

9.2.1.1 Design Requirements

Table 9-1. Design Requirements

PARAMETER	DESIGN REQUIREMENT
Shunt resistor	10 mΩ
Input current	15 A_{PP}
Output voltage	3 V_{PP}
Switching frequency	50 kHz
Data acquisition	1 MSPS with 0.1% accuracy
Input voltage due to ground bounce	10 Vpk

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9.2.1.2 Detailed Design Procedure

In a difference amplifier circuit, the output voltage is given by:

$$V_O = \frac{R_F}{R_G} I_{SH} R_{SH} + V_{REF} \tag{2}$$

For lowest system noise, small values of R_F and R_G are preferred. The smallest value of R_G is limited by the input transient voltage (10 V here) seen by the circuit, and is given by:

$$R_G = \frac{V_{IN(max.)} - V_D - V_S}{I_{D(max.)}} \tag{3}$$

Where,

- $V_{IN(maximum)}$ is the maximum input transient voltage seen by the circuit.
- V_D is the forward voltage drop of ESD diodes at the amplifier input.
- $I_{D(maximum)}$ is the maximum current rating of the ESD diodes at the amplifier input.

For a difference amplifier gain of 20 V/V, an R_F of 12 kΩ and R_G of 600 Ω are used. With a clock frequency of 40 MHz and the ADS7056 sampling at 1 MSPS, the available acquisition time for amplifier output settling is 550 ns. Figure 9-2 shows the simulation results for the circuit in Figure 9-1. The worst-case peak-to-peak input transient condition is simulated. The output of the OPAx863 device settles to within 0.1% accuracy within 543 ns. If using a slower clock frequency with the ADC is desired, then the acquisition time reduces with the same sampling rate, which degrades measurement accuracy. Alternatively, the sampling rate can be reduced to recover the required acquisition time and 0.1% accuracy.

9.2.1.3 Application Curves

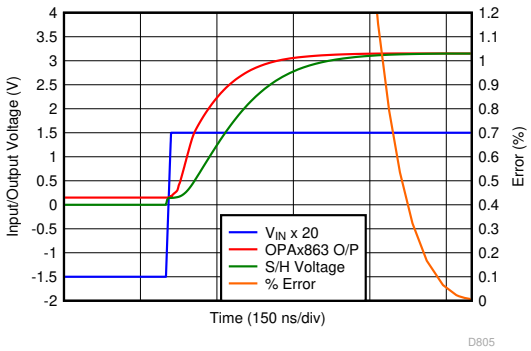


Figure 9-2. 0.1% Settling Performance

9.2.2 Front-End Gain and Filtering

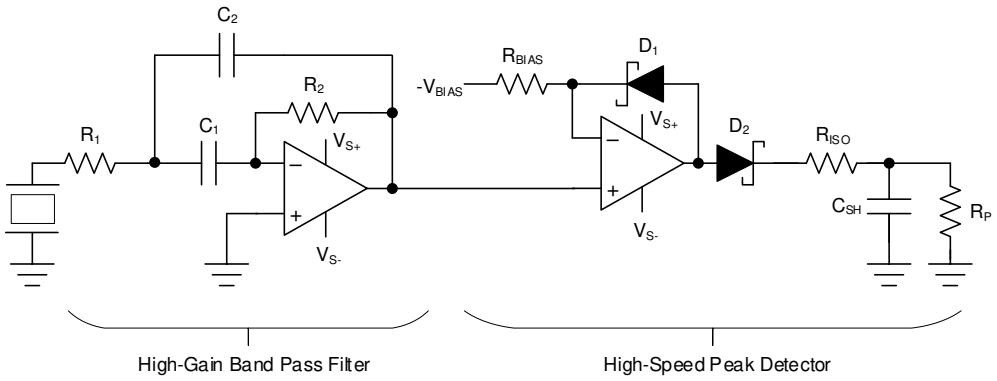


Figure 9-3. High-Gain Narrow Bandpass Filter and Peak Detector Circuit

Ultrasonic signaling is used for proximity and obstacle detection, level sensing, sonars, and so forth. Such signal chains detect the amplitude of received ultrasonic signal at a particular center frequency. Figure 9-3 shows a high-gain narrow bandpass filter and peak detector circuit using any of the OPAx863 devices. The signal at the frequency of interest is filtered out, gained, and peak detected to report the amplitude at the output of this circuit. The phase information is lost in this circuit. The OPAx863 devices are used with the 50-MHz GBW to add a single-stage gain and filtering, and the peak detection capability is easily made with the RRIO capability of these amplifiers.

9.2.3 Low-Power SAR ADC Driver and Reference Buffer

Figure 9-4 shows the use of the OPAx863 as a SAR ADC input driver and reference buffer driving the ADS7945. sensors, which are used for interface with the physical environment, exhibit high output impedance, and cannot drive SAR ADC inputs directly. A wide-GBW amplifier, such as the OPAx863, is needed to charge the switching capacitors at the SAR ADC input, and quickly settle to the required accuracy within the given acquisition time. The ADC core draws transient current from the reference input during the conversion (digitization) phase, which must be driven with a wide-GBW amplifier to offer fast settling and maintain a stable reference voltage for excellent digitization performance. The OPAx863 reference buffer is used in a composite loop with the OPA378 precision amplifier because of limitations in precision performance of wide-GBW amplifiers. The precision amplifier maintains low-offset output, whereas the OPAx863 devices provide the output drive and fast-settling performance.

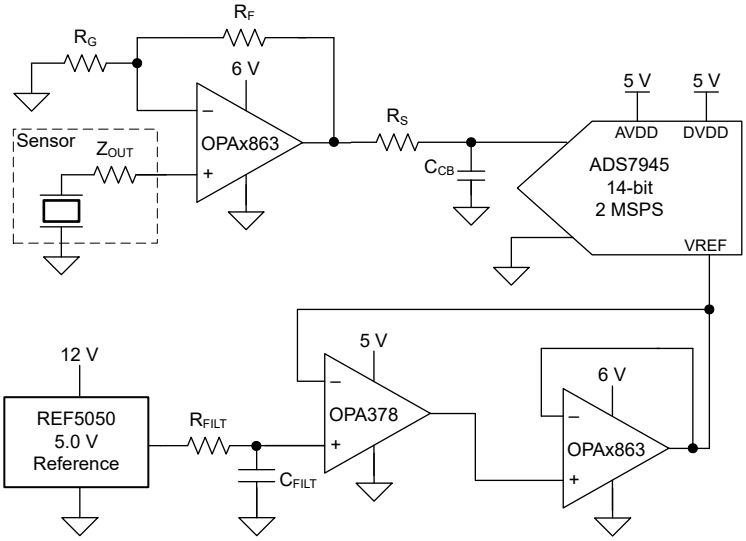


Figure 9-4. OPAx863 as Low-Power SAR ADC Driver

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9.2.4 Variable Reference Generator Using MDAC

High-speed amplifiers can be used as a voltage buffer at MDAC output to generate a fast-settling variable reference voltage. Figure 9-5 shows a representative circuit using DAC8801 and OPAx863.

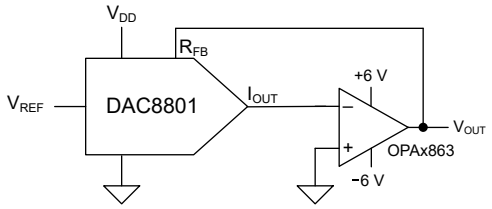


Figure 9-5. Variable Reference Generator Using MDAC and OPAx863

9.2.5 Clamp-On Ultrasonic Flow Meter

Figure 9-6 shows how ultrasonic flow meters measure the rate of flow of a liquid using transit-time difference (t_{12}–t_{21}), which depends on the flow rate. Figure 9-6 shows a representative schematic for a non-intrusive ultrasonic flow meter using the OPAx863 and 12-V transducer excitation. The OPAx863 are used for the forward path as a unity-gain buffer for 12-V pulsed transducer excitation at NODE 1. At the same time, the receiver circuit at NODE 2 (which also uses the OPAx863) first provides an ac-gain followed by a dc-level shift to lead to the PGA, ADC, and processor within the MSP430™ microcontroller.

NODE 2 and NODE 1 use similar transmit and receive circuits (discussed previously) for the reverse path. The OPAx863 wide GBW of 50 MHz introduces minimal phase-delay and low-noise for excellent flow rate measurement. The amplifier stays in power-down mode for a majority of the time in battery-powered systems. This configuration results in very small average system-level power consumption and prolonged battery lifetime with the 1.5-µA (maximum) power-down mode quiescent current with a 3-V supply. The transmit and receive signal chains are connected to the same point at the respective node transducers. Therefore, the OPAx863 12.6-V supply voltage capability enables 12-V transducer excitation without any damage to the front-end, or a need for external switches, thus enabling a more compact solution. These specifications make the OPAx863 an excellent choice for flow measurements in large diameter pipes and non-intrusive flow meters. The TIDM-02003 reference design discusses an ultrasonic gas flow sensing subsystem which uses high-speed amplifiers for front-end amplification.

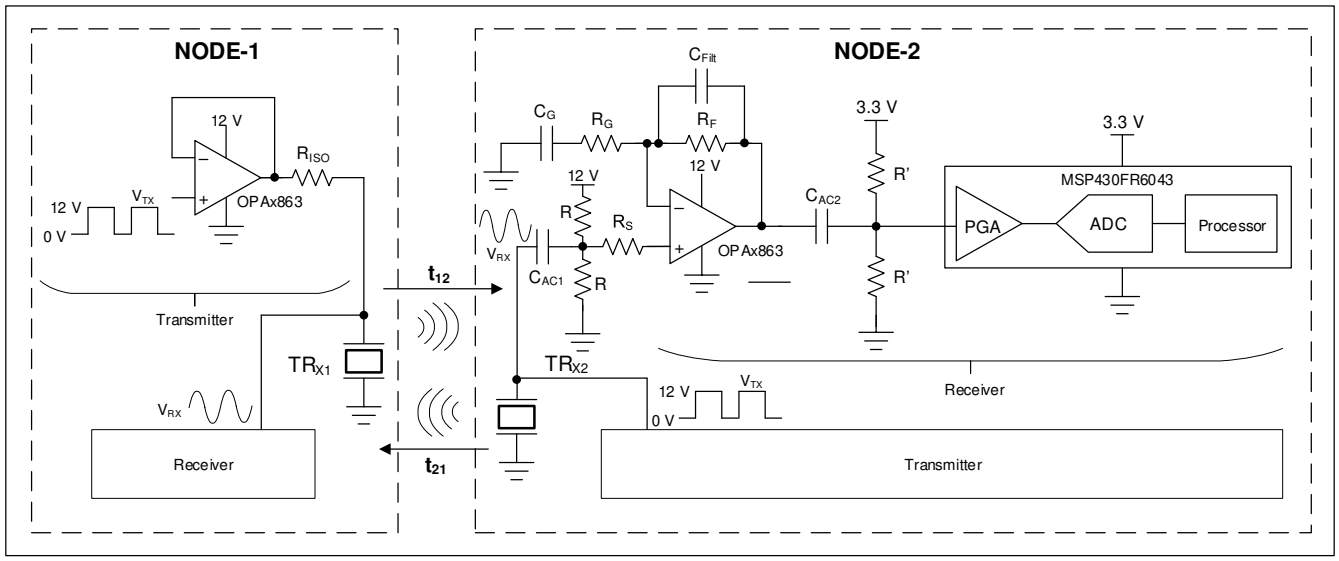


Figure 9-6. Non-Intrusive Ultrasonic Flow Meter

9.3 Power Supply Recommendations

The OPAx863 is intended to operate on supplies ranging from 2.7 V to 12.6 V. The OPAx863 devices operate on single-sided supplies, split and balanced bipolar supplies, or unbalanced bipolar supplies. Operating from a single supply has numerous advantages. The dc errors, due to the –PSRR term, can be minimized with the negative supply at ground. Typically, ac performance improves slightly at 10-V operation with minimal increase in supply current. Minimize the distance (< 0.1 in) from the power supply pins to high-frequency, 0.01-µF decoupling capacitors. A larger capacitor (2.2 µF typical) is used along with a high-frequency, 0.01-µF supply-decoupling capacitor at the device supply pins. Only the positive supply has these capacitors for single-supply operation. Use these capacitors from each supply to ground when a split-supply is used. If necessary, place the larger capacitors further from the device and share these capacitors among several devices in the same area of the printed circuit board (PCB). An optional supply decoupling capacitor across the two power supplies (for split-supply operation) reduces second harmonic distortion.

9.4 Layout

9.4.1 Layout Guidelines

Achieving optimum performance with a high-frequency amplifier (like the OPAx863) requires careful attention to board layout parasitics and external component types. The *OPA2863 DGK Evaluation Module* user's guide can be used as a reference when designing the circuit board. Recommendations that optimize performance includes the following:

1. **Minimize parasitic capacitance** to any ac ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability on the noninverting input and can react with the source impedance to cause unintentional band-limiting. Open a window around the signal I/O pins in all of the ground and power planes around those pins to reduce unwanted capacitance. Otherwise, ground and power planes must be unbroken elsewhere on the board.
2. **Minimize the distance** (< 0.1 in) from the power-supply pins to high-frequency 0.01-µF decoupling capacitors. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections must always be decoupled with these capacitors. Larger (2.2-µF to 6.8-µF) decoupling capacitors, effective at lower frequency, must also be used on the supply pins. These capacitors can be placed somewhat farther from the device and shared among several devices in the same area of the PCB.
3. **Careful selection and placement of external components preserves the high-frequency performance of the OPAx863.** Resistors must be a low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Other network components, such as noninverting input termination resistors, must also be placed close to the package. Keep resistor values as low as possible and consistent with load-driving considerations. Lowering the resistor values keeps the resistor noise terms low and minimizes the effect of the parasitic capacitance. Lower resistor values, however, increase the dynamic power consumption because R_F and R_G become part of the amplifier output load network.

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9.4.1.1 Thermal Considerations

The OPAx863 does not require heat sinking or airflow in most applications. The maximum allowed junction temperature sets the maximum allowed internal power dissipation. Do not allow the maximum junction temperature to exceed 150°C.

Operating junction temperature (T_J) is given by,

$$T_J = T_A + P_D \times R_{\Theta JA} \quad (4)$$

where

- T_A is the ambient temperature
- P_D is the total power dissipation internal to the amplifier
- $R_{\Theta JA}$ is the junction-to-ambient thermal resistance

The total power dissipation $P_D = P_{DQ} + P_{DL}$

where

- $P_{DQ} = (V_{S+} - V_{S-}) \times I_Q$, is the power dissipation due to the amplifier quiescent current
- $P_{DL}(max) = V_S{}^2 / (4 \times R_L)$, is the internal power dissipation due to the output load current

As a worst-case example, compute the maximum T_J using an OPA2863-DGK (VSSOP package) configured as a unity gain buffer, operating on ±6-V supplies at an ambient temperature of 25°C and driving a grounded 500-Ω load.

$$P_D = 12\ V \times 2\ mA + 6^2 / (4 \times 500\ \Omega) = 42\ mW \quad (5)$$

Maximum T_J = 25°C + (0.042 W × 180.3°C/W) = 33°C, which is much less than the maximum allowed junction temperature of 150°C.

9.4.2 Layout Example

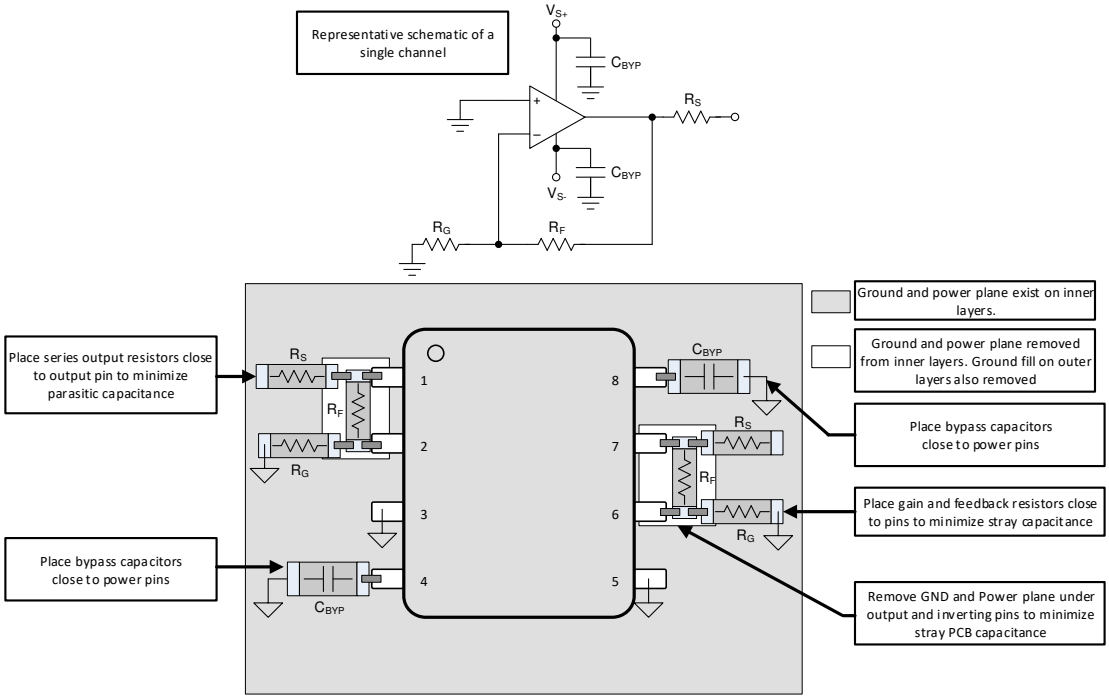


Figure 9-7. Layout Recommendation for Dual-Channel DGK Package

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *OPA2863ADGK Evaluation Module* user's guide
- Texas Instruments, *Single-Supply Op Amp Design Techniques* application report

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

MSP430™ and TI E2E™ are trademarks of Texas Instruments.
All trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2863DR	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O2863D
OPA2863DR.B	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O2863D
OPA2863IDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 125	2FJ4
OPA2863IDGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	2FJ4
OPA2863RUNR	Active	Production	QFN (RUN) | 10	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	O263
OPA2863RUNR.B	Active	Production	QFN (RUN) | 10	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	O263
OPA4863PWR	Active	Production	TSSOP (PW) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OPA4863
OPA863DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2QS5
OPA863DBVR.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	2QS5
OPA863SIDBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	O863
OPA863SIDBVR.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	O863

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF OPA2863 :

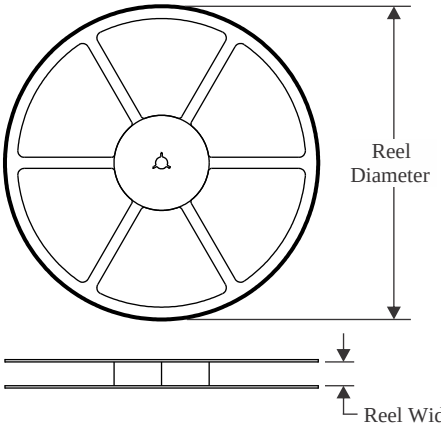
- Automotive : OPA2863-Q1

NOTE: Qualified Version Definitions:

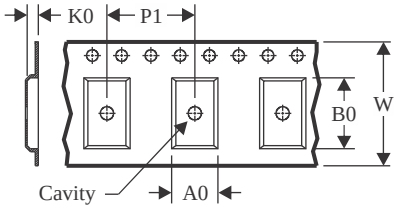
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

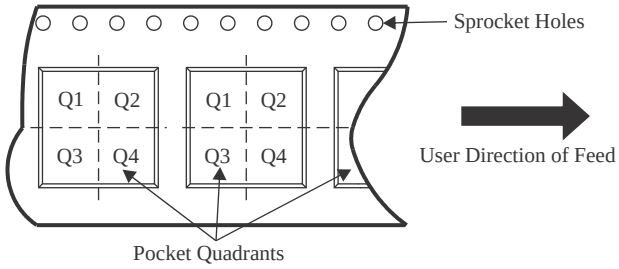


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

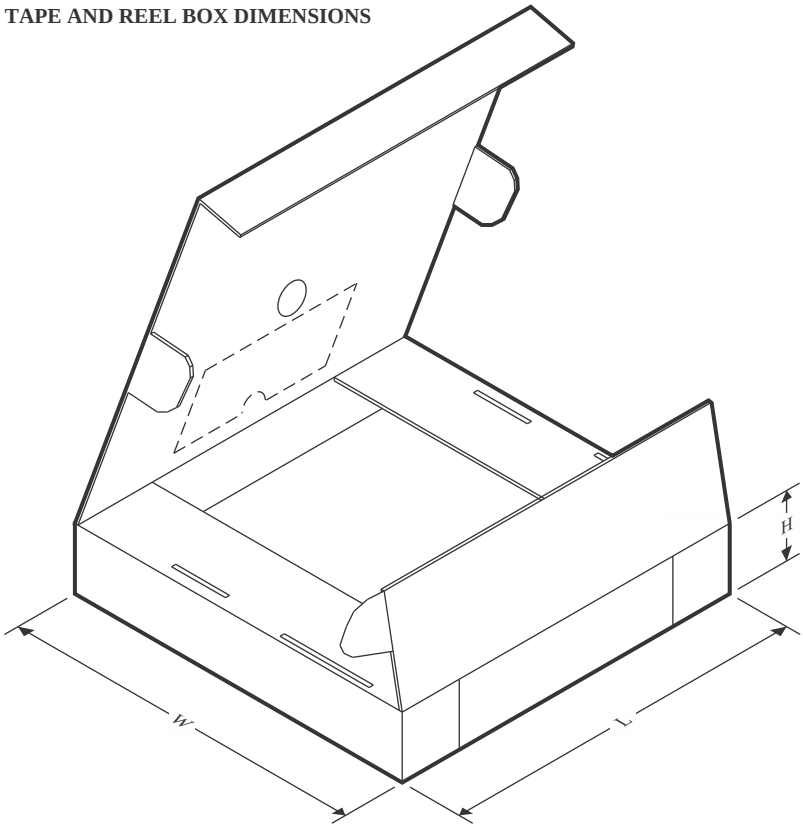
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2863DR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2863IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
OPA2863RUNR	QFN	RUN	10	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
OPA4863PWR	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
OPA863DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA863SIDBVR	SOT-23	DBV	6	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2863DR	SOIC	D	8	3000	353.0	353.0	32.0
OPA2863IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2863RUNR	QFN	RUN	10	3000	213.0	191.0	35.0
OPA4863PWR	TSSOP	PW	14	3000	353.0	353.0	32.0
OPA863DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
OPA863SIDBVR	SOT-23	DBV	6	3000	190.0	190.0	30.0

GENERIC PACKAGE VIEW

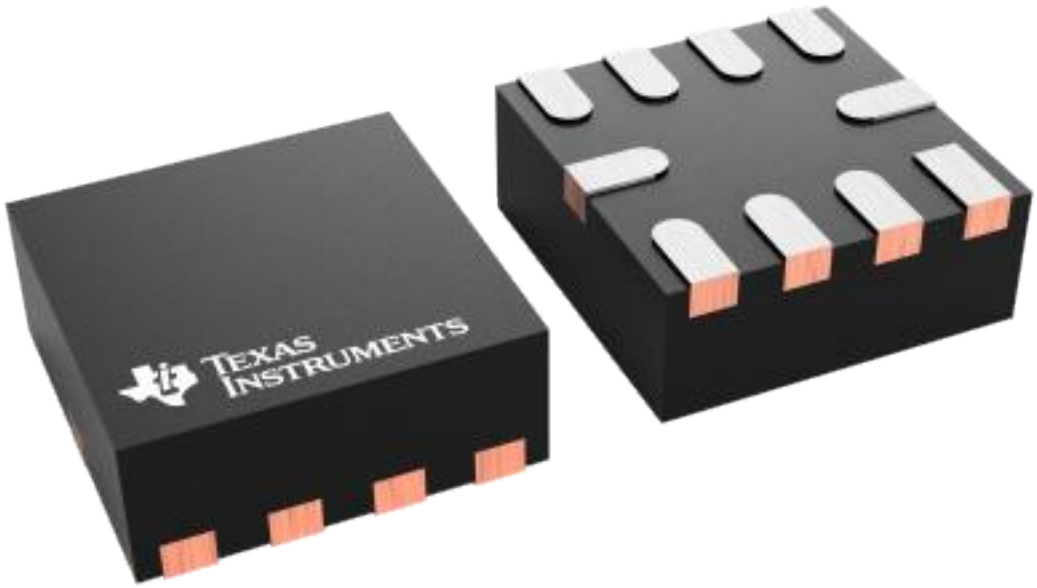
RUN 10

WQFN - 0.8 mm max height

2 X 2, 0.5 mm pitch

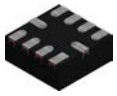
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4228249/A

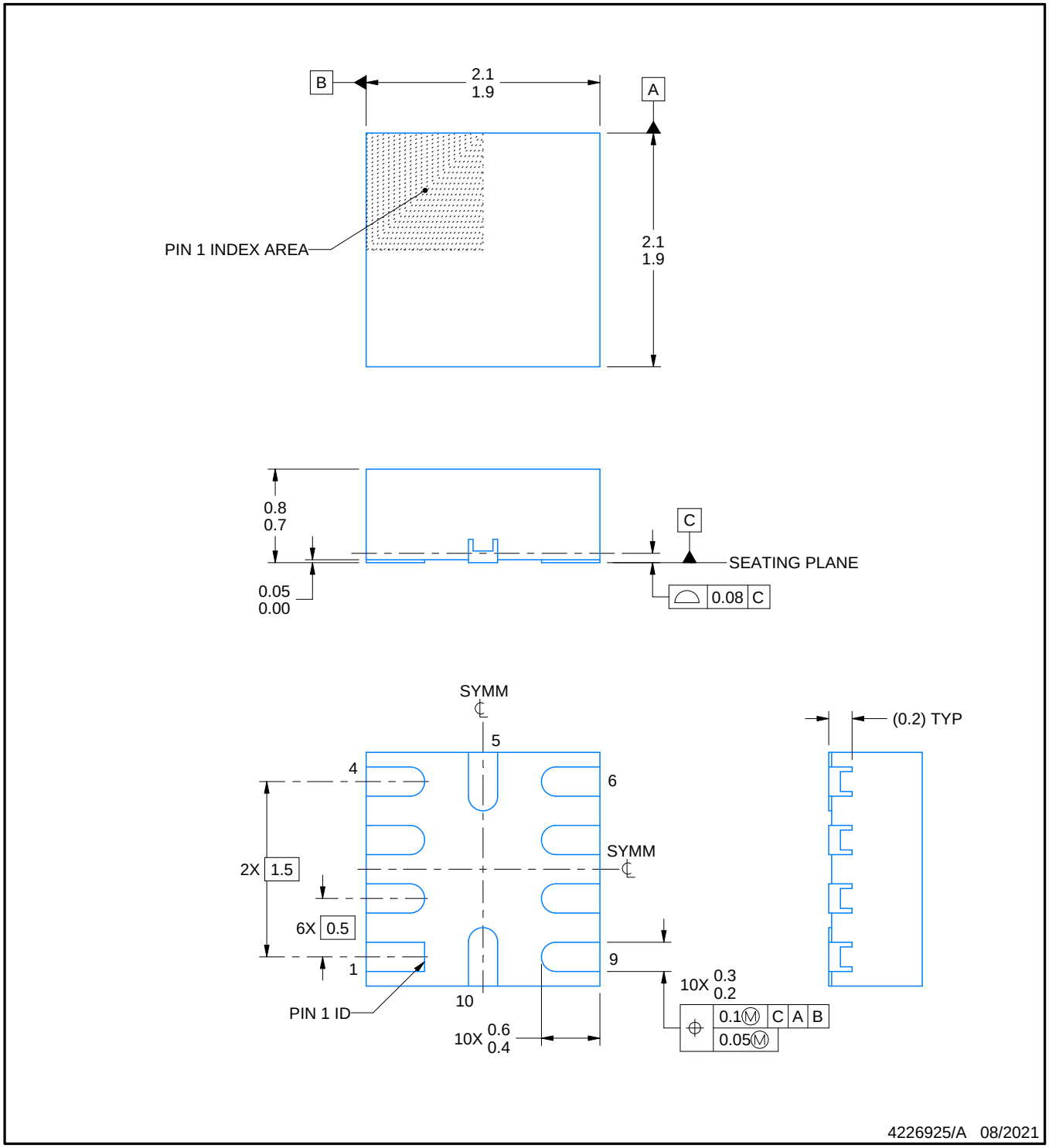
RUN0010B



PACKAGE OUTLINE

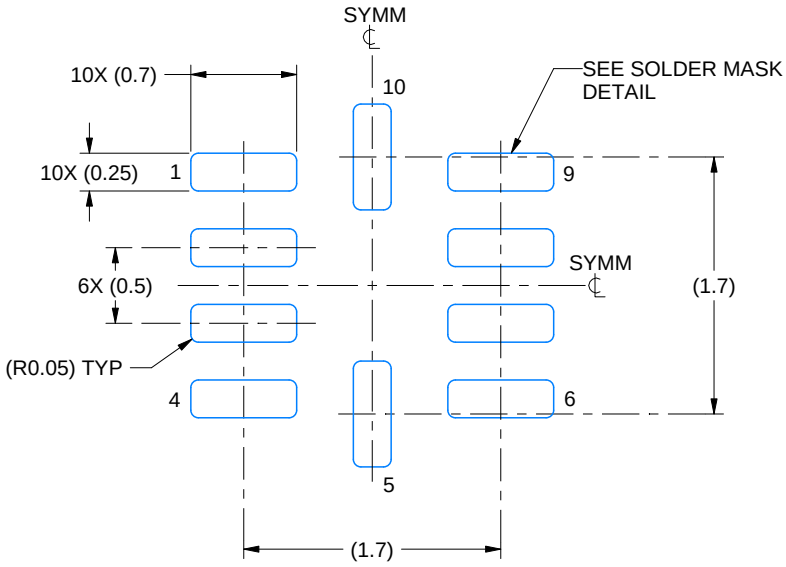
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

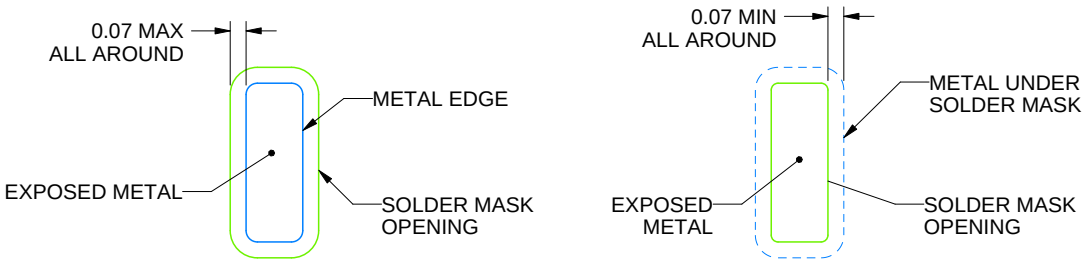


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4226925/A 08/2021

NOTES: (continued)

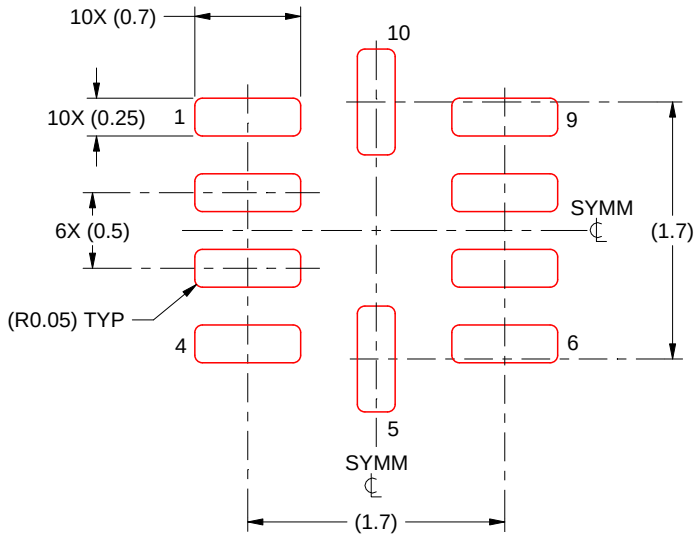
3. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

RUN0010B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

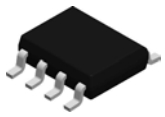


SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

4226925/A 08/2021

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

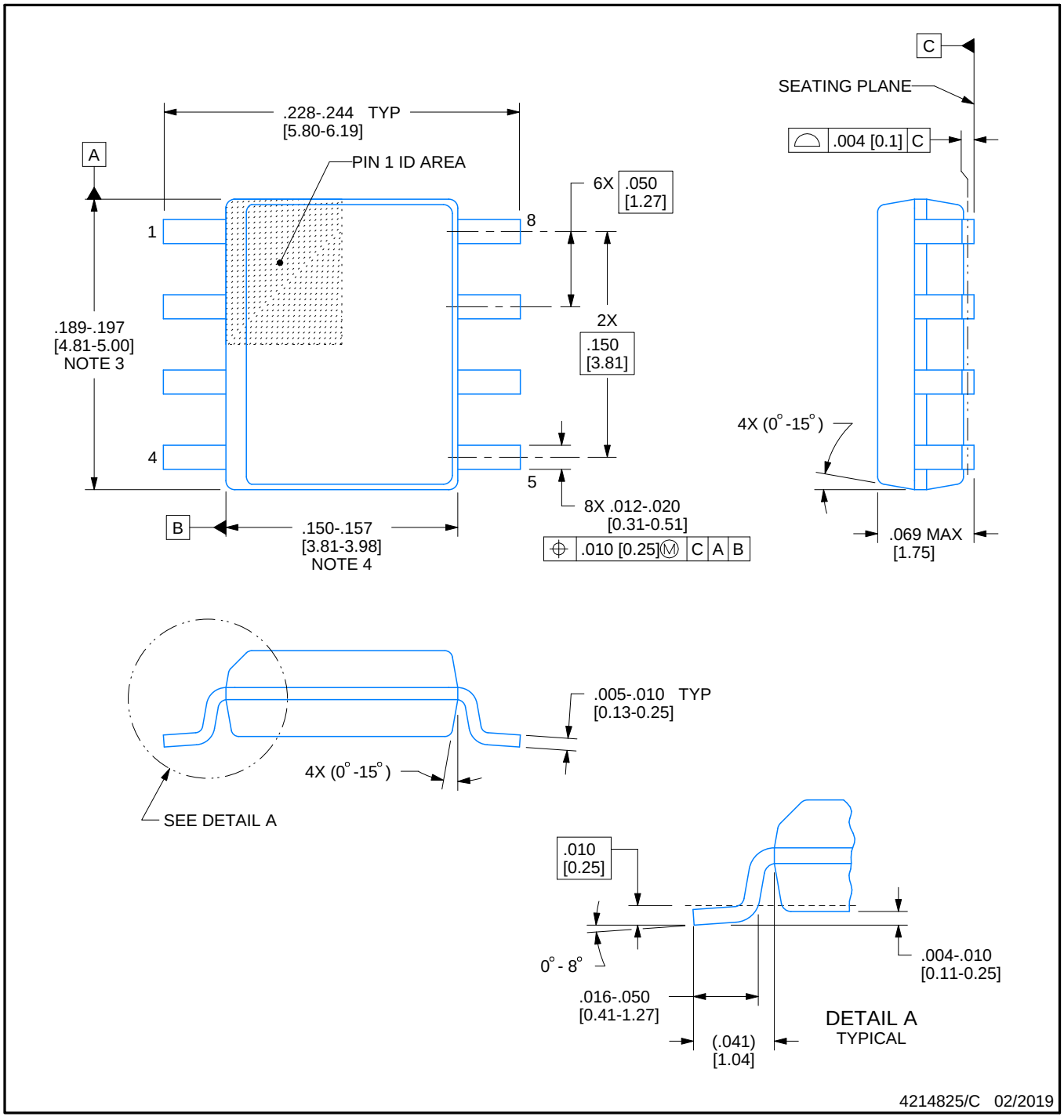


PACKAGE OUTLINE

D0008A

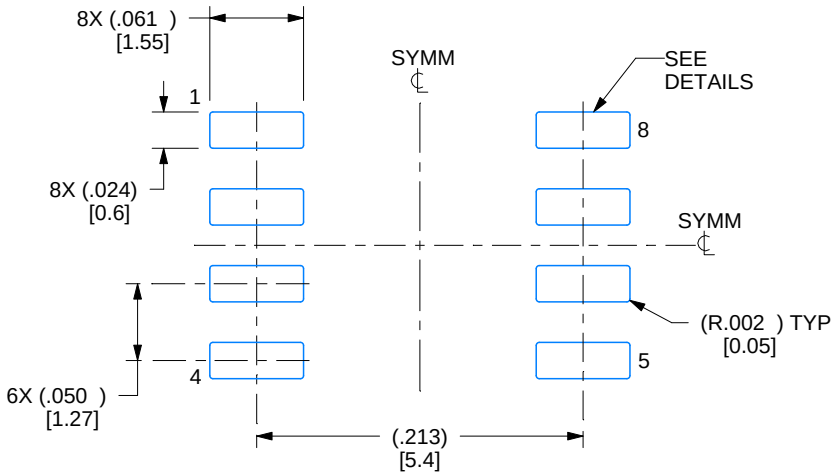
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

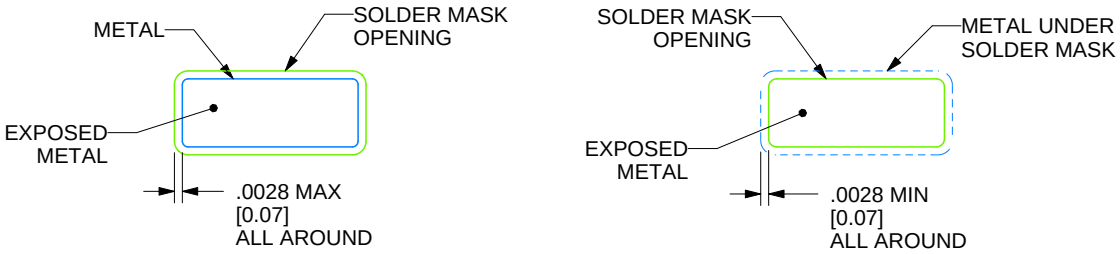


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

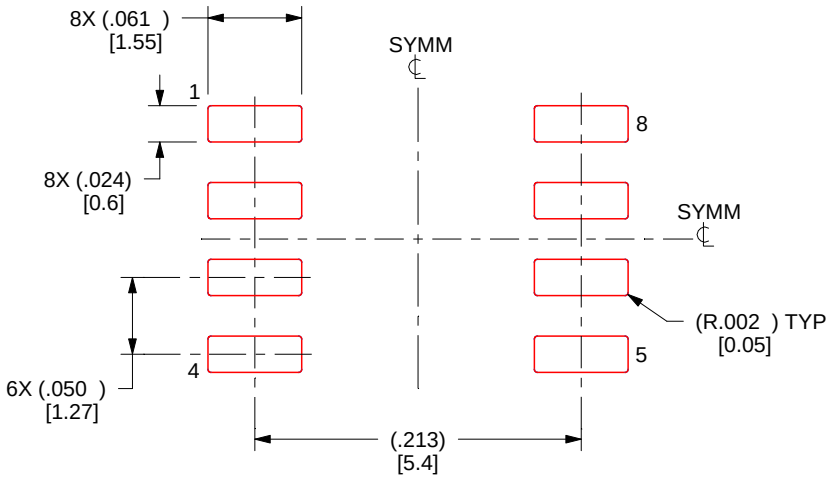
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

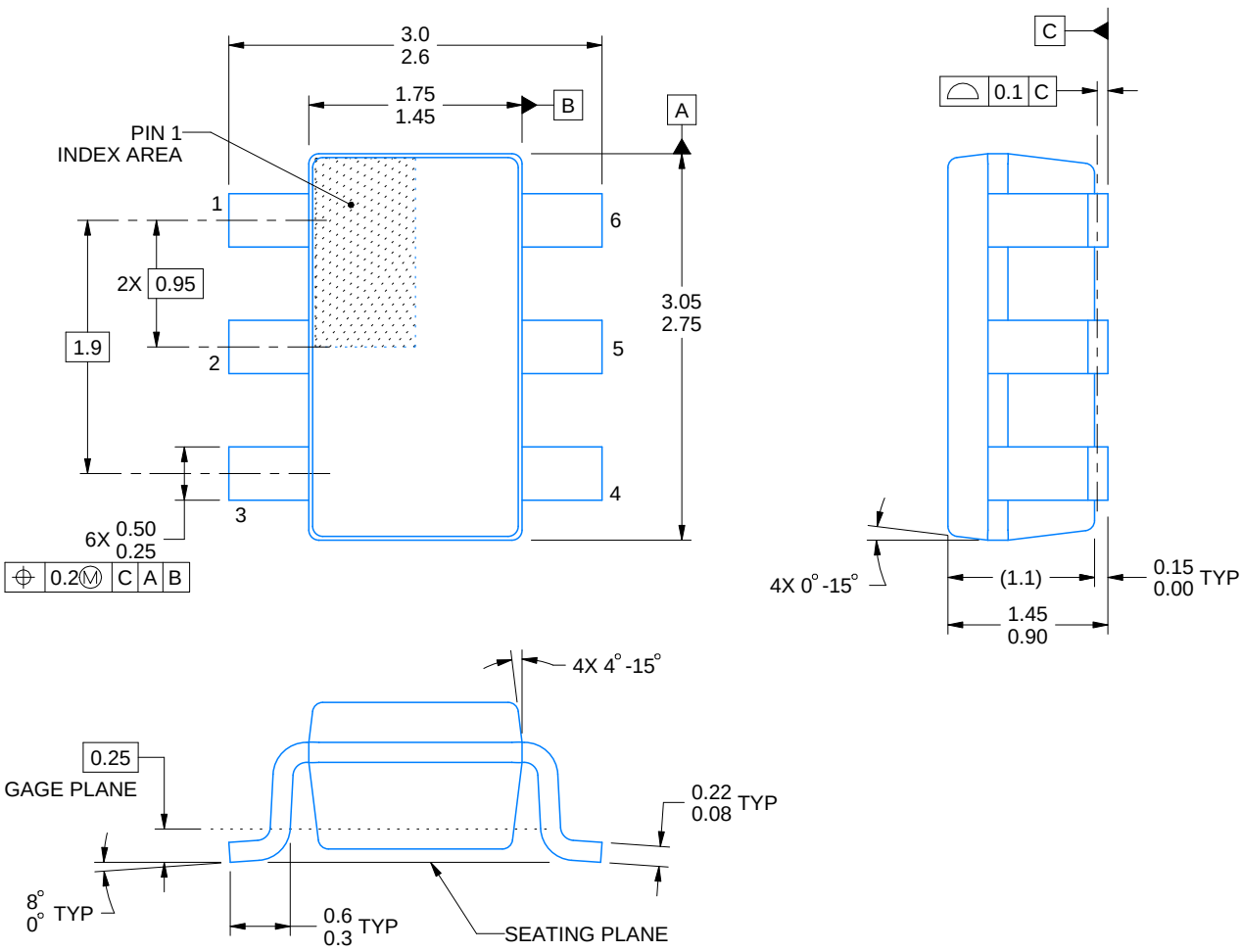
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

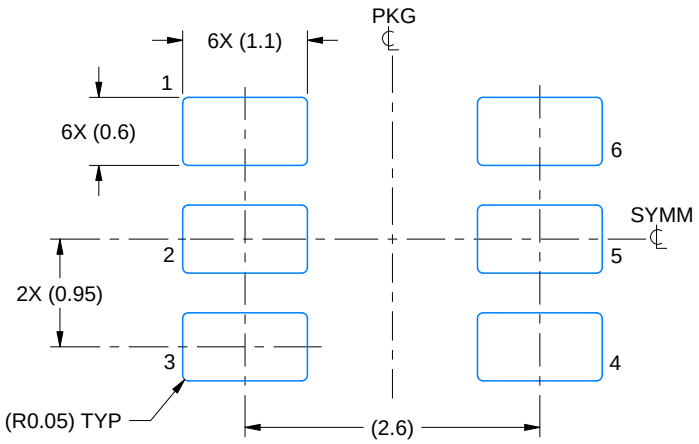
SMALL OUTLINE TRANSISTOR



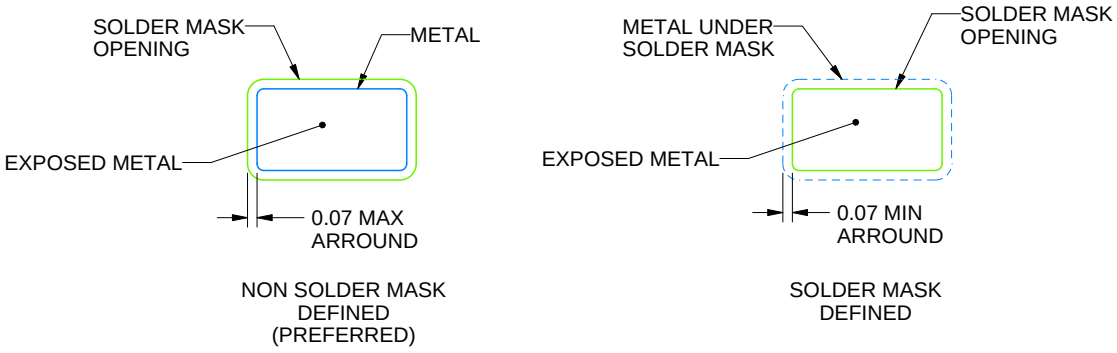
4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

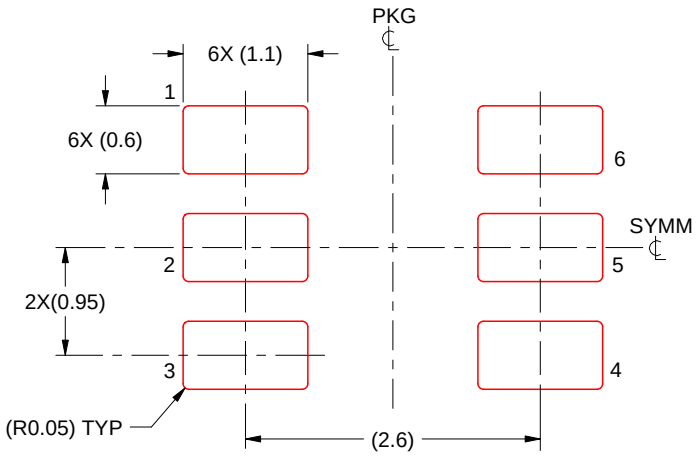


SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

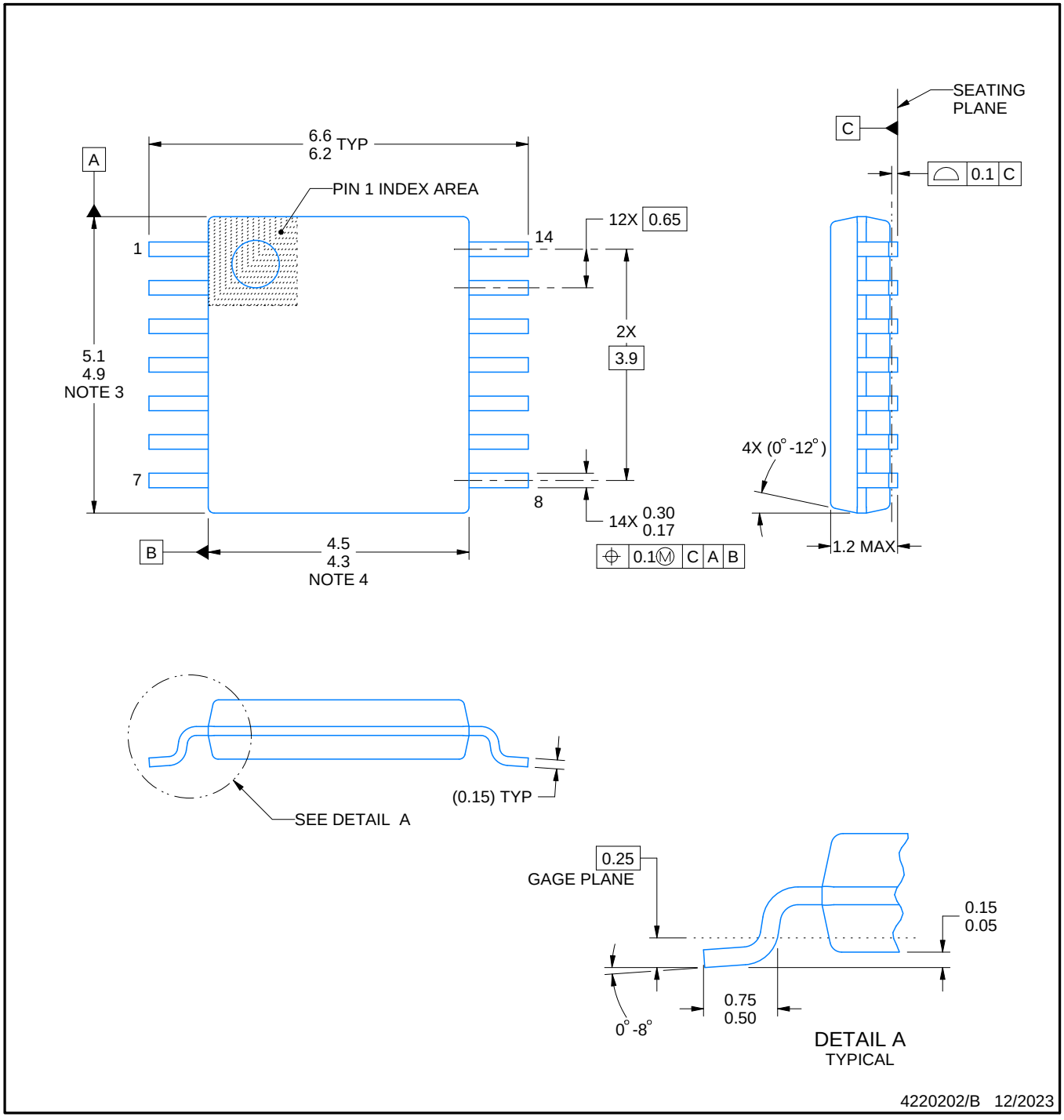
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0014A

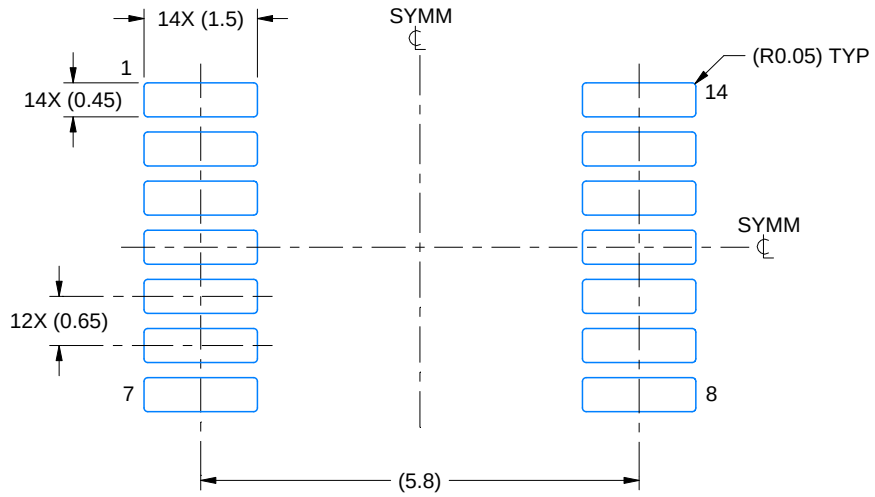
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

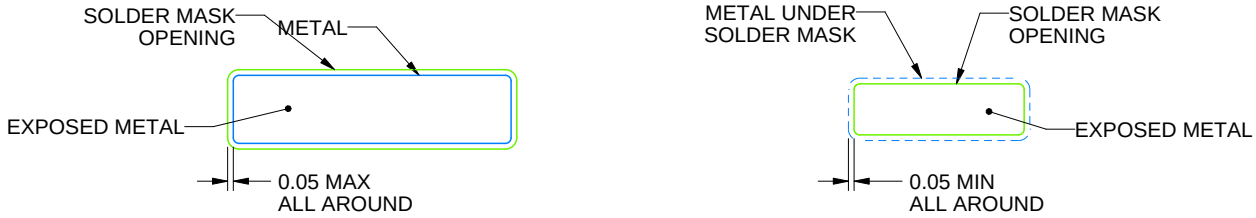


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

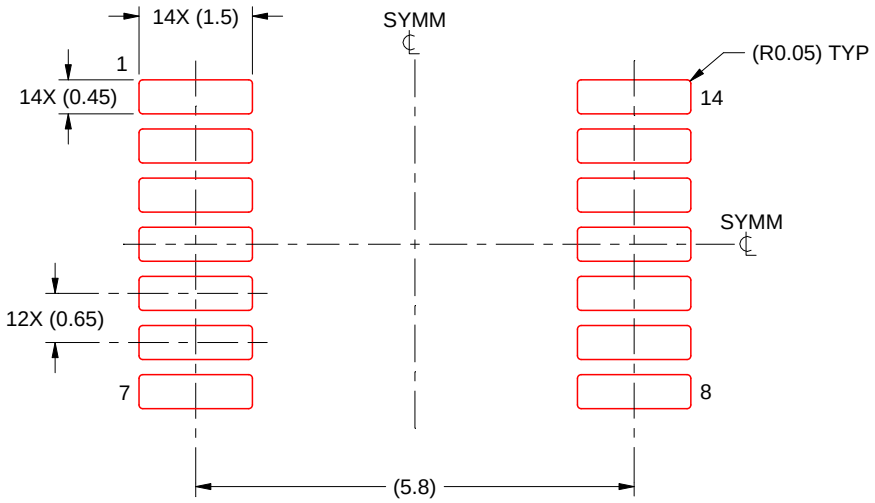


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

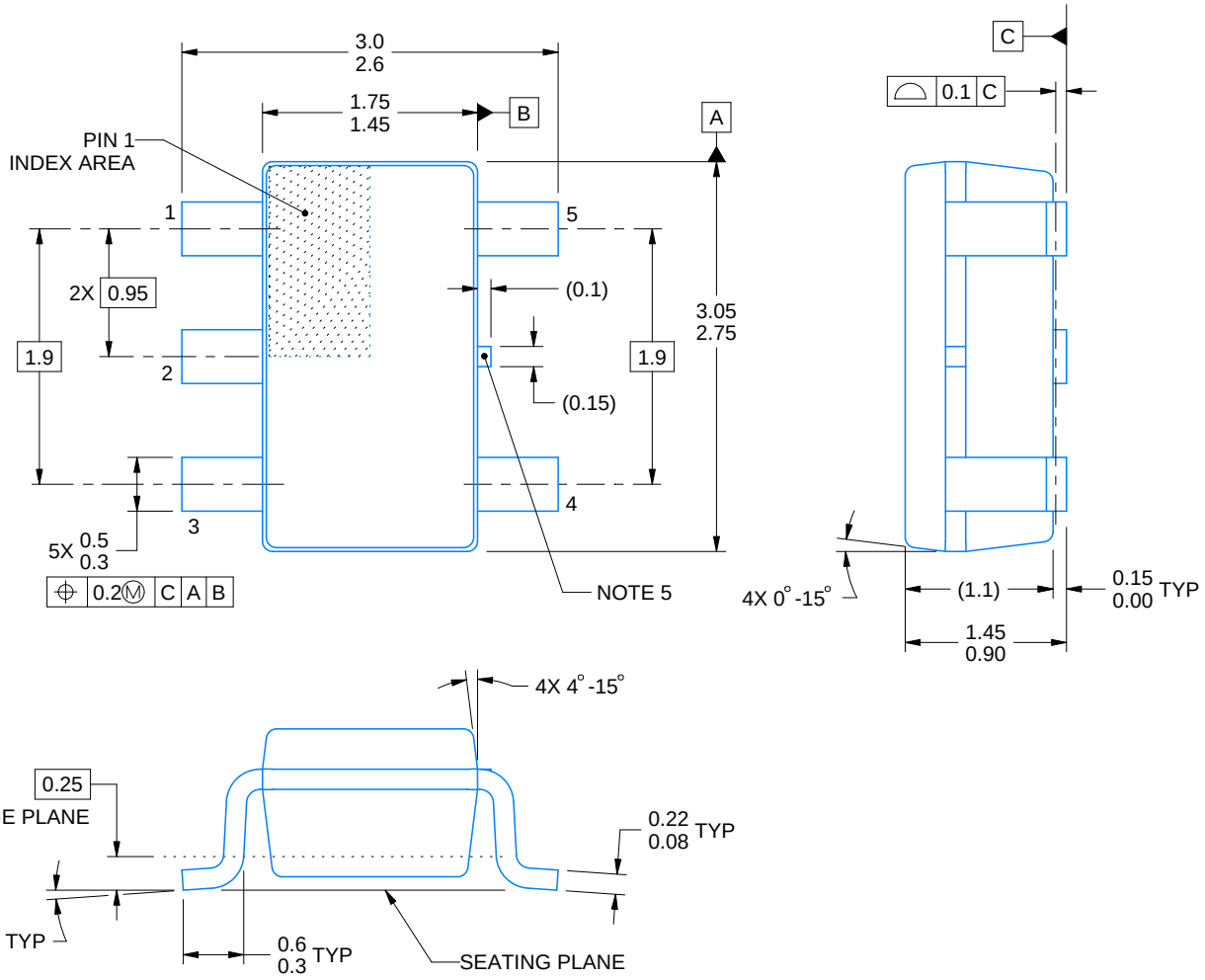
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

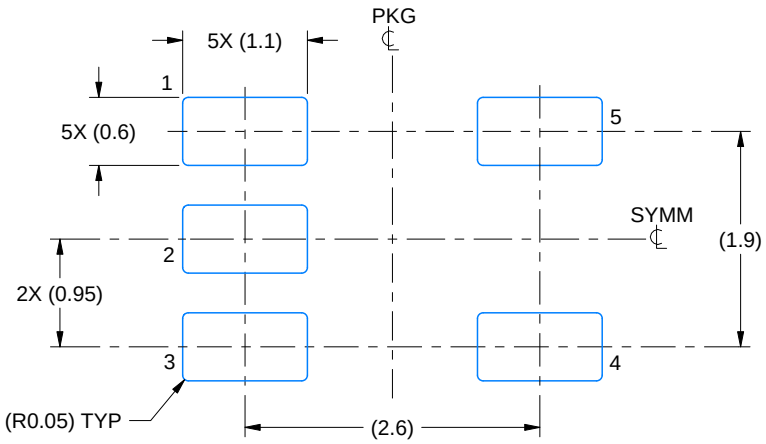
SMALL OUTLINE TRANSISTOR



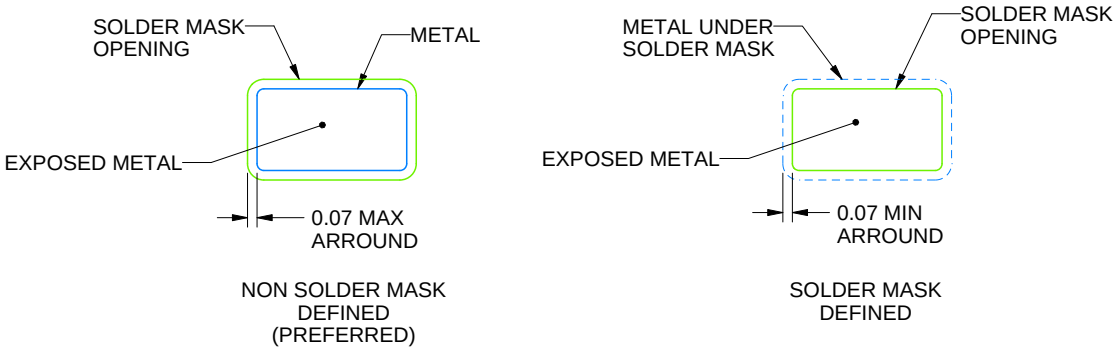
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

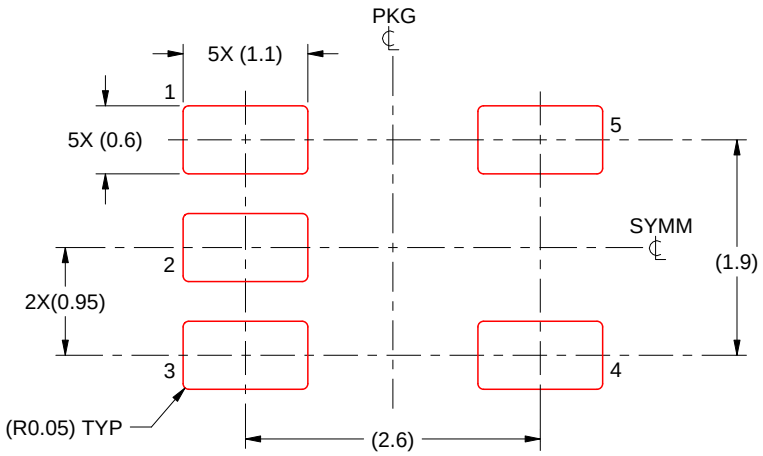


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

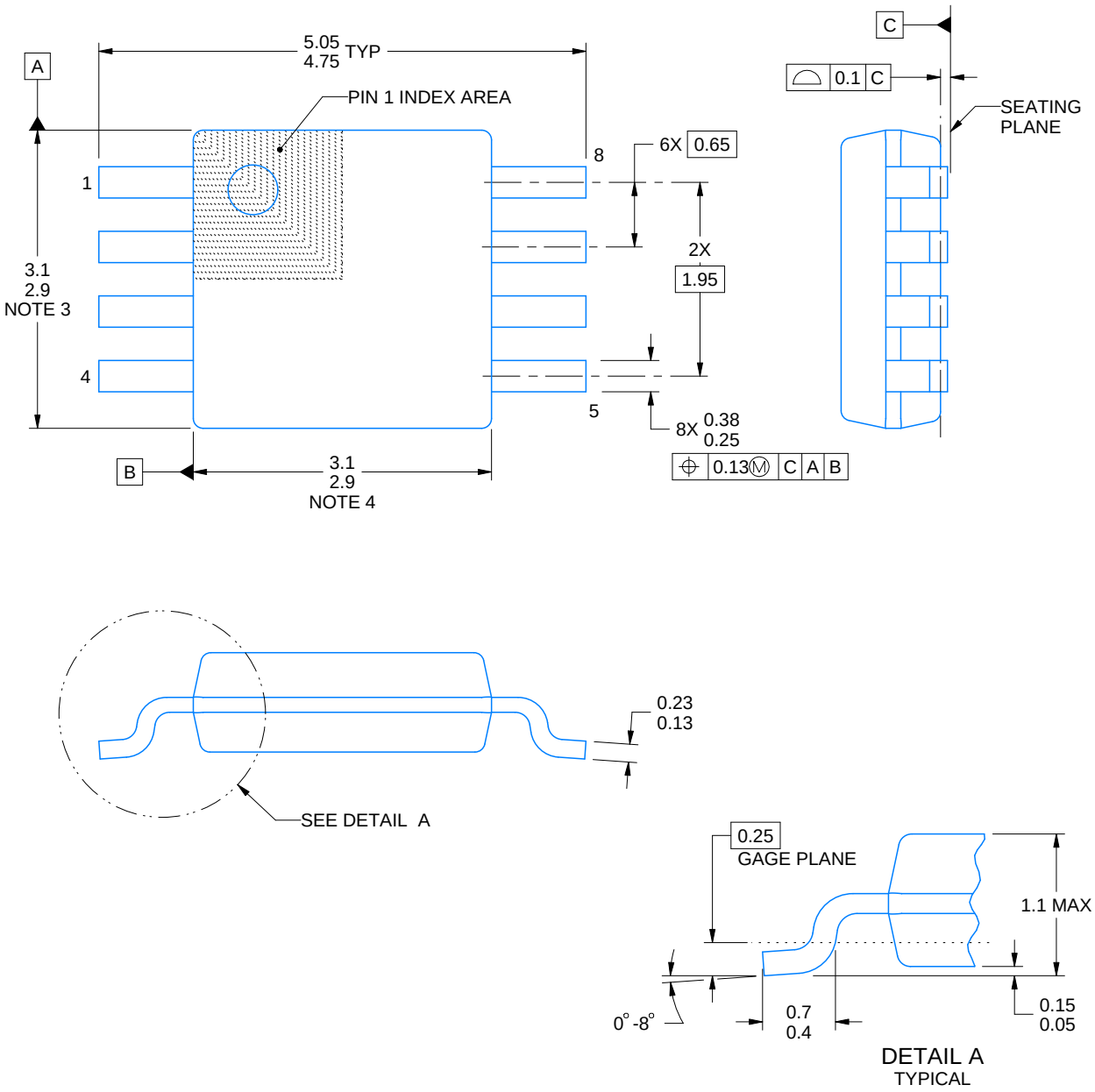
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

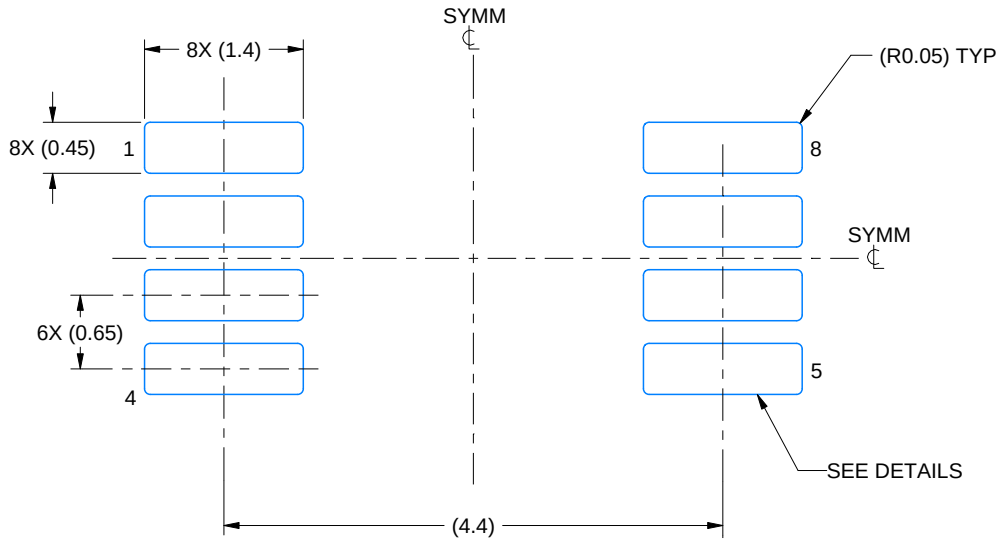
SMALL OUTLINE PACKAGE



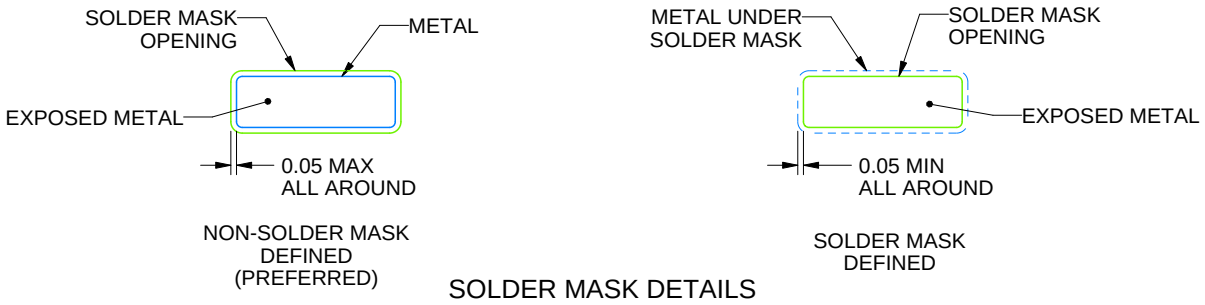
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

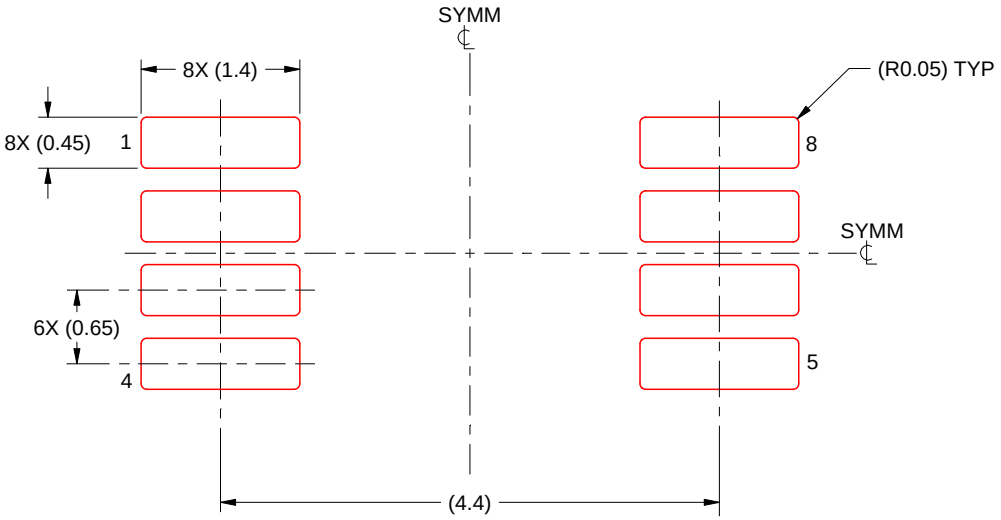


SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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