TEXAS INSTRUMENTS
Burr-Brown Audio

PCM1681 24-Bit, 192-kHz Sampling, Enhanced Multilevel Delta-Sigma, Eight-Channel Audio Digital-to-Analog Converter

1 Features

- Qualified for Automotive Applications: PCM1681-Q1
- 24-Bit Resolution
- Analog Performance:
  - Dynamic Range: 105 dB Typical
  - SNR: 105 dB Typical
  - THD+N: 0.002% Typical
  - Full-Scale Output: 3.75 V_{PP} Typical
- 4×/8× Oversampling Interpolation Filter:
  - Stop-Band Attenuation: –57 dB
  - Pass-Band Ripple: ±0.015 dB
- Sampling Frequency: 5 kHz to 200 kHz
- System Clock: 128 f_S, 192 f_S, 256 f_S, 384 f_S, 512 f_S, 768 f_S, or 1152 f_S with Autodetect
- Zero Flags for Selectable Channel Combinations
- Flexible Mode Control:
  - SPI™/I²C™ Dual Mode for Serial Port
  - Parallel Hardware Control with 4 Functions
- User-Programmable Functions (in SPI/I²C):
  - Flexible Audio Data Formats:
    - Right-Justified, I²S™, Left-Justified, TDM, DSP
    - 16- and 24-Bit Audio Data
  - Digital Attenuation: Mode Selectable
    - 0 dB to –63 dB, 0.5 dB/step
    - 0 dB to –100 dB, 1 dB/step
  - Soft Mute
  - Digital De-Emphasis
  - Digital Filter Roll-Off: Sharp or Slow
  - Oversampling Mode
- User-Programmable Functions (in H/W):
  - Flexible Audio Data Formats:
    - Right-Justified, I²S, Left-Justified, TDM
    - Soft Mute
    - Digital De-Emphasis
    - Oversampling Mode
- Power Supply Voltage: 5-V Analog, 3.3-V Digital
- Package: 28-Lead HTSSOP PowerPAD™
- Operation Temperature Range:
  - –40°C to 85°C for Consumer Grade
  - –40°C to 105°C for Automotive Audio Grade

2 Applications

- Car Audio External Amplifiers
- Car Audio AVN Applications
- Integrated A/V Receivers
- DVD Movie and Audio Players
- HDTV Receivers
- DVD Add-On Cards for High-End PCs
- Digital Audio Workstations
- Other Multichannel Audio Systems

3 Description

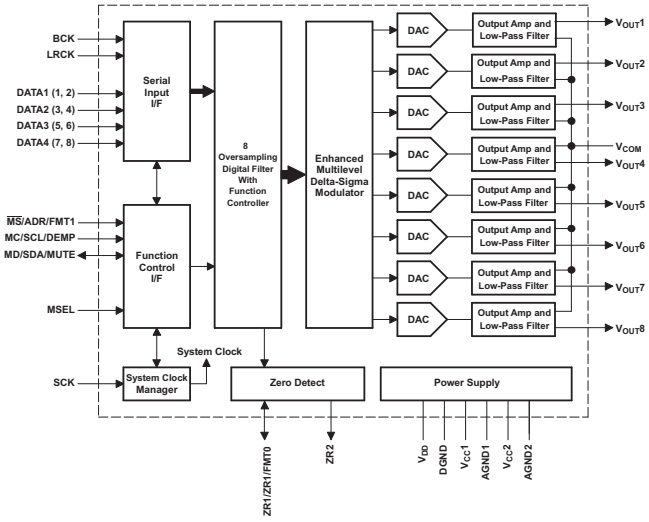
The PCM1681 and PCM1681-Q1 are CMOS monolithic integrated circuits which feature an eight-channel 24-bit audio digital-to-analog converter (DAC) and support circuitry in small 28-lead TSSOP PowerPAD packages. The DACs utilize Burr-Brown's enhanced multilevel delta-sigma (ΔΣ) architecture to achieve excellent signal-to-noise performance and a high tolerance to clock jitter.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
PCM1681	HTSSOP (28)	9.70 mm × 4.40 mm
PCM1681-Q1		

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Functional Block Diagram



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (June 2008) to Revision C — **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision A (June 2008) to Revision B — **Page**

- Added new device grade PCM1681-Q1 ... 1
- Changed device names in Operating Free-Air Temperature row of the *Recommended Operating Conditions* table ... 6
- Changed device names in Operating Temperature row of *Temperature Range* section in the Electrical Characteristics table ... 8
- Added third paragraph to *PCB Layout Guidelines* section ... 35

Changes from Original (February 2008) to Revision A — **Page**

- Added last sub-level bullet to *Features* ... 1
- Added first two bullets to *Applications* ... 1
- Changed last sentence in *Description* ... 1
- Added last row to *Recommended Operating Conditions* table ... 6
- Added second row to *Temperature Range* section of the Electrical Characteristics table ... 8

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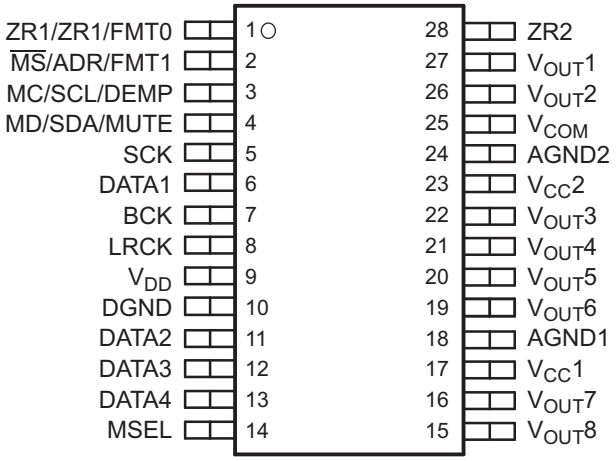
5 Description (continued)

The PCM1681 and PCM1681-Q1 accept TDM (time-division multiplexed) format in addition to industry-standard audio data formats with 16- to 24-bit audio data width. Sampling rates up to 200 kHz are supported. The PCM1681 and PCM1681-Q1 provide a sub-set of user-programmable functions through a parallel control port, in addition to a full set of user-programmable functions through a serial control port, SPI, or I^2C. The PCM1681 supports –40°C to +85°C for consumer grade applications and the PCM1681-Q1 supports –40°C to +105°C for automotive audio grade systems.

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6 Pin Configuration and Functions

PWP Package
28-Pin HTSSOP PowerPAD
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND1	18	–	Analog ground
AGND2	24	–	Analog ground
BCK	7	I	Shift clock input for serial audio data (1) (2)
DATA1	6	I	Serial audio data input for $V_{OUT}1$ and $V_{OUT}2$ (1) (2)
DATA2	11	I	Serial audio data input for $V_{OUT}3$ and $V_{OUT}4$ (1) (2)
DATA3	12	I	Serial audio data input for $V_{OUT}5$ and $V_{OUT}6$ (1) (2)
DATA4	13	I	Serial audio data input for $V_{OUT}7$ and $V_{OUT}8$ (1) (2)
DGND	10	–	Digital ground
LRCK	8	I	Left and right clock input. The frequency of this clock is equal to the sampling rate, f_S. (1) (2)
MC/SCL/DEMP	3	I	Shift clock input for SPI, serial clock input for I^2C, de-emphasis control for H/W (1) (2)
MD/SDA/MUTE	4	I/O	Serial data input for SPI, serial data input/output for I^2C, mute control for H/W (1) (2) (3)
$\overline{MS}$/ADR/FMT1	2	I	Select input for SPI, address input for I^2C, format control input 1 for H/W (1) (2)
MSEL	14	I	Mode control select, I^2C, H/W with narrow mode O/S, H/W with wide mode O/S, SPI select (1) (4)
SCK	5	I	System clock input. Input frequency is 128, 192, 256, 384, 512, 768, or 1152 f_S. (1) (2)
$V_{CC}1$	17	–	Analog power supply, 5-V
$V_{CC}2$	23	–	Analog power supply, 5-V
V_{COM}	25	–	Common voltage output. This pin should be bypassed with a 10-µF capacitor to AGND.
V_{DD}	9	–	Digital power supply, 3.3-V
$V_{OUT}1$	27	O	Voltage output for audio signal corresponding to L-ch on DATA1
$V_{OUT}2$	26	O	Voltage output for audio signal corresponding to R-ch on DATA1
$V_{OUT}3$	22	O	Voltage output for audio signal corresponding to L-ch on DATA2
$V_{OUT}4$	21	O	Voltage output for audio signal corresponding to R-ch on DATA2
$V_{OUT}5$	20	O	Voltage output for audio signal corresponding to L-ch on DATA3

(1) Schmitt-trigger input.
(2) 5-V tolerant.
(3) Open-drain output in I^2C mode.
(4) $V_{DD}/2$ biased, quad state input.

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Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
$V_{OUT}6$	19	O	Voltage output for audio signal corresponding to R-ch on DATA3
$V_{OUT}7$	16	O	Voltage output for audio signal corresponding to L-ch on DATA4
$V_{OUT}8$	15	O	Voltage output for audio signal corresponding to R-ch on DATA4
ZR1/ZR1 /FMT0	1	I/O	Zero-flag output 1 for SPI, zero-flag output 1 for I^2C, format control input 0 for H/W(1)
ZR2	28	O	Zero-flag output 2

7 Specifications

7.1 Absolute Maximum Ratings(1)

Over operating free-air temperature range (unless otherwise noted).

		MIN	MAX	UNIT
Supply voltage	$V_{CC}1$, $V_{CC}2$	–0.3	6.5	V
	V_{DD}	–0.3	4	V
Supply voltage differences	$V_{CC}1$, $V_{CC}2$	–0.1	0.1	V
Ground voltage differences	AGND1, AGND2, DGND	–0.1		V
Input voltage to digital pins	ZR1/ZR1/FMT0, ZR2, MSEL	–0.3	V_{DD} + 0.3, < 4	V
	$\overline{MS}$/ADR/FMT1, MC/SCL/DEMP, MD/SDA/MUTE, SCK, BCK, LRCK, DATA1, 2, 3, 4	–0.3	6.5	V
Input voltage to analog pins		–0.3	V_{CC} + 0.3, < 6.5	V
Input current any pins except supplies		–10	10	mA
Ambient temperature under bias		–40	125	°C
Junction temperature , T_J			150	°C
Package temperature (IR reflow, peak)			260	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings: PCM1681

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 ESD Ratings: PCM1681-Q1

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

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7.4 Recommended Operating Conditions

Over operating free-air temperature range.

		MIN	NOM	MAX	UNIT
Analog supply voltage, $V_{CC}1$, $V_{CC}2$		4.5	5	5.5	V
Digital supply voltage, V_{DD}		3	3.3	3.6	V
Digital input logic family			TTL		
Digital input clock frequency	System clock	1.024		36.864	MHz
	Sampling clock	8		192	kHz
Analog output load resistance		5			kΩ
Analog output load capacitance				50	pF
Digital output load capacitance				20	pF
Operating free-air temperature, T_A	PCM1681	–40		85	°C
	PCM1681-Q1	–40		105	°C

7.5 Thermal Information

THERMAL METRIC(1)		PCM1681, PCM1681-Q1 PWP (HTSSOP) 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	14.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	12.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	12.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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7.6 Electrical Characteristics

All specifications at V_{CC} = 5.0 V, V_{DD} = 3.3 V, f_S = 48 kHz, system clock = 512 f_S, and 24-bit data, narrow o/s mode, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RESOLUTION				24		bits
DATA FORMAT						
	Audio data interface format			Right-justified, I²S, left-justified, TDM		
	Audio data bit length			16-, 18-, 20-, or 24-bits, selectable		
	Audio data format			MSB-first, 2s complement		
f_S	Sampling frequency		5		200	kHz
	System clock frequency			128, 192, 256, 384, 512, 768, 1152 f_S		
DIGITAL INPUT/OUTPUT						
	Logic family			TTL compatible		
V_{IH} (1)	Input logic level		2.0		V_{DD}	V_{DC}
V_{IL} (1)					0.8	
V_{IH} (2)			2.0		5.5	
V_{IL} (2)					0.8	
I_{IH} (1) (2)	Input logic current	$V_{IN} = V_{DD}$			10	µA
I_{IL} (1) (2)		V_{IN} = 0 V			–10	
V_{OH} (3)	Output logic level	I_{OH} = –1 mA	2.4			V_{DC}
V_{OL} (3) (4)		I_{OL} = 1 mA			0.4	
DYNAMIC PERFORMANCE (5)						
THD+N	Total harmonic distortion + noise	V_{OUT} = 0 dB, f_S = 48 kHz		0.002%	0.008%	
		V_{OUT} = 0 dB, f_S = 96 kHz, system clock = 256 f_S		0.002%		
		V_{OUT} = 0 dB, f_S = 192 kHz, system clock = 128 f_S		0.002%		
	Dynamic range	EIAJ, A-weighted, f_S = 48 kHz	100	105		dB
		A-weighted, f_S = 96 kHz, system clock = 256 f_S		105		
		A-weighted, f_S = 192 kHz, system clock = 128 f_S		105		
SNR	Signal-to-noise ratio	EIAJ, A-weighted, f_S = 48 kHz	100	105		dB
		A-weighted, f_S = 96 kHz, system clock = 256 f_S		105		
		A-weighted, f_S = 192 kHz, system clock = 128 f_S		105		
	Channel separation	f_S = 48 kHz	94	102		dB
		f_S = 96 kHz, system clock = 256 f_S		102		
		f_S = 192 kHz, system clock = 128 f_S		102		
DC ACCURACY						
	Gain error			±2.0	±6	% of FSR
	Gain mismatch, channel-to-channel			±2.0	±6	% of FSR
	Bipolar zero error	V_{OUT} = 0.486 V_{CC} at BPZ input		±30	±80	mV

(1) Pins 1, 14: ZR1/ZR1/FMT0 (input mode), MSEL
(2) Pins 2, 3, 4, 5, 6, 7, 8, 11, 12, 13: MS/ADR/FMT1, MC/SCL/DEMP, MD/SDA/MUTE (input mode), SCK, DATA1, BCK, LRCK, DATA2, DATA3, DATA4
(3) Pins 1, 28: ZR1/ZR1/FMT0 (output mode), ZR2
(4) Pin 4: MD/SDA/MUTE (output mode)
(5) Analog performance characteristics are measured using the System Two™ Cascade audio measurement system by Audio Precision™, f_{IN} = 1 kHz, average mode, with 20-kHz LPF and 400-Hz HPF.

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Electrical Characteristics (continued)

All specifications at V_{CC} = 5.0 V, V_{DD} = 3.3 V, f_S = 48 kHz, system clock = 512 f_S, and 24-bit data, narrow o/s mode, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG OUTPUT						
	Output voltage	Full-scale (–0 dB)		0.75 V_{CC}		V_{PP}
	Bipolar zero voltage			0.486 V_{CC}		V_{DC}
	Load impedance	AC-coupled load	5			kΩ
DIGITAL FILTER PERFORMANCE						
Filter Characteristics (Sharp Roll-Off)						
	Passband	±0.015 dB			0.454 f_S	
	Stop band		0.546 f_S			
	Passband ripple				±0.015	dB
	Stop band attenuation	Stop band = 0.546 f_S	–57			dB
Filter Characteristics (Slow Roll-Off)						
	Passband	±0.004 dB			0.261 f_S	
	Stop band		0.727 f_S			
	Passband ripple				±0.004	dB
	Stop band attenuation	Stop band = 0.727 f_S	–56			dB
Filter Characteristics						
	Delay time			24/f_S		
	De-emphasis error			±0.1		dB
ANALOG FILTER PERFORMANCE						
	Frequency response	at 20 kHz		–0.02		dB
		at 44 kHz		–0.07		
POWER-SUPPLY REQUIREMENTS						
V_{DD}	Voltage range		3	3.3	3.6	V_{DC}
V_{CC}			4.5	5.0	5.5	
I_{DD}	Supply current	f_S = 48 kHz		13	20	mA
		f_S = 96 kHz, system clock = 256 f_S		18		
		f_S = 192 kHz, system clock = 128 f_S		23		
I_{CC}	Supply current	f_S = 48 kHz		62	80	mA
		f_S = 96 kHz, system clock = 256 f_S		62		
		f_S = 192 kHz, system clock = 128 f_S		62		
	Power dissipation	f_S = 48 kHz		353	466	mW
		f_S = 96 kHz, system clock = 256 f_S		369		
		f_S = 192 kHz, system clock = 128 f_S		386		
TEMPERATURE RANGE						
	Operating temperature	PCM1681	–40		85	°C
		PCM1681-Q1	–40		105	°C
θ_{JA}	Thermal resistance	28-pin TSSOP PowerPAD™		28		°C/W

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7.7 Interface Timing Requirements

PARAMETER		MIN	MAX	UNIT
$f_{(SCL)}$	SCL clock frequency		100	kHz
$t_{(BUF)}$	Bus free time between a STOP and START condition	4.7		µs
$t_{(LOW)}$	Low period of the SCL clock	4.7		µs
$t_{(HI)}$	High period of the SCL clock	4		µs
$t_{(RS-SU)}$	Setup time for (repeated) START condition	4.7		µs
$t_{(S-HD)}$ $t_{(RS-HD)}$	Hold time for (repeated) START condition	4		µs
$t_{(D-SU)}$	Data setup time	250		ns
$t_{(D-HD)}$	Data hold time	0	900	ns
$t_{(SCL-R)}$	Rise time of SCL signal	20 + 0.1 C_B	1000	ns
$t_{(SCL-R1)}$	Rise time of SCL signal after a repeated START condition and after an acknowledge bit	20 + 0.1 C_B	1000	ns
$t_{(SCL-F)}$	Fall time of SCL signal	20 + 0.1 C_B	1000	ns
$t_{(SDA-R)}$	Rise time of SDA signal	20 + 0.1 C_B	1000	ns
$t_{(SDA-F)}$	Fall time of SDA signal	20 + 0.1 C_B	1000	ns
$t_{(P-SU)}$	Setup time for STOP condition	4		µs
C_B	Capacitive load for SDA and SCL lines		400	pF
V_{NH}	Noise margin at high level for each connected device (including hysteresis)	0.2 V_{DD}		V

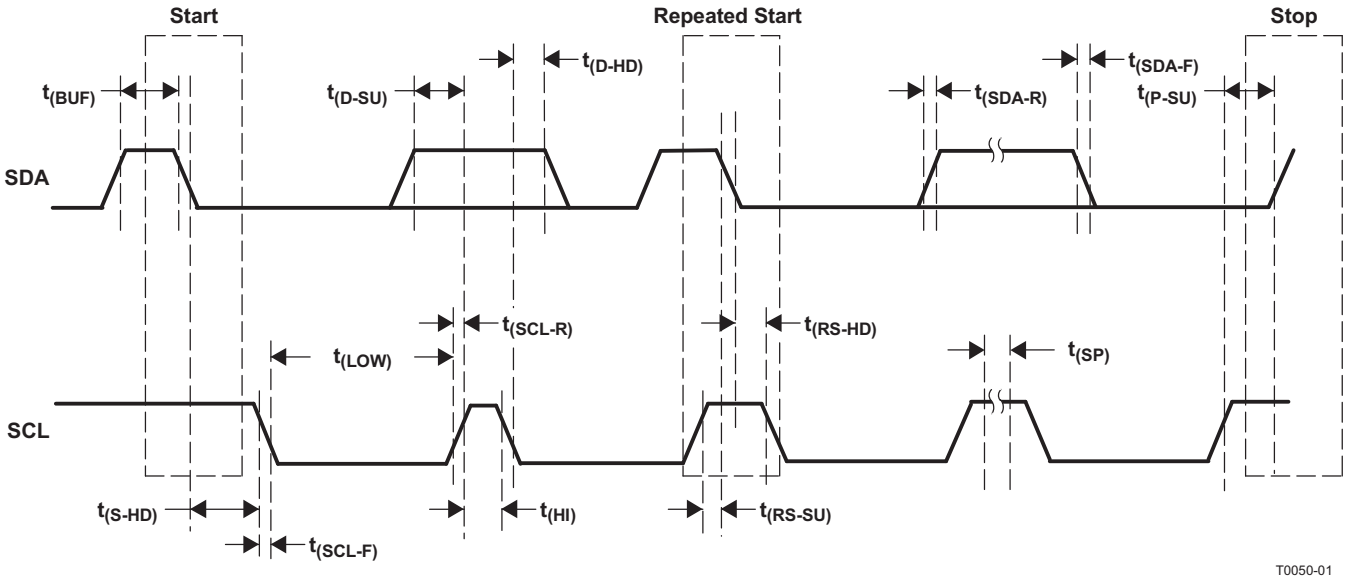


Figure 1. Interface Timing

7.8 Typical Characteristics

All specifications at T_A = +25°C, V_{CC} = 5 V, V_{DD} = 3.3 V, f_S = 48 kHz, system clock = 512 f_S, and 24-bit data, unless otherwise noted.

7.8.1 Digital Filter (De-Emphasis Off)

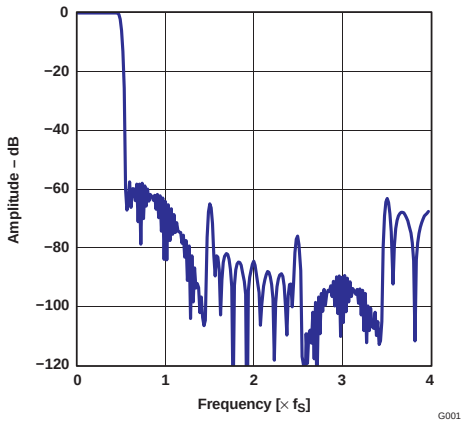


Figure 2. Frequency Response (Sharp Roll-off)

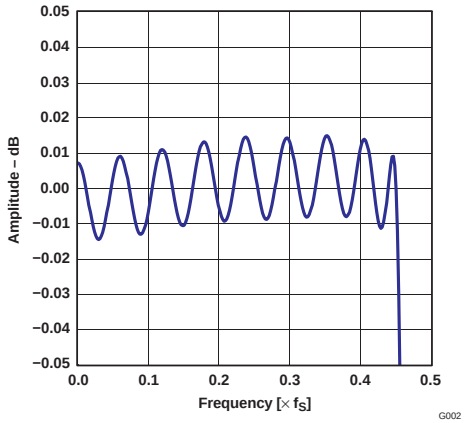


Figure 3. Passband Frequency Response (Sharp Roll-off)

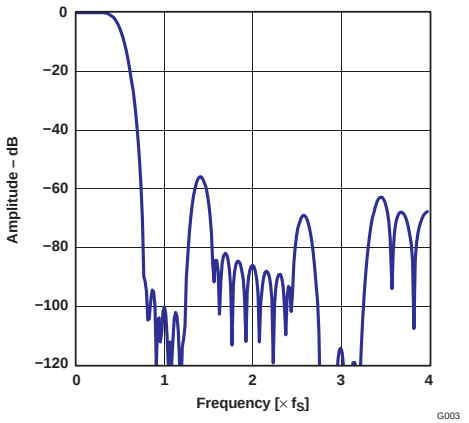


Figure 4. Frequency Response (Slow Roll-off)

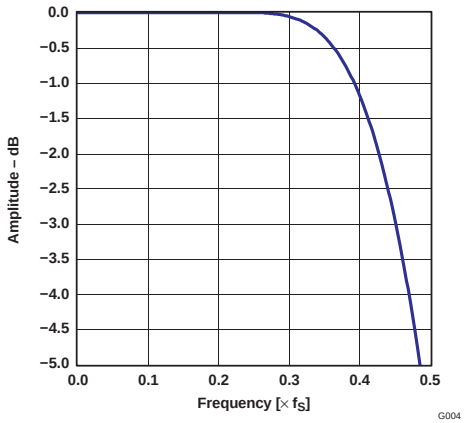


Figure 5. Transition Characteristics (Slow Roll-off)

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7.8.2 De-Emphasis Filter

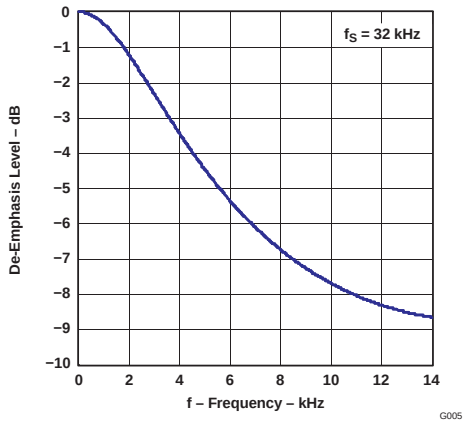


Figure 6. De-Emphasis

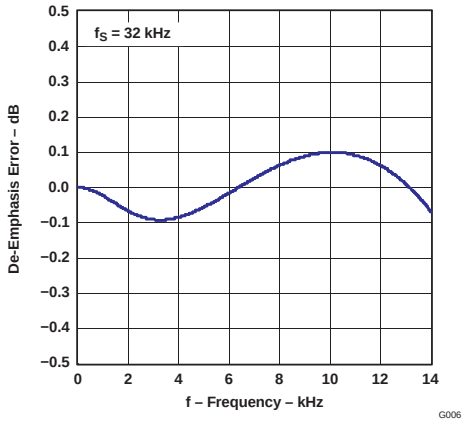


Figure 7. De-Emphasis Error

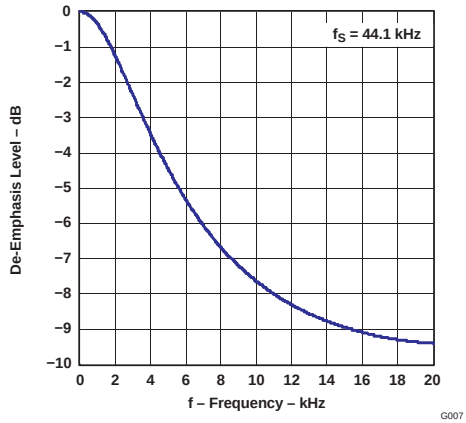


Figure 8. De-Emphasis

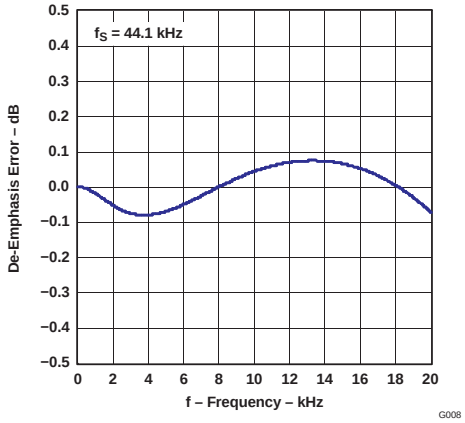


Figure 9. De-Emphasis Error

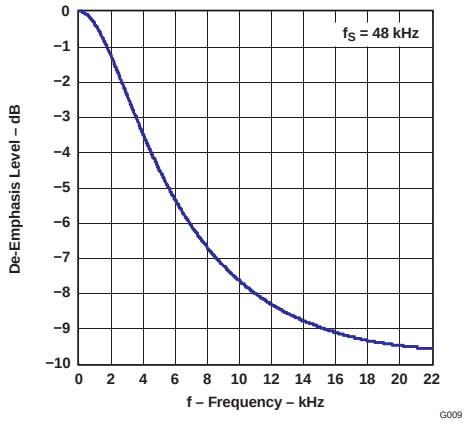


Figure 10. De-Emphasis

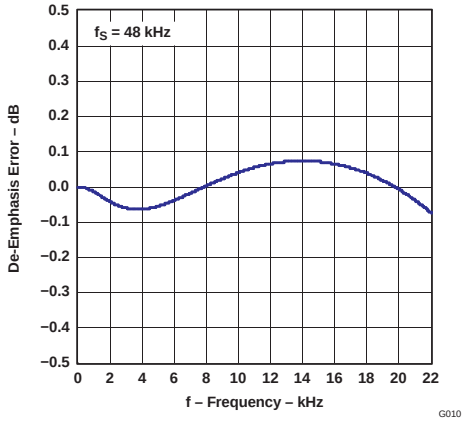


Figure 11. De-Emphasis Error

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7.8.3 Analog Filter

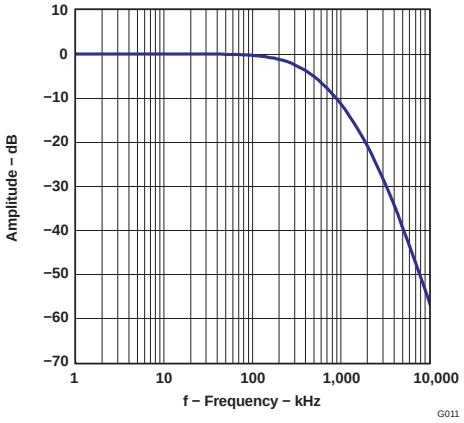


Figure 12. Analog Filter Performance

7.8.4 Analog Dynamic Performance

7.8.4.1 Supply Voltage Characteristics

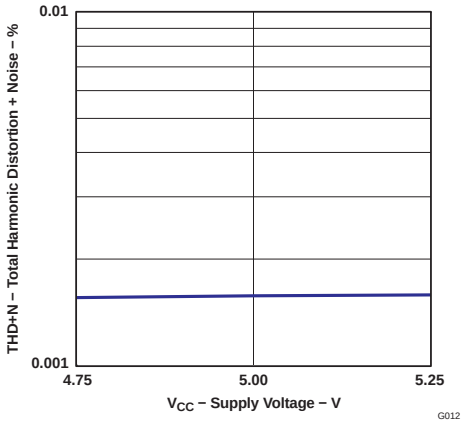


Figure 13. Total Harmonic Distortion + Noise vs Supply Voltage

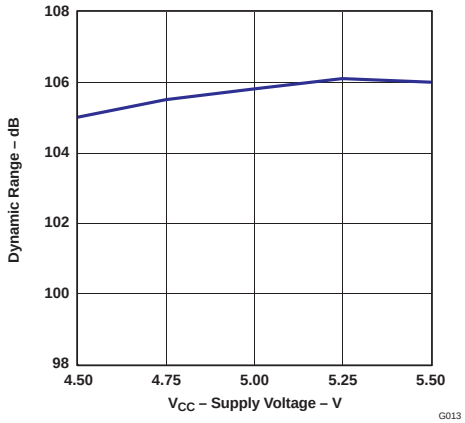


Figure 14. Dynamic Range vs Supply Voltage

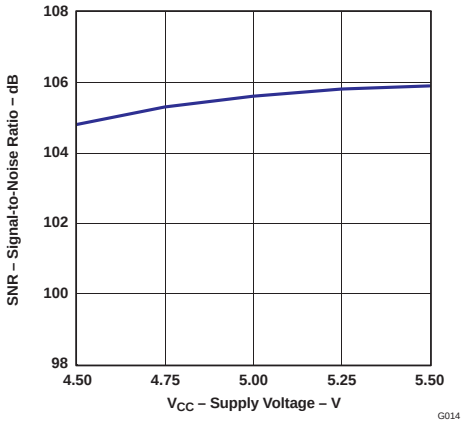


Figure 15. Signal-to-Noise Ratio vs Supply Voltage

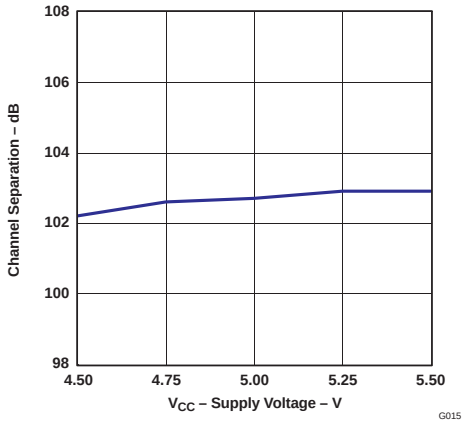


Figure 16. Channel Separation vs Supply Voltage

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Analog Dynamic Performance (continued)

7.8.4.2 Temperature Characteristics

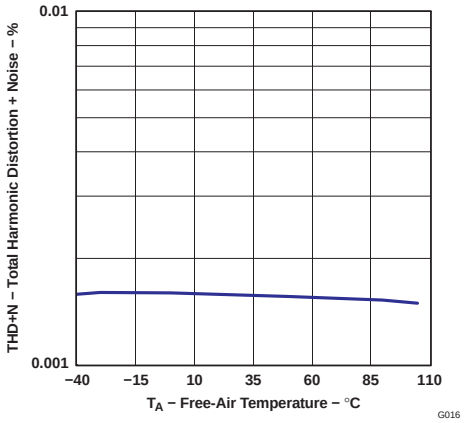


Figure 17. Total Harmonic Distortion + Noise vs Temperature

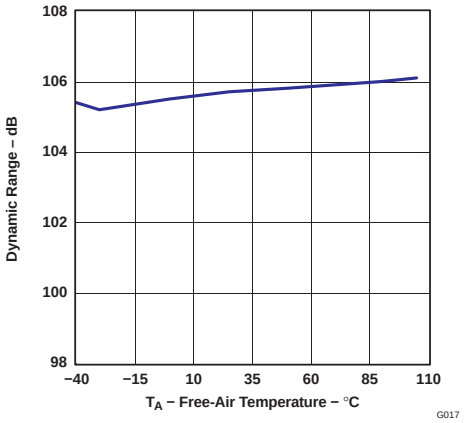


Figure 18. Dynamic Range vs Temperature

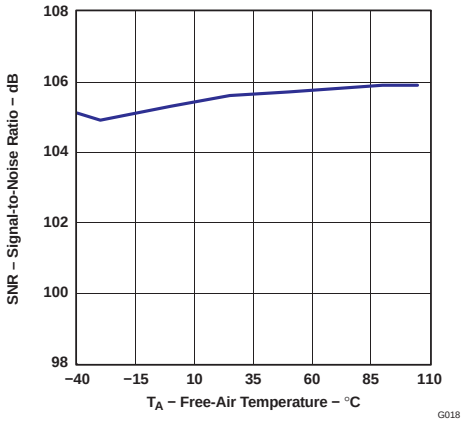


Figure 19. Signal-to-Noise Ratio vs Temperature

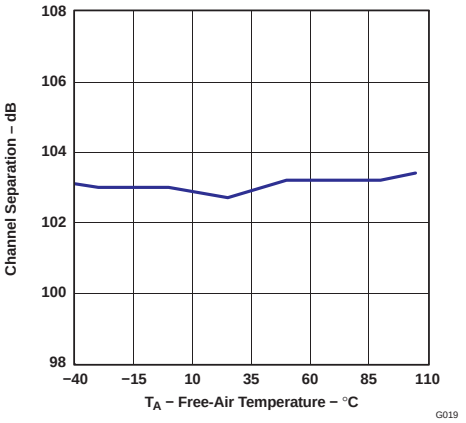


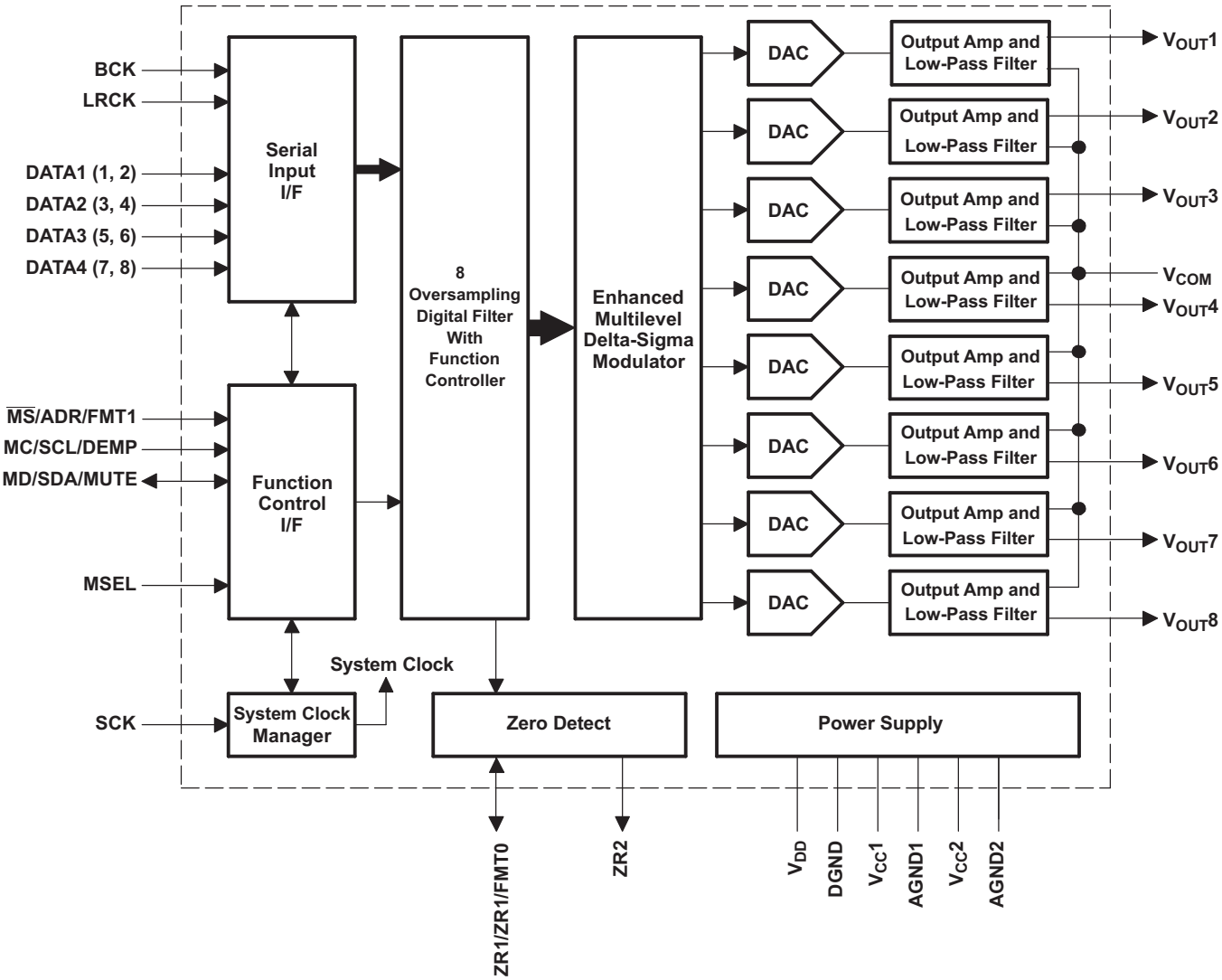
Figure 20. Channel Separation vs Temperature

8 Detailed Description

8.1 Overview

The PCM1681 and PCM1681-Q1 are CMOS monolithic integrated circuits which feature an eight-channel 24-bit audio digital-to-analog converter (DAC) and support circuitry in small 28-lead TSSOP PowerPAD packages. The DACs utilize a Burr-Brown enhanced multilevel delta-sigma (ΔΣ) architecture to achieve excellent signal-to-noise performance and a high tolerance to clock jitter. The system clock can operate anywhere from 128 fs to 1152 fs and with respect to the system clock rate the DAC can oversample anywhere from ×16 to ×128. The PCM1681 and PCM1681-Q1 accept TDM (time-division multiplexed) format in addition to industry-standard audio data formats with 16- to 24-bit audio data width. This includes right justified, I^2S, left justified, and DSP formats along with sampling rates up to 200 kHz. The PCM1681 and PCM1681-Q1 provide a sub-set of user-programmable functions through a parallel control port, in addition to a full set of user-programmable functions through a serial control port, SPI, or I^2C. This is controlled through the MSEL pin as explained in Table 7. A 5-V analog supply and a 3.3-V digital supply are required. The PCM1681 supports –40°C to 85°C for consumer grade applications and the PCM1681-Q1 supports –40°C to 105°C for automotive audio grade systems.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 System Clock Input

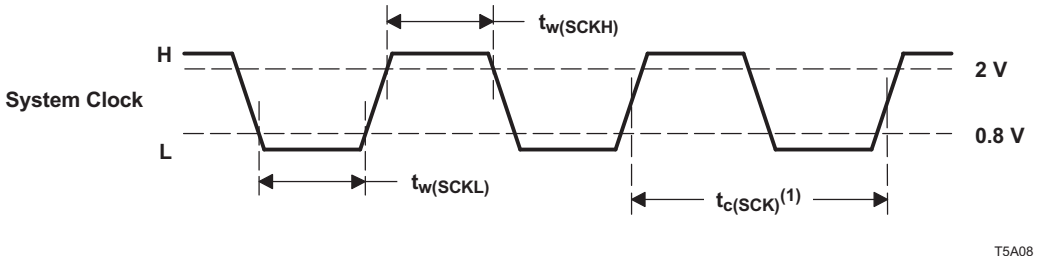
The PCM1681 and PCM1681-Q1 require a system clock for operating the digital interpolation filters and multilevel ΔΣ modulators. The system clock is applied at the SCK input (pin 5). Table 1 shows examples of system clock frequencies for common audio sampling rates.

Figure 21 shows the timing requirements for the system clock input. For optimal performance, it is important to use a clock source with low phase jitter and noise. A Texas Instruments PLL170x multi-clock generator is an excellent choice for providing the PCM1681 and PCM1681-Q1 system clock source.

Table 1. System Clock Frequencies for Common Audio Sampling Frequencies

SAMPLING FREQUENCY	SYSTEM CLOCK FREQUENCY (f_{SCK}), MHz						
	128 f_S	192 f_S	256 f_S	384 f_S	512 f_S	768 f_S	1152 f_S
8 kHz	1.024	1.536	2.048	3.072	4.096	6.144	9.216
16 kHz	2.048	3.072	4.096	6.144	8.192	12.288	18.432
32 kHz	4.096	6.144	8.192	12.288	16.384	24.576	36.864
44.1 kHz	5.6448	8.4672	11.2896	16.9344	22.5792	33.8688	—(1)
48 kHz	6.144	9.216	12.288	18.432	24.576	36.864	—(1)
88.2 kHz	11.2896	16.9344	22.5792	33.8688	—(1)	—(1)	—(1)
96 kHz	12.288	18.432	24.576	36.864	—(1)	—(1)	—(1)
192 kHz	24.576	36.864	—(1)	—(1)	—(1)	—(1)	—(1)

(1) This system clock frequency is not supported for the given sampling frequency.



(1) System clock pulse cycle time; 1/128 f_S, 1/192 f_S, 1/256 f_S, 1/384 f_S, 1/512 f_S, 1/768 f_S, or 1/1152 f_S

Figure 21. System Clock Timing Diagram

Table 2. System Clock Timing

PARAMETER		MIN	MAX	UNIT
$t_{c(SCK)}$	System clock cycle time	25		ns
$t_{w(SCKH)}$	System clock pulse duration, HIGH	10		ns
$t_{w(SCKL)}$	System clock pulse duration, LOW	10		ns
	System clock duty cycle	40%	60%	

8.3.2 Power-on-Reset Function

The PCM1681 and PCM1681-Q1 include a power-on-reset function. Figure 22 shows the operation of this function. With the system clock active and V_{DD} > 2.2 V (typical, 1.4 V to 2.9 V), the power-on-reset function is enabled. The initialization sequence requires 65,536 system clocks from the time V_{DD} > 2.2 V. V_{DD} must rise up with a ramp-up rate greater than 1V/ms to ensure reliable initialization. After the initialization period, the PCM1681 and PCM1681-Q1 are set to the respective reset default state, as described in the *Mode Control Registers* section of this data sheet.

During the reset period (65,536 system clocks), the analog output is forced to the common voltage (V_{COM}), or $V_{CC}/2$. After the reset period, the internal register is initialized in the next $1/f_S$ period and if SCK, BCK, and LRCK are provided continuously, the PCM1681 and PCM1681-Q1 provide the proper analog output with group delay corresponding to the input data.

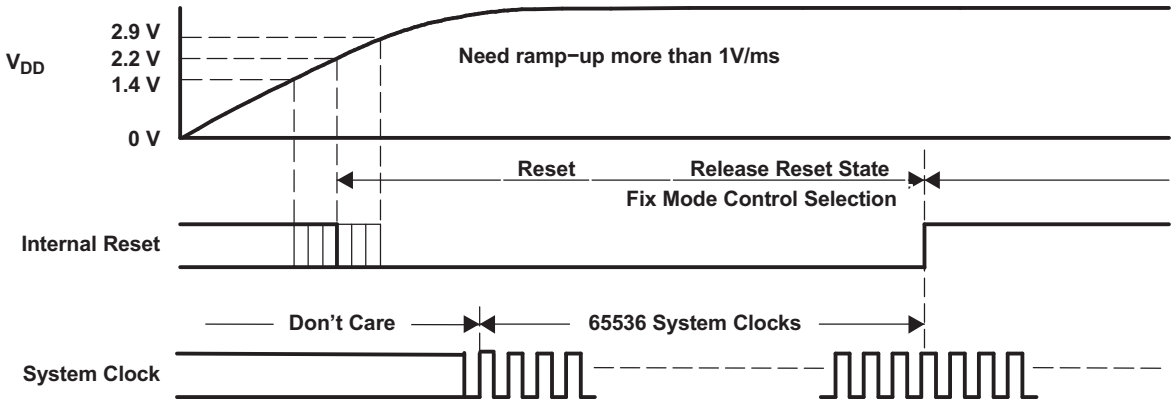


Figure 22. Power-On-Reset Timing

8.3.3 Audio Serial Interface

The audio serial interface for the PCM1681 and PCM1681-Q1 is comprised of a 6-wire synchronous serial port. It includes LRCK (pin 8), BCK (pin 7), and DATA1 (pin 6), DATA2 (pin 11), DATA3 (pin 12), and DATA4 (pin 13). BCK is the serial audio bit clock, and it is used to clock the serial data present on DATA1, DATA2, DATA3, and DATA4 into the audio interface serial shift register. Serial data are clocked into the PCM1681 and PCM1681-Q1 on the rising edge of BCK. LRCK is the serial audio left/right word clock. It is used to latch serial data into the serial audio interface internal registers.

Both LRCK and BCK must be synchronous with the system clock, SCK. Ideally, it is recommended that LRCK and BCK are derived from SCK. LRCK is operated at the sampling frequency, f_S. BCK can be operated at 32, 48, or 64 times the sampling frequency for the PCM formats and times at 128 and 256 the sampling frequency for the TDM formats.

Internal operation of the PCM1681 and PCM1681-Q1 is synchronized with LRCK. Accordingly, internal operation is suspended when LRCK is changed or when SCK and/or BCK is interrupted for at least 3-bit clock cycles. If SCK, BCK, and LRCK are provided continuously after this held condition, the internal operation is resynchronized automatically within the following $3/f_S$ period. External resetting is not required.

8.3.4 Audio Data Formats and Timing

The PCM1681 and PCM1681-Q1 support industry-standard audio data formats, including right-justified, I^2S, left-justified, and DSP. The PCM1681 and PCM1681-Q1 also support a time-division-multiplexed (TDM) format. The TDM format is supported only at system clocks of 128 f_S, 256 f_S, and 512 f_S. The data formats are shown in Figure 23 and Figure 24. Data formats are selected using the format bits, FMT[3:0], located in control register 9 of the PCM1681 and PCM1681-Q1. The default data format is 16- to 24-bit left-justified. All formats require binary 2s complement, MSB-first audio data. Figure 25 shows a detailed timing diagram for the serial audio interface.

DATA1, DATA2, DATA3, and DATA4 each carry two audio channels, designated as the left and right channels in the right-justified, I^2S, left-justified, and DSP formats. The left-channel data always precedes the right-channel data in the serial data stream for all data formats. Table 3 shows the mapping of the digital input data to the analog output pins. DATA1 carries eight audio channels in 256 f_S mode TDM fornat, and DATA1 and DATA2 each carry four audio channels in 128 f_S mode TDM format.

Table 3. Audio Input Data to Analog Output Mapping

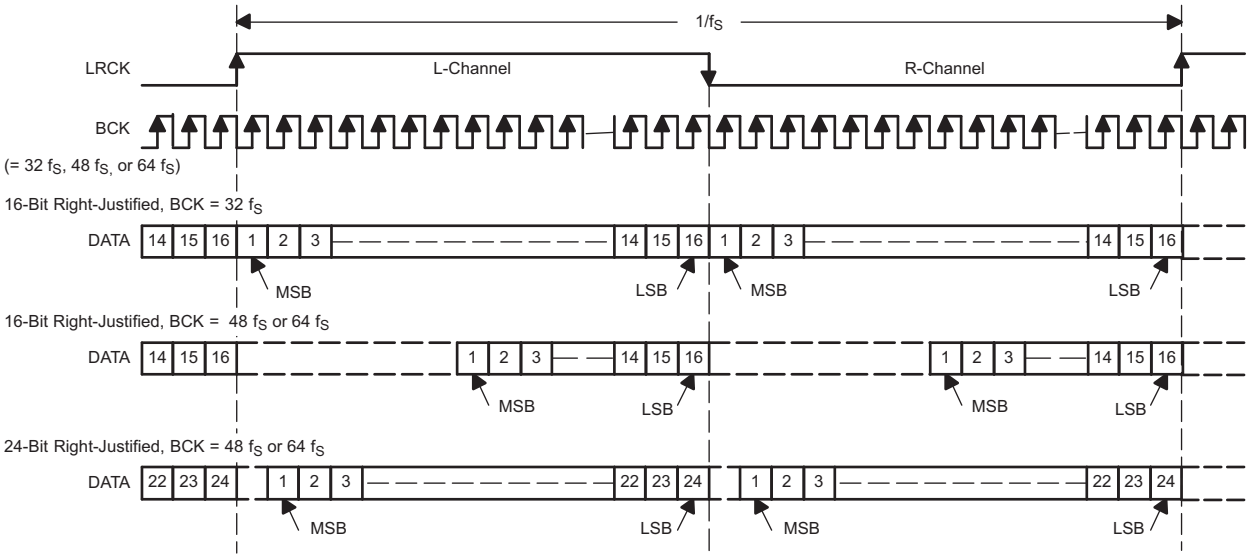
DATA INPUT	CHANNEL	ANALOG OUTPUT
DATA1	Left	$V_{OUT}1$
	Right	$V_{OUT}2$

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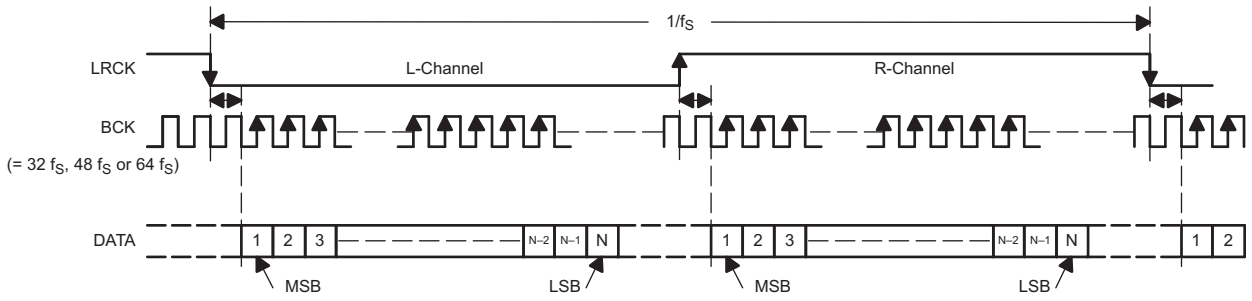
Table 3. Audio Input Data to Analog Output Mapping (continued)

DATA INPUT	CHANNEL	ANALOG OUTPUT
DATA2	Left	$V_{OUT}3$
	Right	$V_{OUT}4$
DATA3	Left	$V_{OUT}5$
	Right	$V_{OUT}6$
DATA4	Left	$V_{OUT}7$
	Right	$V_{OUT}8$

(1) Right-Justified Data Format; L-Channel = HIGH, R-Channel = LOW



(2) I²S Data Format; L-Channel = LOW, R-Channel = HIGH



(3) Left-Justified Data Format; L-Channel = HIGH, R-Channel = LOW (default)

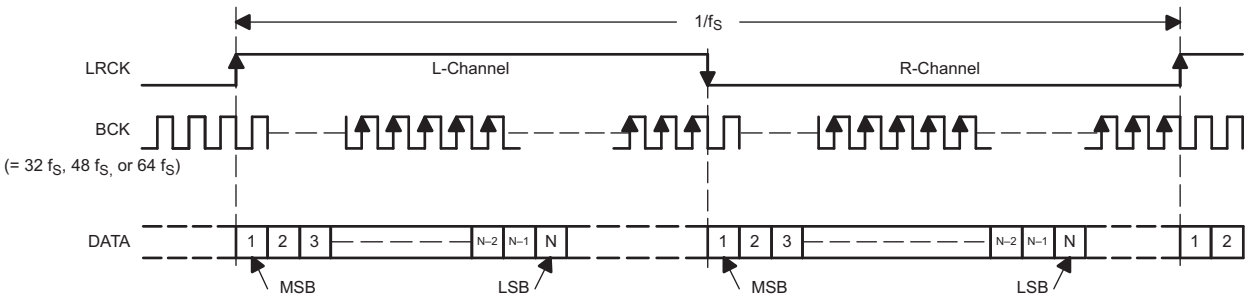
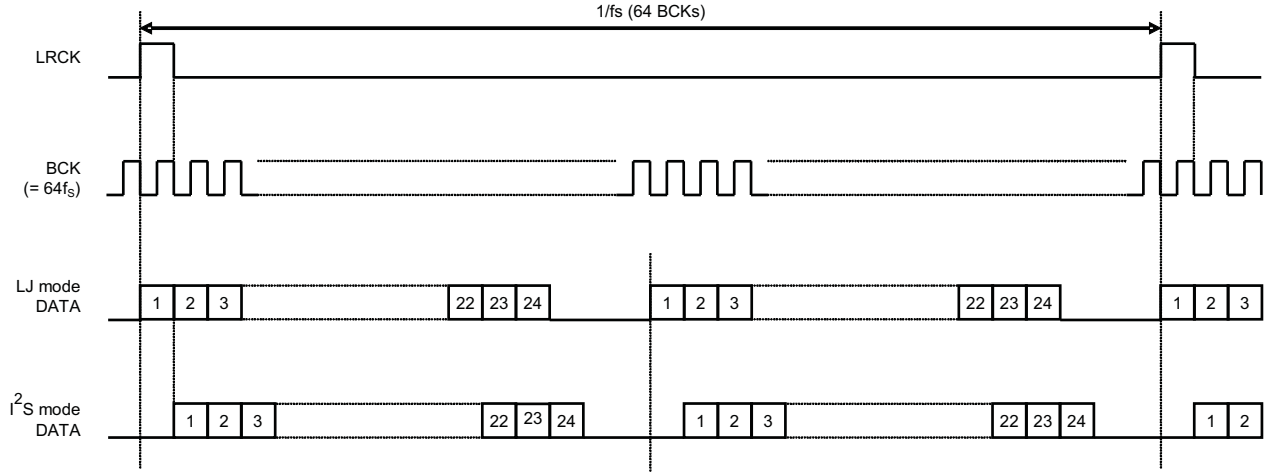
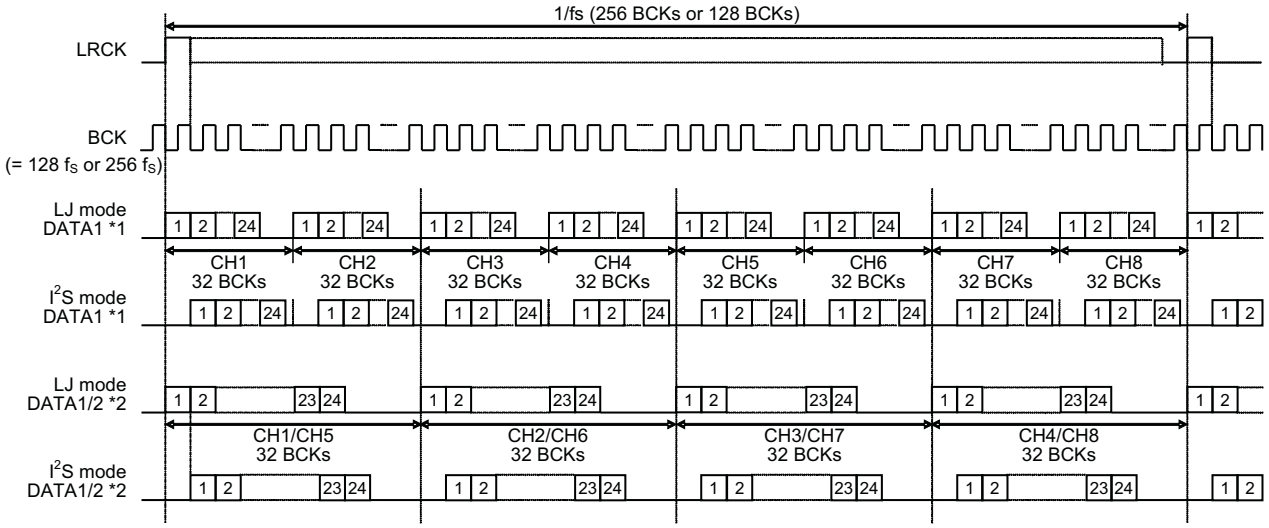


Figure 23. Audio Data Input Formats

(4) 24-Bit DSP Format



(5) 24-Bit TDM Format



*1: BCK = 256 f_S mode
*2: BCK = 128 f_S mode

Figure 24. Audio Data Input Formats

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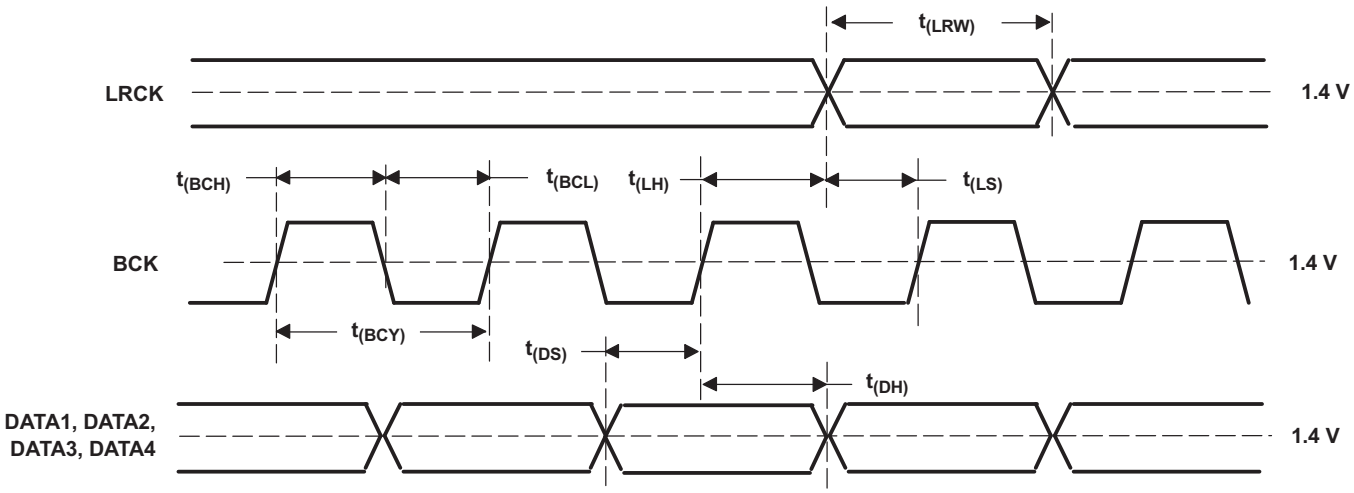


Figure 25. Audio Interface Timing Diagram

Table 4. Audio Interface Timing

PARAMETER		MIN	MAX	UNIT
$t_{(BCY)}$	BCK cycle time	75(1)		ns
$t_{(BCH)}$	BCK pulse duration HIGH	35		ns
$t_{(BCL)}$	BCK pulse duration LOW	35		ns
$t_{(LRW)}$	LRCK pulse duration HIGH, right-justified, I^2S, left-justified	1/2 f_S	1/2 f_S	
	LRCK pulse duration HIGH, DSP format	$t_{(BCY)}$	$t_{(BCY)}$	
	LRCK pulse duration HIGH, TDM format	$t_{(BCY)}$	$1/f_S - t_{(BCY)}$	
$t_{(LS)}$	LRCK setup time to BCK rising edge	10		ns
$t_{(LH)}$	LRCK hold time to BCK rising edge	10		ns
$t_{(DS)}$	DATA1, DATA2, DATA3, DATA4 setup time to BCK rising edge	10		ns
$t_{(DH)}$	DATA1, DATA2, DATA3, DATA4 hold time to BCK rising edge	10		ns

(1) For right-justified, I^2S, left-justified, and DSP formats, there is no f_S (sampling frequency) limitation for all of 1/32 f_S, 1/48 f_S, or 1/64 f_S. However, for TDM format, allowable f_S is limited to $f_S \leq 50$ kHz for BCK = 256 f_S mode and $f_S \leq 100$ kHz for BCK = 128 f_S mode.

8.3.5 De-Emphasis Filter

The PCM1681 and PCM1681-Q1 include a digital de-emphasis filter for 32 kHz, 44.1 kHz, and 48 kHz sampling frequencies.

8.3.6 Oversampling Rate Control

The PCM1681 and PCM1681-Q1 automatically control the oversampling rate of the ΔΣ DACs according to system clock frequency and oversampling mode. Oversampling mode, narrow or wide, can be selected by the MSEL pin in H/W control mode and the OVER bit of control register 12 in S/W control mode. The oversampling rate is set to 64× oversampling with a 1152 f_S, 768 f_S, 512 f_S system clock, 32× oversampling with a 384 f_S, 256 f_S system clock, and 16× oversampling with a 192 f_S, 128 f_S system clock in default, narrow mode, and 128× oversampling with a 1152 f_S, 768 f_S, 512 f_S system clock, 64× oversampling with a 384 f_S, 256 f_S system clock, and 32× oversampling with a 192 f_S, 128 f_S system clock in wide mode. Wide mode is recommended for $f_S \leq 96$ kHz at SCK = 128 f_S or 192 f_S, $f_S \leq 48$ kHz at SCK = 256 f_S or 384 f_S, and $f_S \leq 24$ kHz at SCK = 512 f_S, 768 f_S, or 1152 f_S.

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Table 5. Oversampling Rate Control

OVERSAMPLING MODE	OVERSAMPLING RATE		
	SCK = 128 f_S or 192 f_S	SCK = 256 f_S or 384 f_S	SCK = 512 f_S, 768 f_S, or 1152 f_S
Narrow mode	16×	32×	64×
Wide mode	32×	64×	128×

8.3.7 Zero Flag

The PCM1681 and PCM1681-Q1 have two zero-flag pins, ZR1 (pin 1) and ZR2 (pin 28), which are assigned to the combinations A through D as shown in Table 6. Zero-flag combinations are selected using the zero-flag combination bits, AZRO[1:0], located in control register 13 of the PCM1681 and PCM1681-Q1. If the input data of the L-channel and/or R-channel of all assigned channels remains at a logic-0 level for 1024 sampling periods (LRCK clock periods), ZR1 and ZR2 are set to logic-1 states, or high level. If the input data of any of the assigned channels contains a logic-1 level, ZR1 and ZR2 are set to logic-0 states or low level immediately.

The active polarity of a zero-flag output can be inverted by setting the ZREV bit of control register 10 to 1. The reset default is ZREV = 0, active-high for zero detection.

In parallel hardware control mode, ZR1 is not applicable due to the reassignment of ZR1 as the FMT0 control pin, and the zero-flag output combination is fixed as all 8 channel (DATA1-DATA4) data zero on the ZR2 pin.

Table 6. Zero-Flag Output Combinations

ZERO-FLAG COMBINATION	ZR1/ZR1/FMT0 (PIN 1)	ZR2 (PIN 28)
A	DATA1 L-ch	DATA1 R-ch
B	DATA1-4	DATA1-4
C	DATA4	DATA1-3
D	DATA1	DATA2-4

8.3.8 Mode Control

The PCM1681 and PCM1681-Q1 support three types of interface mode control with three types of oversampling configuration, according to the input state of MSEL (pin 14) as listed in Table 7. The required values of the pull-up and pull-down resistors are 220 kΩ ± 5%.

Table 7. Interface Mode Control

MSEL	INTERFACE MODE CONTROL
Tied with DGND	2-Wire (I^2C) serial control, selectable oversampling configuration
Pull-down resistor to DGND	4-Wire parallel H/W control, narrow mode oversampling configuration
Pull-up resistor to V_{DD}	4-Wire parallel H/W control, wide mode oversampling configuration
Tied with V_{DD}	3-Wire (SPI) serial control, selectable oversampling configuration

The input state of the MSEL pin is sampled at power-on with the system clock input; therefore, an input change after a reset is ignored until the next power-on. The assignments of the four pins are controlled by the interface mode control setting as listed in Table 8.

Table 8. Interface Mode Control Pin Assignments

PIN	DEFINITION (Assignment)		
	I^2C	SPI	PARALLEL H/W
4	SDA (input/output)	MD (input)	MUTE (input)
3	SCL (input)	MC (input)	DEMP (input)
2	ADR (input)	$\overline{MS}$ (input)	FMT1 (input)
1	ZR1 (output)	ZR1 (output)	FMT0 (input)

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In serial control mode, actual mode control is performed by a register write (and read) through the I^2C or SPI compatible serial control port. In parallel H/W control mode, the specific four functions are controlled directly through high-level/low-level control of five specific pins (see *Parallel Hardware Control* section), and the zero-flag function of ZR1 is not applicable.

8.3.8.1 Parallel Hardware Control

Four functions are controlled by five pins, MSEL, FMT0, FMT1, DEMP, and MUTE in parallel hardware control mode.

MSEL TERMINATION(1)	DESCRIPTION
Pull-down resistor to DGND	Narrow oversampling mode
Pull-up resistor to V_{DD}	Wide oversampling mode

(1) The MSEL termination controls the oversampling mode for all eight channels.

FMT1(1)	FMT0(1)	DESCRIPTION
LOW	LOW	24-bits right-justified format
LOW	HIGH	16 to 24-bits I^2S format
HIGH	LOW	16 to 24-bits left-justified format
HIGH	HIGH	24-bits I^2S mode TDM format

(1) The FMT0 and FMT1 pins control the audio interface format for all eight channels.

DEMP(1)	DESCRIPTION
LOW	De-emphasis off
HIGH	44.1-kHz De-emphasis on

(1) The DEMP pin controls the 44.1-kHz digital de-emphasis function of all eight channels.

MUTE(1)	DESCRIPTION
LOW	Mute off (mute disable)
HIGH	Mute on (mute enable)

(1) The MUTE pin controls all 8 channel outputs at the same time.

8.3.8.2 SPI Control Interface

The SPI control interface of the PCM1681 and PCM1681-Q1 is a 3-wire synchronous serial port that operates asynchronously to the serial audio interface. The SPI control interface is used to program the on-chip mode registers. The control interface includes MD (pin 4), MC (pin 3), and $\overline{MS}$ (pin 2). MD is the serial data input, used to program the mode registers. MC is the control port for the serial bit clock, used to shift in the serial data, and $\overline{MS}$ is the control port for mode control select, which is used to enable the mode control. The SPI control interface is available when MSEL (pin 14) is tied with V_{DD} and after power-on reset completion.

8.3.8.3 Analog Outputs

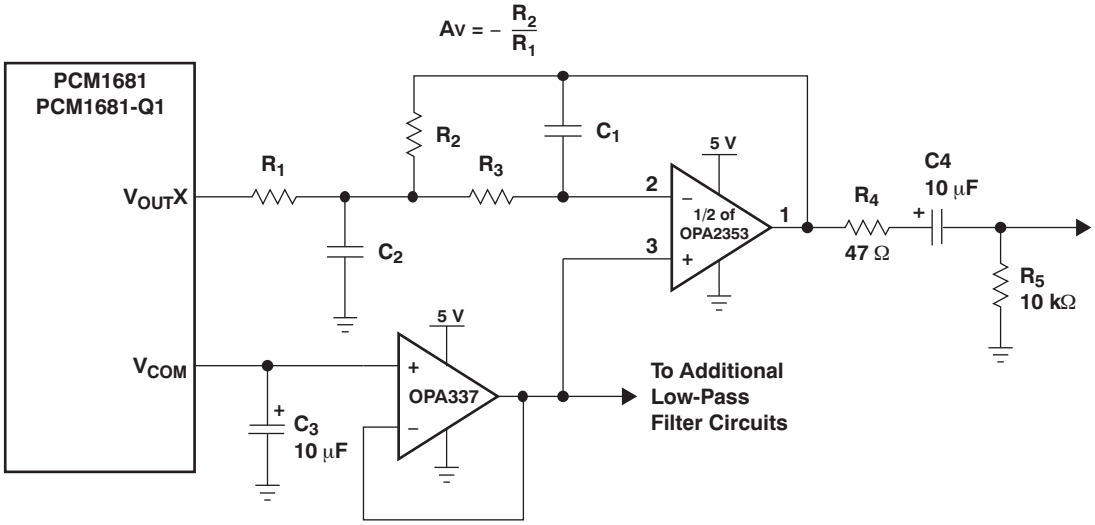
The PCM1681 and PCM1681-Q1 include eight independent output channels, $V_{OUT}1$ through $V_{OUT}8$. These are unbalanced outputs, each capable of driving 3.75 V_{PP} typical into a 5-kΩ ac load with V_{CC} = 5 V. The internal output amplifiers for $V_{OUT}1$ through $V_{OUT}8$ are biased to the dc common voltage, equal to 0.486 V_{CC}.

The output amplifiers include an RC continuous-time filter, which helps to reduce the out-of-band noise energy present at the DAC outputs due to the noise-shaping characteristics of the PCM1681 and PCM1681-Q1 ΔΣ DACs. The frequency response of this filter is shown in Figure 12. By itself, this filter is not enough to attenuate the out-of-band noise to an acceptable level for most applications. An external low-pass filter is required to provide sufficient out-of-band noise rejection. Further discussion of DAC post-filter circuits is provided in the *Application and Implementation* section of this data sheet.

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8.3.8.3.1 V_{COM} Output

One unbuffered common voltage output pin, V_{COM} (pin 25), is brought out for decoupling purposes. This pin is nominally biased to the dc common voltage, equal to $V_{CC}/2$. If this pin is to be used to bias external circuitry, a voltage follower is required for buffering purposes. Figure 26 shows an example of a 5-V single-supply filter circuit using the V_{COM} pin for external biasing applications.



Example:
R_1: 6.2 kΩ
R_2: 6.8 kΩ
R_3: 430 Ω
C_1: 470 pF
C_2: 4700 pF
A_V: –1.10 (1.45 Vrms Output)
f_C: 70 kHz

Figure 26. Single-Supply Filter Circuit Using V_{COM} for External Biasing Applications

8.3.8.4 Register Write Operation

All write operations for the serial control port use 16-bit data words. Figure 27 shows the control data word format. The most significant bit is a fixed 0 for the write operation. Seven bits, labeled IDX[6:0], set the register index (or address) for the write operation. The least significant eight bits, D[7:0], contain the data to be written to the register specified by IDX[6:0].

Figure 28 shows the functional timing diagram for writing to the serial control port. $\overline{MS}$ is held at a logic-1 state until a register needs to be written. To start the register write cycle, $\overline{MS}$ is set to logic-0. 16 clock cycles are then provided on MC, corresponding to the 16 bits of the control data word on MD. After completion of the 16th clock cycle, $\overline{MS}$ is set to logic-1 to latch the data into the indexed mode control register.

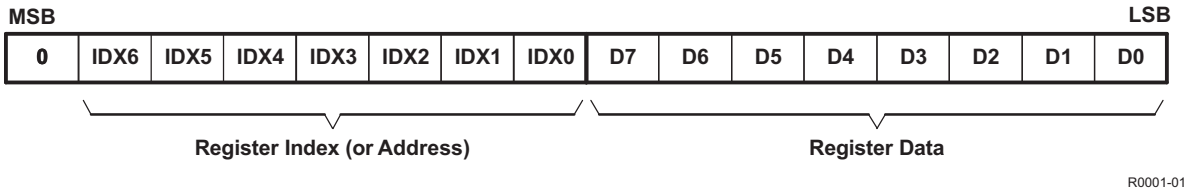


Figure 27. Control Data Word Format for MD

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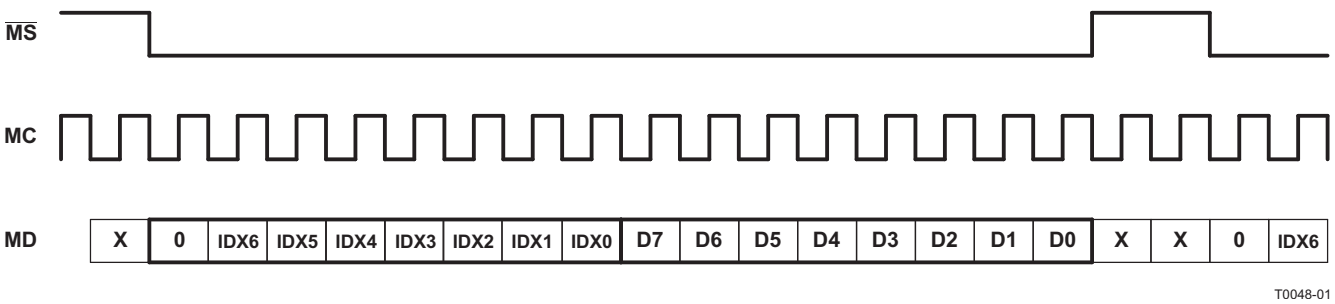


Figure 28. Write Operation Timing

8.3.8.5 Interface Timing Requirements

Figure 29 shows a detailed timing diagram for the serial control interface. Special attention to the setup and hold times is required. Also, $t_{(MSS)}$ and $t_{(MSH)}$, which define the minimum delays between the edges of the MS and MC clocks, require special attention. These timing parameters are critical for proper control port operation.

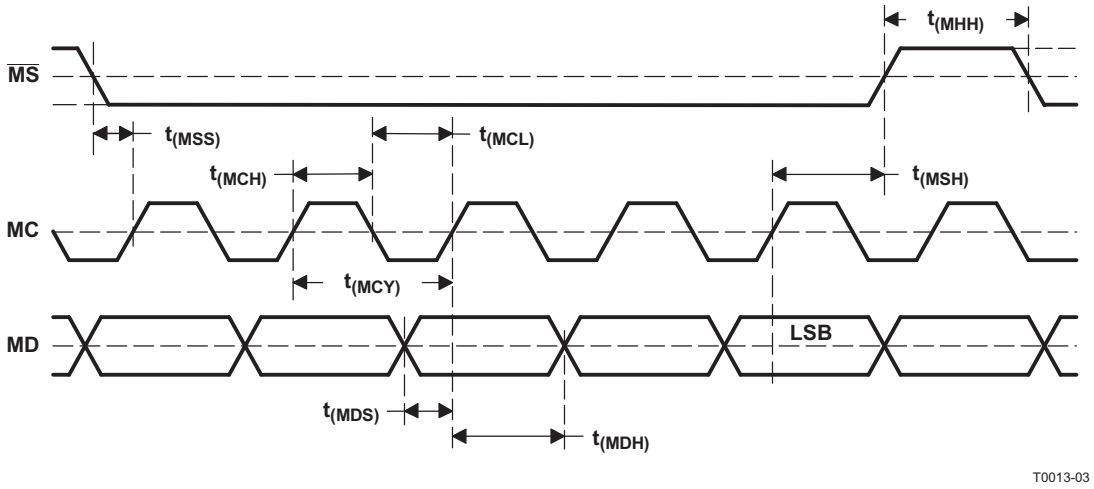


Figure 29. Interface Timing Diagram

Table 9. Interface Timing

PARAMETER		MIN	UNIT
$t_{(MCY)}$	MC cycle time	100	ns
$t_{(MCL)}$	MC pulse duration, LOW	50	ns
$t_{(MCH)}$	MC pulse duration, HIGH	50	ns
$t_{(MHH)}$	$\overline{MS}$ pulse duration, HIGH		ns (1)
$t_{(MSS)}$	$\overline{MS}$ falling edge to MC rising edge	20	ns
$t_{(MSH)}$	$\overline{MS}$ hold time, MC rising edge for LSB to $\overline{MS}$ rising edge	20	ns
$t_{(MDH)}$	MD hold time	15	ns
$t_{(MDS)}$	MD setup time	20	ns

(1) $3/(256\ f_S)$ s (minimum), f_S: sampling rate

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8.4 Device Functional Modes

8.4.1 Control Modes

- 3-wire SPI
- I^2C
- Hardware Control

8.4.2 Audio Modes

- Right or left justified
- I^2S
- TDM
- DSP

8.5 Programming

8.5.1 I^2C Interface

The PCM1681 and PCM1681-Q1 support the I^2C serial bus and the data transmission protocol for standard mode as a slave device. This protocol is explained in the I^2C specification 2.0. The PCM1681 and PCM1681-Q1 do not support a board-to-board interface. The I^2C control interface is available when MSEL (pin 14) is tied with DGND and after power-on reset completion.

8.5.1.1 Slave Address

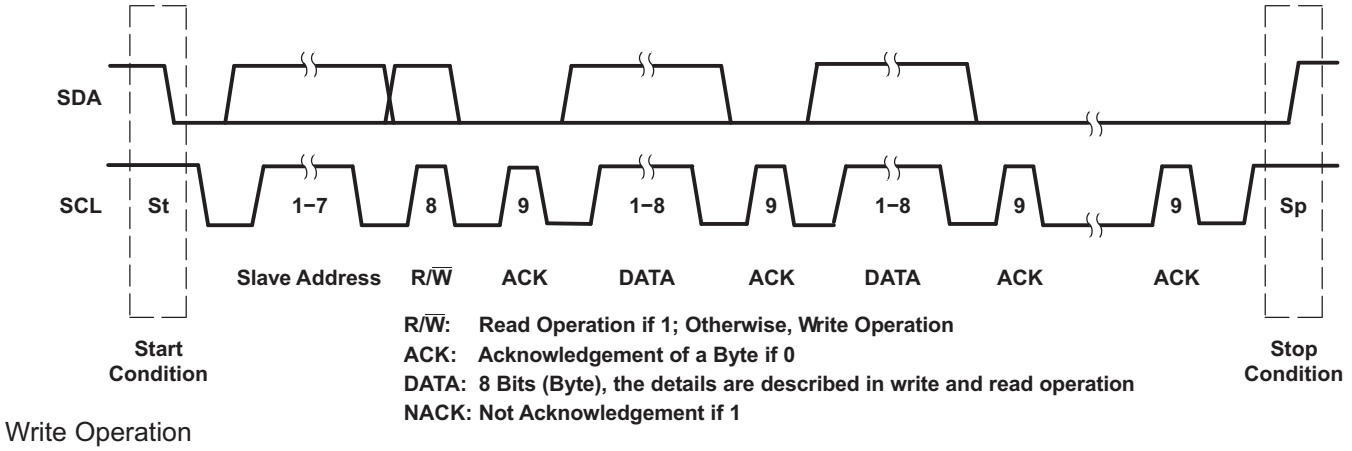
MSB							LSB
1	0	0	1	1	0	ADR	R/$\overline{W}$

The PCM1681 and PCM1681-Q1 have seven bits for the respective slave address. The first six bits (MSBs) of the slave address are factory preset to 1001 10. The next bit of the address byte is the device select bit, which can be user-defined using the ADR terminal. A maximum of two PCM1681s or PCM1681-Q1s can be connected on the same bus at one time. Each PCM1681 or PCM1681-Q1 responds when it receives its own slave address.

8.5.1.2 Packet Protocol

A master device must control packet protocol, which consists of a start condition, slave address, read/write bit, data if writing or acknowledge if reading, and stop condition. The PCM1681 and PCM1681-Q1 support only slave receivers and slave transmitters. The details about DATA for write and read operation are described in the following sections.

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Write Operation

Transmitter	M	M	M	S	M	S	M	S		S	M
Data Type	St	Slave Address	W	ACK	DATA	ACK	DATA	ACK		ACK	Sp

Read Operation

Transmitter	M	M	M	S	S	M	S	M		M	M
Data Type	St	Slave Address	R	ACK	DATA	ACK	DATA	ACK		NACK	Sp

M: Master Device S: Slave Device St: Start Condition
Sp: Stop Condition W: Write R: Read

T0049-01

Figure 30. Basic I²C Framework

8.5.1.3 Write Operation

A master can write to any PCM1681 and PCM1681-Q1 registers using a single access. The master sends a PCM1681 or PCM1681-Q1 slave address with a write bit, a register address, and the data. When undefined registers are accessed, the PCM1681 or PCM1681-Q1 sends an acknowledgment, but the write operation does not occur. Figure 31 is a diagram of the write operation.

Transmitter	M	M	M	S	M	S	M	S	M
Data Type	St	Slave Address	W	ACK	Reg Address	ACK	Write Data	ACK	Sp

M: Master Device S: Slave Device
St: Start Condition W: Write ACK: Acknowledge Sp: Stop Condition

R0002-01

Figure 31. Write Operation

8.5.1.4 Read Operation

A master can read any PCM1681 or PCM1681-Q1 register using a single access. The master sends a PCM1681 or PCM1681-Q1 slave address with a read bit after transferring the register address. Then the PCM1681 or PCM1681-Q1 transfers the data in the register specified. Figure 32 is a diagram of the read operation.

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Transmitter	M	M	M	S	M	S	M	M	M	S	S	M	M
Data Type	St	Slave Address	$\overline{W}$	ACK	Reg Address	ACK	Sr	Slave Address	R	ACK	Read Data	NACK	Sp

M: Master Device S: Slave Device St: Start Condition
Sr: Repeated Start Condition ACK: Acknowledge Sp: Stop Condition NACK: Not Acknowledge
$\overline{W}$: Write R: Read

R0002-02

NOTE: The slave address after the repeated start condition must be the same as the previous slave address.

Figure 32. Read Operation

8.5.2 Mode Control Registers

8.5.2.1 User-Programmable Mode Controls

The PCM1681 and PCM1681-Q1 include a number of user-programmable functions which are accessed via control registers. The registers are programmed using the serial control interface which is discussed in the *Mode Control* section of this data sheet. Table 10 lists the available mode control functions, along with the respective reset default conditions and associated register index.

8.6 Register Maps

The mode control register map is shown in Table 11. The MSB of all registers is fixed to 0. Each register also includes an index (or address) indicated by the IDX[6:0] bits.

8.6.1 Reserved Registers

Registers 0 and 15 are reserved for factory use. To ensure proper operation, the user should not write to these registers.

Table 10. User-Programmable Mode Control Functions

FUNCTION	RESET DEFAULT	REGISTER	BIT
Digital attenuation control, 0 dB to –63 dB in 0.5-dB steps	0 dB, no attenuation	1–6, 16, 17	AT1[7:0], AT2[7:0], AT3[7:0], AT4[7:0], AT5[7:0], AT6[7:0], AT7[7:0], AT8[7:0]
Soft mute control	Mute disabled	7, 18	MUT[8:1], MUT[8:7]
DAC1–DAC8 operation control	DAC1–DAC8 enabled	8, 19	DAC[8:1], DAC[8:7]
Audio data format control	16- to 24-bit, left-justified	9	FMT[3:0]
Digital filter roll-off control	Sharp roll-off	9	FLT
De-emphasis all-channel function control	De-emphasis of all channels disabled	10	DMC
De-emphasis all-channel sample rate selection	44.1 kHz	10	DMF[1:0]
Output phase select	Normal phase	10	DREV
Zero-flag polarity select	High	10	ZREV
Software reset control	Reset disabled	10	SRST
Output phase select per channel	Reverse phase	11	REV[8:1]
Oversampling rate control	Narrow (×64, ×32, ×16) mode	12	OVER
Digital filter roll-off control per DATA group	Slow roll-off	12	FLT[4:1]
Zero-flag combination select	ZR1: DATA1 Lch ZR2: DATA1 Rch	13	AZRO[1:0]
Digital attenuation mode select	0 to –63 dB, 0.5-dB step	13	DAMS
Zero-detect status (read-only, I^2C interface only)	N/A	14	ZERO[8:1]

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Table 11. Mode Control Register Map

IDX (B8–B14)	REGISTER	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
00h	0	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	N/A(1)	N/A(1)	N/A(1)	N/A(1)	N/A(1)	N/A(1)	N/A(1)	N/A(1)
01h	1	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT17	AT16	AT15	AT14	AT13	AT12	AT11	AT10
02h	2	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT27	AT26	AT25	AT24	AT23	AT22	AT21	AT20
03h	3	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT37	AT36	AT35	AT34	AT33	AT32	AT31	AT30
04h	4	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT47	AT46	AT45	AT44	AT43	AT42	AT41	AT40
05h	5	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT57	AT56	AT55	AT54	AT53	AT52	AT51	AT50
06h	6	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT67	AT66	AT65	AT64	AT63	AT62	AT61	AT60
07h	7	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	MUT8	MUT7	MUT6	MUT5	MUT4	MUT3	MUT2	MUT1
08h	8	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	DAC8	DAC7	DAC6	DAC5	DAC4	DAC3	DAC2	DAC1
09h	9	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV(2)	RSV(2)	FLT	RSV(2)	FMT3	FMT2	FMT1	FMT0
0Ah	10	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	SRST	ZREV	DREV	DMF1	DMF0	RSV(2)	RSV(2)	DMC
0Bh	11	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	REV8	REV7	REV6	REV5	REV4	REV3	REV2	REV1
0Ch	12	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	OVER	RSV(2)	RSV(2)	RSV(2)	FLT4	FLT3	FLT2	FLT1
0Dh	13	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	DAMS	AZRO1	AZRO0	RSV(2)	RSV(2)	RSV(2)	RSV(2)	RSV(2)
0Eh	14	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	ZERO8	ZERO7	ZERO6	ZERO5	ZERO4	ZERO3	ZERO2	ZERO1
10h	16	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT77	AT76	AT75	AT74	AT73	AT72	AT71	AT70
11h	17	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT87	AT86	AT85	AT84	AT83	AT82	AT81	AT80
12h	18	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV(2)	RSV(2)	RSV(2)	RSV(2)	RSV(2)	RSV(2)	MUT8	MUT7
13h	19	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV(2)	RSV(2)	RSV(2)	RSV(2)	RSV(2)	RSV(2)	DAC8	DAC7

(1) Not assigned. No operation even if setting any data
(2) Reserved for test operation. It should be set to 0 during normal operation.

8.6.2 Register Definitions

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 1	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT17	AT16	AT15	AT14	AT13	AT12	AT11	AT10
REGISTER 2	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT27	AT26	AT25	AT24	AT23	AT22	AT21	AT20
REGISTER 3	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT37	AT36	AT35	AT34	AT33	AT32	AT31	AT30
REGISTER 4	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT47	AT46	AT45	AT44	AT43	AT42	AT41	AT40
REGISTER 5	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT57	AT56	AT55	AT54	AT53	AT52	AT51	AT50
REGISTER 6	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT67	AT66	AT65	AT64	AT63	AT62	AT61	AT60
REGISTER 16	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT77	AT76	AT75	AT74	AT73	AT72	AT71	AT70
REGISTER 17	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT87	AT86	AT85	AT84	AT83	AT82	AT81	AT80

8.6.2.1 ATx[7:0]: Digital Attenuation Level Setting

where x = 1–8, corresponding to the DAC output $V_{OUT}x$. Default value: 1111 1111b

ATx[7:0]	DECIMAL VALUE	ATTENUATION LEVEL SETTING	
		DAMS = 0	DAMS = 1
1111 1111b	255	0 dB, no attenuation (default)	0 dB, no attenuation (default)
1111 1110b	254	–0.5 dB	–1 dB
1111 1101b	253	–1 dB	–2 dB
:	:	:	:
1001 1100b	156	–49.5 dB	–99 dB
1001 1011b	155	–50 dB	–100 dB
1001 1010b	154	–50.5 dB	Mute
:	:	:	:
1000 0010b	130	–62.5 dB	Mute
1000 0001b	129	–63 dB	Mute
1000 0000b	128	Mute	Mute
:	:	:	:
0000 0000b	0	Mute	Mute

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Each DAC output, $V_{OUT}1$ through $V_{OUT}8$, has a digital attenuation function. The attenuation level can be set from 0 dB to R dB, in S-dB steps. Changes in attenuation levels are made by incrementing or decrementing by one step (S-dB) for every $8/f_S$ time interval until the programmed attenuation setting is reached. Alternatively, the attenuation level can be set to infinite attenuation (or mute). Range (R) and step (S) are –63 and 0.5, respectively, for DAMS = 0 and –100 and 1, respectively, for DAMS = 1. The DAMS bit is defined in register 13. The attenuation data for each channel can be set individually. The attenuation level can be calculated using the following formula:

$$\text{Attenuation level (dB)} = S \bullet (ATx[7:0]_{DEC} - 255)$$

where $ATx[7:0]_{DEC}$ = 0 through 255. For $ATx[7:0]_{DEC}$ = 0 through 128 with DAMS = 0 or for $ATx[7:0]_{DEC}$ = 0 through 154 with DAMS = 1, the attenuation is set to infinite attenuation (mute).

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 7	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	MUT8	MUT7	MUT6	MUT5	MUT4	MUT3	MUT2	MUT1
REGISTER 18	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	RSV	RSV	RSV	RSV	MUT8	MUT7

8.6.2.2 MUTx: Soft Mute Control

where x = 1–8, corresponding to the DAC output $V_{OUT}x$. Default value: 0

MUTx	SOFT MUTE CONTROL
0	Mute disabled (default)
1	Mute enabled

The mute bits, MUT1 through MUT8, are used to enable or disable the soft mute function for the corresponding DAC outputs, $V_{OUT}1$ through $V_{OUT}8$. MUT7 and MUT8 of register 7 and register 18 work as an OR function, either one or both can be used according to the requirements of the application. The soft mute function is incorporated into the digital attenuators. When mute is disabled (MUTx = 0), the attenuator and DAC operate normally. When mute is enabled by setting MUTx = 1, the digital attenuator for the corresponding output is decreased from the current setting to the infinite-attenuation setting one attenuator step (S-dB) at a time. This provides a quiet, pop-free muting of the DAC output. On returning from soft mute, by setting MUTx = 0, the attenuator is increased one step at a time to the previously programmed attenuator level. The step size, S, is 0.5 dB for DAMS = 0 and 1 dB for DAMS = 1.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 8	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	DAC8	DAC7	DAC6	DAC5	DAC4	DAC3	DAC2	DAC1
REGISTER 19	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	RSV	RSV	RSV	RSV	DAC8	DAC7

8.6.2.3 DACx: DAC Operation Control

where x = 1–8, corresponding to the DAC output $V_{OUT}x$. Default value: 0

DACx	DAC OPERATION CONTROL
0	DAC operation enabled (default)
1	DAC operation disabled

The DAC operation controls are used to enable and disable the DAC outputs, $V_{OUT}1$ through $V_{OUT}8$. When DACx = 0, the output amplifier input is connected to the DAC output. When DACx = 1, the output amplifier input is switched to the dc common voltage (V_{COM}), equal to $V_{CC}/2$. DAC7 and DAC8 of register 8 and register 19 work as an OR function, either one or both can be used according to the requirements of the application.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 9	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	FLT	RSV	FMT3	FMT2	FMT1	FMT0

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8.6.2.4 FLT: Digital Filter Roll-Off Control

Default value: 0

FLT	DIGITAL FILTER ROLL-OFF CONTROL
0	Sharp roll-off (default)
1	Slow roll-off

The FLT bit allows users to select the digital filter roll-off that is best suited to their application. Two filter roll-off selections are available: sharp or slow. The filter responses for these selections are shown in the *Typical Characteristics* section of this data sheet.

8.6.2.5 FMT[3:0]: Audio Interface Data Format

Default value: 0101b

FMT[3:0]	AUDIO DATA FORMAT SELECTION
0000	Right-justified format, 24-bit
0001	Reserved
0010	Reserved
0011	Right-justified format, 16-bit
0100	I^2S format, 16- to 24-bit
0101	Left-justified format, 16- to 24-bit (default)
0110	I^2S format, TDM format, 24-bit
0111	Left-justified format, TDM format, 24-bit
1000	I^2S format, DSP format, 24-bit
1001	Left-justified format, DSP format, 24-bit

The FMT[3:0] bits are used to select the data format for the serial audio interface.

The format details and restrictions related with the system clock are described in the section *Audio Data Formats and Timing*.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 10	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	SRST	ZREV	DREV	DMF1	DMF0	RSV	RSV	DMC

8.6.2.6 SRST: Reset

Default value: 0

SRST	RESET
0	Reset disabled (default)
1	Reset enabled

The SRST bit is used to enable or disable the soft reset function. The operation is the same as the power-on-reset function with the exception of the reset period, which is 1024 system clocks for the SRST function. All registers are initialized.

8.6.2.7 ZREV: Zero-Flag Polarity Select

Default value: 0

ZREV	ZERO-FLAG POLARITY SELECT
0	Zero-flag pins high at a zero detect (default)
1	Zero-flag pins low at a zero detect

The ZREV bit allows the user to select the polarity of the zero-flag pins.

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8.6.2.8 DREV: Output Phase Select

Default value: 0

DREV	OUTPUT PHASE SELECT
0	Normal output (default)
1	Inverted output

The DREV bit allows the user to select the phase of the analog output signal.

8.6.2.9 DMF[1:0]: Sampling Frequency Selection for the De-Emphasis Function

Default value: 00b

DMF[1:0]	DE-EMPHASIS SAMPLING RATE SELECTION
00	44.1 kHz (default)
01	48 kHz
10	32 kHz
11	Reserved

The DMF[1:0] bits select the sampling frequency used for the digital de-emphasis function when it is enabled. The de-emphasis curves are shown in the *Typical Characteristics* section of this data sheet. The preceding table shows the available sampling frequencies.

8.6.2.10 DMC: Digital De-Emphasis All-Channel Function Control

Default value: 0

DMC	DIGITAL DE-EMPHASIS ALL-CHANNEL FUNCTION CONTROL
0	De-emphasis disabled for all channels (default)
1	De-emphasis enabled for all channels

The DMC bit is used to enable or disable the de-emphasis function for all channels.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 11	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	REV8	REV7	REV6	REV5	REV4	REV3	REV2	REV1

8.6.2.11 REV[8:1]: Output Phase Select per Channel

Where x = 1 – 8, corresponding to the DAC output $V_{OUT}x$. Default value: 1

REVx	OUTPUT PHASE SELECT PER CHANNEL
0	Normal output
1	Inverted output (default)

The REVx bit allows the user to select the phase of the analog output signal per channel when DREV = 1 is set on Register 10.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 12	0	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	OVER	RSV	RSV	RSV	FLT4	FLT3	FLT2	FLT1

8.6.2.12 OVER: Oversampling Rate Control

Default value: 0

OVER	512 f_S, 768 f_S, 1152 f_S	256 f_S, 384 f_S	128 f_S, 192 f_S
0	×64 oversampling, narrow mode (default)	×32 oversampling, narrow mode (default)	×16 oversampling, narrow mode (default)
1	×128 oversampling, wide mode	×64 oversampling, wide mode	×32 oversampling, wide mode

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8.6.2.13 FLTx: Digital Filter Roll-Off Control per DATA Group

Where x = 1 – 4, corresponding to the DATAx. Default value: 1

FLTx	DIGITAL FILTER ROLL-OFF CONTROL PER DATA GROUP
0	Sharp roll-off
1	Slow roll-off (default)

The FLTx bit allows the user to select the digital filter roll-off characteristic per 2 channels when FLT = 1 is set, so that it is best suited to the application. Two filter roll-off sections are available: sharp or slow. The filter responses for these selections are shown in the *Typical Characteristics* section.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 13	0	IDX 6	IDX 5	IDX 4	IDX 3	IDX 2	IDX 1	IDX 0	DAMS	AZRO1	AZRO0	RSV	RSV	RSV	RSV	RSV

8.6.2.14 DAMS: Digital Attenuation Mode Select

Default value: 0

DAMS	DIGITAL ATTENUATION MODE SELECT
0	Fine step, 0.5 dB/step for 0 to –63 dB range (default)
1	Wide range, 1 dB/step for 0 to –100 dB range

The DAMS bit is used to select the digital attenuation mode.

8.6.2.15 AZRO[1:0]: Zero-Flag Channel-Combination Select

Default value: 00b

AZRO[1:0]	ZERO-FLAG CHANNEL-COMBINATION SELECT
00	Combination A (ZR1: DATA1 L-ch, ZR2: DATA1 R-ch) (default)
01	Combination B (ZR1: DATA1–DATA4, ZR2: DATA1–DATA4)
10	Combination C (ZR1: DATA4, ZR2: DATA1–DATA3)
11	Combination D (ZR1: DATA1, ZR2: DATA2–DATA4)

The AZRO[1:0] bits are used to select the zero-flag channel combinations for ZR1 and ZR2.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 14	0	IDX 6	IDX 5	IDX 4	IDX 3	IDX 2	IDX 1	IDX 0	ZERO8	ZERO7	ZERO6	ZERO5	ZERO4	ZERO3	ZERO2	ZERO1

8.6.2.16 ZERO[8:1]: Zero-Detect Status (Read-Only, I^2C Interface Only)

Default value: N/A

The ZERO[8:1] bits show the status of zero detect for each channel. The status is set to 1 by detecting a zero state without regard to the ZREV bit setting.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 D/A Output Filter Circuits

ΔΣ DACs use noise shaping techniques to improve in-band signal-to-noise ratio (SNR) performance at the expense of generating increased out-of-band noise above the Nyquist frequency, or $f_S/2$. The out-of-band noise must be low-pass filtered in order to provide optimal converter performance. This is accomplished by a combination of on-chip and external low-pass filtering.

Figure 26 and Figure 33 show the recommended external low-pass active filter circuits for dual- and single-supply applications. These circuits are second-order Butterworth filters using a multiple-feedback (MFB) circuit arrangement, which reduces sensitivity to passive component variations over frequency and temperature. For more information regarding MFB active filter design, see *Dynamic Performance Testing of Digital Audio D/A Converters* (SBAA055).

Because the overall system performance is defined by the quality of the D/A converters and their associated analog output circuitry, high-quality audio operational amplifiers are recommended for the active filters. Texas Instruments' OPA2353 and OPA2134 dual operational amplifiers are shown in Figure 26 and Figure 33, and are recommended for use with the PCM1681 and PCM1681-Q1.

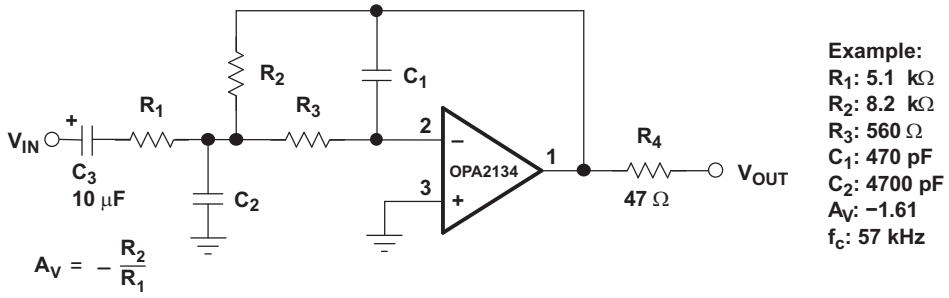


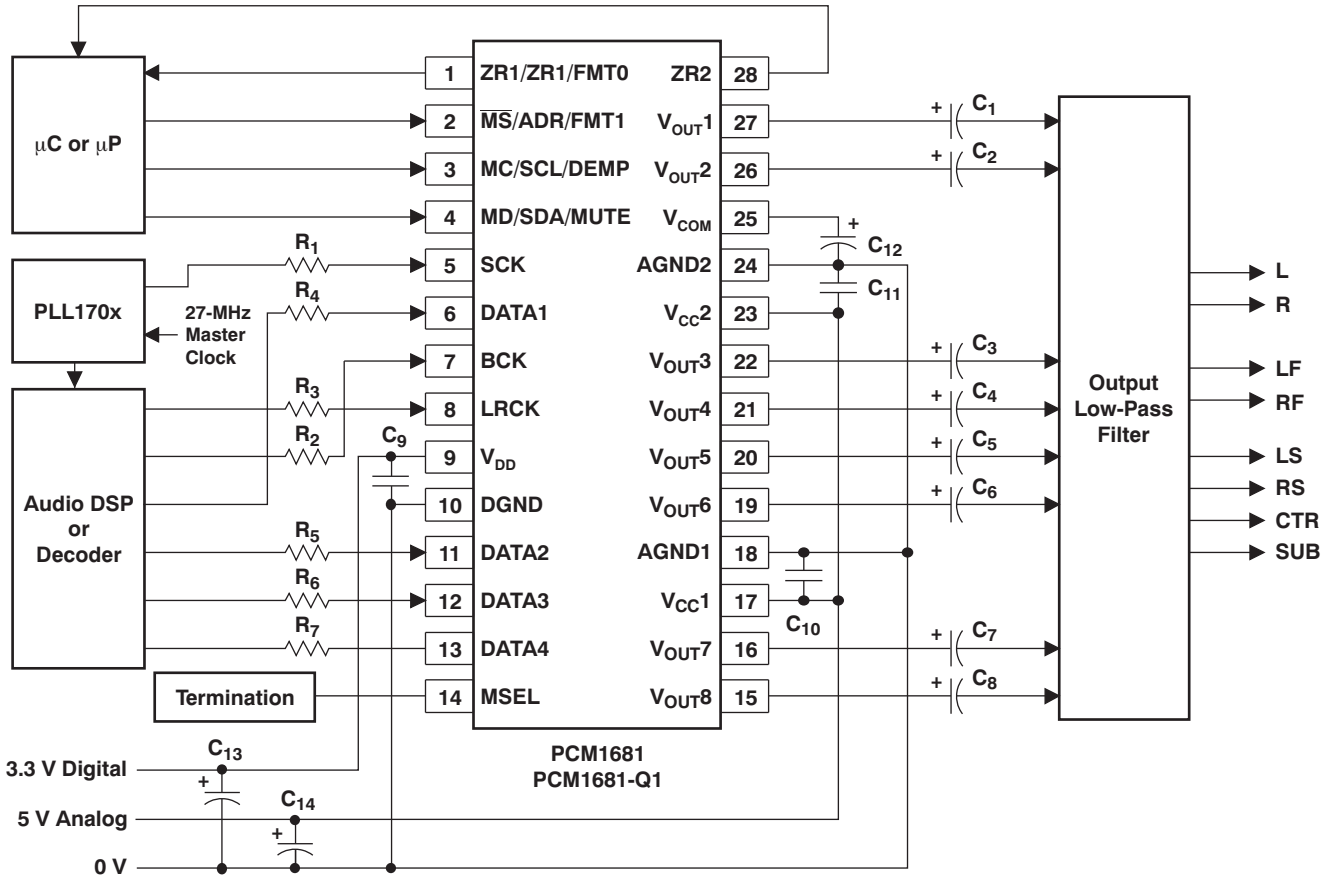
Figure 33. Dual-Supply Filter Circuit

9.2 Typical Application

A basic connection diagram is shown in Figure 34, with the necessary power supply bypassing and decoupling components. Texas Instruments' PLL170x is used to generate the system clock input at SCK, as well as generating the clock for the audio signal processor. The use of series resistors (22 Ω to 100 Ω) is recommended for SCK, LRCK, BCK, DATA1, DATA2, DATA3, and DATA4. The series resistor combines with the stray PCB capacitance and device input capacitance to form a low-pass filter that removes high-frequency noise from the digital signal, thus reducing high-frequency emission.

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Typical Application (continued)



C_1–C_8: 4.7-μF to 10-μF Electrolytic Typical
C_9–C_{11}: 1-μF Ceramic Typical
C_{12}: 2.2-μF to 10-μF Electrolytic Typical
C_{13}, C_{14}: 10-μF Electrolytic Typical
R_1–R_7: 22 Ω to 100 Ω Typical
The termination for mode/configuration control:
Either one of the following circuits has to be applied according to necessary mode/configuration.
Resistor value has to be 220 kΩ ±5% tolerant.

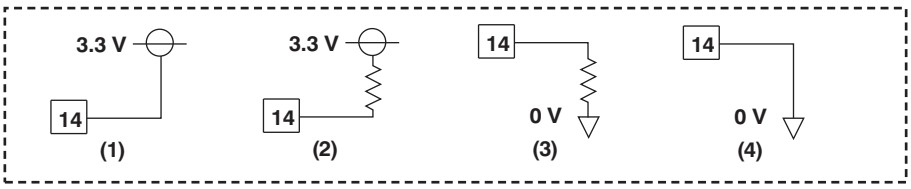


Figure 34. Basic Connection Diagram

9.2.1 Design Requirements

- Control: Hardware, I^2C, or SPI
- Audio Input: PCM Serial data, TDM, or DSP
- Audio Output: 3.75-Vpp analog audio
- Master Clock: PLL170X IC

Typical Application (continued)

9.2.2 Detailed Design Procedure

9.2.2.1 Hardware Control Method

There are 3 ways to control the PCM1681, hardware control, SPI, or I^2C. Hardware control will provide a limited access to control features available in the PCM1681 but can be implemented with pull up and pull downs, or with GPIO of a microcontroller. Control via SPI or I^2C will provide access to all control registers and features but will require a digital device that can implement SPI or I^2C.

9.2.2.2 Audio Input

For audio input there are 3 options, PCM serial data, TDM, or DSP. All three will support the same quality of audio data, but having these 3 options to match the audio sources available outputs allows for greater flexibility. This selection is made by configuring the MSEL pin which is detailed in Table 7 and shown in Figure 34.

9.2.2.3 Audio Output

The output of the PCM1681 will produce a 3.75-Vpp signal at full scale into a 5-kΩ load, that should be filtered before being sent to an amplifier.

9.2.2.4 Master Clock

The master clock can come from wither a dedicated IC such as the PLL170X series, a crystal or the audio source IC. What is important is that the audio source and the PCM1681 are driven from the same source so that the audio clocks will be synchronous.

9.2.3 Application Curve

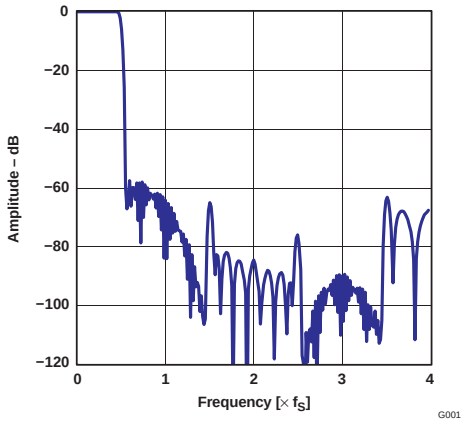


Figure 35. Frequency Response (Sharp Roll-off)

10 Power Supply Recommendations

The PCM1681 and PCM1681-Q1 require 5 V for the analog supply and 3.3 V for the digital supply. The 5-V supply is used to power the DAC analog and output filter circuitry, and the 3.3 V supply is used to power the digital filter and serial interface circuitry. For best performance, a 5-V supply and a 3.3-V supply with linear regulators are recommended.

Five capacitors are required for supply bypassing, as shown in Figure 34. These capacitors should be located as close as possible to the PCM1681 and PCM1681-Q1 package. The 10-µF capacitor should be tantalum or aluminum electrolytic, while the three 1-µF capacitors are ceramic.

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11 Layout

11.1 Layout Guidelines

A typical printed circuit board (PCB) floor plan for the PCM1681 and PCM1681-Q1 is shown in Figure 36. A ground plane is recommended, with the analog and digital sections being isolated from one another using a split or cut in the circuit board. The PCM1681 and PCM1681-Q1 should be oriented with the digital I/O pins facing the ground plane split/cut to allow for short, direct connections to the digital audio interface and control signals originating from the digital section of the board.

Separate power supplies are recommended for the digital and analog sections of the board. This prevents the switching noise present on the digital supply from contaminating the analog power supply and degrading the dynamic performance of the PCM1681 and PCM1681-Q1.

The PowerPAD can be left open without being soldered to the ground plane of the PCB for the PCM1681. However, it must be soldered to the ground plane which has low thermal resistance for the PCM1681-Q1.

11.2 Layout Example

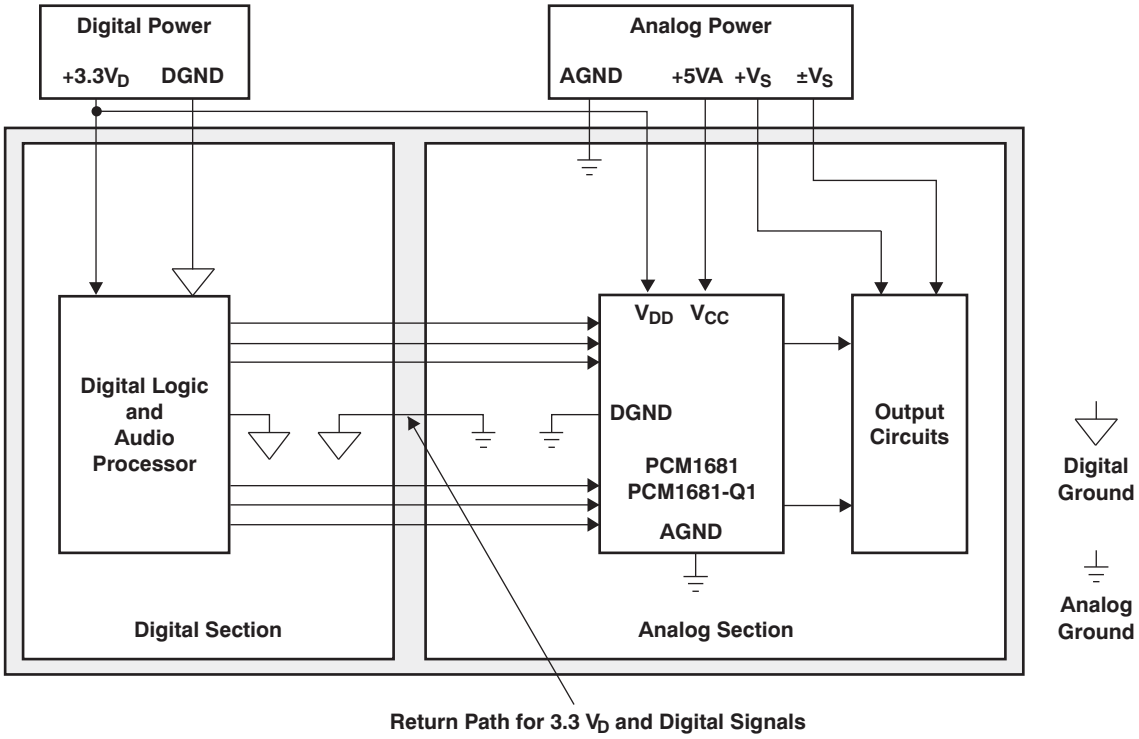


Figure 36. Recommended PCB Layout

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

Dynamic Performance Testing of Digital Audio D/A Converters (SBAA055)

12.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 12. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
PCM1681	Click here	Click here	Click here	Click here	Click here
PCM1681-Q1	Click here	Click here	Click here	Click here	Click here

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System Two, Audio Precision are trademarks of Audio Precision, Inc.
SPI is a trademark of Motorola.
I^2C, I^2S are trademarks of NXP Semiconductors.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PCM1681PWP	Active	Production	HTSSOP (PWP) | 28	50 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	PCM1681
PCM1681PWP.B	Active	Production	HTSSOP (PWP) | 28	50 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	PCM1681
PCM1681PWPR	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	PCM1681
PCM1681PWPR.B	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	PCM1681
PCM1681PWPRG4	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	PCM1681
PCM1681PWPRG4.B	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	PCM1681
PCM1681TPWPQ1	Active	Production	HTSSOP (PWP) | 28	50 | TUBE	Yes	NIPDAU	Level-4-260C-72 HR	-40 to 105	PCM1681TQ1
PCM1681TPWPQ1.B	Active	Production	HTSSOP (PWP) | 28	50 | TUBE	Yes	NIPDAU	Level-4-260C-72 HR	-40 to 105	PCM1681TQ1
PCM1681TPWPRQ1	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-4-260C-72 HR	-40 to 105	PCM1681TQ1
PCM1681TPWPRQ1.B	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-4-260C-72 HR	-40 to 105	PCM1681TQ1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF PCM1681, PCM1681-Q1 :

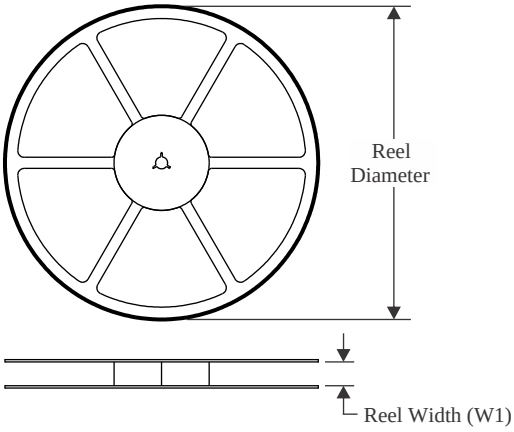
- Catalog : PCM1681
- Automotive : PCM1681-Q1

NOTE: Qualified Version Definitions:

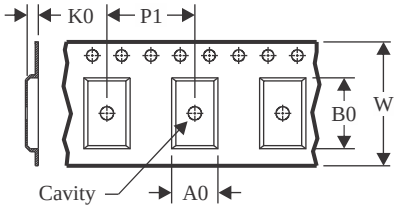
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

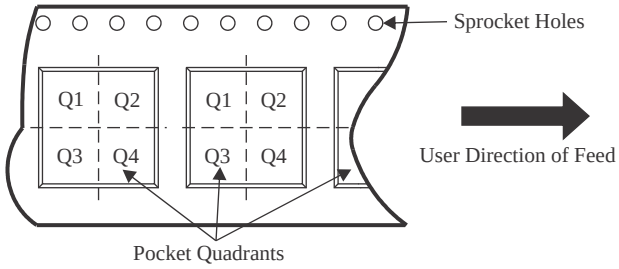


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

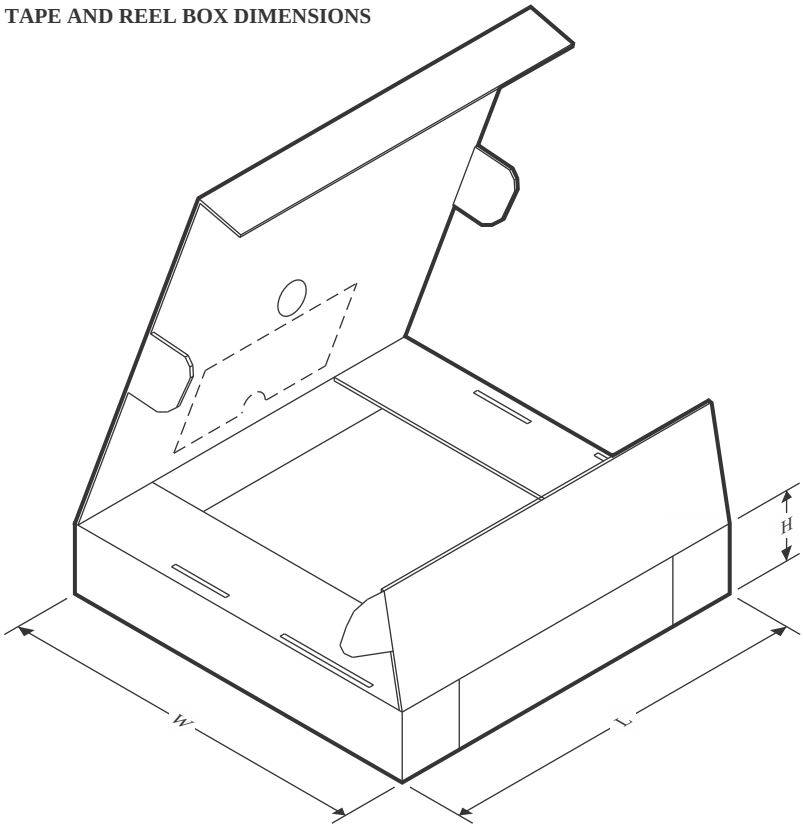
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCM1681PWPR	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
PCM1681PWPRG4	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
PCM1681TPWPRQ1	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

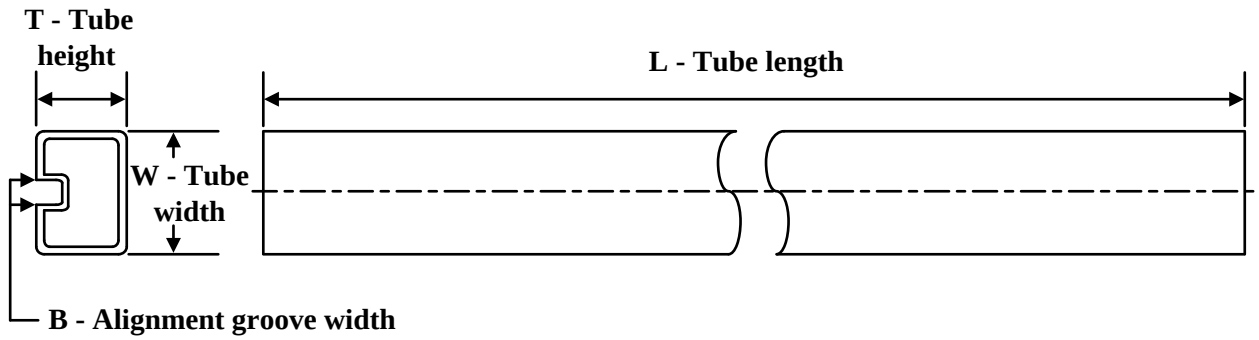
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCM1681PWPR	HTSSOP	PWP	28	2000	350.0	350.0	43.0
PCM1681PWPRG4	HTSSOP	PWP	28	2000	350.0	350.0	43.0
PCM1681TPWPRQ1	HTSSOP	PWP	28	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
PCM1681PWP	PWP	HTSSOP	28	50	530	10.2	3600	3.5
PCM1681PWP.B	PWP	HTSSOP	28	50	530	10.2	3600	3.5
PCM1681TPWPQ1	PWP	HTSSOP	28	50	530	10.2	3600	3.5
PCM1681TPWPQ1.B	PWP	HTSSOP	28	50	530	10.2	3600	3.5

GENERIC PACKAGE VIEW

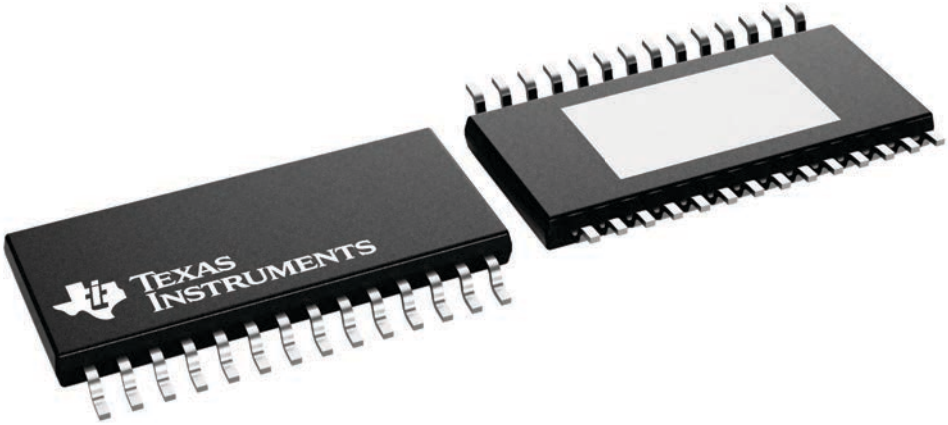
PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 9.7, 0.65 mm pitch

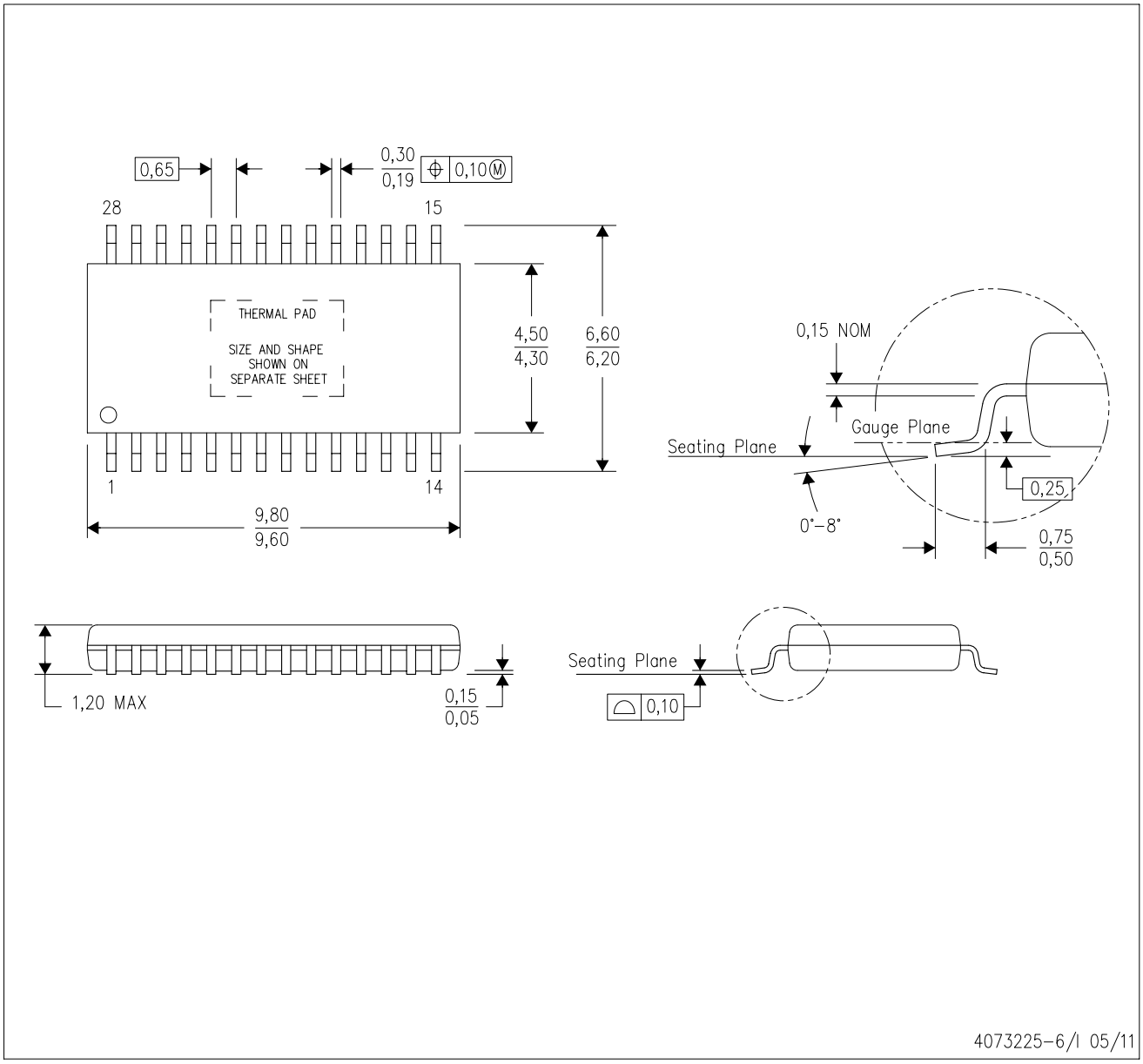
SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224765/B

PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

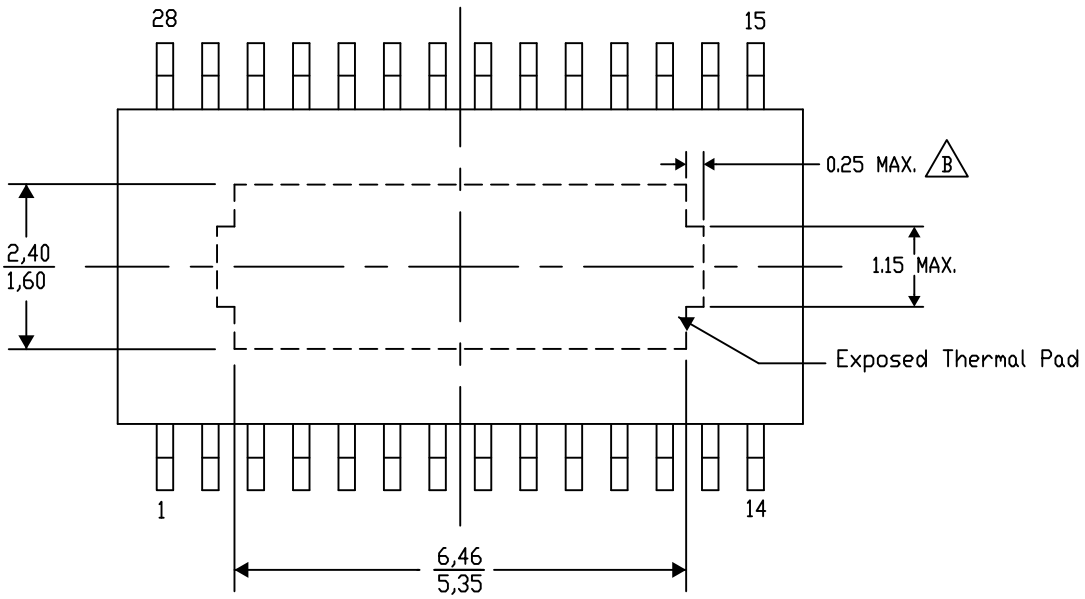
PWP (R–PDSO–G28) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

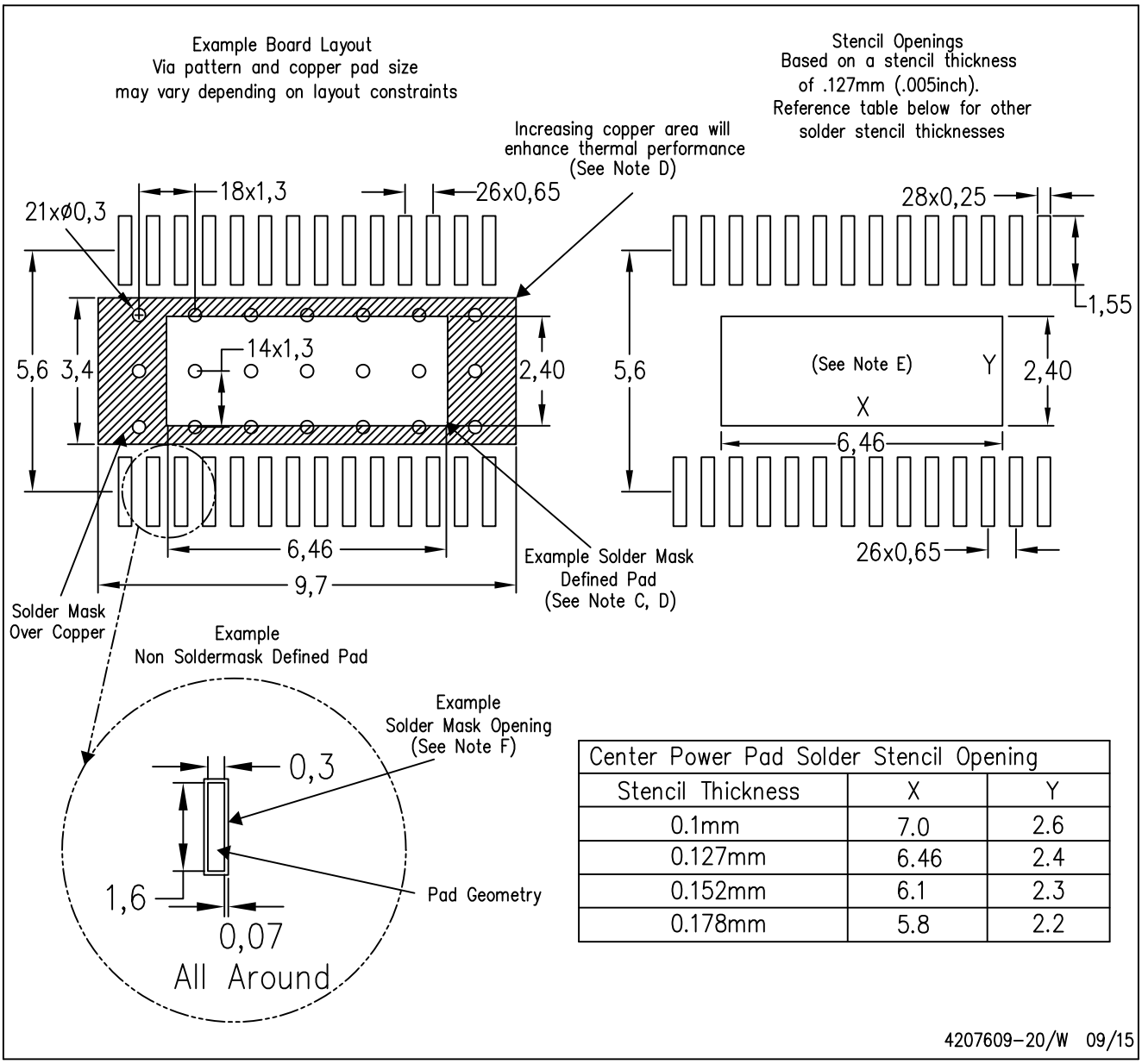
4206332–34/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	7.0	2.6
0.127mm	6.46	2.4
0.152mm	6.1	2.3
0.178mm	5.8	2.2

4207609–20/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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Last updated 10/2025