Stereo Audio Codec with USB Interface, Single-Ended Analog Input/Output, and S/PDIF

Check for Samples: PCM2900C, PCM2902C

FEATURES

- PCM2900C: Without S/PDIF
- PCM2902C: With S/PDIF
- On-Chip USB Interface:
  - With Full-Speed Transceivers
  - Fully Compliant with USB 2.0 Specification
  - Certified by USB-IF
  - Partially Programmable Descriptors
  - USB Adaptive Mode for Playback
  - USB Asynchronous Mode for Record
  - Bus Powered
- 16-Bit Delta-Sigma ADC and DAC
- Sampling Rate:
  - DAC: 32 kHz, 44.1 kHz, 48 kHz
  - ADC: 8 kHz, 11.025 kHz, 16 kHz, 22.05 kHz, 32 kHz, 44.1 kHz, 48 kHz
- On-Chip Clock Generator with Single 12-MHz Clock Source
- Single Power Supply:
  - 5 V Typical (V_{BUS})
- Stereo ADC:
  - Analog Performance at V_{BUS} = 5 V:
    - THD+N = 0.01%
    - SNR = 89 dB
    - Dynamic Range = 89 dB
  - Decimation Digital Filter:
    - Passband Ripple = ±0.05 dB
    - Stop Band Attenuation = –65 dB
  - Single-Ended Voltage Input
  - Antialiasing Filter Included
  - Digital HPF Included
- Stereo DAC:
  - Analog Performance at V_{BUS} = 5 V:
    - THD+N = 0.005%
    - SNR = 96 dB
    - Dynamic Range = 93 dB
  - Oversampling Digital Filter:
    - Passband Ripple = ±0.1 dB
    - Stop Band Attenuation = –43 dB
  - Single-Ended Voltage Output
  - Analog LPF Included
- Multifunctions:
  - Human Interface Device (HID) Function:
    - Volume and Mute Controls
  - Suspend Flag Function
- 28-Pin SSOP Package

APPLICATIONS

- USB Audio Speaker
- USB Headset
- USB Monitor
- USB Audio Interface Box

DESCRIPTION

The PCM2900C/2902C are Texas Instruments' single-chip, USB, stereo audio codecs with a USB-compliant full-speed protocol controller and S/PDIF (PCM2902C only). The USB protocol controller requires no software code. The PCM2900C/2902C employ SpAct™ architecture, TI's unique system that recovers the audio clock from USB packet data. On-chip analog PLLs with SpAct architecture enable playback and record with low clock jitter as well as independent playback and record sampling rates.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGING/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
PCM2900CDB	SSOP-28	DB	–25°C to +85°C	PCM2900C	PCM2900CDB	Rails, 47
					PCM2900CDBR	Tape and Reel, 2000
PCM2902CDB	SSOP-28	DB	–25°C to +85°C	PCM2902C	PCM2902CDB	Rails, 47
					PCM2902CDBR	Tape and Reel, 2000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER			PCM2900C/PCM2902C	UNIT
V_{BUS}	Supply voltage		–0.3 to 6.5	V
	Ground voltage differences, AGNDC, AGNDP, AGNDX, DGND, DGNDU		±0.1	V
	Digital input voltage	SEL0, SEL1, TEST0 (DIN)(2)	–0.3 to 6.5	V
		D+, D–, HID0, HID1, HID2, XTI, XTO, TEST1 (DOUT)(2), $\overline{SSPND}$	–0.3 to (V_{DDI} + 0.3) < 4	V
	Analog input voltage	$V_{IN}L$, $V_{IN}R$, V_{COM}, $V_{OUT}R$, $V_{OUT}L$	–0.3 to (V_{CCCI} + 0.3) < 4	V
		V_{CCCI}, V_{CCP1I}, V_{CCP2I}, V_{CCXI}, V_{DDI}	–0.3 to 4	V
	Input current (any pins except supplies)		±10	mA
	Ambient temperature under bias		–40 to +125	°C
T_{stg}	Storage temperature		–55 to +150	°C
T_J	Junction temperature		+150	°C
	Package temperature (IR reflow, peak)		+250	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) TEST0 and TEST1 apply to the PCM2900C; DIN and DOUT apply to the PCM2902C.

THERMAL INFORMATION

THERMAL METRIC(1)		PCM2900C DB 28 PINS	PCM2902C DB 28 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	64.5	64.5	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	24.5	24.5	
θ_{JB}	Junction-to-board thermal resistance	25.4	25.4	
ψ_{JT}	Junction-to-top characterization parameter	2.0	2.0	
ψ_{JB}	Junction-to-board characterization parameter	25.0	25.0	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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ELECTRICAL CHARACTERISTICS

All specifications at T_A = +25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, and 16-bit data, unless otherwise noted.

PARAMETER			TEST CONDITIONS	PCM2900C, PCM2902C			UNIT
				MIN	TYP	MAX	
DIGITAL INPUT/OUTPUT							
Host interface			Apply USB Revision 2.0, full speed				
Audio data format			USB isochronous data format				
INPUT LOGIC							
V_{IH}	High-level input voltage	D+, D–		2		3.3	VDC
		XTI, HID0, HID1, and HID2		2.52		3.3	VDC
		SEL0, SEL1		2		5.25	VDC
		DIN (PCM2902C)		2.52		5.25	VDC
V_{IL}	Low-level input voltage	D+, D–				0.8	VDC
		XTI, HID0, HID1, and HID2				0.9	VDC
		SEL0, SEL1				0.8	VDC
		DIN (PCM2902C)				0.9	VDC
I_{IH}	High-level input voltage	D+, D–, XTI, SEL0, SEL1	V_{IN} = 3.3 V			±10	µA
		HID0, HID1, and HID2			50	80	µA
		DIN (PCM2902C)			65	100	µA
I_{IL}	Low-level input voltage	D+, D–, XTI, SEL0, SEL1	V_{IN} = 0 V			±10	µA
		HID0, HID1, and HID2				±10	µA
		DIN (PCM2902C)				±10	µA
OUTPUT LOGIC							
V_{OH}	High-level output voltage	D+, D–		2.8			VDC
		DOUT (PCM2902C)	I_{OH} = –4 mA	2.8			VDC
		$\overline{\text{SSPND}}$	I_{OH} = –2 mA	2.8			VDC
V_{OL}	Low-level output voltage	D+, D–				0.3	VDC
		DOUT (PCM2902C)	I_{OL} = 4 mA			0.5	VDC
		$\overline{\text{SSPND}}$	I_{OL} = 2 mA			0.5	VDC
CLOCK FREQUENCY							
Input clock frequency, XTI				11.994	12	12.008	MHz

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ELECTRICAL CHARACTERISTICS (continued)

All specifications at T_A = +25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, and 16-bit data, unless otherwise noted.

PARAMETER		TEST CONDITIONS	PCM2900C, PCM2902C MIN	TYP	MAX	UNIT
ADC CHARACTERISTICS						
	Resolution			8, 16		Bits
	Audio data channel			1, 2		Channel
ADC Clock Frequency						
f_S	Sampling frequency			8, 11.025, 16, 22.05, 32, 44.1, 48		kHz
ADC DC Accuracy						
	Gain mismatch, channel-to-channel			±1	±5	% of FSR
	Gain error			±2	±10	% of FSR
	Bipolar zero error			±0		% of FSR
ADC Dynamic Performance(1)						
THD+N	Total harmonic distortion plus noise	V_{IN} = –1 dB(2), V_{CCCI} = 3.67 V		0.01	0.02	%
		V_{IN} = –1 dB(3)		0.1		%
		V_{IN} = –60 dB		5		%
	Dynamic range	A-weighted	81	89		dB
SNR	Signal-to-noise ratio	A-weighted	81	89		dB
	Channel separation		80	85		dB
Analog Input						
	Input voltage			0.6 V_{CCCI}		V_{PP}
	Center voltage			0.5 V_{CCCI}		V
	Input impedance			30		kΩ
	Antialiasing filter frequency response	–3 dB		150		kHz
		f_{IN} = 20 kHz		–0.08		dB
ADC Digital Filter Performance						
	Passband				0.454 f_S	Hz
	Stop band		0.583 f_S			Hz
	Passband ripple				±0.05	dB
	Stop band attenuation		–65			dB
t_d	Delay time			17.4/f_S		s
	HPF frequency response	–3 dB		0.078 f_S/1000		Hz

(1) f_{IN} = 1 kHz, using a System Two™ audio measurement system by Audio Precision™ in RMS mode with 20-kHz LPF, 400-Hz HPF in calculation.
(2) Using external voltage regulator for V_{CCCI} (as shown in Table 7 and Figure 37, using with REG103xA-A).
(3) Using internal voltage regulator for V_{CCCI} (as shown in Figure 38 and Figure 39).

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ELECTRICAL CHARACTERISTICS (continued)

All specifications at T_A = +25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, and 16-bit data, unless otherwise noted.

PARAMETER		TEST CONDITIONS	PCM2900C, PCM2902C			UNIT
			MIN	TYP	MAX	
DAC CHARACTERISTICS						
	Resolution			8, 16		Bits
	Audio data channel			1, 2		Channel
DAC Clock Frequency						
f_S	Sampling frequency			32, 44.1, 48		kHz
DAC DC Accuracy						
	Gain mismatch channel-to-channel			±1	±5	% of FSR
	Gain error			±2	±10	% of FSR
	Bipolar zero error			±2		% of FSR
DAC Dynamic Performance(4)						
THD+N	Total harmonic distortion plus noise	V_{OUT} = 0 dB		0.005	0.016	%
		V_{OUT} = –60 dB		3		%
	Dynamic range	EIAJ, A-weighted	87	93		dB
SNR	Signal-to-noise ratio	EIAJ, A-weighted	90	96		dB
	Channel separation		86	92		dB
Analog Output						
V_O	Output voltage			0.6 V_{CCCI}		V_{PP}
	Center voltage			0.5 V_{CCCI}		V
	Load impedance	AC coupling	10			kΩ
	LPF frequency response	–3 dB		250		kHz
		f = 20 kHz		–0.03		dB
DAC Digital Filter Performance						
	Passband				0.445 f_S	Hz
	Stop band		0.555 f_S			Hz
	Passband ripple				±0.1	dB
	Stop band attenuation		–43			dB
t_d	Delay time			14.3 f_S		s
POWER-SUPPLY REQUIREMENTS						
V_{BUS}	Voltage range		4.35	5	5.25	VDC
	Supply current	ADC, DAC operation		56	67	mA
		Suspend mode(5)		250		µA
P_D	Power dissipation	ADC, DAC operation		280	352	mW
		Suspend mode(5)		1.25		mW
V_{CCCI}, V_{CCP1I}, V_{CCP2I}, V_{CCXI}, V_{DDI}	Internal power-supply voltage		3.1	3.3	3.5	VDC
TEMPERATURE RANGE						
	Operating temperature range		–25		+85	°C

(4) f_{OUT} = 1 kHz, using a System Two audio measurement system by Audio Precision in RMS mode with 20-kHz LPF, 400-Hz HPF.
(5) Under USB suspend state.

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PCM2900C PIN ASSIGNMENTS

DB PACKAGE
SSOP-28
(TOP VIEW)

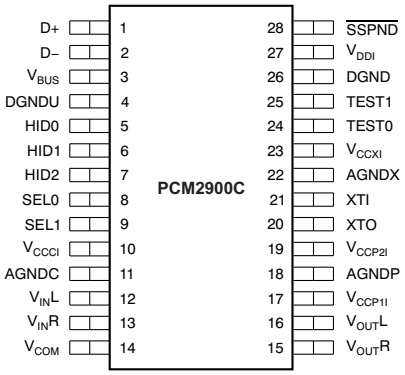


Table 1. PCM2900C TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AGNDC	11	–	Analog ground for codec
AGNDP	18	–	Analog ground for PLL
AGNDX	22	–	Analog ground for oscillator
D–	2	I/O	USB differential input/output minus(1)
D+	1	I/O	USB differential input/output plus(1)
DGND	26	–	Digital ground
DGNDU	4	–	Digital ground for USB transceiver
HID0	5	I	HID key state input (mute), active-high(2)
HID1	6	I	HID key state input (volume up), active-high(2)
HID2	7	I	HID key state input (volume down), active-high(2)
SEL0	8	I	Must be set to high(3)
SEL1	9	I	Must be set to high(3)
$\overline{\text{SSPND}}$	28	O	Suspend flag, active-low (low: suspend, high: operational)
TEST0	24	I	Test pin, must be connected to GND
TEST1	25	O	Test pin, must be left open
V_{BUS}	3	–	Connect to USB power (V_{BUS})
V_{CCCI}	10	–	Internal analog power supply for codec(4)
V_{CCP1I}	17	–	Internal analog power supply for PLL(4)
V_{CCP2I}	19	–	Internal analog power supply for PLL(4)
V_{CCXI}	23	–	Internal analog power supply for oscillator(4)
V_{COM}	14	–	Common for ADC/DAC (V_{CCCI}/2)(4)
V_{DDI}	27	–	Internal digital power supply(4)
V_{IN}L	12	I	ADC analog input for L-channel
V_{IN}R	13	I	ADC analog input for R-channel
V_{OUT}L	16	O	DAC analog output for L-channel
V_{OUT}R	15	O	DAC analog output for R-channel
XTI	21	I	Crystal oscillator input (5)
XTO	20	O	Crystal oscillator output

(1) LV-TTL level.
(2) 3.3-V CMOS-level input with internal pull-down. This pin informs the PC of serviceable control signals such as mute, volume up, or volume down, which have no connection with the internal DAC or ADC directly. See the *Interface #3* and *End-Points* sections.
(3) TTL Schmitt trigger, 5-V tolerant.
(4) Connect a decoupling capacitor to GND.
(5) 3.3-V, CMOS-level input.

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PCM2902C PIN ASSIGNMENTS

DB PACKAGE
SSOP-28
(TOP VIEW)

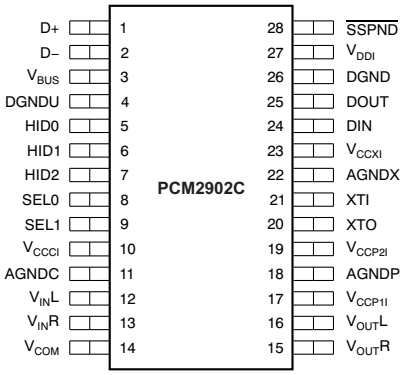


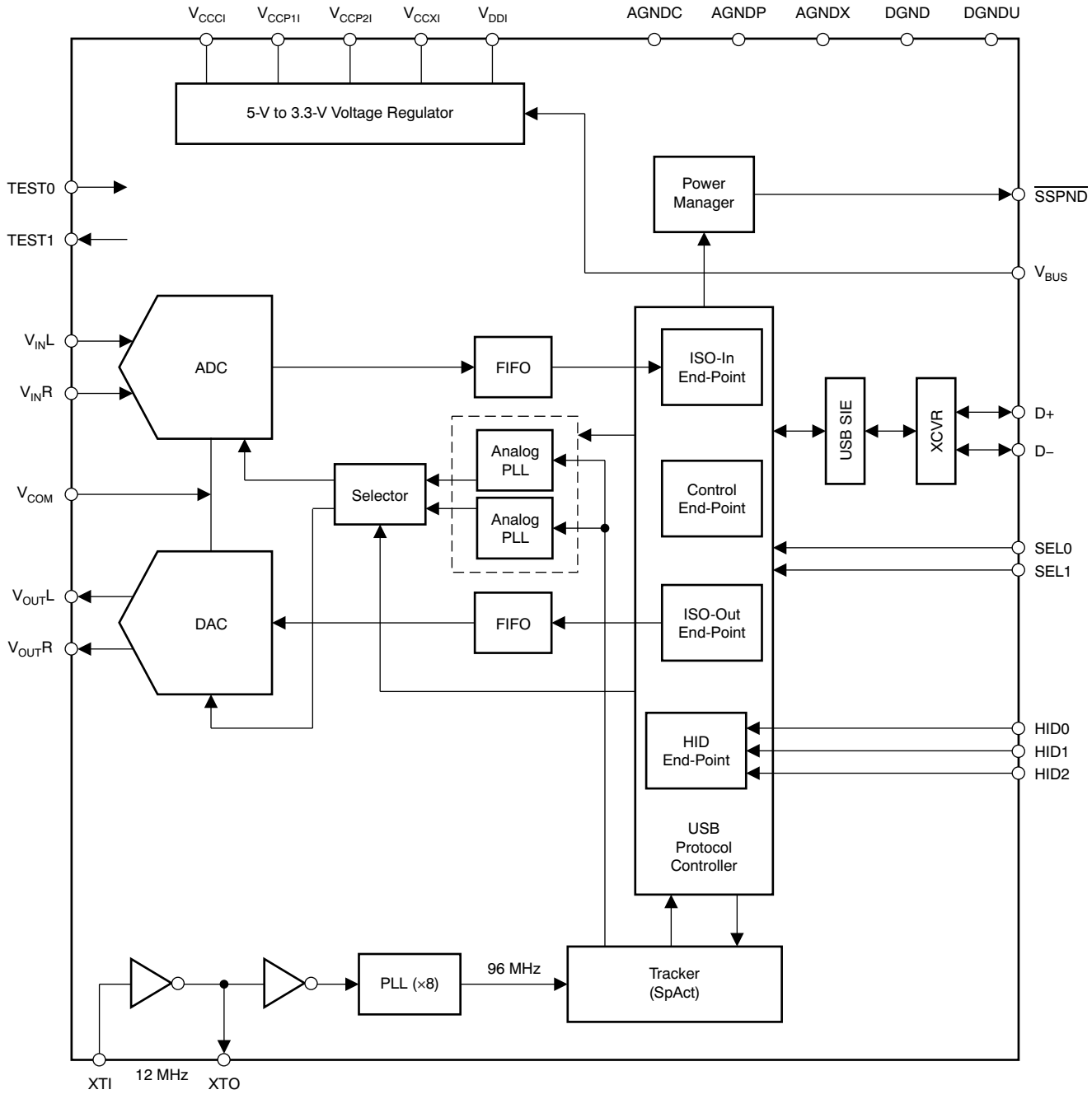
Table 2. PCM2902C TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AGNDC	11	–	Analog ground for codec
AGNDP	18	–	Analog ground for PLL
AGNDX	22	–	Analog ground for oscillator
D–	2	I/O	USB differential input/output minus(1)
D+	1	I/O	USB differential input/output plus(1)
DGND	26	–	Digital ground
DGNDU	4	–	Digital ground for USB transceiver
DIN	24	I	S/PDIF input(2)
DOUT	25	O	S/PDIF output
HID0	5	I	HID key state input (mute), active high(3)
HID1	6	I	HID key state input (volume up), active high(3)
HID2	7	I	HID key state input (volume down), active high(3)
SEL0	8	I	Must be set to high(4)
SEL1	9	I	Must be set to high(4)
$\overline{\text{SSPND}}$	28	O	Suspend flag, active-low (low: suspend, high: operational)
V_{BUS}	3	–	Connect to USB power (V_{BUS})
V_{CCCI}	10	–	Internal analog power supply for codec(5)
V_{CCP1I}	17	–	Internal analog power supply for PLL(5)
V_{CCP2I}	19	–	Internal analog power supply for PLL(5)
V_{CCXI}	23	–	Internal analog power supply for oscillator(5)
V_{COM}	14	–	Common for ADC/DAC (V_{CCCI}/2)(5)
V_{DDI}	27	–	Internal digital power supply
V_{IN}L	12	I	ADC analog input for L-channel
V_{IN}R	13	I	ADC analog input for R-channel
V_{OUT}L	16	O	DAC analog output for L-channel
V_{OUT}R	15	O	DAC analog output for R-channel
XTI	21	I	Crystal oscillator input(6)
XTO	20	O	Crystal oscillator output

(1) LV-TTL level.
(2) 3.3-V CMOS-level input with internal pull-down, 5-V tolerant.
(3) 3.3-V CMOS-level input with internal pull-down. This pin informs the PC of serviceable control signals such as mute, volume up, or volume down, which have no connection with the internal DAC or ADC directly. See the *Interface #3* and *End-Points* sections.
(4) TTL Schmitt trigger, 5-V tolerant.
(5) Connect a decoupling capacitor to GND.
(6) 3.3-V, CMOS-level input.

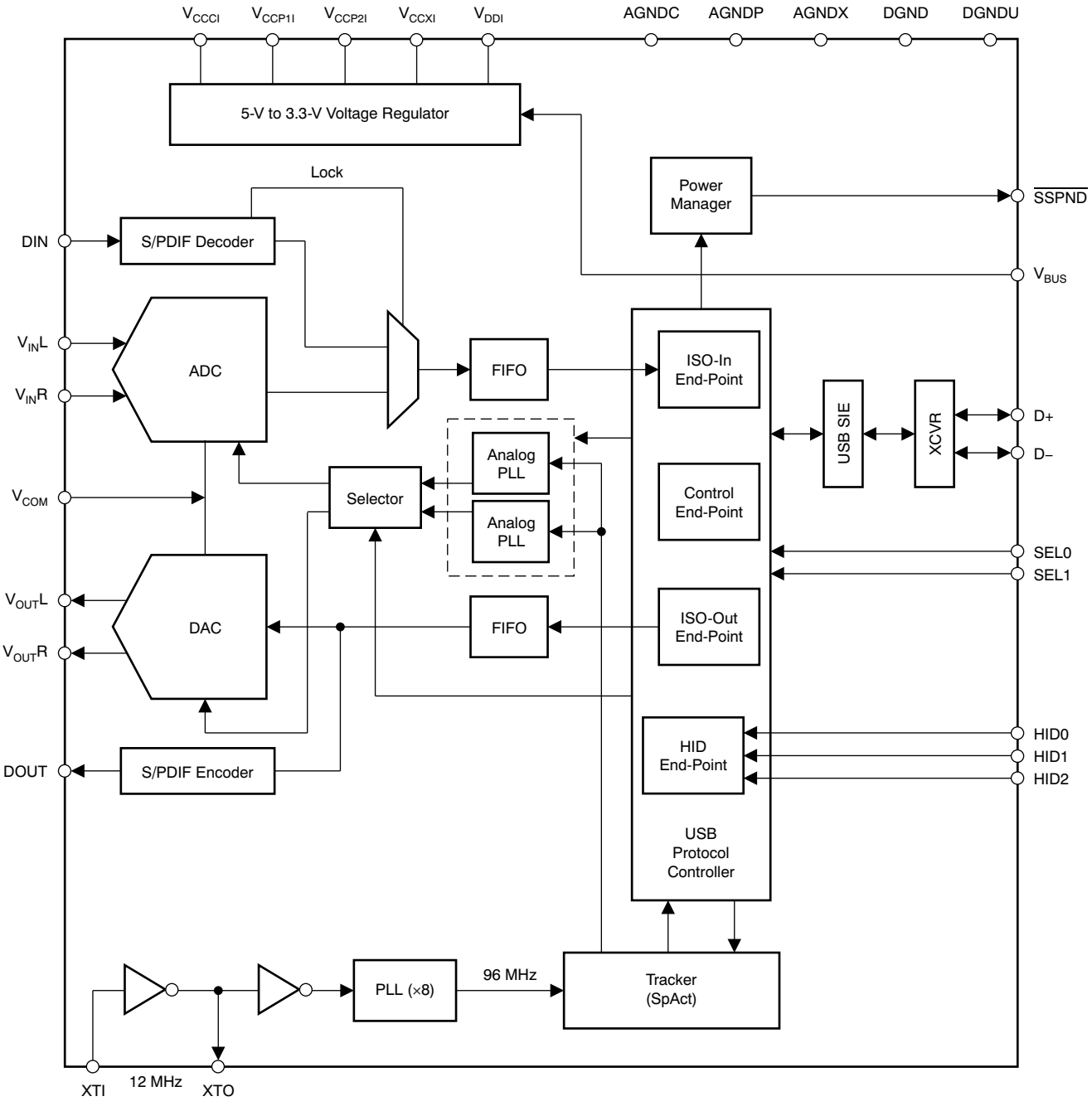
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PCM2900C FUNCTIONAL BLOCK DIAGRAM

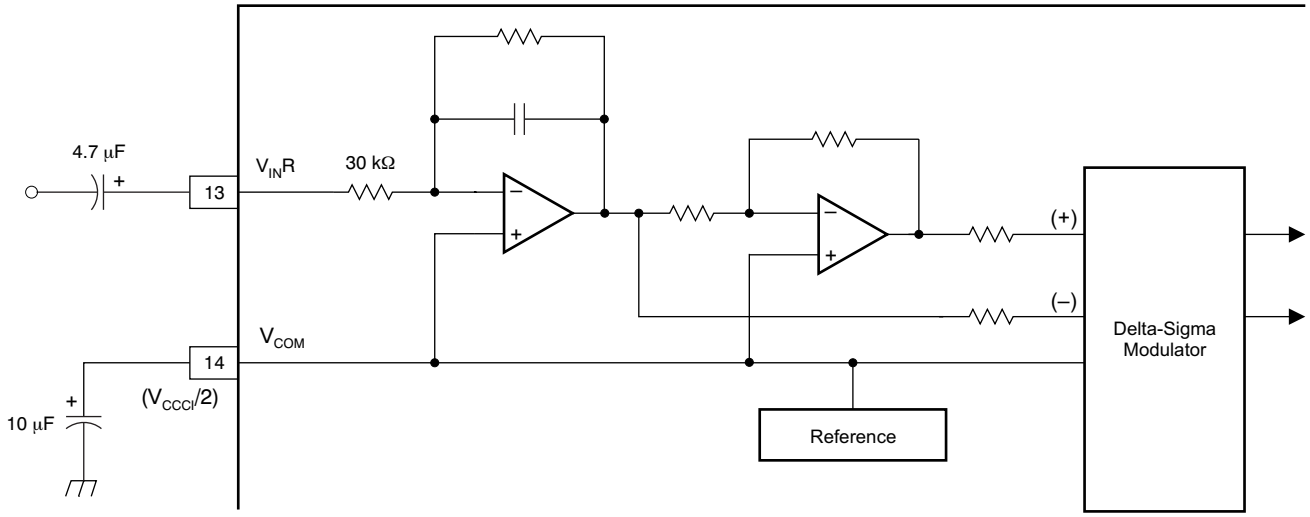


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PCM2902C FUNCTIONAL BLOCK DIAGRAM



PCM2900C/2902C DIAGRAM OF ANALOG FRONT-END (RIGHT CHANNEL)



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TYPICAL CHARACTERISTICS: ADC

All specifications at T_A = +25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{in} = 1 kHz, 16-bit data, using REG 103xA-A, unless otherwise noted.

TOTAL HARMONIC DISTORTION + NOISE at –1 dB vs FREE-AIR TEMPERATURE

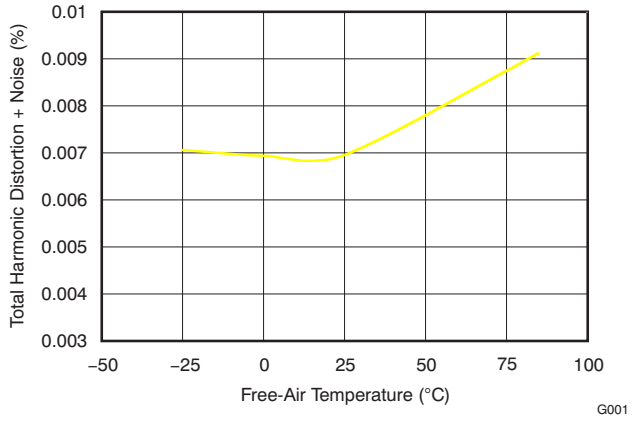


Figure 1.

DYNAMIC RANGE and SNR vs FREE-AIR TEMPERATURE

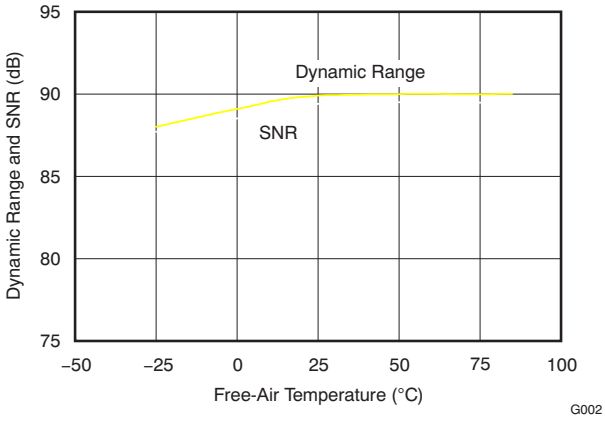


Figure 2.

TOTAL HARMONIC DISTORTION + NOISE at –1 dB vs SUPPLY VOLTAGE

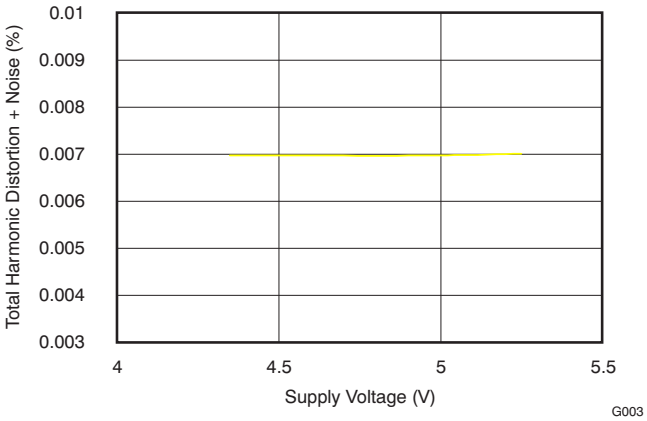


Figure 3.

DYNAMIC RANGE and SNR vs SUPPLY VOLTAGE

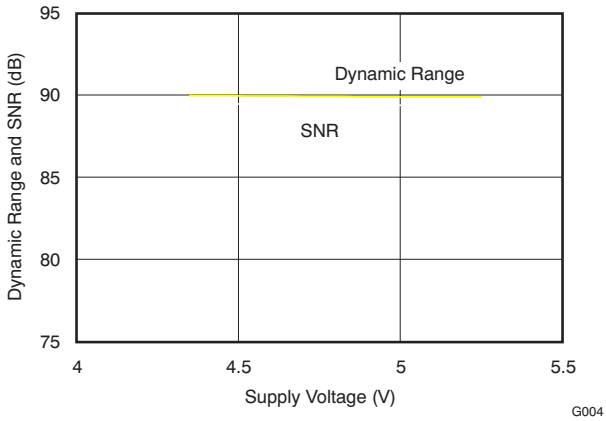


Figure 4.

TOTAL HARMONIC DISTORTION + NOISE at –1 dB vs SAMPLING FREQUENCY

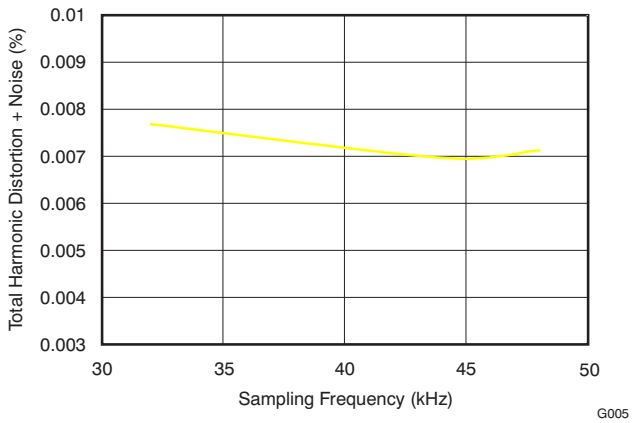


Figure 5.

DYNAMIC RANGE AND SNR vs SAMPLING FREQUENCY

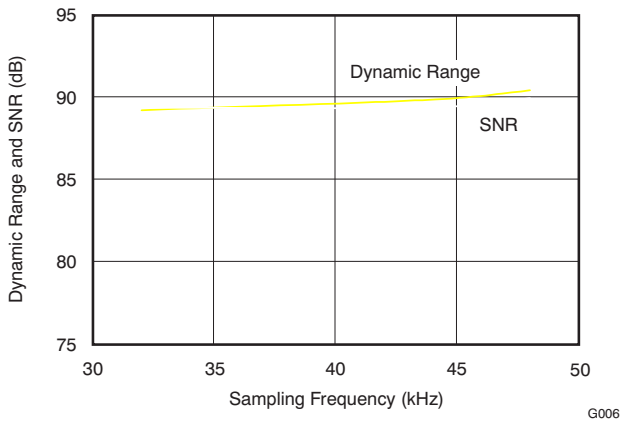


Figure 6.

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TYPICAL CHARACTERISTICS: DAC

All specifications at T_A = +25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{in} = 1 kHz, 16-bit data, using REG 103xA-A, unless otherwise noted.

TOTAL HARMONIC DISTORTION + NOISE at 0 dB vs FREE-AIR TEMPERATURE

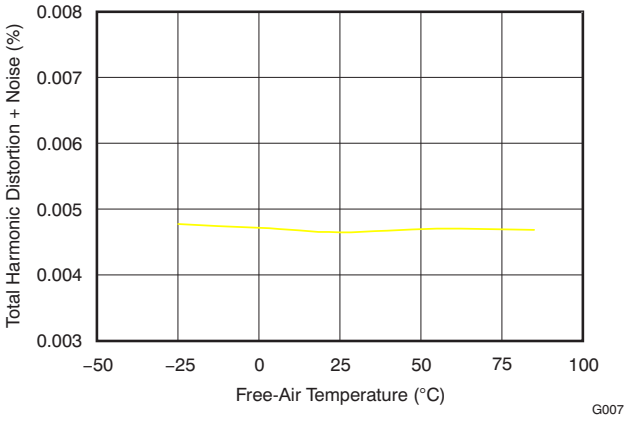


Figure 7.

DYNAMIC RANGE AND SNR vs FREE-AIR TEMPERATURE

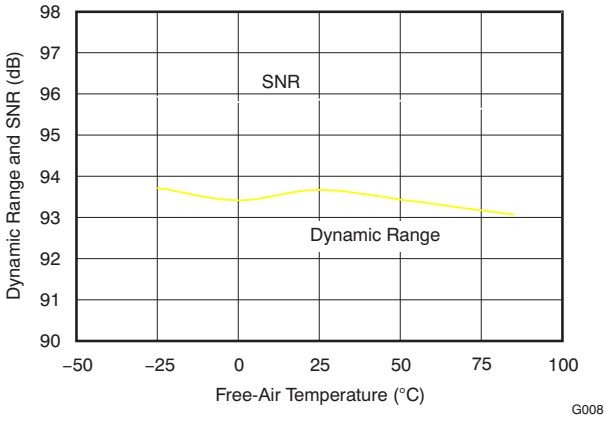


Figure 8.

TOTAL HARMONIC DISTORTION + NOISE at 0 dB vs SUPPLY VOLTAGE

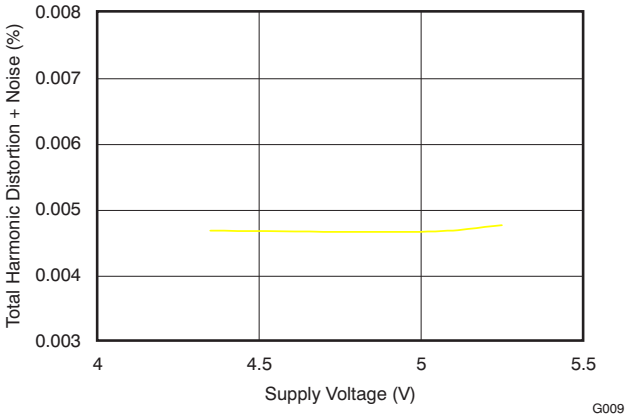


Figure 9.

DYNAMIC RANGE AND SNR vs SUPPLY VOLTAGE

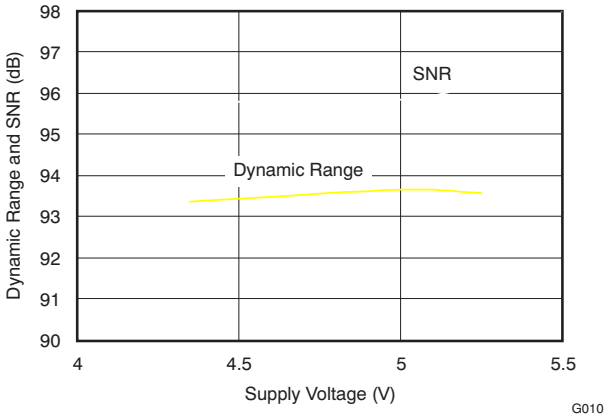


Figure 10.

TOTAL HARMONIC DISTORTION + NOISE at 0 dB vs SAMPLING FREQUENCY

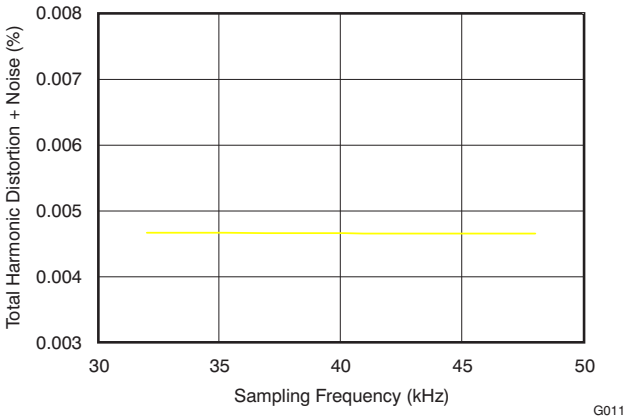


Figure 11.

DYNAMIC RANGE AND SNR vs SAMPLING FREQUENCY

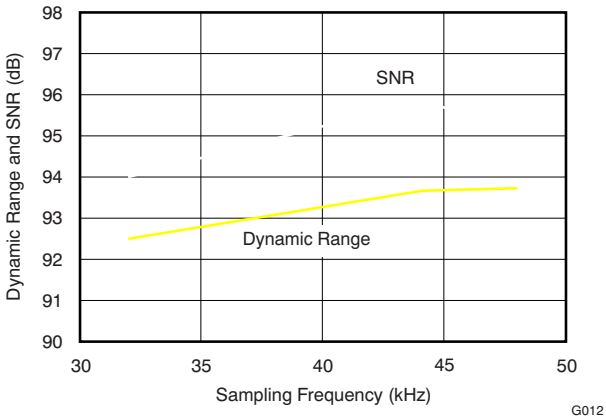


Figure 12.

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TYPICAL CHARACTERISTICS: SUPPLY CURRENT

All specifications at T_A = +25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{in} = 1 kHz, 16-bit data, using REG 103xA-A, unless otherwise noted.

OPERATIONAL AND SUSPEND SUPPLY CURRENT vs SUPPLY VOLTAGE

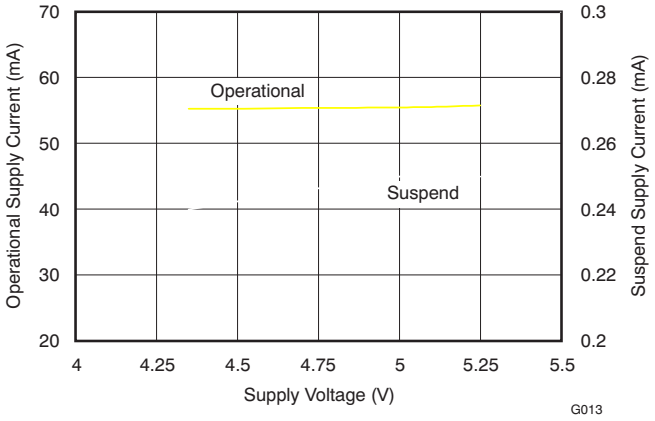


Figure 13.

OPERATIONAL SUPPLY CURRENT vs SAMPLING FREQUENCY

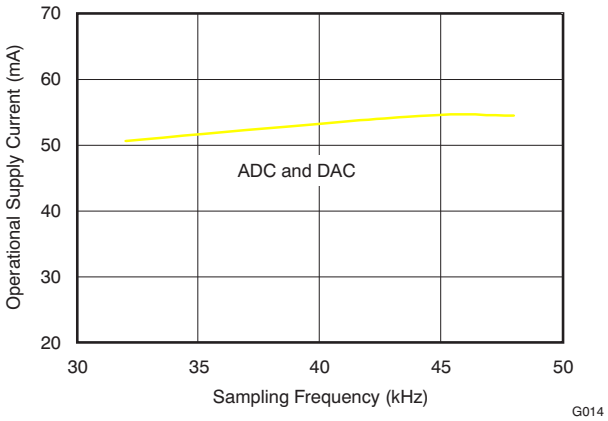


Figure 14.

SUSPEND SUPPLY CURRENT vs FREE-AIR TEMPERATURE

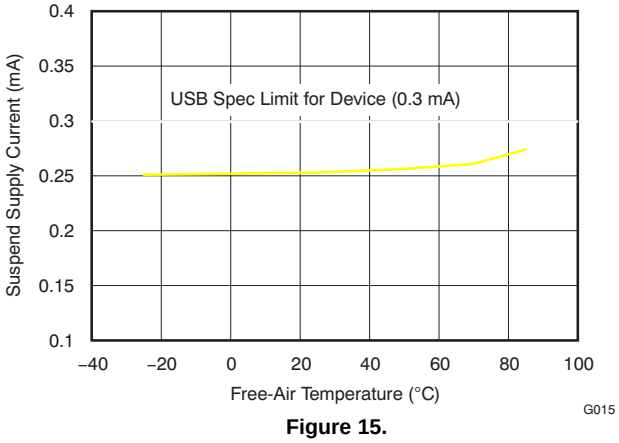


Figure 15.

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TYPICAL CHARACTERISTICS: ADC DIGITAL DECIMATION FILTER FREQUENCY RESPONSE

All specifications at T_A = +25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{in} = 1 kHz, 16-bit data, unless otherwise noted.

OVERALL CHARACTERISTICS

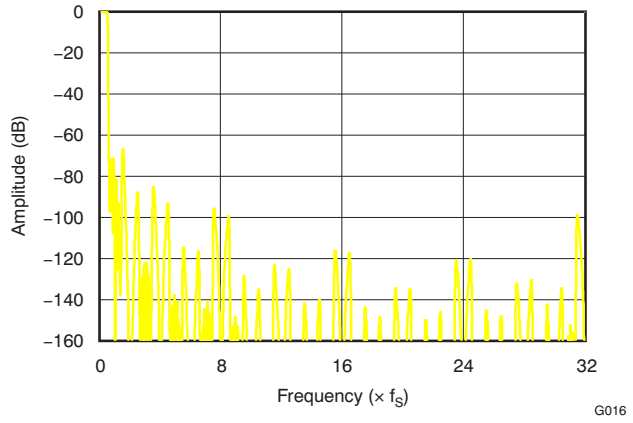


Figure 16.

STOP BAND ATTENUATION

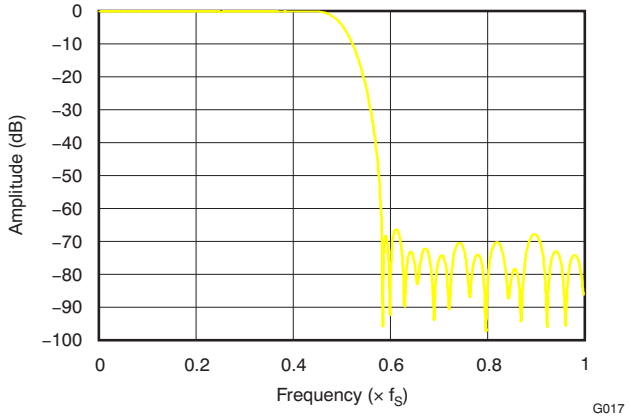


Figure 17.

PASSBAND RIPPLE

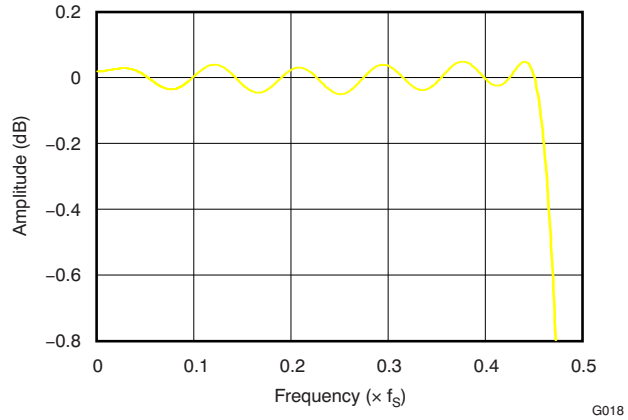


Figure 18.

TRANSITION-BAND RESPONSE

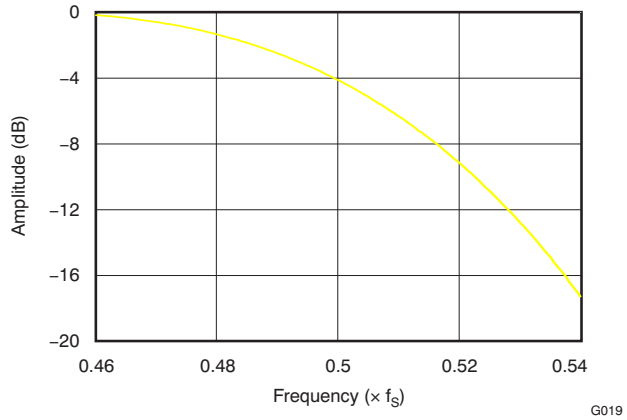


Figure 19.

TYPICAL CHARACTERISTICS: ADC DIGITAL HIGH-PASS FILTER FREQUENCY RESPONSE

All specifications at T_A = +25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{in} = 1 kHz, 16-bit data, unless otherwise noted.

STOP BAND CHARACTERISTICS

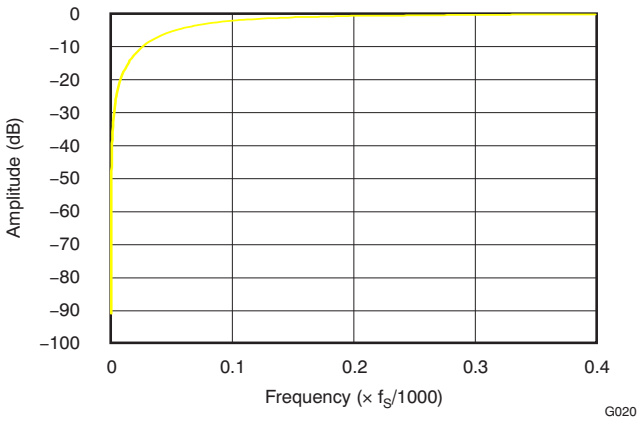


Figure 20.

PASSBAND CHARACTERISTICS

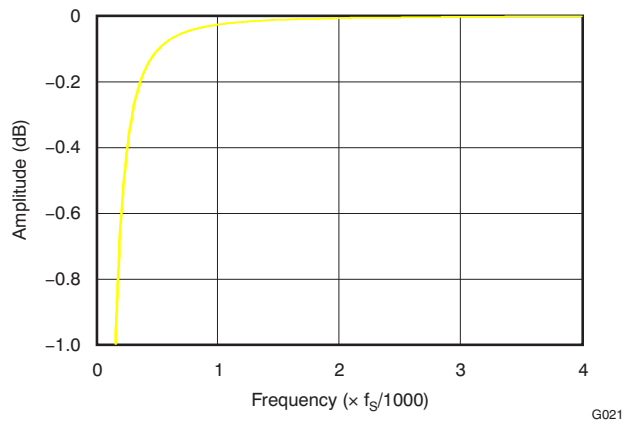


Figure 21.

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TYPICAL CHARACTERISTICS: ADC ANALOG ANTIALIASING FILTER FREQUENCY RESPONSE

All specifications at T_A = +25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{in} = 1 kHz, 16-bit data, unless otherwise noted.

STOP BAND CHARACTERISTICS

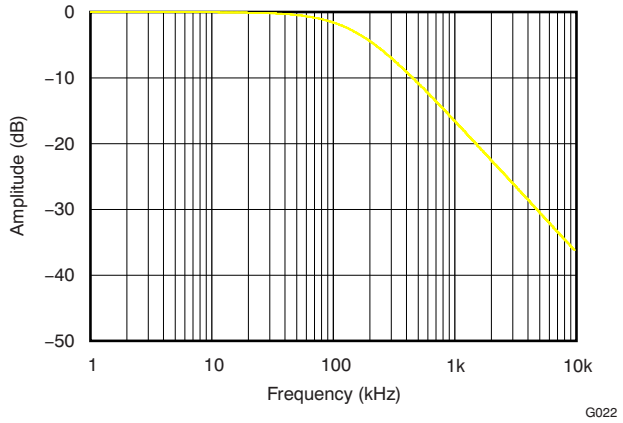


Figure 22.

PASSBAND CHARACTERISTICS

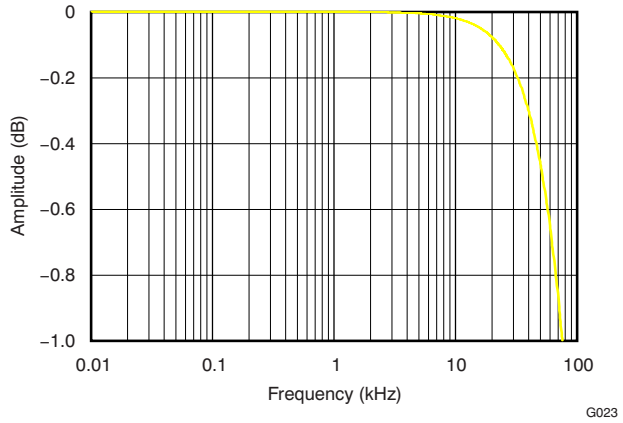


Figure 23.

TYPICAL CHARACTERISTICS: DAC DIGITAL INTERPOLATION FILTER FREQUENCY RESPONSE

All specifications at T_A = +25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{in} = 1 kHz, 16-bit data, unless otherwise noted.

STOP BAND ATTENUATION

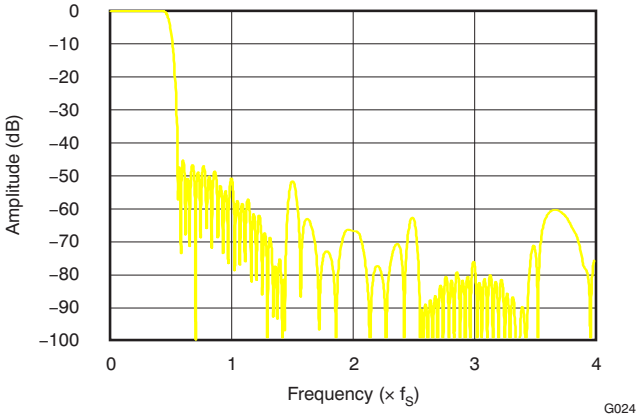


Figure 24.

PASSBAND RIPPLE

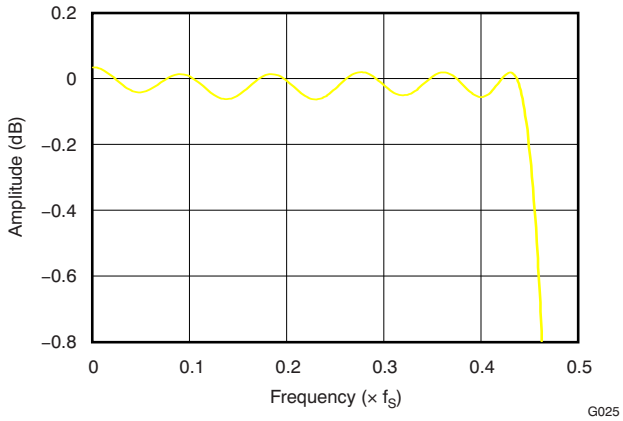


Figure 25.

TRANSITION-BAND RESPONSE

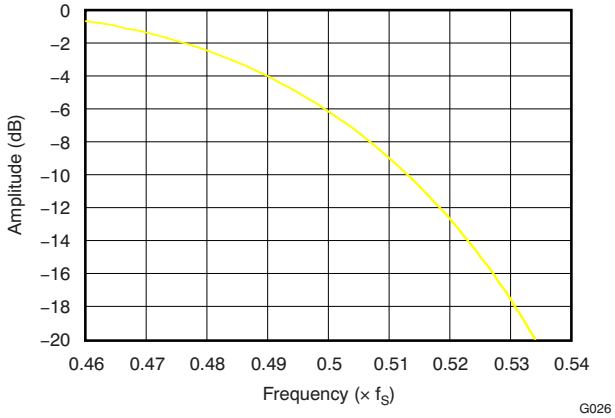


Figure 26.

TYPICAL CHARACTERISTICS: DAC ANALOG FIR FILTER FREQUENCY RESPONSE

All specifications at T_A = +25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{in} = 1 kHz, 16-bit data, unless otherwise noted.

STOP BAND CHARACTERISTICS

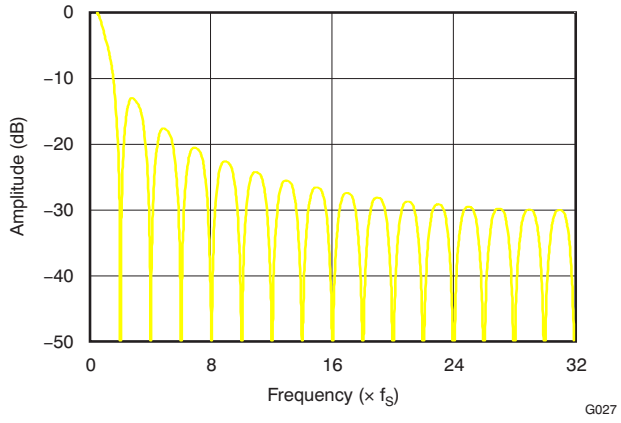


Figure 27.

PASSBAND CHARACTERISTICS

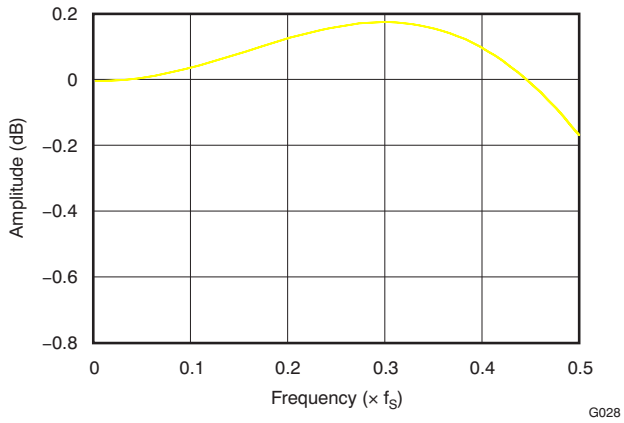


Figure 28.

TYPICAL CHARACTERISTICS: DAC ANALOG LOW-PASS FILTER FREQUENCY RESPONSE

All specifications at T_A = +25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{in} = 1 kHz, 16-bit data, unless otherwise noted.

STOP BAND CHARACTERISTICS

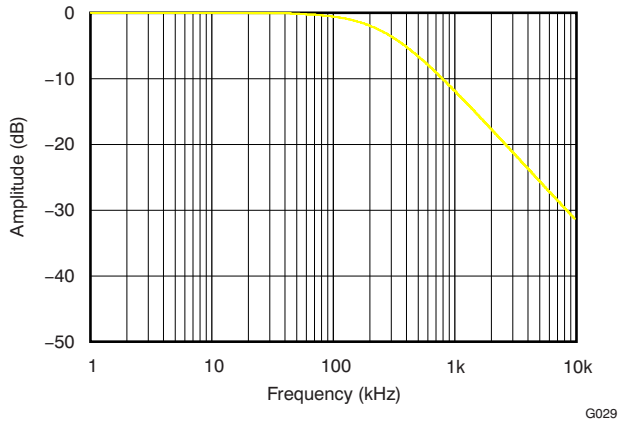


Figure 29.

PASSBAND CHARACTERISTICS

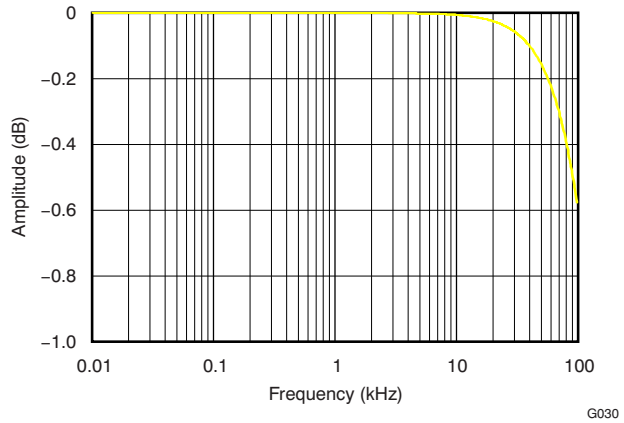


Figure 30.

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DETAILED DESCRIPTION

USB INTERFACE

Control data and audio data are transferred to the PCM2900C/2902C via D+ (pin 1) and D– (pin 2). All data to/from the PCM2900C/2902C are transferred at full speed. The device descriptor contains the information described in Table 3.

Table 3. Device Description

USB revision	2.0 compliant
Device class	0x00 (device-defined interface level)
Device subclass	0x00 (not specified)
Device protocol	0x00 (not specified)
Max packet size for end-point 0	8 bytes
Vendor ID	0x08BB
Product ID	0x29C0 / 0x29C2
Device release number	1.0 (0x0100)
Number of configurations	1
Vendor strings	String #1 (see Table 5)
Product strings	String #2 (see Table 5)
Serial number	Not supported

The configuration descriptor contains the information described in Table 4.

Table 4. Configuration Descriptor

Interface	Four interfaces
Power attribute	0x80 (Bus-powered, no remote wakeup)
Max power	0x32 (100 mA)

The string descriptor contains the information described in Table 5.

Table 5. String Descriptor

#0	0x0409
#1	BurrBrown from Texas Instruments
#2	USB AUDIO CODEC

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DEVICE CONFIGURATION

Figure 31 illustrates the USB audio function topology. The PCM2900C/2902C has four interfaces. Each interface consists of alternative settings.

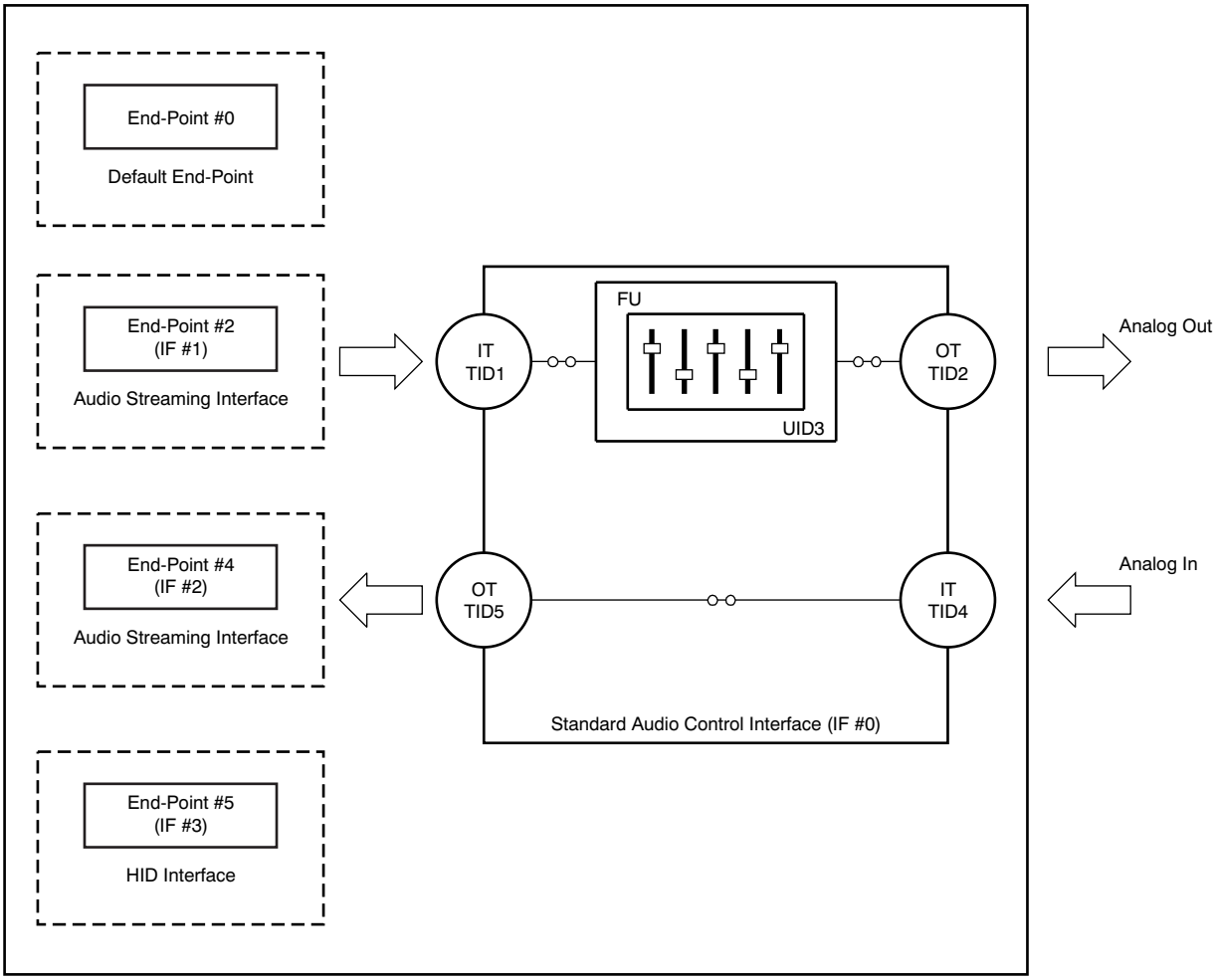


Figure 31. USB Audio Function Topology

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Interface #0

Interface #0 is defined as the control interface. Alternative setting #0 is the only possible setting for interface #0. Alternative setting #0 describes the standard audio control interface. The audio control interface consists of a single terminal. The PCM2900C/2902C has five terminals:

- Input terminal (IT #1) for isochronous-out stream
- Output terminal (OT #2) for audio analog output
- Feature unit (FU #3) for DAC digital attenuator
- Input terminal (IT #4) for audio analog input
- Output terminal (OT #5) for isochronous-in stream

Input terminal #1 is defined as a *USB stream* (terminal type 0x0101). Input terminal #1 can accept two-channel audio streams consisting of left and right channels. Output terminal #2 is defined as a *speaker* (terminal type 0x0301). Input terminal #4 is defined as a *line connector* (terminal type 0x0603). Output terminal #5 is defined as a *USB stream* (terminal type 0x0101). Output terminal #5 can generate two-channel audio streams composed of left and right channel data. Feature unit #3 supports the following sound control features:

- Volume control
- Mute control

The built-in digital volume controller can be manipulated by an audio class specific request from 0 dB to –64 dB in 1-dB steps. Changes are made by incrementing or decrementing by one step (1 dB) for every $1/f_S$ time interval until the volume level has reached the requested value. Each channel can be set for different values. The master volume control is not supported. A request to the master volume is stalled and ignored. The built-in digital mute controller can be manipulated by an audio class specific request. A master mute control request is acceptable. A request to an individual channel is stalled and ignored.

Interface #1

Interface #1 is the audio streaming data-out interface. Interface #1 has five alternative settings listed in Table 6. Alternative setting #0 is the zero bandwidth setting. All other alternative settings are operational settings.

Table 6. Interface #1 Alternative Settings

ALTERNATIVE SETTING	DATA FORMAT			TRANSFER MODE	SAMPLING RATE (kHz)
00	Zero Bandwidth				
01	16-bit	Stereo	Twos complement (PCM)	Adaptive	32, 44.1, 48
02	16-bit	Mono	Twos complement (PCM)	Adaptive	32, 44.1, 48
03	8-bit	Stereo	Twos complement (PCM)	Adaptive	32, 44.1, 48
04	8-bit	Mono	Twos complement (PCM)	Adaptive	32, 44.1, 48

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Interface #2

Interface #2 is the audio streaming data-in interface. Interface #2 has the 19 alternative settings listed in Table 7. Alternative setting #0 is the zero bandwidth setting. All other alternative settings are operational settings.

Table 7. Interface #2 Alternative Settings

ALTERNATIVE SETTING	DATA FORMAT			TRANSFER MODE	SAMPLING RATE (kHz)
00	Zero Bandwidth				
01	16-bit	Stereo	Twos complement (PCM)	Asynchronous	48
02	16-bit	Mono	Twos complement (PCM)	Asynchronous	48
03	16-bit	Stereo	Twos complement (PCM)	Asynchronous	44.1
04	16-bit	Mono	Twos complement (PCM)	Asynchronous	44.1
05	16-bit	Stereo	Twos complement (PCM)	Asynchronous	32
06	16-bit	Mono	Twos complement (PCM)	Asynchronous	32
07	16-bit	Stereo	Twos complement (PCM)	Asynchronous	22.05
08	16-bit	Mono	Twos complement (PCM)	Asynchronous	22.05
09	16-bit	Stereo	Twos complement (PCM)	Asynchronous	16
0A	16-bit	Mono	Twos complement (PCM)	Asynchronous	16
0B	8-bit	Stereo	Twos complement (PCM)	Asynchronous	16
0C	8-bit	Mono	Twos complement (PCM)	Asynchronous	16
0D	8-bit	Stereo	Twos complement (PCM)	Asynchronous	8
0E	8-bit	Mono	Twos complement (PCM)	Asynchronous	8
0F	16-bit	Stereo	Twos complement (PCM)	Synchronous	11.025
10	16-bit	Mono	Twos complement (PCM)	Synchronous	11.025
11	8-bit	Stereo	Twos complement (PCM)	Synchronous	11.025
12	8-bit	Mono	Twos complement (PCM)	Synchronous	11.025

Interface #3

Interface #3 is the interrupt data-in interface. Alternative setting #0 is the only possible setting for interface #3. Interface #3 consists of the HID consumer control device and reports the status of three key parameters:

- Mute (0xE209)
- Volume up (0xE909)
- Volume down (0xEA09)

End-Points

The PCM2900C/2902C has the following four end-points:

- Control end-point (EP #0)
- Isochronous-out audio data stream end-point (EP #2)
- Isochronous-in audio data stream end-point (EP #4)
- HID end-point (EP #5)

The control end-point is a default end-point. The control end-point is used to control all functions of the PCM2900C/2902C by a standard USB request and an USB audio class-specific request from the host. The isochronous-out audio data stream end-point is an audio sink end-point, which receives the PCM audio data. The isochronous-out audio data stream end-point accepts the adaptive transfer mode. The isochronous-in audio data stream end-point is an audio source end-point, which transmits the PCM audio data. The isochronous-in audio data stream end-point uses asynchronous transfer mode. The HID end-point is an interrupt-in end-point. HID end-point reports HID0, HID1, and HID2 pin status every 32 ms.

The human interface device (HID) pins are defined as consumer control devices. The HID function is designed as an independent end-point from both isochronous-in and -out end-points. Therefore, the result obtained from the HID operation depends on the host software. Typically, the HID function is used as the primary audio-out device.

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Clock and Reset

The PCM2900C/2902C requires a 12-MHz (±500 ppm) clock for the USB and audio functions, which can be generated by a built-in crystal oscillator with a 12-MHz crystal resonator. The 12-MHz crystal resonator must be connected to XTI (pin 21) and XTO (pin 20) with one high (1-MΩ) resistor and two small capacitors, the capacitance of which depends on the load capacitance of the crystal resonator. The external clock can be supplied from XTI (pin 21). If the external clock is supplied, XTO (pin 20) must be left open. Because there is no clock-disabling signal, it is not recommended to use the external clock supply. $\overline{\text{SSPND}}$ (pin 28) is unable to use clock disabling.

The PCM2900C/2902C has an internal power-on reset circuit, which triggers automatically when V_{BUS} (pin 3) exceeds 2.5 V typical (2.7 V to 2.2 V). Approximately 700 µs is required until internal reset release.

Digital Audio Interface (PCM2902C)

The PCM2902C employs both S/PDIF input and output. Isochronous-out data from the host are encoded to the S/PDIF output and the DAC analog output. Input data are selected as either S/PDIF or ADC analog input. When the device detects an S/PDIF input and successfully locks the received data, the isochronous-in transfer data source is automatically selected from S/PDIF itself; otherwise, the data source is selected to ADC analog input.

This feature is a customer option. It is the responsibility of the user to implement this feature.

Supported Input/Output Data (PCM2902C)

The following data formats are accepted by the S/PDIF input and output. All other data formats are unable to use S/PDIF.

- 48-kHz 16-bit stereo
- 44.1-kHz 16-bit stereo
- 32-kHz 16-bit stereo

Any mismatch of the sampling rate between the input S/PDIF signal and the host command is not acceptable. Any mismatch of the data format between the input S/PDIF signal and the host command may cause unexpected results, with the following exceptions:

- Recording in monaural format from stereo data input at the same data rate
- Recording in 8-bit format from 16-bit data input at the same data rate

A combination of these two conditions is not acceptable.

For playback, all possible data rate sources are converted to 16-bit stereo format at the same source data rate.

Channel Status Information (PCM2902C)

The channel status information is fixed as consumer application, PCM mode, copyright, and digital/digital converter. All other bits are fixed as 0s except for the sample frequency, which is set automatically according to the data received through the USB.

Copyright Management (PCM2902C)

Isochronous-in data are affected by the serial copy management system (SCMS). When receiving digital audio data that are indicated as original data in the control bit, input digital audio data transfer to the host. If the data are indicated as first generation or higher, the transferred data are routed to the analog input.

Digital audio data output is always encoded as original with SCMS control.

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INTERFACE SEQUENCE

Power On, Attach, and Playback Sequence

The PCM2900C/2902C is ready for setup when the reset sequence has finished and the USB bus is attached. After connection has been established by setup, the PCM2900C/2902C is ready to accept USB audio data. While waiting, the audio data (idle state) and analog output are set to bipolar zero (BPZ).

When receiving the audio data, the PCM2900C/2902C stores the first audio packet, which contains 1-ms audio data, into the internal storage buffer. The PCM2900C/2902C starts to play the audio data when detecting the next start of frame (SOF) packet, as illustrated in Figure 32.

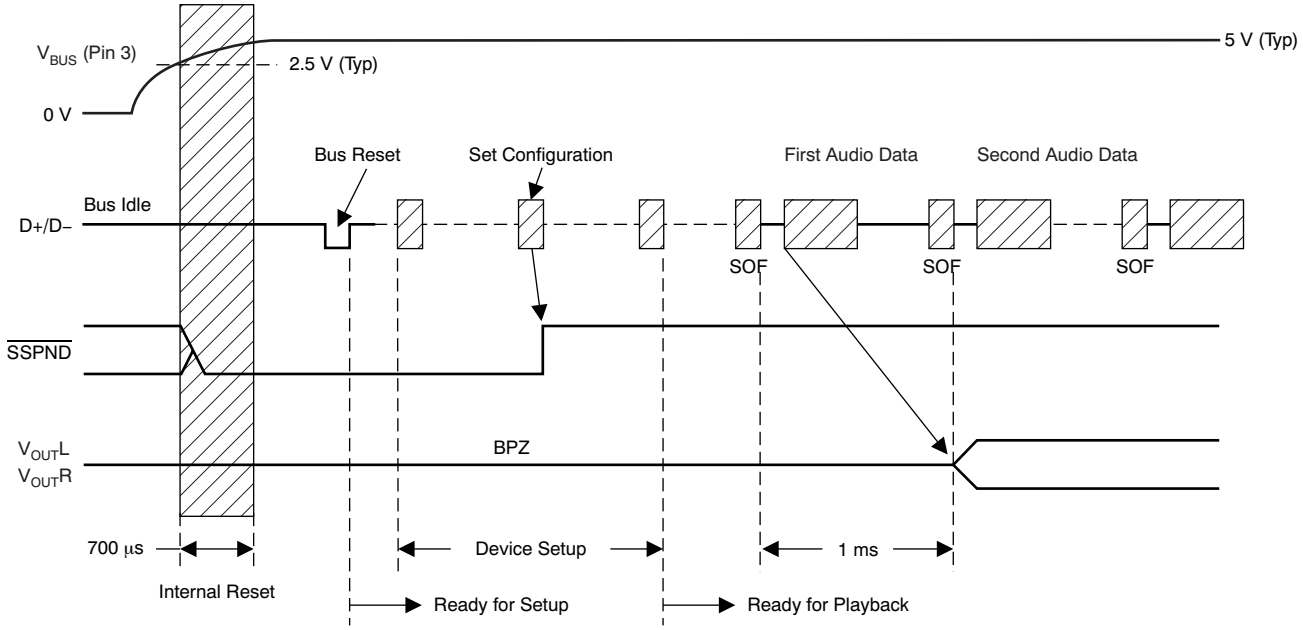


Figure 32. Initial Sequence

Play, Stop, and Detach Sequence

When the host finishes or aborts playback, the PCM2900C/2902C stops playing after the last audio data have played, as shown in Figure 33.

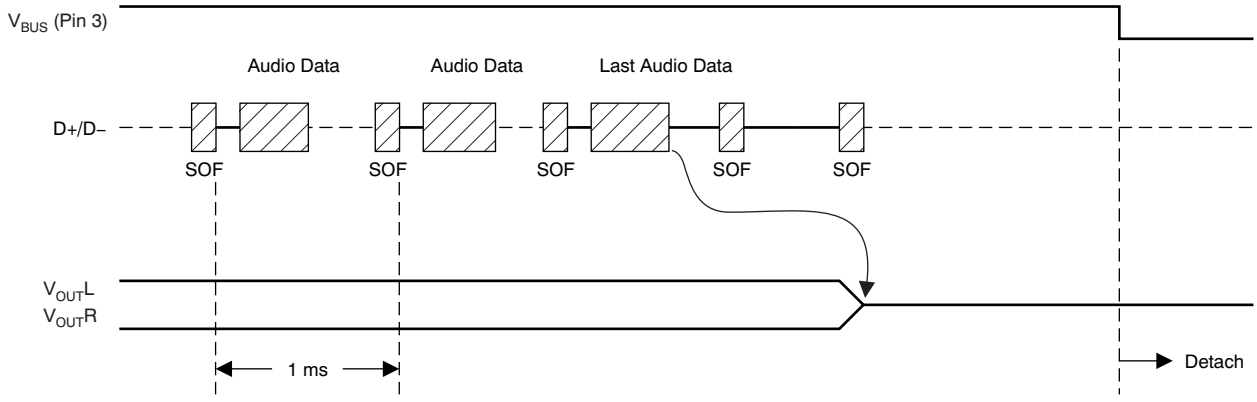


Figure 33. Play, Stop, and Detach Sequence

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Record Sequence

The PCM2900C/2902C starts the audio capture into the internal memory after receiving the SET_INTERFACE command, as shown in Figure 34.

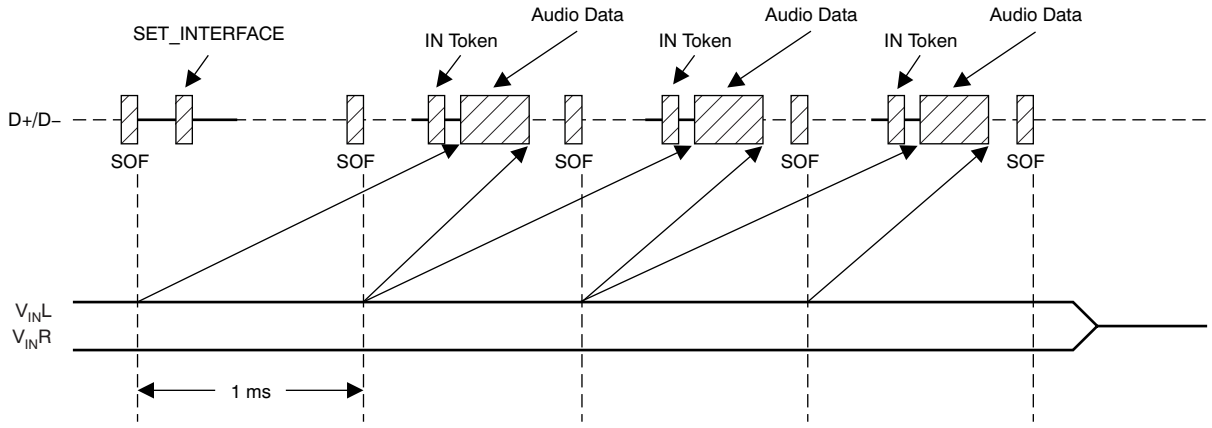


Figure 34. Record Sequence

Suspend and Resume Sequence

The PCM2900C/2902C enters the suspend state after it sees a constant idle state on the USB bus (approximately 5 ms), as shown in Figure 35. While the PCM2900C/2902C enters the suspend state, $\overline{\text{SSPND}}$ flag (pin 28) is asserted. The PCM2900C/2902C wakes up immediately upon detecting a non-idle state on the USB bus.

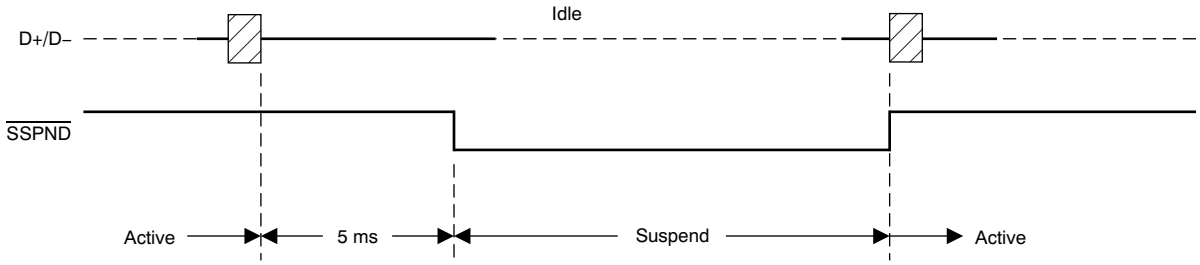


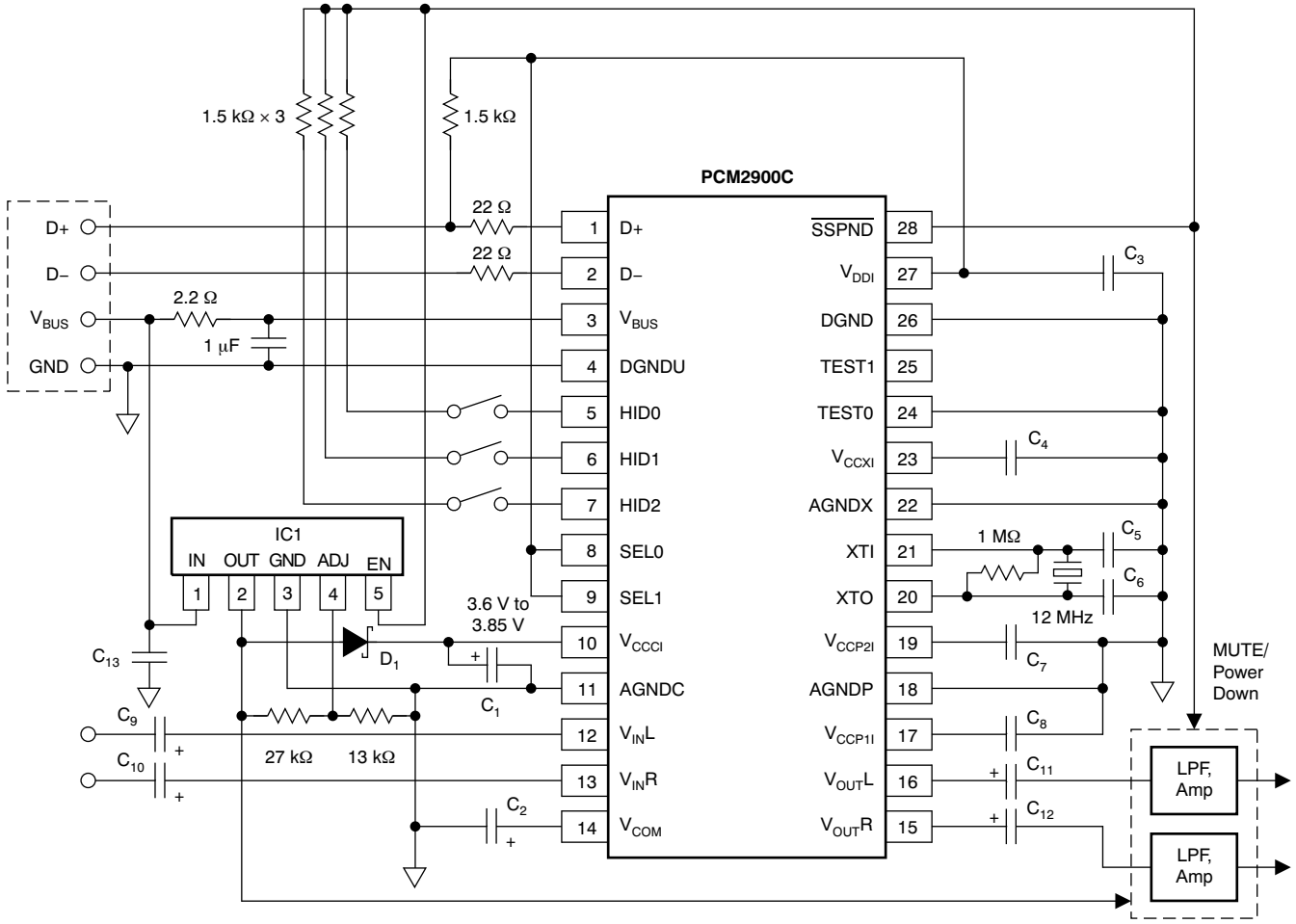
Figure 35. Suspend and Resume Sequence

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APPLICATION INFORMATION

PCM2900C TYPICAL CIRCUIT CONNECTION 1

Figure 36 illustrates a typical circuit connection for a high-performance application. The circuit illustrated is for information only. The entire board design should be considered to meet the USB specification as a USB-compliant product.



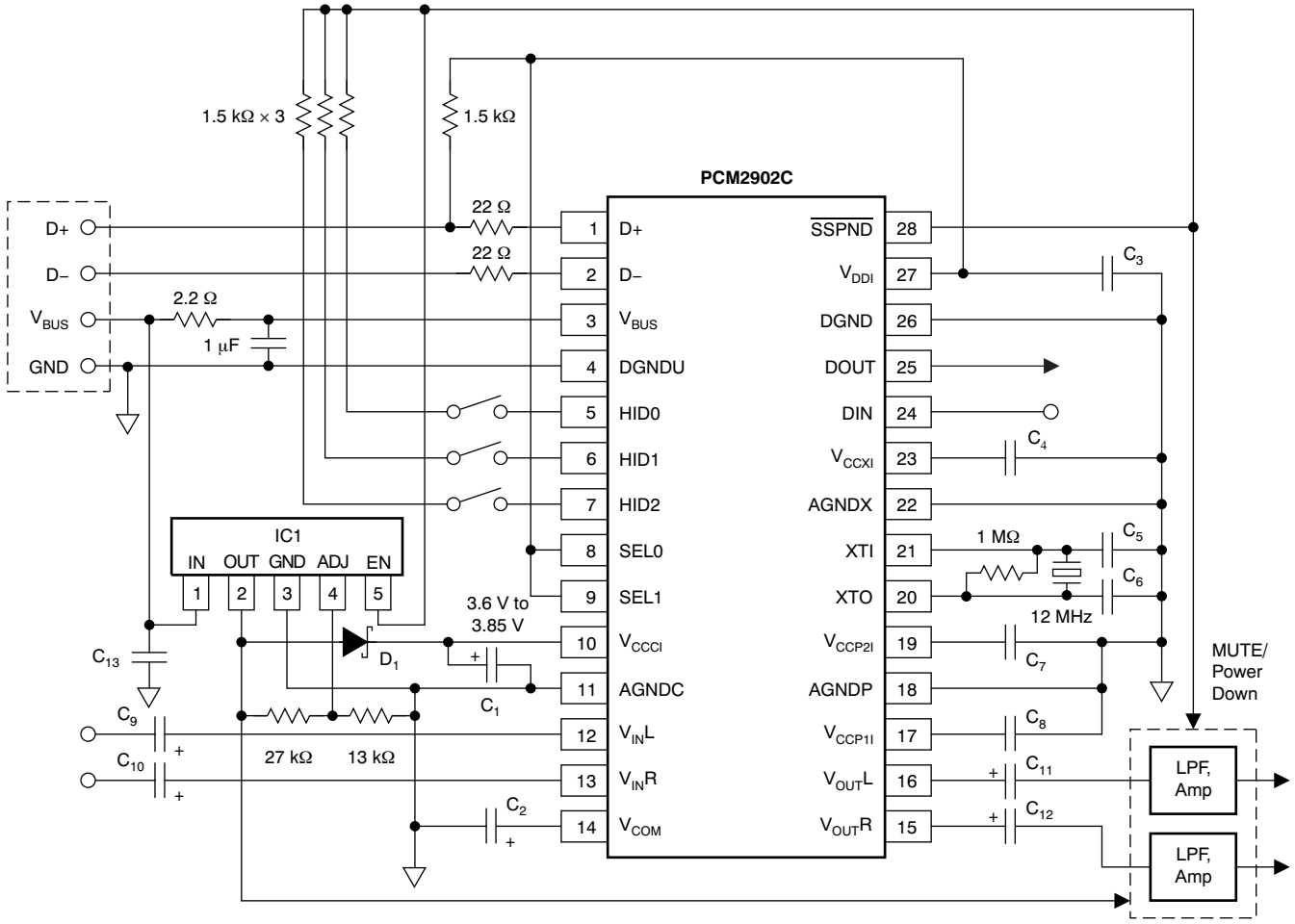
NOTE: C_1, C_2: 10 µF
C_3, C_4, C_7, C_8, C_{13}: 1 µF (These capacitors must be less than 2 µF.)
C_5, C_6: 10 pF to 33 pF (depending on crystal resonator)
C_9, C_{10}, C_{11}, C_{12}: The capacitance may vary depending on design.
IC1: REG103xA-A (TI) or equivalent. Analog performance may vary depending on IC1.
D_1: Schottky barrier diode (V_F ≤ 350 mV at 10 mA, I_R ≤ 2 µA at 4 V)

Figure 36. Bus-Powered Configuration for High-Performance Application

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PCM2902C TYPICAL CIRCUIT CONNECTION 1

Figure 37 illustrates a typical circuit connection for a high-performance application. The circuit illustrated is for information only. The entire board design should be considered to meet the USB specification as a USB-compliant product.



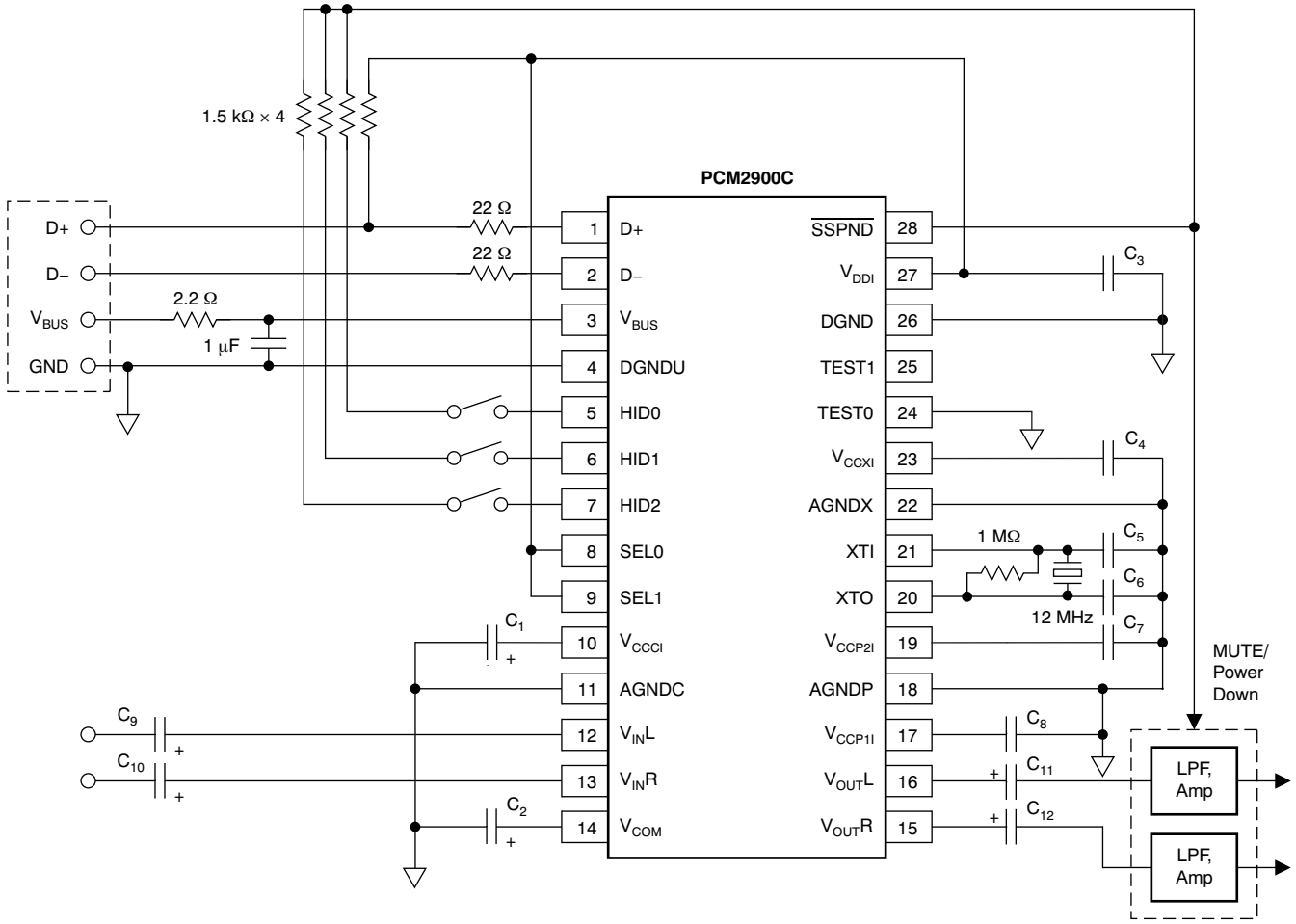
NOTE: C_1, C_2: 10 µF
C_3, C_4, C_7, C_8, C_{13}: 1 µF (These capacitors must be less than 2 µF.)
C_5, C_6: 10 pF to 33 pF (depending on crystal resonator)
C_9, C_{10}, C_{11}, C_{12}: The capacitance may vary depending on design.
IC1: REG103xA-A (TI) or equivalent. Analog performance may vary depending on IC1.
D_1: Schottky barrier diode (V_F ≤ 350 mV at 10 mA, I_R ≤ 2 µA at 4 V)

Figure 37. Bus-Powered Configuration for High-Performance Application

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PCM2900C TYPICAL CIRCUIT CONNECTION 2

Figure 38 illustrates a typical circuit connection for a simple application. The circuit illustrated is for information only. The entire board design should be considered to meet the USB specification as a USB-compliant product.



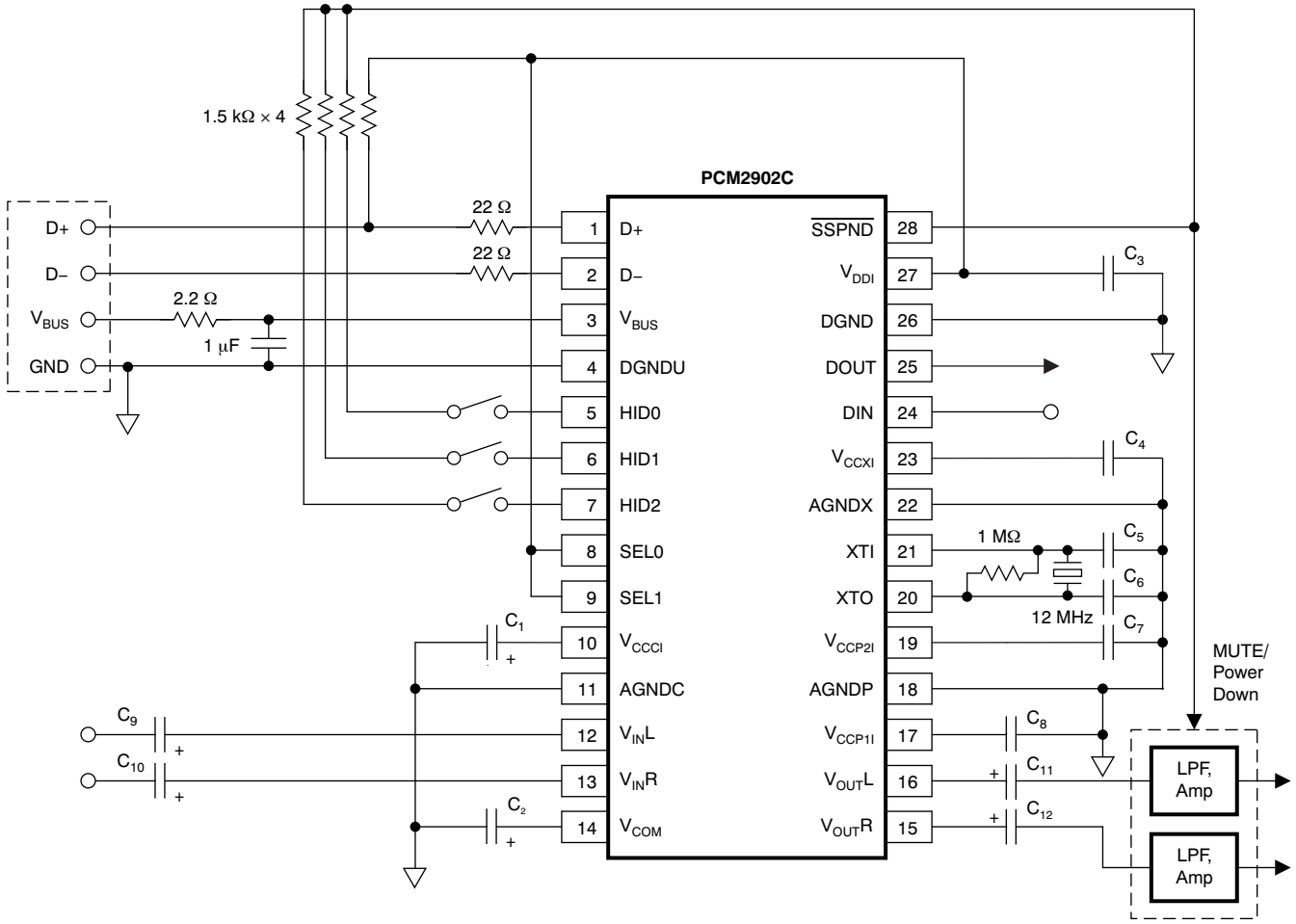
NOTE: C_1, C_2: 10 µF
C_3, C_4, C_7, C_8: 1 µF (These capacitors must be less than 2 µF.)
C_5, C_6: 10 pF to 33 pF (depending on crystal resonator)
C_9, C_{10}, C_{11}, C_{12}: The capacitance may vary depending on design.
In this case, the analog performance of the ADC may be degraded.

Figure 38. Bus-Powered Configuration

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PCM2902C TYPICAL CIRCUIT CONNECTION 2

Figure 39 illustrates a typical circuit connection for a simple application. The circuit illustrated is for information only. The entire board design should be considered to meet the USB specification as a USB-compliant product.



NOTE: C_1, C_2: 10 µF
C_3, C_4, C_7, C_8: 1 µF (These capacitors must be less than 2 µF.)
C_5, C_6: 10 pF to 33 pF (depending on crystal resonator)
C_9, C_{10}, C_{11}, C_{12}: The capacitance may vary depending on design.
In this case, the analog performance of the ADC may be degraded.

Figure 39. Bus-Powered Configuration

OPERATING ENVIRONMENT

For current information on the PCM2900C/2902C operating environment, see the application report, *Updated Operating Environments for PCM270X, PCM290X Applications* (SLAA374), available for download from the TI website.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PCM2900CDB	Active	Production	SSOP (DB) | 28	50 | TUBE	Yes	Call TI | Nipdau	Level-1-260C-UNLIM	-25 to 85	PCM2900C
PCM2900CDB.B	Active	Production	SSOP (DB) | 28	50 | TUBE	Yes	Call TI	Level-1-260C-UNLIM	-25 to 85	PCM2900C
PCM2900CDBR	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM2900C
PCM2900CDBR.B	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM2900C
PCM2900CDBRG4	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM2900C
PCM2900CDBRG4.B	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM2900C
PCM2902CDB	Active	Production	SSOP (DB) | 28	50 | TUBE	Yes	Call TI | Nipdau	Level-1-260C-UNLIM	-25 to 85	PCM2902C
PCM2902CDB.B	Active	Production	SSOP (DB) | 28	50 | TUBE	Yes	Call TI	Level-1-260C-UNLIM	-25 to 85	PCM2902C
PCM2902CDBR	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	Call TI | Nipdau	Level-1-260C-UNLIM	-25 to 85	PCM2902C
PCM2902CDBR.B	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	Call TI	Level-1-260C-UNLIM	-25 to 85	PCM2902C
PCM2902CDBRG4	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM2902C
PCM2902CDBRG4.B	Active	Production	SSOP (DB) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM2902C

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

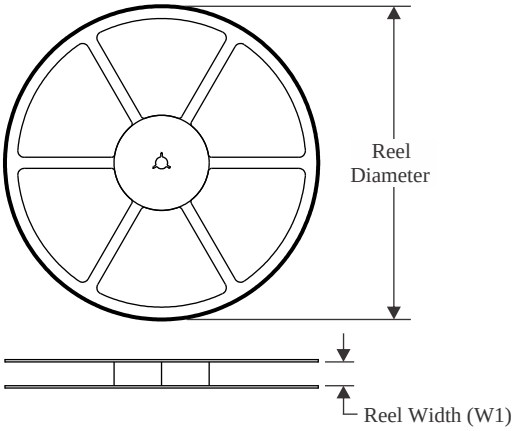
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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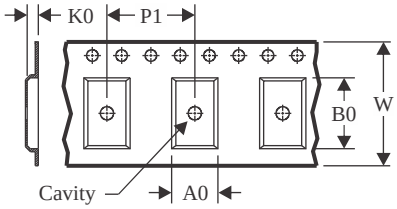
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

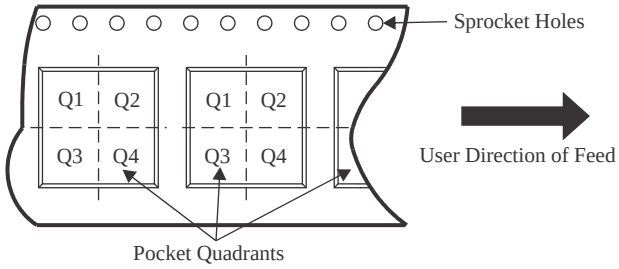


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

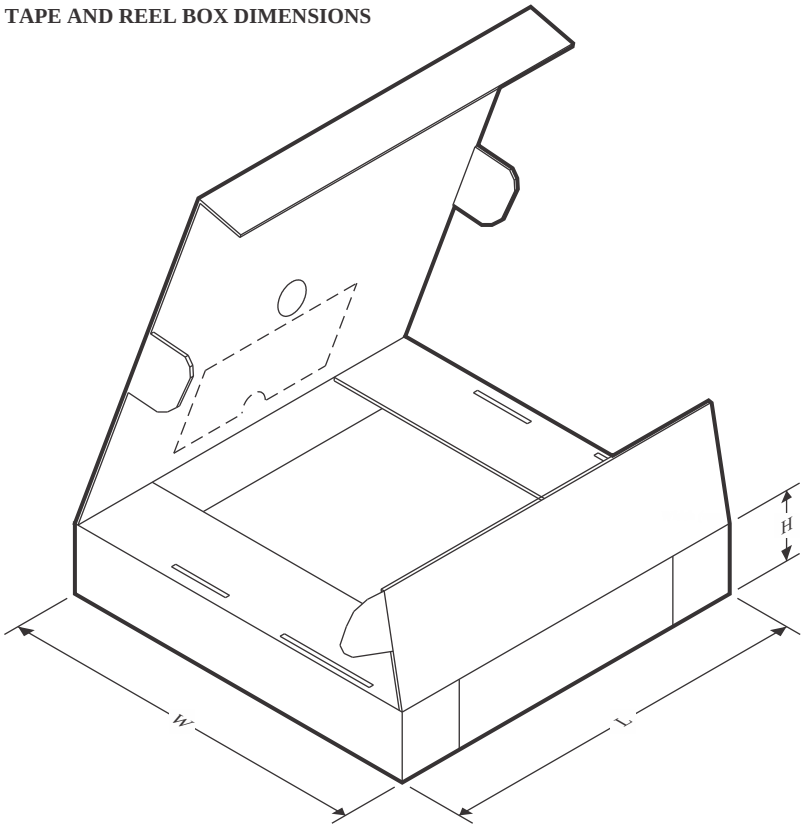
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCM2900CDBR	SSOP	DB	28	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
PCM2900CDBRG4	SSOP	DB	28	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
PCM2902CDBRG4	SSOP	DB	28	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1

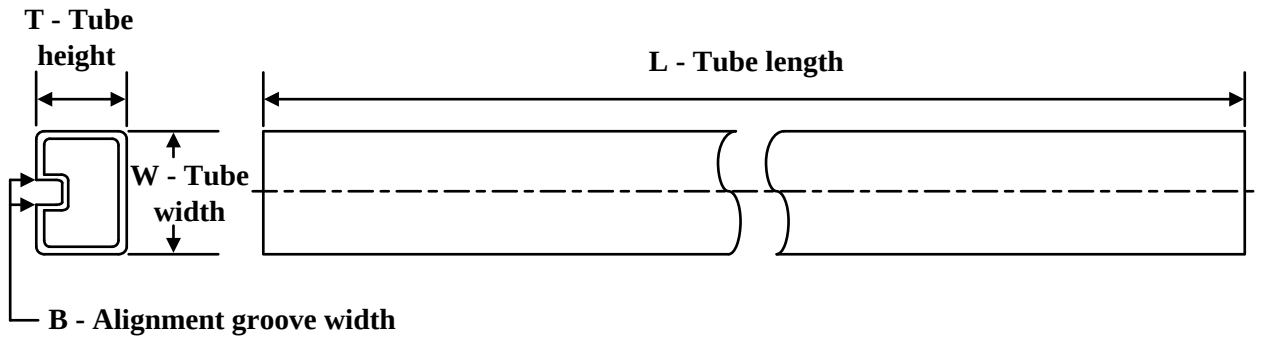
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCM2900CDBR	SSOP	DB	28	2000	353.0	353.0	32.0
PCM2900CDBRG4	SSOP	DB	28	2000	353.0	353.0	32.0
PCM2902CDBRG4	SSOP	DB	28	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

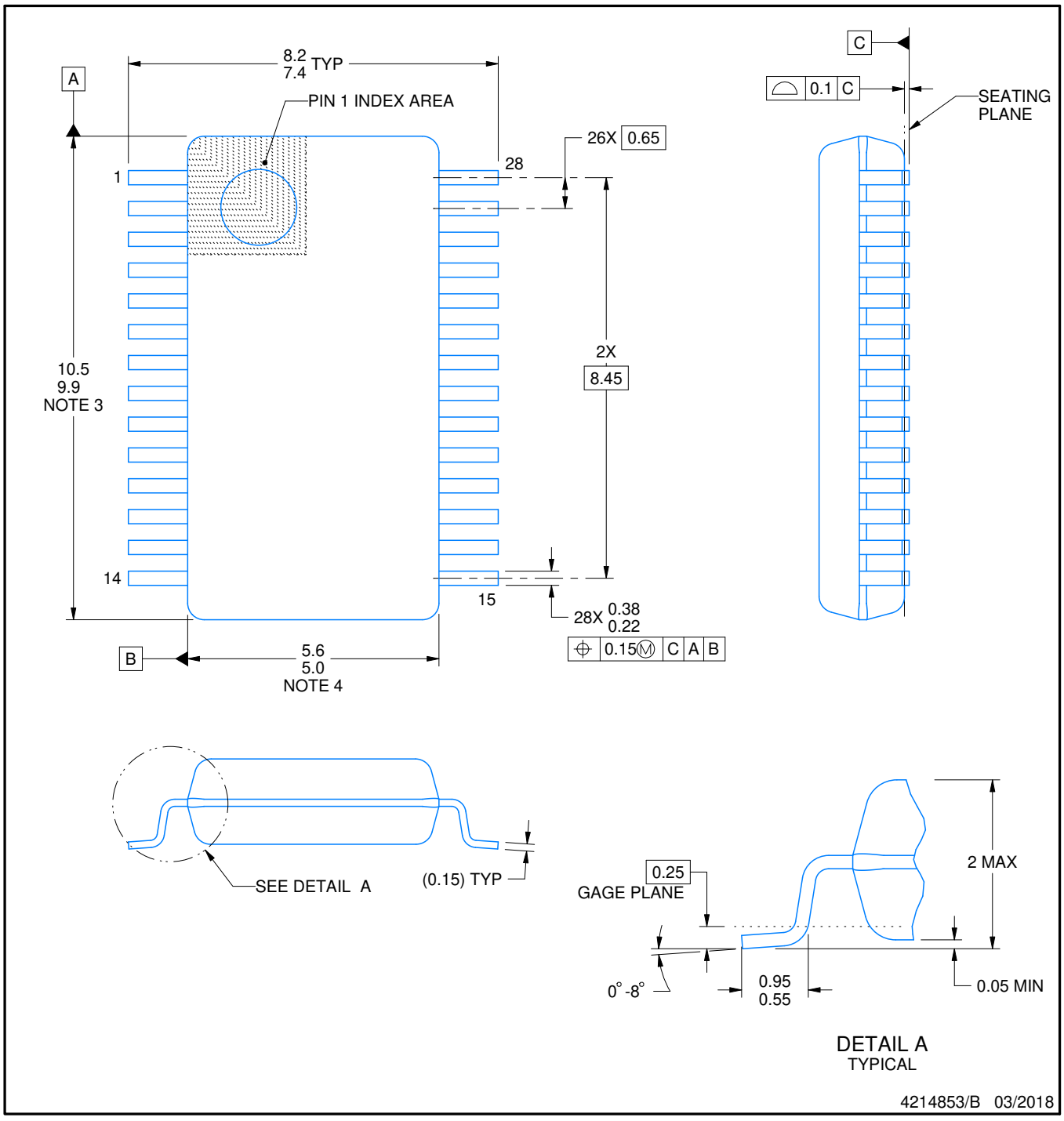
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
PCM2900CDB	DB	SSOP	28	50	530	10.5	4000	4.1
PCM2900CDB	DB	SSOP	28	50	530	10.5	4000	4.1
PCM2900CDB.B	DB	SSOP	28	50	530	10.5	4000	4.1
PCM2900CDB.B	DB	SSOP	28	50	530	10.5	4000	4.1
PCM2902CDB	DB	SSOP	28	50	530	10.5	4000	4.1
PCM2902CDB	DB	SSOP	28	50	530	10.5	4000	4.1
PCM2902CDB.B	DB	SSOP	28	50	530	10.5	4000	4.1
PCM2902CDB.B	DB	SSOP	28	50	530	10.5	4000	4.1

PACKAGE OUTLINE

DB0028A

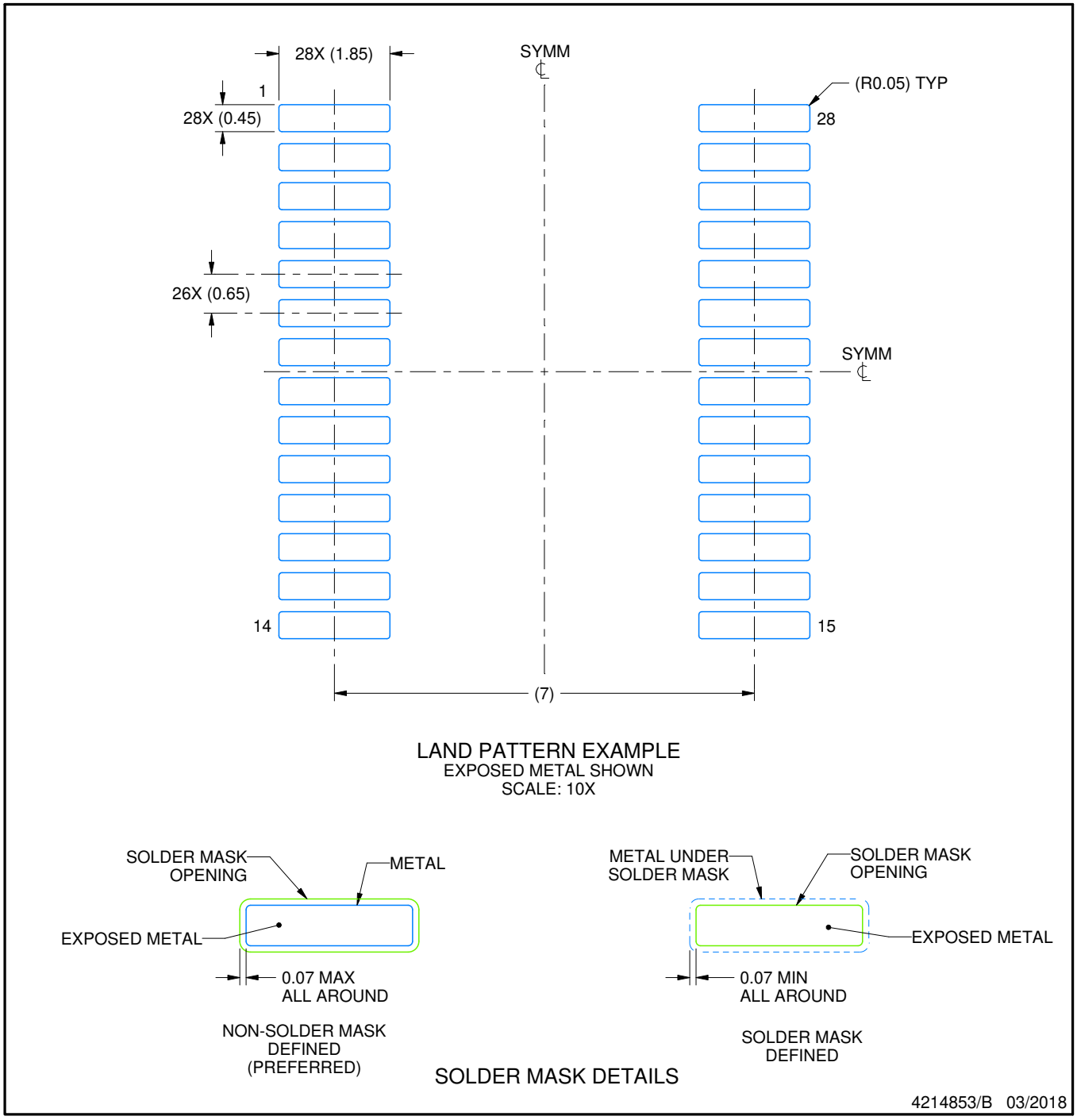
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



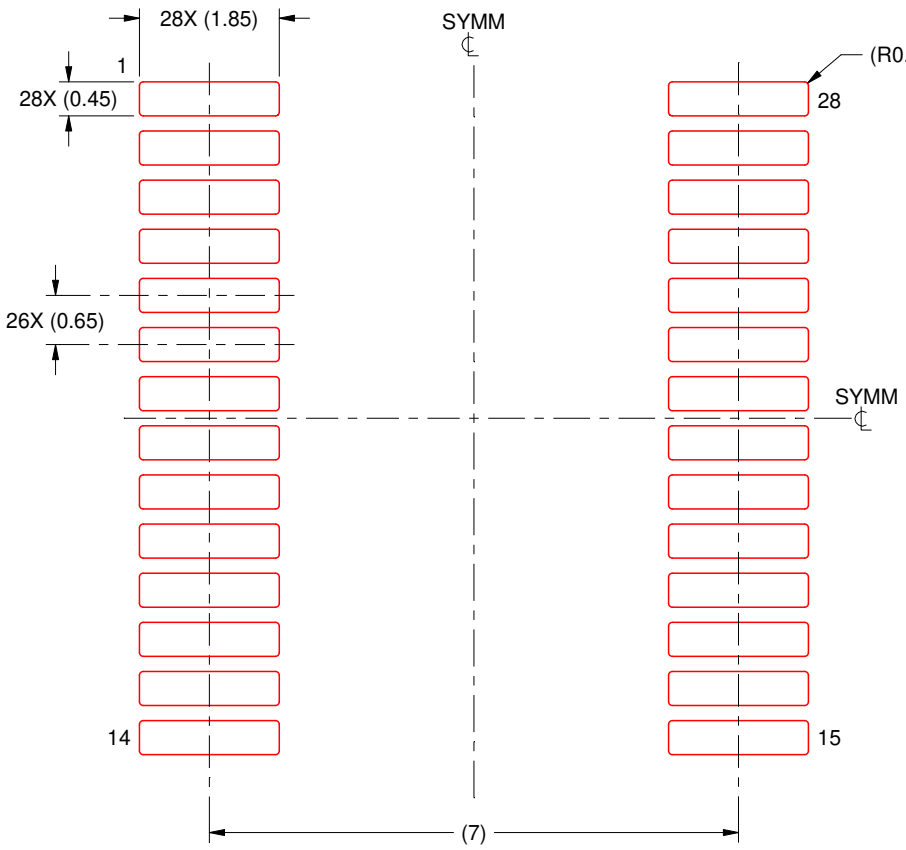
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214853/B 03/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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