BURR-BROWN®




# PCM3500

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# Low Voltage, Low Power, 16-Bit, Mono SoundPLUS™ VOICE/MODEM CODEC

## FEATURES

- 16-BIT DELTA-SIGMA DAC AND ADC
- DESIGNED FOR MODEM ANALOG FRONT END: Supports up to 56kbps Operation
- ANALOG PERFORMANCE: Sampling Frequency: 7.2kHz to 26kHz Dynamic Range: 88dB (typ) at $f_S$ = 8kHz, $f_{IN}$ = 1kHz
- SYSTEM CLOCK: 512$f_S$
- MASTER OR SLAVE OPERATION
- ON-CHIP CRYSTAL OSCILLATOR CIRCUIT
- ADC-TO-DAC LOOP-BACK MODE
- TIME SLOT MODE SUPPORTS UP TO FOUR CODECs ON A SINGLE SERIAL INTERFACE
- POWER-DOWN MODE: 60μA (typ)
- POWER SUPPLY: Single +2.7V to +3.6V
- SMALL PACKAGE: SSOP-24

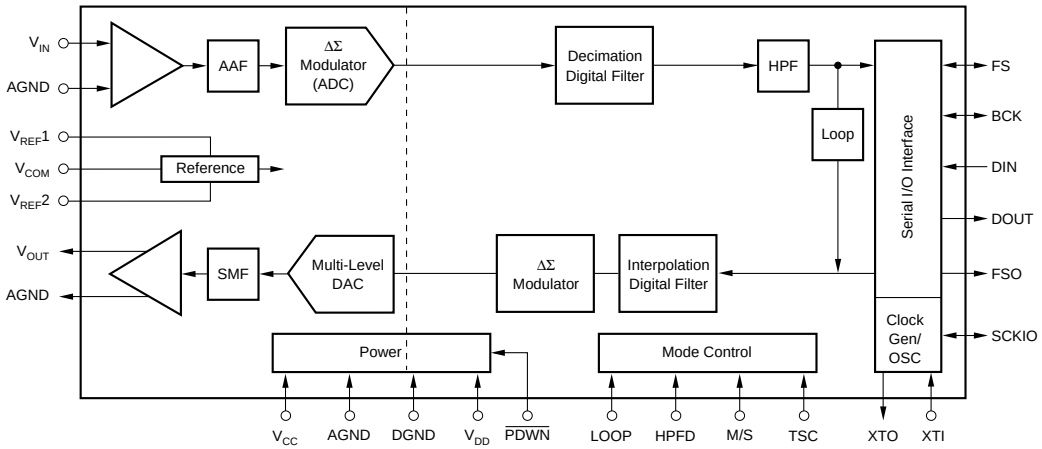
## APPLICATIONS

- SOFTWARE MODEMS FOR: Personal Digital Assistant Notebook and Hand-Held PCs Set-Top Box Digital Television Embedded Systems
- PORTABLE VOICE RECORDER/PLAYER
- SPEECH RECOGNITION/SYNTHESIS
- TELECONFERENCING PRODUCTS

## DESCRIPTION

The PCM3500 is a low cost, 16-bit CODEC designed for modem Analog Front End (AFE) and speech processing applications. The PCM3500's low power operation from +2.7V to +3.6V power supplies, along with an integrated power-down mode, make it ideal for portable applications.

The PCM3500 integrates all of the functions needed for a modem or voice CODEC, including delta-sigma digital-to-analog and analog-to-digital converters, input anti-aliasing filter, digital high-pass filter for DC blocking, and an output low-pass filter. The synchronous serial interface provides for a simple, or glue-free interface to popular DSP and RISC processors. The serial interface also supports Time Division Multiplexing (TDM), allowing up to four CODECs to share a single 4-wire serial bus.




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# SPECIFICATIONS

All specifications at +25°C, $V_{DD}$ = $V_{CC}$ = 3.3V, $f_S$ = 8kHz, and nominal system clock (XTI) = 512$f_S$, unless otherwise noted. Measurement band is 100Hz to 0.425$f_S$.

| PARAMETER | CONDITIONS | PCM3500E MIN | PCM3500E TYP | PCM3500E MAX | UNITS |
|---|---|---|---|---|---|
| **RESOLUTION** | | | 16 | | Bits |
| **DATA FORMAT** | | | | | |
| Serial Data Interface Format | | | DSP Format | | |
| Serial Data Bit Length | | | 16 | | Bits |
| Serial Data Format | | | MSB-First, Binary Two's Complement | | |
| Sampling Frequency, $f_S$ | ADC and DAC | 7.2 | 8 | 26 | kHz |
| System Clock Frequency, 512$f_S$ | | 3.686 | 4.096 | 13.312 | MHz |
| **DIGITAL INPUT/OUTPUT** | | | | | |
| Logic Family | | | CMOS | | |
| Input Logic Level: $V_{IH}$(1) | | 0.7 • $V_{DD}$ | | | VDC |
| $V_{IL}$(1) | | | | 0.3 • $V_{DD}$ | VDC |
| Input Logic Current: $I_{IN}$(2) | | | | ±1 | µA |
| $I_{IN}$(3) | | | | 100 | µA |
| Output Logic Level: $V_{OH}$(4) | $I_{OUT}$ = –1mA | $V_{DD}$ – 0.3 | | | VDC |
| $V_{OL}$(4) | $I_{OUT}$ = +1mA | | | 0.3 | VDC |
| **ADC CHARACTERISTICS** | | | | | |
| **DC ACCURACY** | | | | | |
| Input Voltage | | | 0.6 $V_{CC}$ | | Vp-p |
| Gain Error | | | ±2 | ±5 | % of FSR |
| Offset Error | High-Pass Filter Disabled | | ±2 | | % of FSR |
| Input Resistance | | | 50 | | kΩ |
| **AC ACCURACY** | | | | | |
| THD+N | $f_{IN}$ = 1kHz, $V_{IN}$ = –0.5dB | | –85 | –80 | dB |
| Dynamic Range | Without A-Weighting | 82 | 88 | | dB |
| Signal-to-Noise Ratio | Without A-Weighting | 82 | 88 | | dB |
| Crosstalk | DAC Channel Idle, 0dB Input | 80 | 85 | | dB |
| Passband Ripple (internal HPF enabled) | 0.0002$f_S$ to 0.425$f_S$ | | ±0.05 | | dB |
| Passband Ripple (internal HPF disabled) | 0$f_S$ to 0.425$f_S$ | | ±0.05 | | dB |
| Roll-Off at 0.00002$f_S$ | High-Pass Filter Enabled | | –3 | | dB |
| Roll-Off at 0.56$f_S$ | High-Pass Filter Enabled | | –30 | | dB |
| Stopband Rejection | 0.58$f_S$ to $f_S$ | | –65 | | dB |
| Group Delay | | | 18/$f_S$ | 4m | sec |
| **DAC CHARACTERISTICS** | | | | | |
| **DC ACCURACY** | | | | | |
| Output Voltage | | | 0.6 $V_{CC}$ | | Vp-p |
| Gain Error | | | ±1 | ±5 | % of FSR |
| Offset Error | High Pass Filter Disabled | | ±1 | | % of FSR |
| Load Resistance | | 10 | | | kΩ |
| **AC ACCURACY** | | | | | |
| THD+N | $f_{IN}$ = 1kHz, $V_{OUT}$ = 0dB | | –90 | –82 | dB |
| Dynamic Range | Without A-Weighted | 84 | 92 | | dB |
| Signal-to-Noise Ratio | Without A-Weighted | 84 | 92 | | dB |
| Crosstalk | ADC Channel Idle, 0dB Input | 84 | 92 | | dB |
| Passband Ripple | 0$f_S$ to 0.425$f_S$ | | ±0.4 | | dB |
| Group Delay | | | 12/$f_S$ | 4m | sec |
| **POWER SUPPLY REQUIREMENTS** | | | | | |
| Voltage Range | $V_{CC}$, $V_{DD}$ | 2.7 | 3.3 | 3.6 | VDC |
| Supply Current, $I_{CC}$ + $I_{DD}$ | $V_{CC}$ = 3.3V | | 9 | 12 | mA |
| Total Supply Current in Power-Down Mode | $V_{CC}$ = $V_{DD}$ = 3.3V, XTI Stopped | | 60 | | µA |
| Total Power Dissipation | $V_{CC}$ = $V_{DD}$ = 3.3V | | 30 | 40 | mW |
| **TEMPERATURE RANGE** | | | | | |
| Operating | | –25 | | +85 | °C |
| Storage | | –55 | | +125 | °C |
| Thermal Resistance, $\Theta_{JA}$ | | | 100 | | °C/W |

NOTES: (1) Pins 6, 7, 8, 9, 10, 15, 17, 18, 19, 20 (M/S, TSC, BCK, FS, DIN, SCKIO, XTI, HPFD, LOOP, $\overline{\text{PDWN}}$). (2) Pins 8, 9, 10, 15, 17 (BCK, FS, DIN, SCKIO (Schmitt-Trigger input) XTI. (3) Pins 6, 7, 18, 19, 20 (M/S, TSC, HPFD, LOOP, $\overline{\text{PDWN}}$; Schmitt-Trigger input with internal pull-down). (4) Pins 8, 9, 11, 12, 15, 16 (BCK, FS, DOUT, FSO, SCKIO, XTO).

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage, $+V_{DD}$, $+V_{CC}$ | +6.5V |
| Supply Voltage Differences | ±0.1V |
| GND Voltage Differences | ±0.1V |
| Digital Input Voltage | –0.3V to $V_{DD}$ + 0.3V |
| Input Current (any pins except supply) | ±10mA |
| Power Dissipation | 300mW |
| Operating Temperature Range | –25°C to +85°C |
| Storage Temperature | –55°C to +125°C |
| Junction Temperature | 150°C |
| Lead Temperature (soldering, 5s) | +260°C |
| (reflow, 10s) | +235°C |

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER | SPECIFIED TEMPERATURE RANGE | PACKAGE MARKING | ORDERING NUMBER(1) | TRANSPORT MEDIA |
|---|---|---|---|---|---|---|
| PCM3500E | 24-Lead SSOP | 338 | –25°C to +85°C | PCM3500E | PCM3500E | Rails |
| " | " | " | " | " | PCM3500E/2K | Tape and Reel |

NOTES: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K indicates 2000 devices per reel). Ordering 2,000 pieces of "PCM3500E/2K" will get a single 2000-piece Tape and Reel.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

## PIN CONFIGURATION

**Top View** **SSOP**




## PIN ASSIGNMENTS

| PIN | NAME | I/O | DESCRIPTION |
|---|---|---|---|
| 1 | $V_{COM}$ | OUT | Common-Mode Voltage ($0.5V_{CC}$). This pin should be connected to ground through a capacitor. |
| 2 | $V_{REF}1$ | — | Decouple Pin for Reference Voltage 1 ($0.99V_{CC}$). This pin should be connected to ground through a capacitor. |
| 3 | $V_{REF}2$ | — | Decouple Pin for Reference Voltage 2 ($0.2V_{CC}$). This pin should be connected to ground through a capacitor. |
| 4 | $V_{IN}$ | IN | Analog Input for the ADC. |
| 5 | AGND | — | Analog Ground for the ADC Input Signal. |
| 6 | M/S | IN | Master/Slave Select. This pin is used to determine the operating mode for the serial interface. A logic '0' on this pin selects the Slave Mode. A logic '1' on this pin selects the Master Mode.(2) |
| 7 | TSC | IN | Time Slot Mode Control. This pin is used to select the time slot operating mode. A logic '0' on this pin disables Time Slot Mode. A logic '1' on this pin enables Time Slot Mode.(2) |
| 8 | BCK | I/O | Bit Clock. This pin serves as the bit (or shift) clock for the serial interface. This pin is an input in Slave Mode and an output in Master Mode.(1) |
| 9 | FS | I/O | Frame Sync. This pin serves as the frame synchronization clock for the serial interface. This pin is an input in Slave Mode and an output in Master Mode.(1) |
| 10 | DIN | IN | Serial Data Input. This pin is used to write 16-bit data to the DAC.(1) |
| 11 | DOUT | OUT | Serial Data Output. The ADC outputs 16-bit data on this pin.(3) |
| 12 | FSO | OUT | Frame Sync Output. Active only when Time Slot Mode is enabled. This pin is set to a high impedance state when Time Slot mode is disabled (TSC = 0). |
| 13 | $V_{DD}$ | — | Digital Power Supply. Used to power the digital section of the ADC and DAC, as well as the serial interface and mode control logic. This pin is not internally connected to $V_{CC}$. |
| 14 | DGND | — | Digital Ground. Internally connected through the substrate to analog ground. |
| 15 | SCKIO | I/O | System Clock Input/Output. This pin is a system clock output when using the crystal oscillator or XTI as the system clock input; when XTI is connected to ground, this pin is a system clock input.(1) |
| 16 | XTO | OUT | Crystal Oscillator Output. |
| 17 | XTI | IN | Crystal Oscillator Input or an External System Clock Input. |
| 18 | HPFD | IN | High-Pass Filter Disable. When this pin is set to a logic '1', the HPF function in the ADC is disabled.(2) |
| 19 | LOOP | IN | ADC-to-DAC Loop-Back Control. When this pin is set to logic '1', the ADC data is fed to the DAC input.(2) |
| 20 | $\overline{PDWN}$ | IN | Power Down and Reset Control. When this pin is logic '0', Power-Down Mode is enabled. The PCM3500 is reset on the rising edge of this signal.(2) |
| 21 | AGND | — | Analog Ground for the DAC Output Signal. |
| 22 | $V_{OUT}$ | OUT | Analog Output from the DAC Output Filter. |
| 23 | AGND | — | Analog Ground. This is the ground for the internal analog circuitry. |
| 24 | $V_{CC}$ | — | Analog Power Supply. Used to power the analog circuitry of the ADC and DAC. |

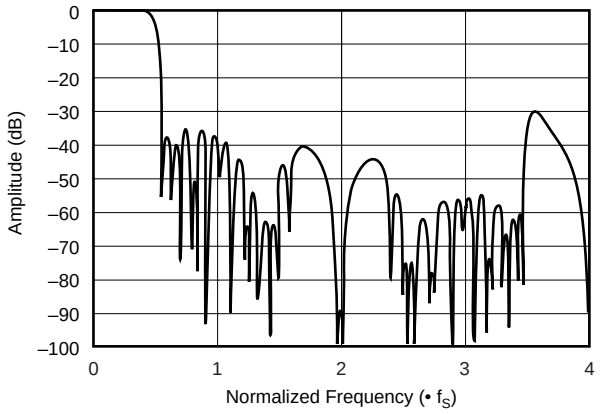
NOTES: (1) Schmitt-Trigger input. (2) Schmitt-Trigger input with an internal pull-down resistor. (3) Tri-state output in Time Slot Mode.

# TYPICAL PERFORMANCE CURVES

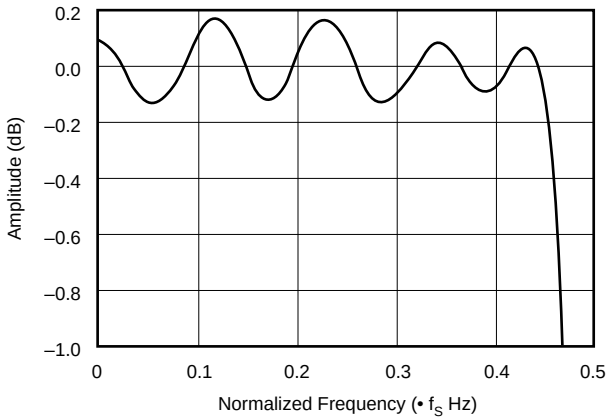
## DAC SECTION

### DIGITAL FILTER

INTERPOLATION FILTER FREQUENCY RESPONSE

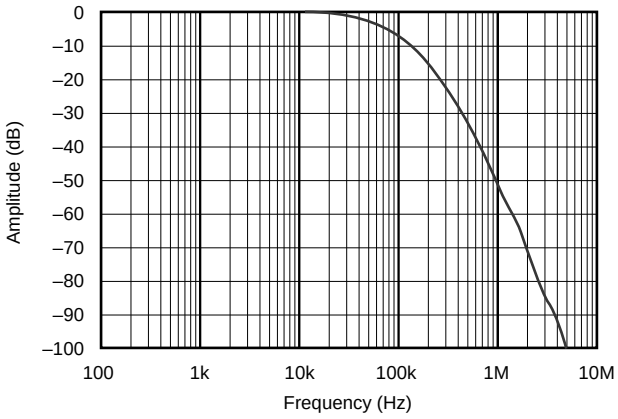



INTERPOLATION FILTER
PASSBAND RIPPLE CHARACTERISTICS

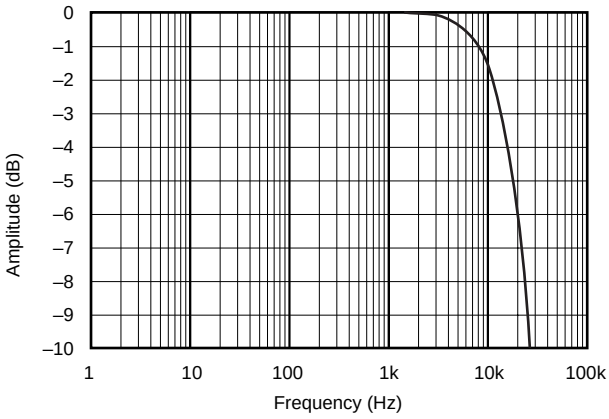



### ANALOG FILTER

OUTPUT FILTER FREQUENCY RESPONSE
STOPBAND CHARACTERISTICS




OUTPUT FILTER FREQUENCY RESPONSE
PASSBAND CHARACTERISTICS



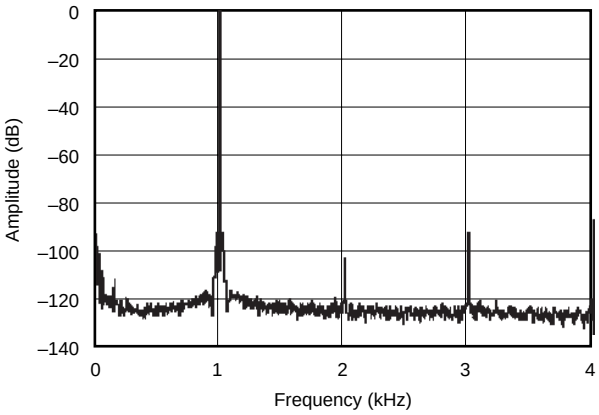
# TYPICAL PERFORMANCE CURVES (Cont.)

$T_A$ = +25°C, $V_{CC}$ = $V_{DD}$ = +3.3V, $f_S$ = 8kHz, and $f_{SIGNAL}$ = 1kHz, unless otherwise specified.

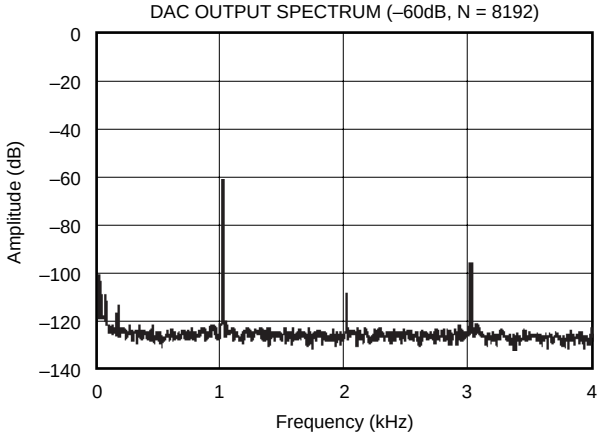
# DAC SECTION

## DAC OUTPUT SPECTRA

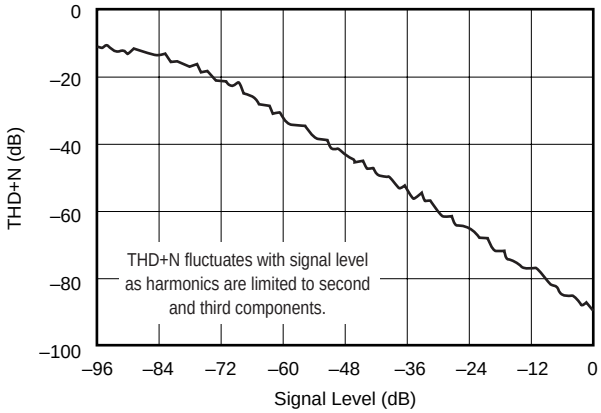
DAC OUTPUT SPECTRUM (–0dB, N = 8192)



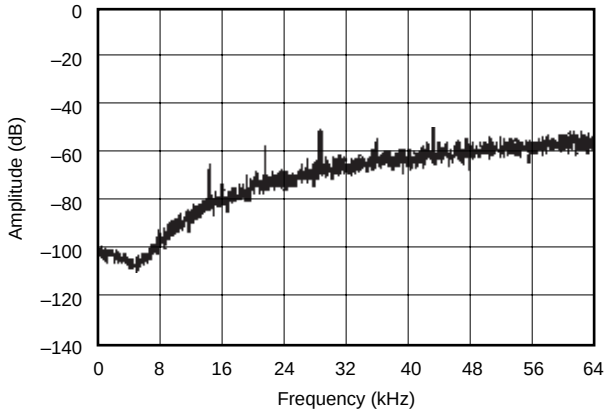

DAC OUTPUT SPECTRUM (–60dB, N = 8192)




TOTAL HARMONIC DISTORTION + NOISE
vs SIGNAL NOISE




DAC OUT-OF-BAND NOISE SPECTRUM
(BPZ, N = 2048)

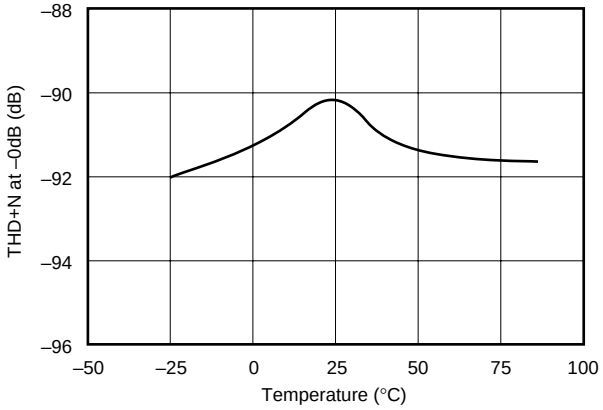


# TYPICAL PERFORMANCE CURVES (Cont.)

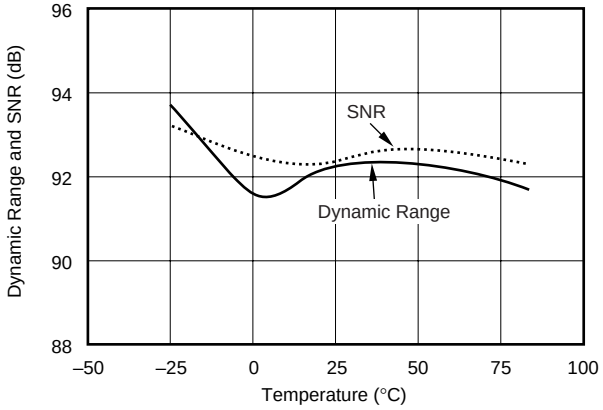
## DAC SECTION

### DAC CHARACTERISTICS vs TEMPERATURE, SUPPLY, AND SAMPLING FREQUENCY

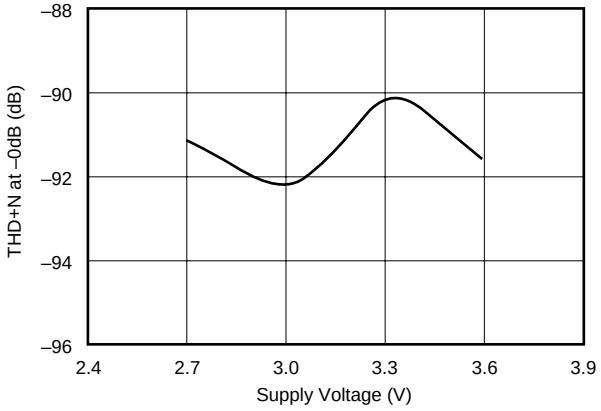
TOTAL HARMONIC DISTORTION + NOISE
vs TEMPERATURE
($T_A$ = –25°C to +85°C)



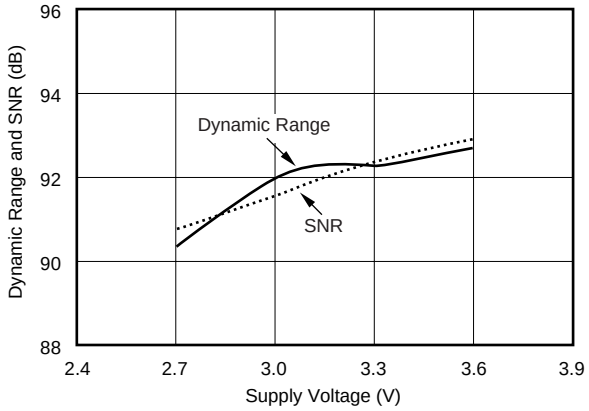

DYNAMIC RANGE AND SIGNAL-TO-NOISE RATIO
vs TEMPERATURE
($T_A$ = –25°C to +85°C)



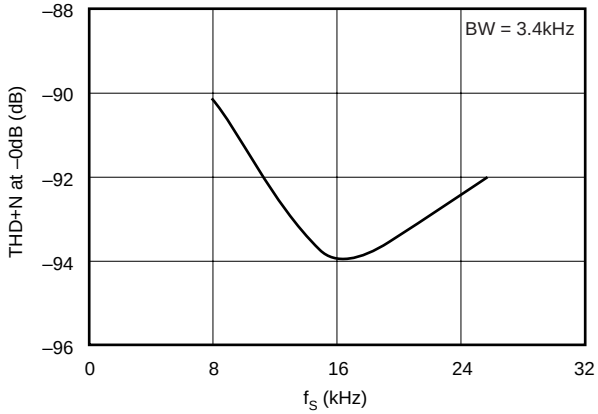

TOTAL HARMONIC DISTORTION + NOISE
vs SUPPLY VOLTAGE
($V_{CC}$ = $V_{DD}$ = +2.7V to +3.6V)



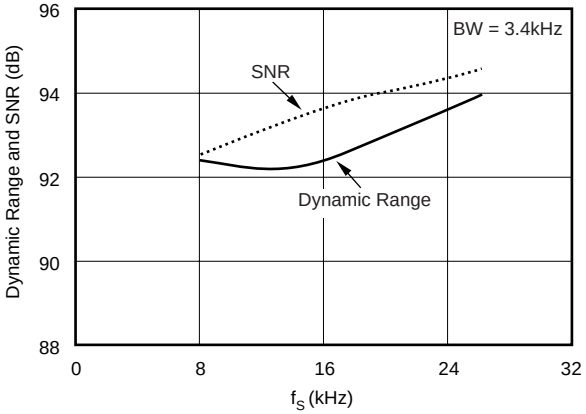

DYNAMIC RANGE AND SIGNAL-TO-NOISE RATIO
vs SUPPLY VOLTAGE
($V_{CC}$ = $V_{DD}$ = +2.7V to +3.6V)




TOTAL HARMONIC DISTORTION + NOISE
vs SAMPLING FREQUENCY
($f_S$ = 8kHz to 26kHz)




DYNAMIC RANGE AND SIGNAL-TO-NOISE RATIO
vs SAMPLING FREQUENCY
($f_S$ = 8kHz to 26kHz)

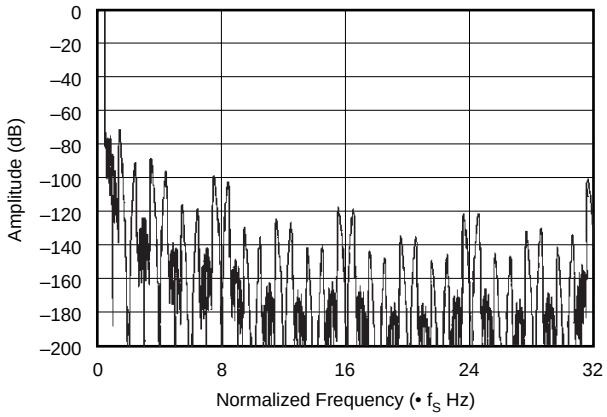


# TYPICAL PERFORMANCE CURVES

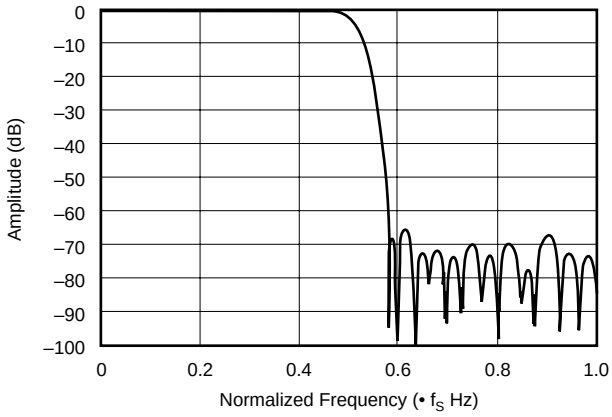
## ADC SECTION

### DIGITAL FILTER

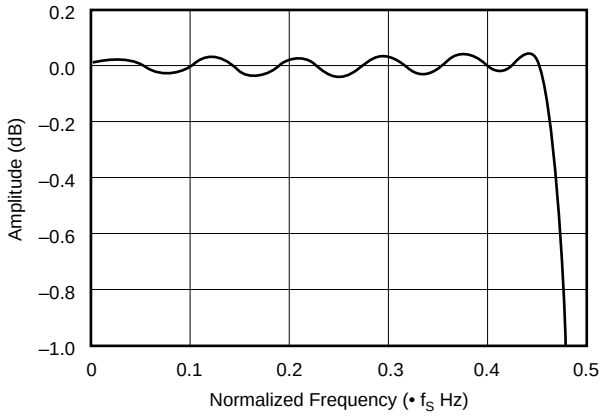
DECIMATION FILTER FREQUENCY RESPONSE



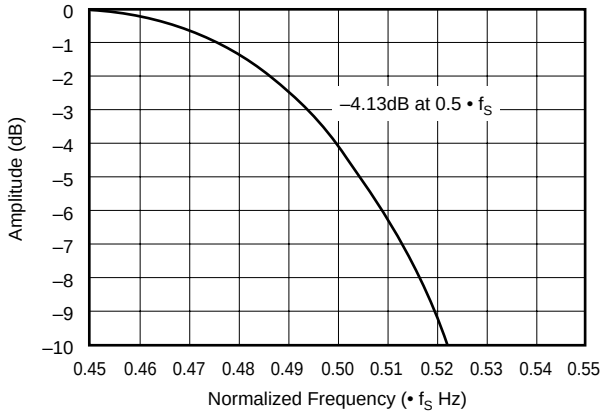

DECIMATION FILTER
STOPBAND ATTENUATION CHARACTERISTICS



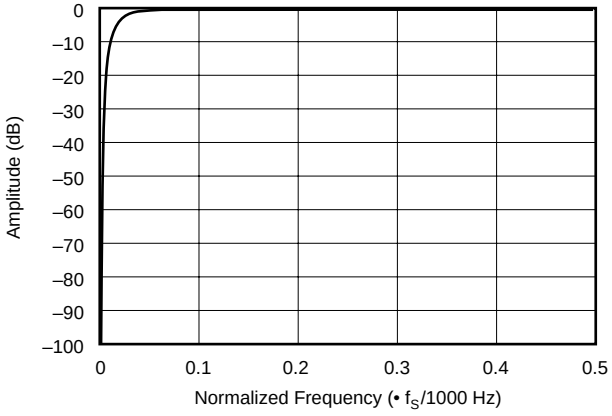

DECIMATION FILTER
PASSBAND RIPPLE CHARACTERISTICS



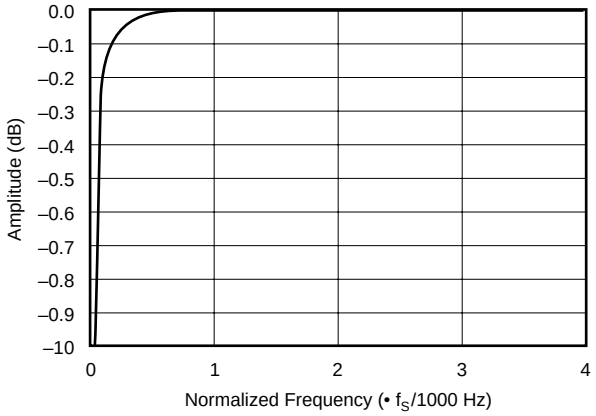

DECIMATION FILTER TRANSITION
BAND CHARACTERISTICS




HIGH-PASS FILTER FREQUENCY RESPONSE
STOPBAND CHARACTERISTICS




HIGH-PASS FILTER FREQUENCY RESPONSE
PASSBAND CHARACTERISTICS



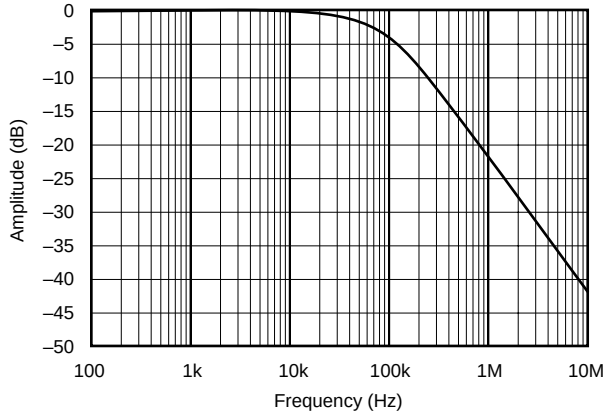
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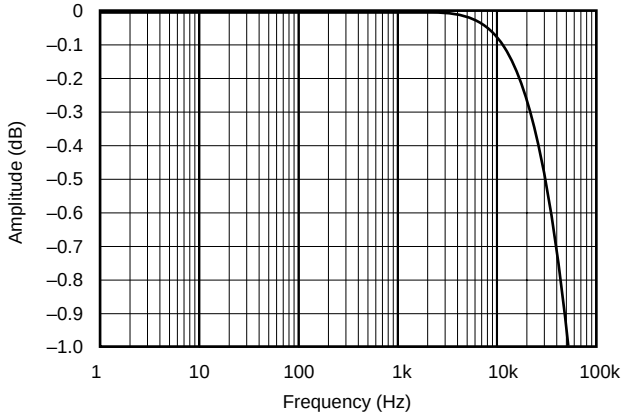
# ADC SECTION

## ANALOG FILTER

ANTI-ALIASING FILTER
STOPBAND CHARACTERISTICS

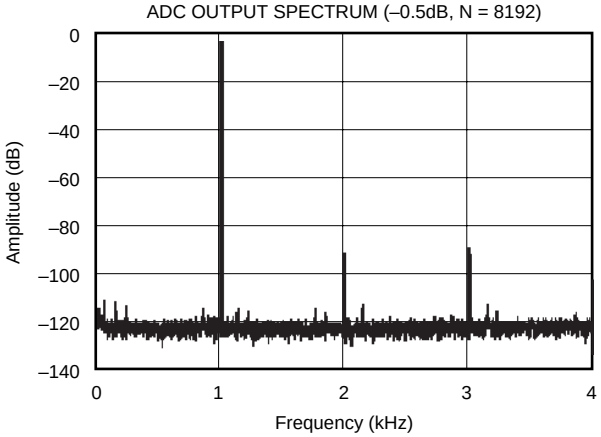



ANTI-ALIASING FILTER
PASSBAND CHARACTERISTICS

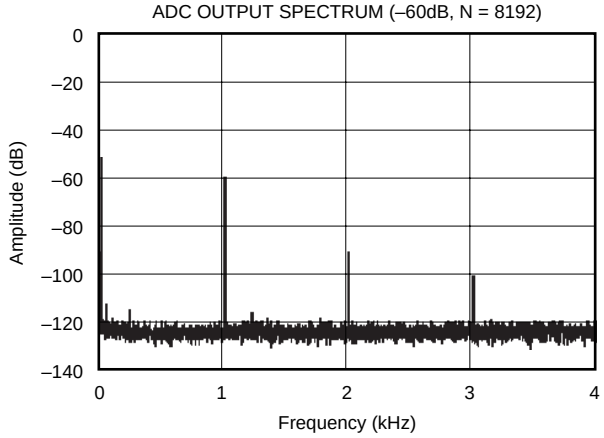



## ADC OUTPUT SPECTRA

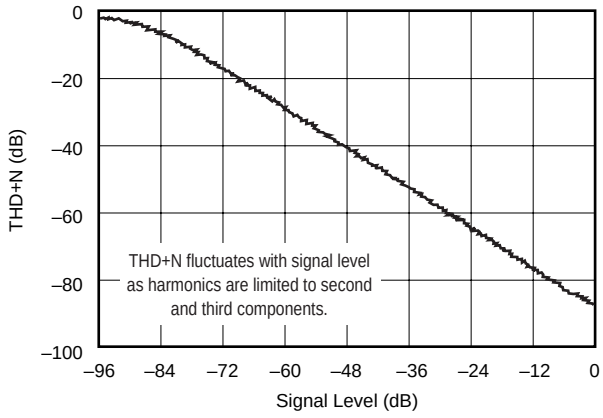
ADC OUTPUT SPECTRUM (–0.5dB, N = 8192)




ADC OUTPUT SPECTRUM (–60dB, N = 8192)




TOTAL HARMONIC DISTORTION + NOISE
vs SIGNAL NOISE



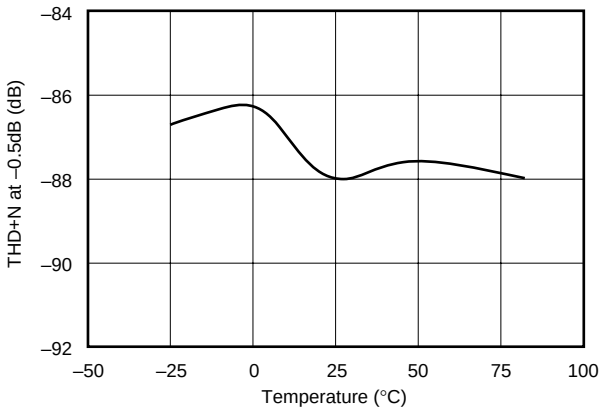
# TYPICAL PERFORMANCE CURVES (Cont.)

$T_A$ = +25°C, $V_{CC}$ = $V_{DD}$ = +3.3V, $f_S$ = 8kHz, and $f_{SIGNAL}$ = 1kHz, unless otherwise specified.

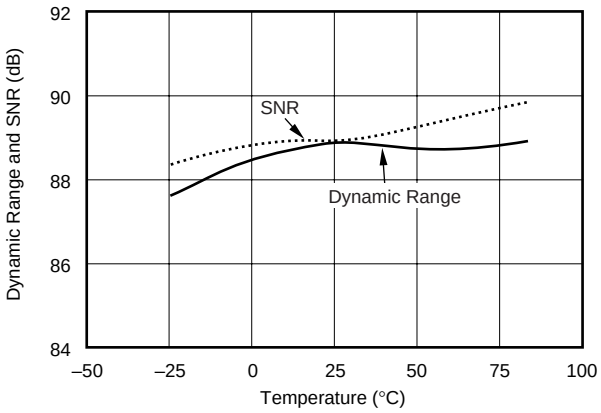
# ADC SECTION

## ADC CHARACTERISTICS vs TEMPERATURE, SUPPLY AND SAMPLING FREQUENCY

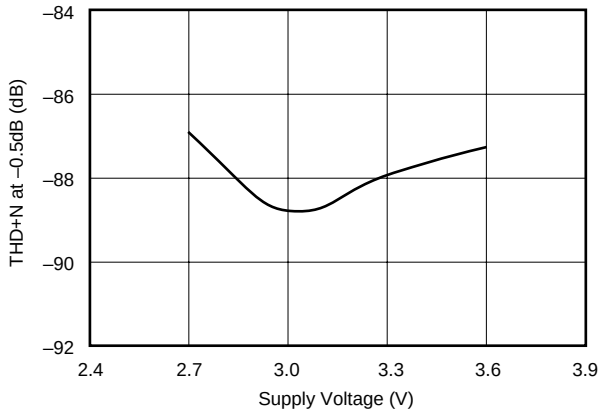
TOTAL HARMONIC DISTORTION + NOISE
vs TEMPERATURE
($T_A$ = –25°C to +85°C)



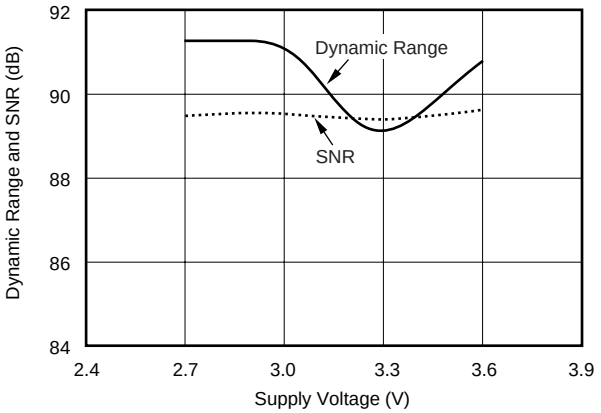

DYNAMIC RANGE AND SIGNAL-TO-NOISE RATIO
vs TEMPERATURE
($T_A$ = –25°C to +85°C)



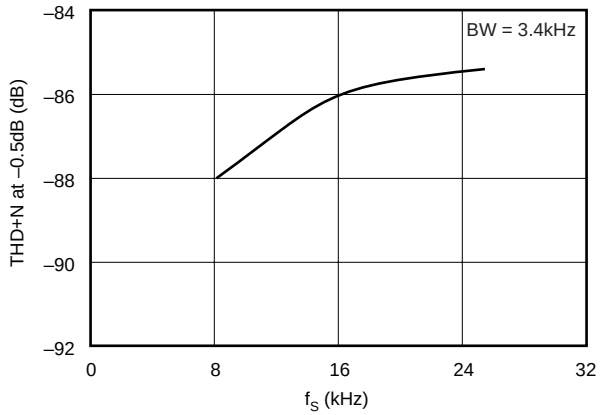

TOTAL HARMONIC DISTORTION + NOISE
vs SUPPLY VOLTAGE
($V_{CC}$ = $V_{DD}$ = +2.7V to +3.6V)



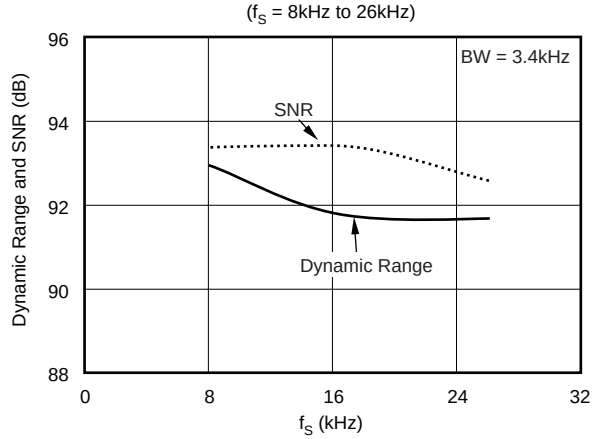

DYNAMIC RANGE AND SIGNAL-TO-NOISE RATIO
vs SUPPLY VOLTAGE
($V_{CC}$ = $V_{DD}$ = +2.7V to +3.6V)




TOTAL HARMONIC DISTORTION + NOISE
vs SAMPLING FREQUENCY
($f_S$ = 8kHz to 26kHz)




DYNAMIC RANGE AND SIGNAL-TO-NOISE RATIO
vs SAMPLING FREQUENCY
($f_S$ = 8kHz to 26kHz)

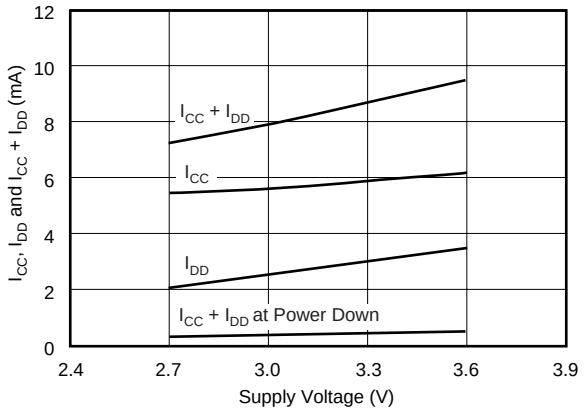


# TYPICAL PERFORMANCE CURVES (Cont.)

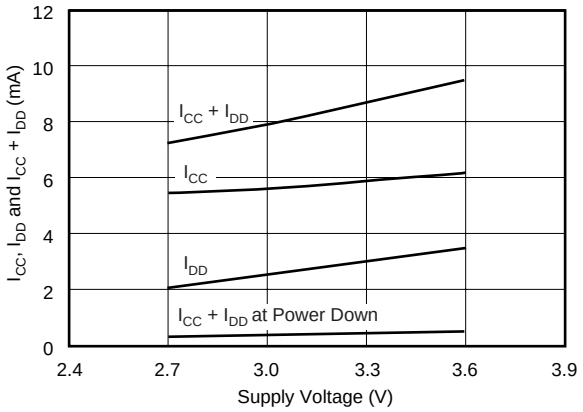
$T_A$ = +25°C, $V_{CC}$ = $V_{DD}$ = +3.3V, $f_S$ = 8kHz, and $f_{SIGNAL}$ = 1kHz, unless otherwise specified.

## SUPPLY CURRENT vs SUPPLY VOLTAGE AND SAMPLING FREQUENCY

SUPPLY CURRENT vs SUPPLY VOLTAGE




SUPPLY CURRENT vs SUPPLY VOLTAGE



# SYSTEM CLOCK AND RESET/ POWER DOWN

## SYSTEM CLOCK INPUT AND OUTPUT

The PCM3500 requires a system clock for operating the digital filters and delta-sigma data converters.

The system clock may be supplied from an external master clock or generated using the on-chip crystal oscillator circuit. Figure 1 shows the required connections for external and crystal clock operation. The system clock must operate at 512 times the sampling frequency, $f_S$, with sampling frequencies from 7.2kHz to 26kHz. This gives an effective system clock frequency range of 3.6864MHz to 13.312MHz.

Table I shows system clock frequencies for common sampling frequencies.

For external clock operation, XTI (pin 17) or SCKIO (pin 15) is driven by a master clock source. If SCKIO is used as the system clock input, then XTI must be connected to ground.

| SAMPLING FREQUENCY (kHz) | SYSTEM CLOCK FREQUENCY (MHz) |
|---|---|
| 8 | 4.096 |
| 11.025 | 5.6448 |
| 16 | 8.192 |
| 22.05 | 11.2896 |
| 24 | 12.288 |

TABLE I. System Clock Frequencies for Common Sampling Frequencies.

For either case, XTO (pin 16) should be left open. The system clock source should be free of noise and exhibit low phase jitter in order to obtain optimal dynamic performance from the PCM3500. Figure 2 shows the system clock timing requirements associated with an external master clock.

For crystal oscillator operation, a crystal is connected between XTI (pin 17) and XTO (pin 16), along with the necessary load capacitors (10pF to 33pF per pin, as shown in Figure 1). A fundamental-mode, parallel resonant crystal is required.

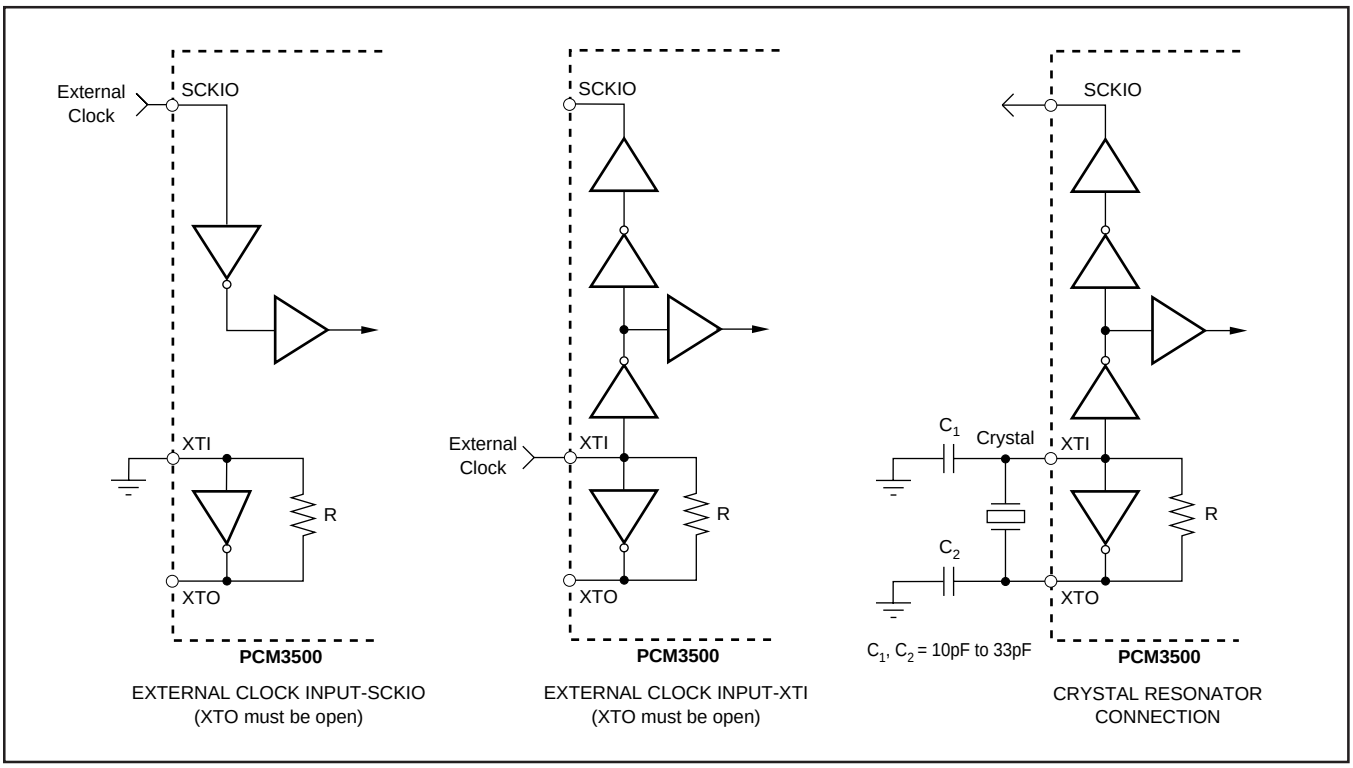



FIGURE 1. System Clock Generation.

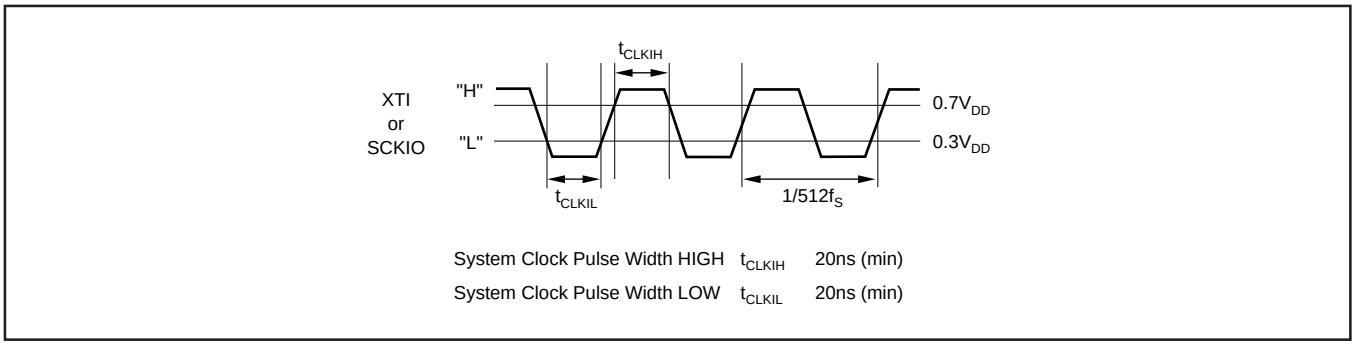



FIGURE 2. External System Clock Timing Requirements.

## Reset and Power Down

The PCM3500 supports power-on reset, external reset, and power-down operations. Power-on reset is performed by internal circuitry automatically at power up, while the external reset is initiated using the $\overline{\text{PDWN}}$ input (pin 20).

Power-on reset occurs when power and system clock are initially applied to the PCM3500. The internal reset circuitry requires that the system clock be active at power up, with at least three system clock cycles occurring prior to $V_{DD}$ = 2.2V. When $V_{DD}$ exceeds 2.2V, the power-on reset comparator enables the initialization sequence, which requires 1024 system clock periods for completion. During the initialization sequence, the DAC output is forced to AGND, and the ADC output is forced to a high impedance state. After the initialization sequence has completed, the DAC and ADC outputs experience a delay before they output a valid signal or data. Refer to Figures 3 and 5 for power-on reset and post-reset delay timing.

External reset is performed by first setting $\overline{\text{PDWN}}$ = '0' and then setting $\overline{\text{PDWN}}$ = '1'. The LOW to HIGH transition on $\overline{\text{PDWN}}$ causes the reset initialization sequence to start. During the initialization sequence, the DAC output is forced to AGND, and the ADC output is forced to a high impedance state. After the initialization sequence has completed, the DAC and ADC outputs experience a delay before they output a valid signal or data. Refer to Figures 4 and 5 for external reset and post-reset delay timing.

Power-down mode is enabled by setting $\overline{\text{PDWN}}$ = '0'. During power-down mode, minimum current is drawn when the system clock is removed, resulting in 60µA (typical) power supply current. The $\overline{\text{PDWN}}$ input includes an internal pull-down resistor, which places the PCM3500 in power-down mode at power-up if the $\overline{\text{PDWN}}$ pin is left unconnected. Ideally, the $\overline{\text{PDWN}}$ input should be driven by active logic in order to control reset and power-down operation. If the $\overline{\text{PDWN}}$ pin is to be unused in the system application, it should be connected to $V_{DD}$ to enable normal operation. By setting $\overline{\text{PDWN}}$ = '1' when exiting power-down mode, the PCM3500 will initiate an external reset as described earlier in this section.

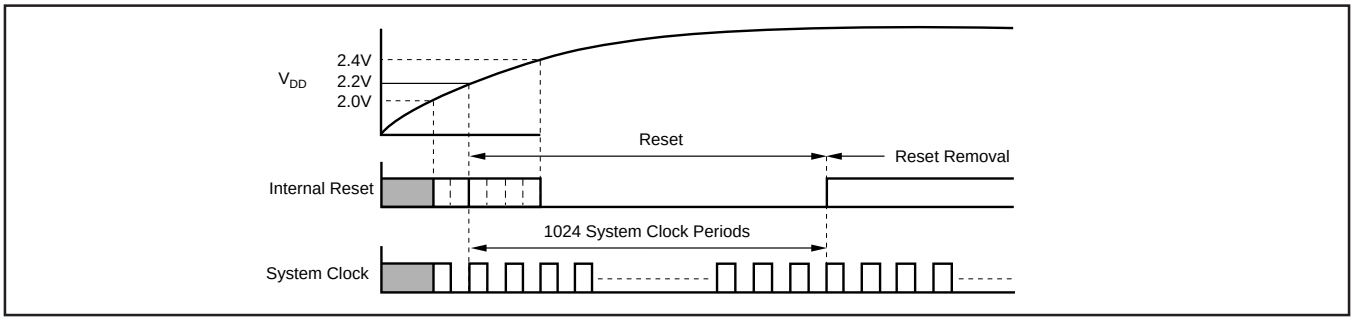



FIGURE 3. Power-On Reset Timing.

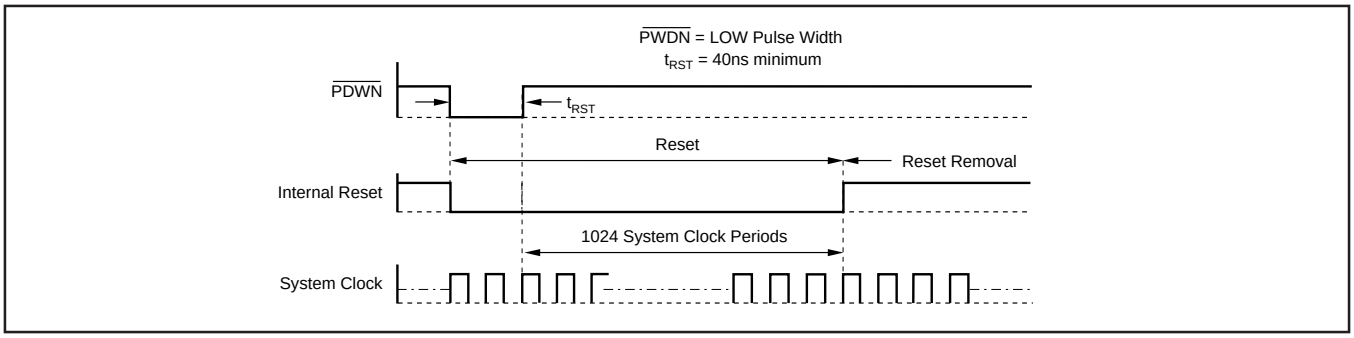
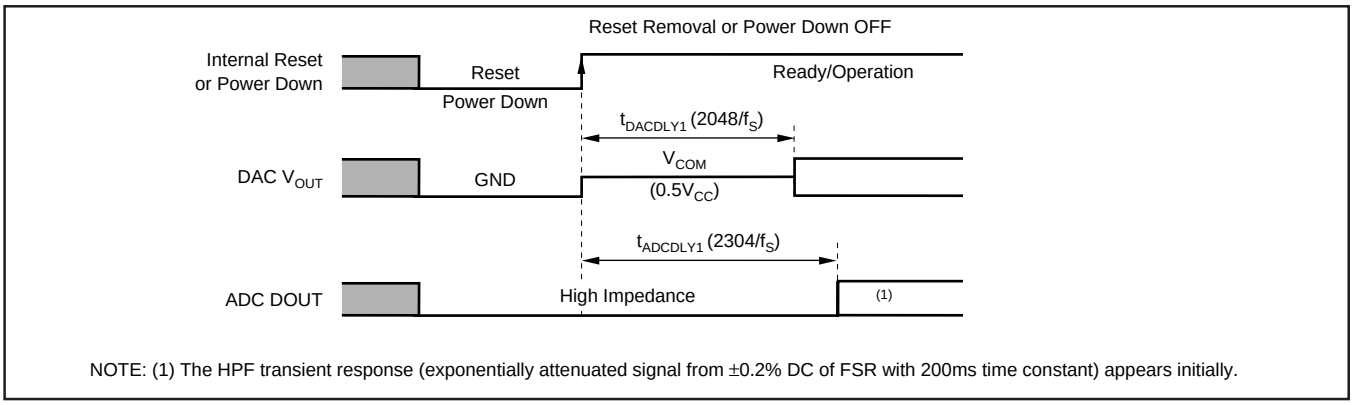



FIGURE 4. External Reset Timing.




NOTE: (1) The HPF transient response (exponentially attenuated signal from ±0.2% DC of FSR with 200ms time constant) appears initially.

FIGURE 5. DAC and ADC Output for Reset and Power Down.

## SERIAL INTERFACE

The serial interface of the PCM3500 is a 4-wire synchronous serial port. It includes FS (pin 9), BCK (pin 8), DIN (pin 10) and DOUT (pin 11). FS is the frame synchronization clock, BCK is the serial bit or shift clock, DIN is the serial data input for the DAC, and DOUT is the serial data output for the ADC.

The frame sync, FS, operates at the sampling frequency ($f_S$). The bit clock, BCK, operates at $16f_S$ for normal operation. DIN and DOUT also operate at the bit clock rate. Both FS and BCK must be synchronous with the system clock (guaranteed in Master Mode). Data for DIN is clocked into the serial interface on the rising edge of BCK, while data for DOUT is clocked out of the serial interface on the falling edge of BCK.

Figure 6 shows the serial interface format for the PCM3500. The serial data for DIN and DOUT must be in Binary Two's Complement, MSB-first format. Figures 7 and 8 show the timing specifications for the serial interface when used in Slave and Master Modes.

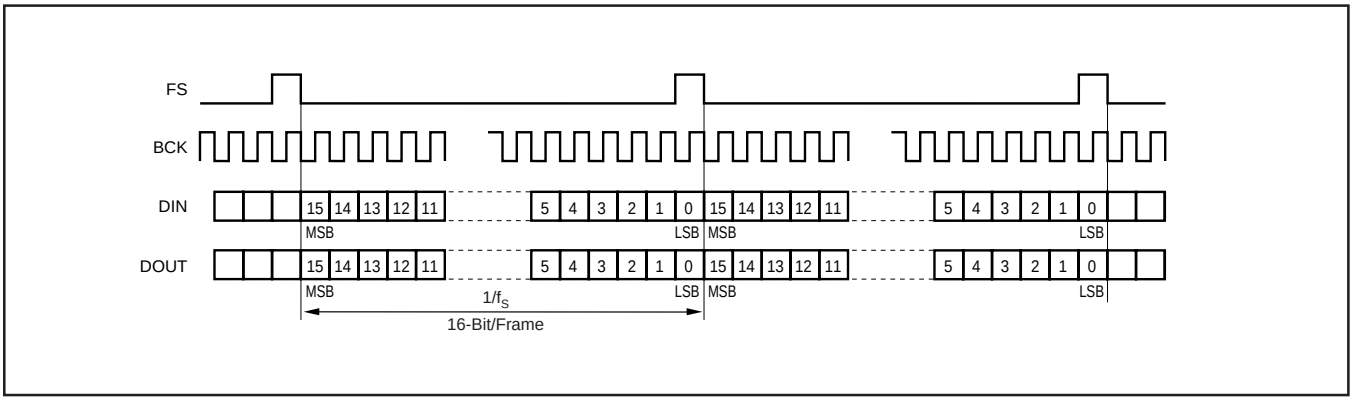
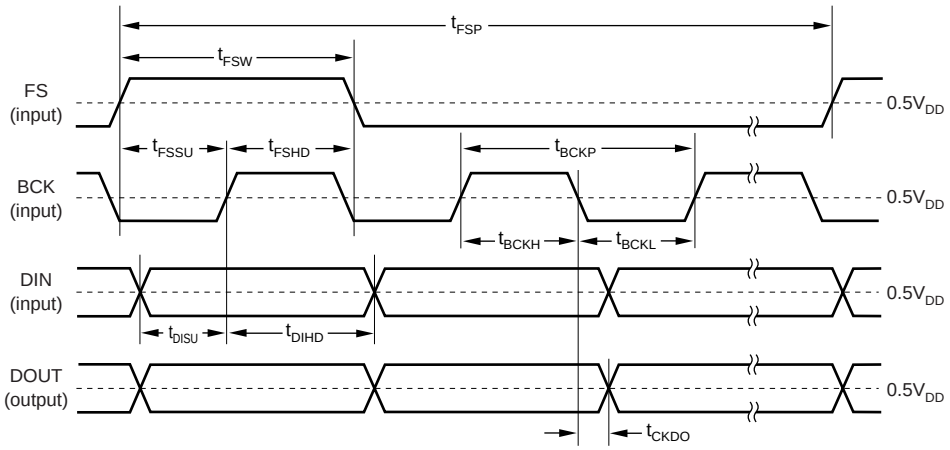


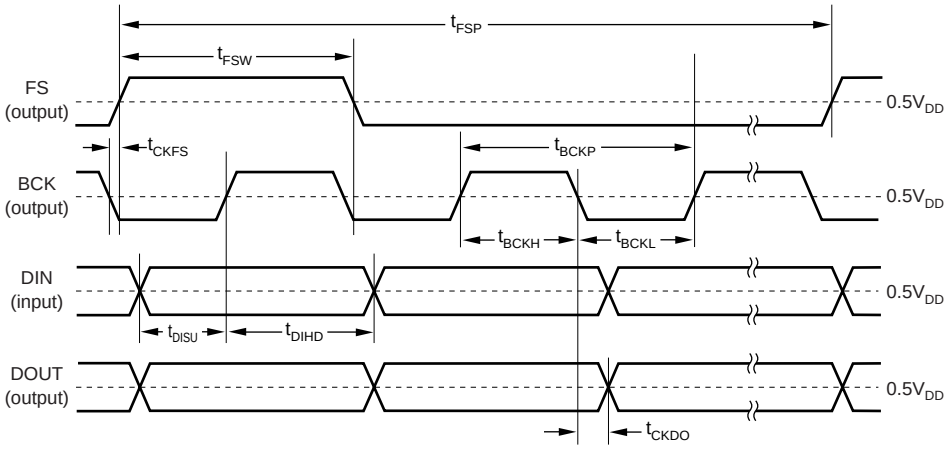

FIGURE 6. Serial Interface Format.




NOTES: Timing measurement reference level is $(V_{IH}/V_{IL})/2$. RIsing and falling time is measured from 10% to 90% of IN/OUT signal swing. Load capacitance of DOUT signal is 50pF.

| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| $t_{BCKP}$ | BCK Period | 2400 | | | ns |
| $t_{BCKH}$ | BCK Pulse Width HIGH | 800 | | | ns |
| $t_{BCKL}$ | BCK Pulse Width LOW | 800 | | | ns |
| $t_{FSW}$ | FS Pulse Width HIGH | $t_{BCKP}$ – 60 | $t_{BCKP}$ | $t_{BCKP}$ + 60 | ns |
| $t_{FSP}$ | FS Period | | $1/f_S$ | | |
| $t_{FSSU}$ | FS Set Up Time to BCK Rising Edge | 60 | | | ns |
| $t_{FSHD}$ | FS Hold Time to BCK Rising Edge | 60 | | | ns |
| $t_{DISU}$ | DIN Set Up Time to BCK Rising Edge | 60 | | | ns |
| $t_{DIHD}$ | DIN Hold Time to BCK Rising Edge | 60 | | | ns |
| $t_{CKDO}$ | Delay Time BCK Falling Edge to DOUT | 0 | | 80 | ns |
| $t_R$ | Rising Time of All Signals | | | 30 | ns |
| $t_F$ | Falling Time of All Signals | | | 30 | ns |

FIGURE 7. Serial Interface Timing for Slave Mode.




NOTES: Timing measurement reference level is ($V_{IH}$/$V_{IL}$)/2. Rising and falling time is measured from 10% to 90% of IN/OUT signal swing. Load capacitance of DOUT, FS, BCK signal is 50pF.

| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| $t_{BCKP}$ | BCK Period | 2400 | | 16000 | ns |
| $t_{BCKH}$ | BCK Pulse Width HIGH | 1200 | | 8000 | ns |
| $t_{BCKL}$ | BCK Pulse Width LOW | 1200 | | 8000 | ns |
| $t_{CKFS}$ | Delay Time BCK Falling Edge to FS | – 40 | | 40 | ns |
| $t_{FSW}$ | FS Pulse Width HIGH | $t_{BCKP}$ – 60 | $t_{BCKP}$ | $t_{BCKP}$ + 60 | ns |
| $t_{FSP}$ | FS Period | | $1/f_S$ | | |
| $t_{DISU}$ | DIN Set Up Time to BCK Rising Edge | 60 | | | ns |
| $t_{DIHD}$ | DIN Hold Time to BCK Rising Edge | 60 | | | ns |
| $t_{CKDO}$ | Delay Time BCK Falling Edge to DOUT | 0 | | 80 | ns |
| $t_R$ | Rising Time of All Signals | | | 30 | ns |
| $t_F$ | Falling Time of All Signals | | | 30 | ns |

FIGURE 8. Serial Interface Timing for Master Mode.

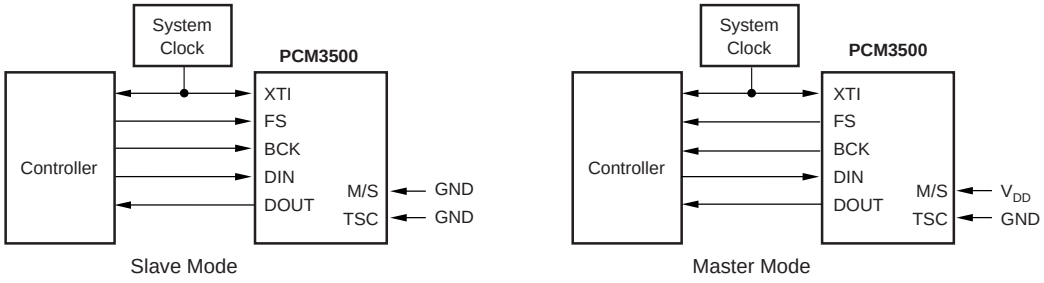



FIGURE 9. Slave and Master Mode Connections.

## MASTER/SLAVE OPERATION

The serial interface supports both Slave and Master Mode operation. The mode is selected by the M/S input (pin 6). Table II shows mode and pin settings corresponding to the M/S input selection. Figure 9 shows connections for Slave and Master mode operation.

| M/S (PIN 6) | SERIAL INTERFACE MODE | FS (PIN) | BCK (PIN 8) |
|---|---|---|---|
| 0 | Slave | Input | Input |
| 1 | Master | Output | Output |

TABLE II. Master/Slave Mode Selection.

### Slave Mode Operation

In Slave Mode, the FS and BCK pins are inputs to the PCM3500. Both FS and BCK should be derived from the system clock signal (XTI or SCKIO) to ensure proper synchronization. Slave Mode is best suited for applications where the DSP or controller is capable of generating the FS, BCK, and system clocks using an on-chip serial port and/or timing generator.

### Master Mode Operation

In Master Mode operation, both FS and BCK are clock outputs generated by the PCM3500 from the system clock input (XTI, SCKIO, or a crystal). In Master Mode, the timing and phase relationships between system clock, FS, and BCK are managed internally to provide optimal synchronization.

## SYNCHRONIZATION REQUIREMENTS

The PCM3500 requires that FS and BCK be synchronous with the system clock. Internal circuitry is included to detect a loss of synchronization between FS and the system clock input. If the phase relationship between FS and the system clock varies more than ± 1.5 BCK periods, the PCM3500 will detect a loss of synchronization. Upon detection, the DAC output is forced to $0.5V_{CC}$ and the DOUT pin is forced to a high impedance state. This occurs within one sampling clock (FS) period of initial detection. Figure 10 shows the loss of synchronization operation and the DAC and ADC output delays associated with it.

## TIME SLOT OPERATION

The PCM3500 serial interface supports Time Division Multiplexing (TDM) using the Time Slot Mode. Up to four PCM3500s may be connected on the same 4-wire serial interface bus. This is useful for system applications that require multiple modem or voice channels. Figure 11 shows examples of Time Slot Mode connections.

Time Slot Mode defines a 64-bit long frame, composed of four time slots. Each slot is 16 bits long and corresponds to one of four CODECs. The FS pin on the first PCM3500 (CODEC A, Slot 0) is used as the master frame sync, and operates at the sampling frequency, $f_S$. The bit clock, BCK, operates at $64f_S$. DIN and DOUT of each CODEC also operate at $64f_S$. Figure 12 shows the operation of the Time Slot Mode.

Time Slot operation is enabled or disabled using the TSC input (pin 7). The state of the TSC pin is updated at power-on reset, or on the rising edge of PWDN input (if using external reset or power-down mode). A forced reset is required when changing from Slave to Master Mode, or visa versa, in real time.

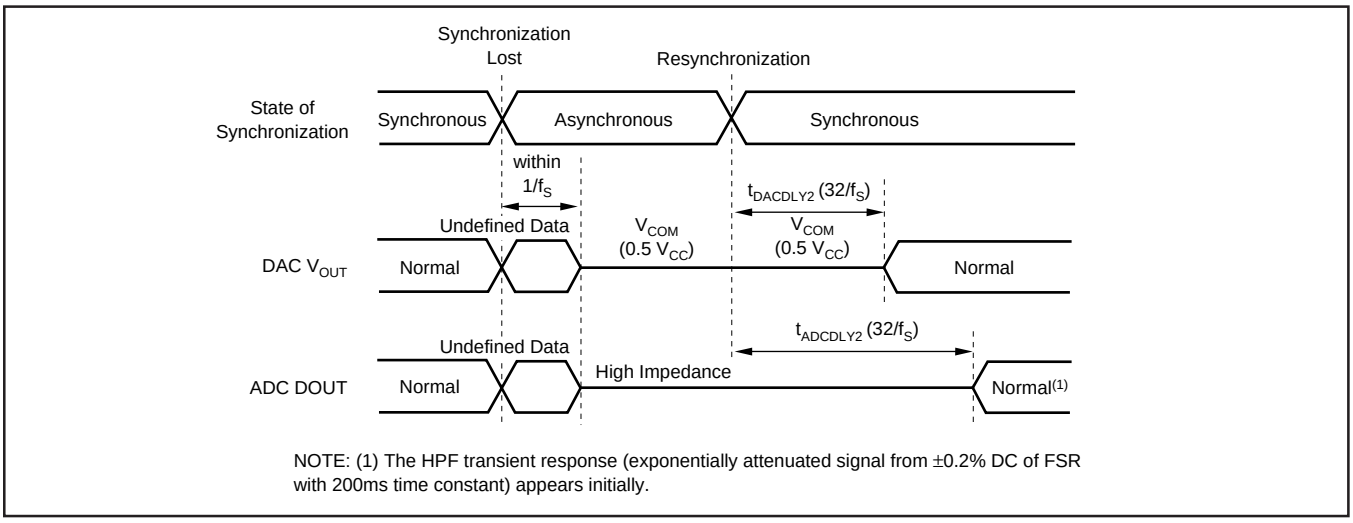



FIGURE 10. Loss of Synchronization Operation and Timing.

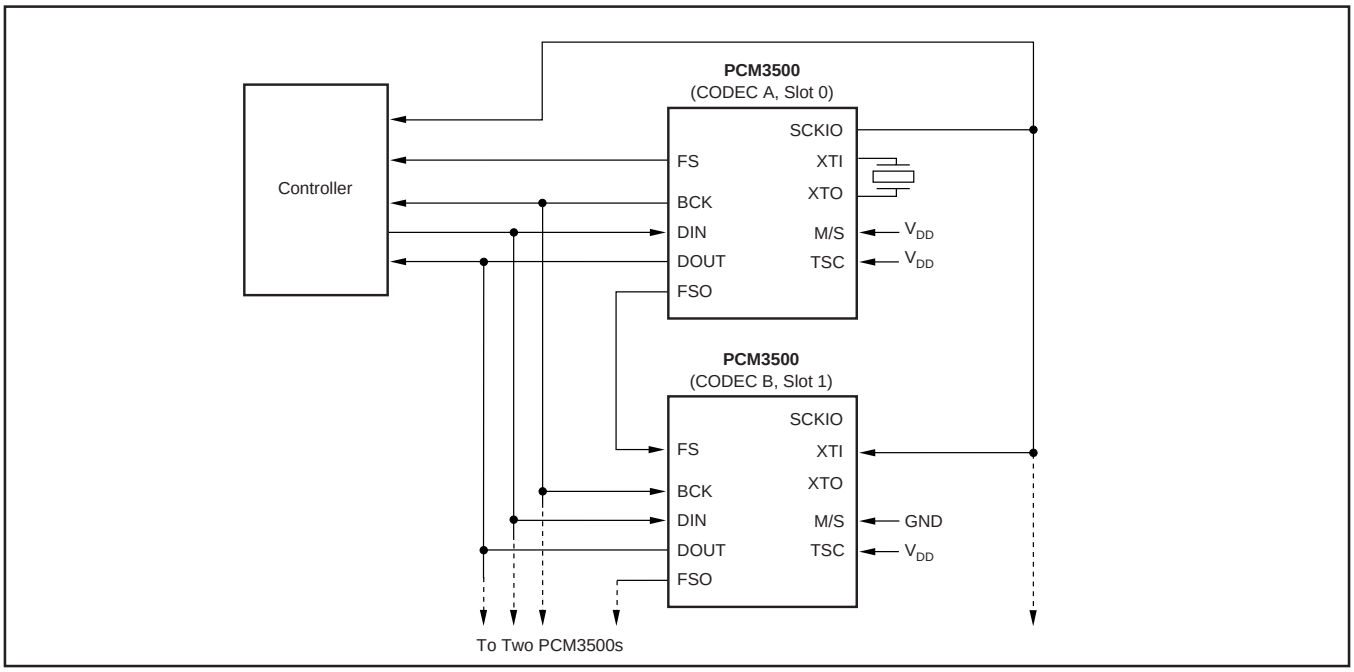



FIGURE 11. Time Slot Mode Connections.

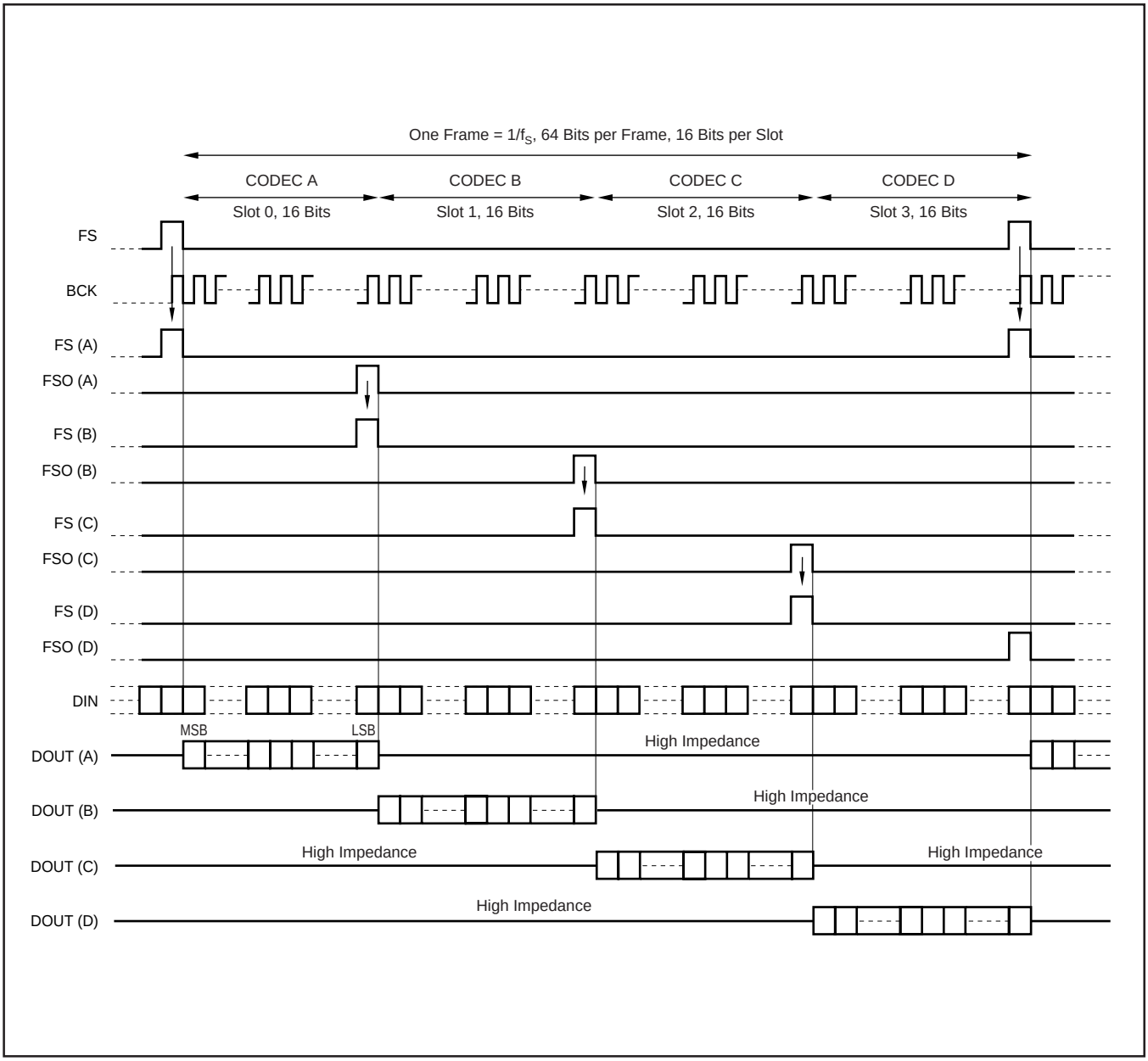



FIGURE 12. Time Slot Mode Operation.

Table III shows the TSC pin settings and corresponding mode selections. When Time Slot Mode is enabled, FSO (pin 12) is used as a frame sync output, which is connected to the FS input of the next PCM3500 in the Time Slot sequence. Figures 13 and 14 provide detailed timing for Time Slot Mode operation.

| TSC (PIN 7) | TIME SLOT MODE |
|---|---|
| 0 | Time Slot Mode Disabled, Normal Operation |
| 1 | Time Slot Operation Enable |

TABLE III. Time Slot Mode Selection.

## ADC-TO-DAC LOOP BACK

The PCM3500 includes a Loop-Back Mode, which directly feeds the ADC data to the DAC input. This mode is designed for diagnostic testing and system adjustment. Loop-Back Mode is enabled and disabled using the LOOP input (pin 19). Table IV shows the LOOP pin settings and corresponding mode selections. The serial interface continues to operate in Loop-Back Mode, allowing the host to read the ADC data at the DOUT pin.

| LOOP (PIN 19) | LOOP-BACK MODE |
|---|---|
| 0 | Loop-Back Mode Disabled, Normal Operation |
| 1 | Loop-Back Mode Enabled |

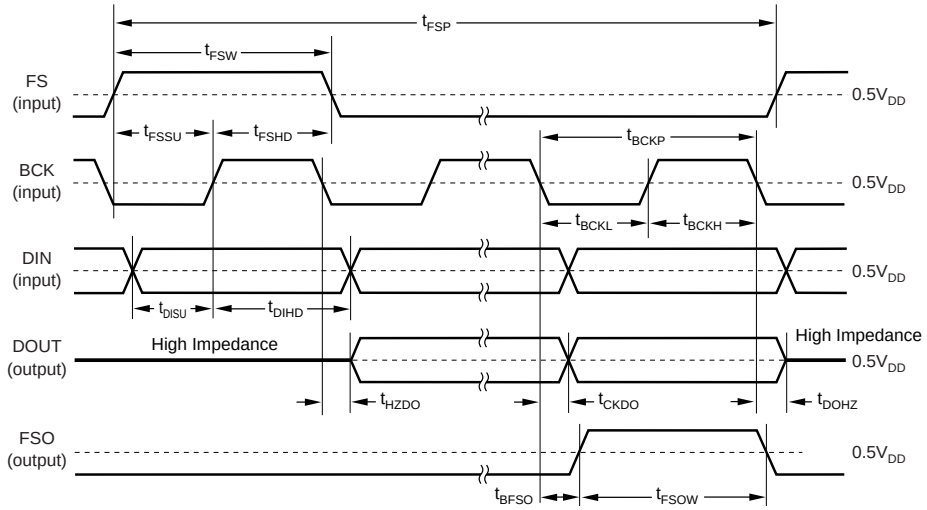
TABLE IV. Loop-Back Mode Selection.

## HIGH-PASS FILTER

The PCM3500 includes a digital high-pass filter in the ADC which may be used to remove the DC offset created by the analog front-end (AFE) section. The high-pass filter response is shown in Figure 15. The high-pass filter may be enabled or disabled using the HPFD input (pin 18). Table V shows the HPFD pin settings and corresponding mode selections.

| HPFD (PIN 18) | HIGH-PASS FILTER MODE |
|---|---|
| 0 | High-Pass Filter On |
| 1 | High-Pass Filter Off |

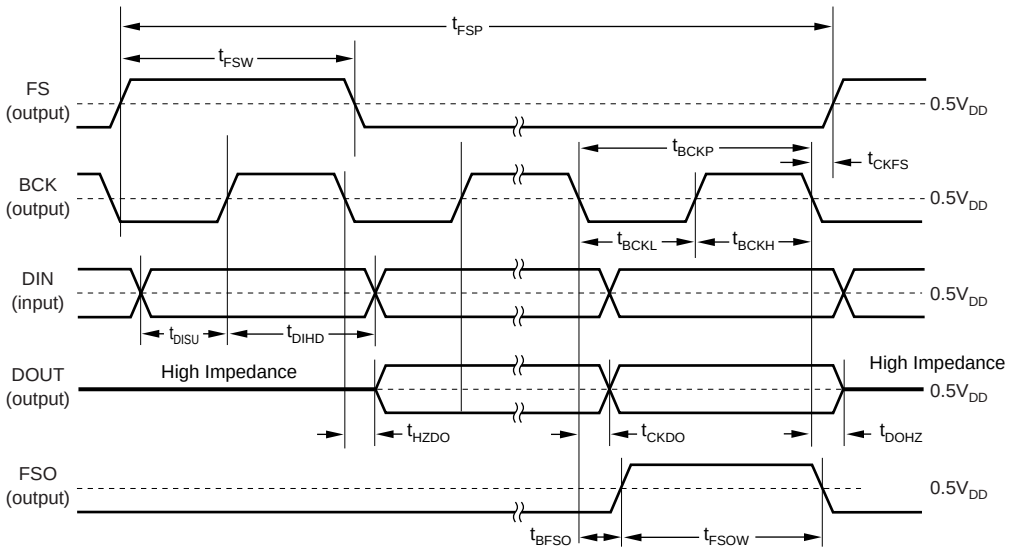
TABLE V. High-Pass Filter Mode Selection.




NOTES: Timing measurement reference level is $(V_{IH}/V_{IL})/2$. Rising and falling time is measured from 10% to 90% of IN/OUT signal swing. Load capacitance of DOUT, and FSO signal is 50pF.

| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| $t_{BCKP}$ | BCK Period | 600 | | | ns |
| $t_{BCKH}$ | BCK Pulse Width HIGH | 200 | | | ns |
| $t_{BCKL}$ | BCK Pulse Width LOW | 200 | | | ns |
| $t_{FSW}$ | FS Pulse Width HIGH | $t_{BCKP}$ – 60 | $t_{BCKP}$ | $t_{BCKP}$ + 60 | ns |
| $t_{FSP}$ | FS Period | | $1/f_S$ | | |
| $t_{FSSU}$ | FS Set Up TIme to BCK Rising Edge | 60 | | | ns |
| $t_{FSHD}$ | FS Hold TIme to BCK RIsing Edge | 60 | | | ns |
| $t_{DISU}$ | DIN Set Up Time to BCK Rising Edge | 60 | | | ns |
| $t_{DIHD}$ | DIN Hold Time to BCK Rising Edge | 60 | | | ns |
| $t_{CKDO}$ | Delay Time BCK Falling Edge to DOUT | 0 | | 80 | ns |
| $t_{HZDO}$ | Delay Time BCK Falling Edge to DOUT Active | | 20 | | ns |
| $t_{DOHZ}$ | Delay Time BCK Falling Edge to DOUT Inactive | | 19.5 | | ns |
| $t_{FSOW}$ | FSO Pulse Width HIGH | $t_{BCKP}$ – 60 | $t_{BCKP}$ | $t_{BCKP}$ + 60 | ns |
| $t_{BFSO}$ | Delay Time BCK Falling Edge to FSO | 0 | | 80 | ns |
| $t_R$ | Rising Time of All Signals | | | 30 | ns |
| $t_F$ | Falling Time of All Signals | | | 30 | ns |

FIGURE 13. Serial Interface Timing for Time Slot Mode Operation (Slave Mode).




NOTES: Timing measurement reference level is $(V_{IH}/V_{IL})/2$. Rising and falling time is measured from 10% to 90% of IN/OUT signal swing. Load capacitance of DOUT, FSO, FS, and BCK signal is 50pF.

| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| $t_{BCKP}$ | BCK Period | 600 | | 4000 | ns |
| $t_{BCKH}$ | BCK Pulse Width HIGH | 300 | | 2000 | ns |
| $t_{BCKL}$ | BCK Pulse Width LOW | 300 | | 2000 | ns |
| $t_{CKFS}$ | Delay Time BCK Falling Edge to FS | –40 | | 40 | ns |
| $t_{FSW}$ | FS Pulse Width HIGH | $t_{BCKP}$ – 60 | $t_{BCKP}$ | $t_{BCKP}$ + 60 | ns |
| $t_{FSP}$ | FS Period | | $1/f_S$ | | |
| $t_{DISU}$ | DIN Set Up Time to BCK Rising Edge | 60 | | | ns |
| $t_{DIHD}$ | DIN Hold Time to BCK Rising Edge | 60 | | | ns |
| $t_{CKDO}$ | Delay Time BCK Falling Edge to DOUT | 0 | | 80 | ns |
| $t_{HZDO}$ | Delay Time BCK Falling Edge to DOUT Active | | 20 | | ns |
| $t_{DOHZ}$ | Delay Time BCK Falling Edge to DOUT Inactive | | 19.5 | | ns |
| $t_{FSOW}$ | FSO Pulse Width HIGH | $t_{BCKP}$ – 60 | $t_{BCKP}$ | $t_{BCKP}$ + 60 | ns |
| $t_{BFSO}$ | Delay Time BCK Falling Edge to FSO | 0 | | 80 | ns |
| $t_R$ | Rising Time of All Signals | | | 30 | ns |
| $t_F$ | Falling Time of All Signals | | | 30 | ns |

FIGURE 14. Serial Interface Timing for Time Slot Mode Operation (Master Mode).

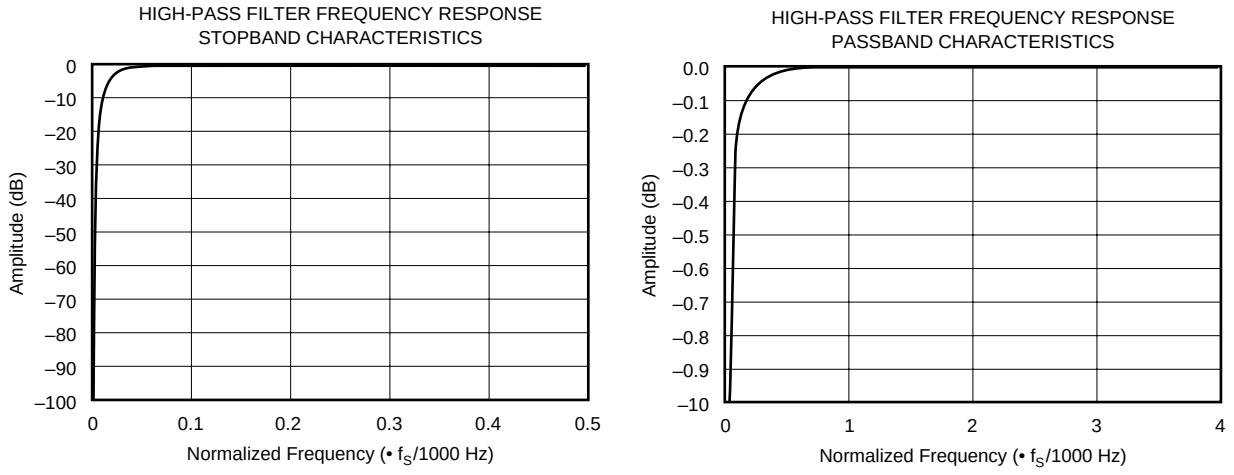



FIGURE 15. High-Pass Filter Response.

# APPLICATIONS INFORMATION

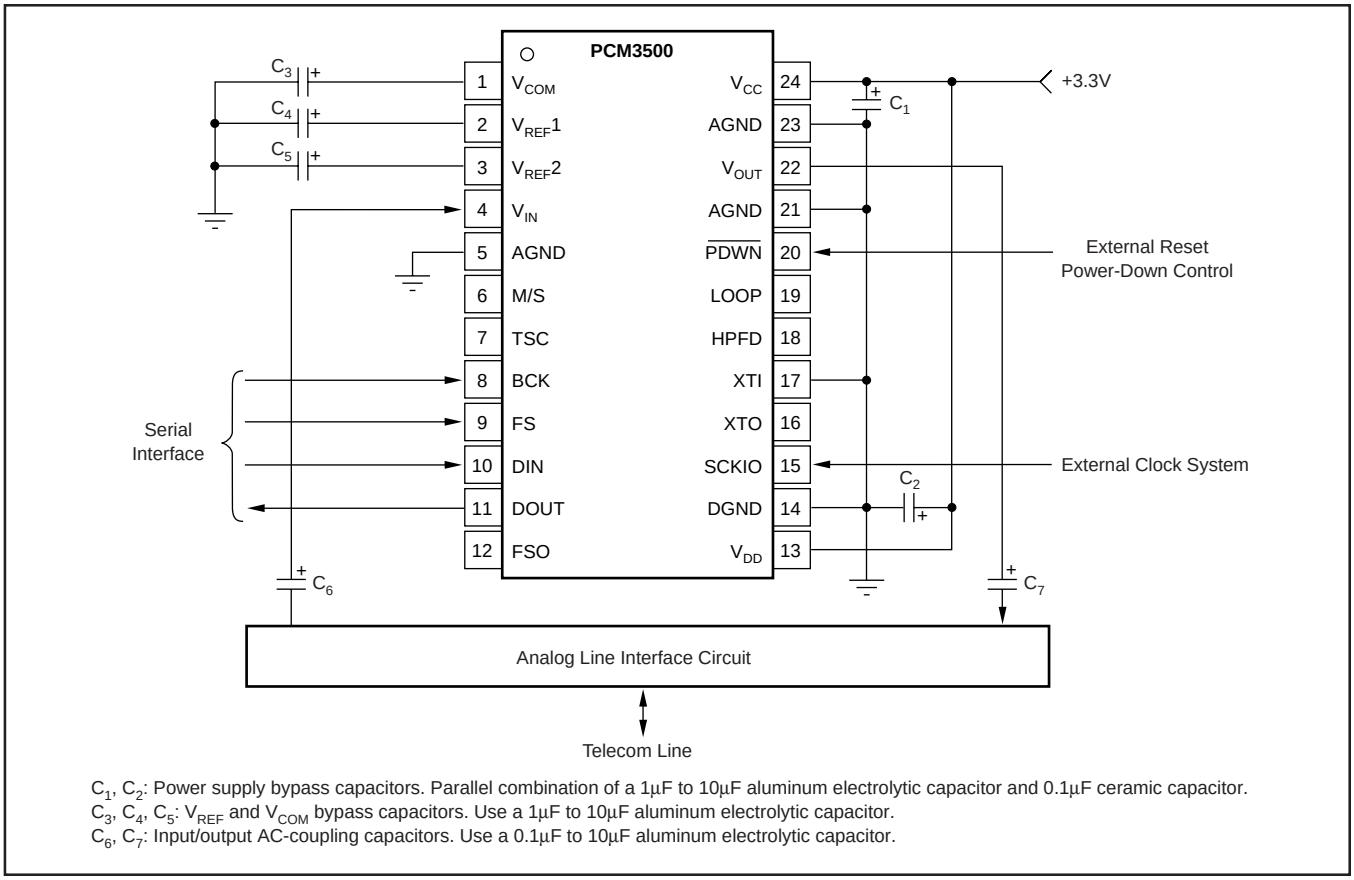
## BASIC CIRCUIT CONNECTIONS

The basic connection diagram for the PCM3500 is shown in Figure 16. Included are the required power supply bypass and reference decoupling capacitors. The DAC output, $V_{OUT}$, and the ADC input, $V_{IN}$, should be AC-coupled to external circuitry.

### Reference Pin Connections

The $V_{COM}$ voltage is used internally to bias the input and output amplifier stages of the PCM3500. It is brought out unbuffered on pin 1 for decoupling. A 1µF to 10µF aluminum electrolytic or tantalum capacitor is recommended for decoupling purposes. This capacitor should be located as close as possible to pin 1.

The $V_{COM}$ voltage is typically equal to $V_{CC}/2$, and may be used to bias external input and output circuitry. However, since the $V_{COM}$ pin is not a buffered output, it must drive a high impedance load to avoid excessive loading. Buffering the $V_{COM}$ pin with an external op amp configured as a voltage follower is recommended when driving multiple bias nodes. Figure 17 shows examples of using $V_{COM}$ with external circuitry.




$C_1$, $C_2$: Power supply bypass capacitors. Parallel combination of a 1µF to 10µF aluminum electrolytic capacitor and 0.1µF ceramic capacitor.
$C_3$, $C_4$, $C_5$: $V_{REF}$ and $V_{COM}$ bypass capacitors. Use a 1µF to 10µF aluminum electrolytic capacitor.
$C_6$, $C_7$: Input/output AC-coupling capacitors. Use a 0.1µF to 10µF aluminum electrolytic capacitor.

FIGURE 16. Basic Connection Diagram.

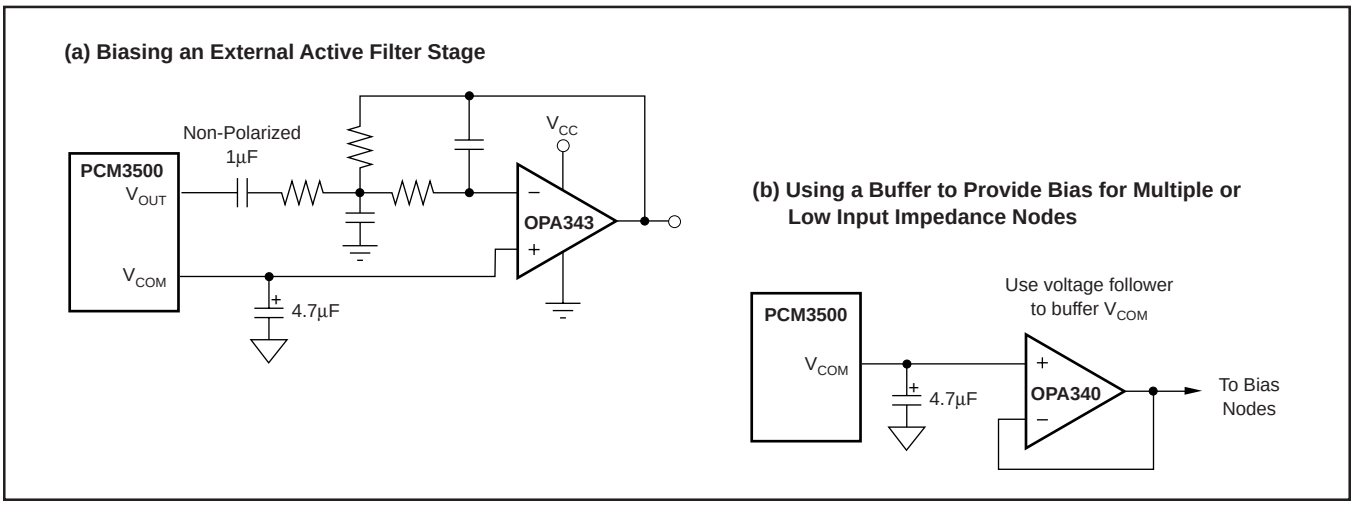



FIGURE 17. Using $V_{COM}$ to Bias External Circuitry.

$V_{REF}1$ (pin 2) and $V_{REF}2$ (pin 3) are reference voltages used by the delta-sigma modulators. They are brought out strictly for decoupling purposes. $V_{REF}1$ and $V_{REF}2$ are not to be used to bias external circuits. A 1µF to 10µF aluminum electrolytic or tantalum capacitor is recommended for decoupling on each pin. These capacitors should be located as close as possible to pins 2 and 3.

### Power Supplies and Grounding

$V_{CC}$ (pin 24) and $V_{DD}$ (pin 13) should be connected directly to the +2.7V to +3.6V analog power supply, as shown in Figure 16. The AGNDs (pins 5, 21, and 23) and DGND (pin 14) should be connected directly to the analog ground. Power supply bypass capacitors should be located as close to the power supply pins as possible in order to ensure a low impedance connection. A combination of a 10µF aluminum electrolytic or tantalum capacitor in parallel with a 0.1µF ceramic capacitor is recommended for both $V_{CC}$ and $V_{DD}$.

$V_{DD}$ and $V_{CC}$ should not be connected to separate digital and analog power supplies. This can lead to an SCR latch-up condition, which can cause either degraded device performance or catastrophic failures.

## PCB LAYOUT GUIDELINES

The recommended PCB layout technique is shown in Figure 18. The analog and digital section of the board are separated by a split ground plane, with the PCM3500 positioned entirely over the analog section of the board. The AGNDs (pins 5, 20, and 23) and DGND (pin 14) are connected directly to the analog ground plane. The power supply pins, $V_{CC}$ (pin 13) and $V_{DD}$ (pin 24), are routed directly to the +2.7V to +3.6V analog power supply using wide copper traces (100 mils or wider recommended) or a power plane. Power supply bypass and reference decoupling capacitors are shown located as close as possible to the PCM3500.

The PCM3500 is oriented so that the digital pins are facing the ground plane split. Digital connections should be made as short and direct as possible to limit high frequency radiation and coupling. Series resistors (from 20Ω to 100Ω) may be put in series with the system clock, FS, BCK, and FSO lines to reduce or eliminate overshoot on clock edges, further reducing radiated emissions. The split ground plane should be connected at one point by a trace, wire, or ferrite bead. Often the board will be designed to have several jumper points for the common ground connection, so that the best performance can be derived through experimentation.

An alternative technique, using a single power supply or battery, is shown in Figure 19. This technique is more suitable for portable applications.

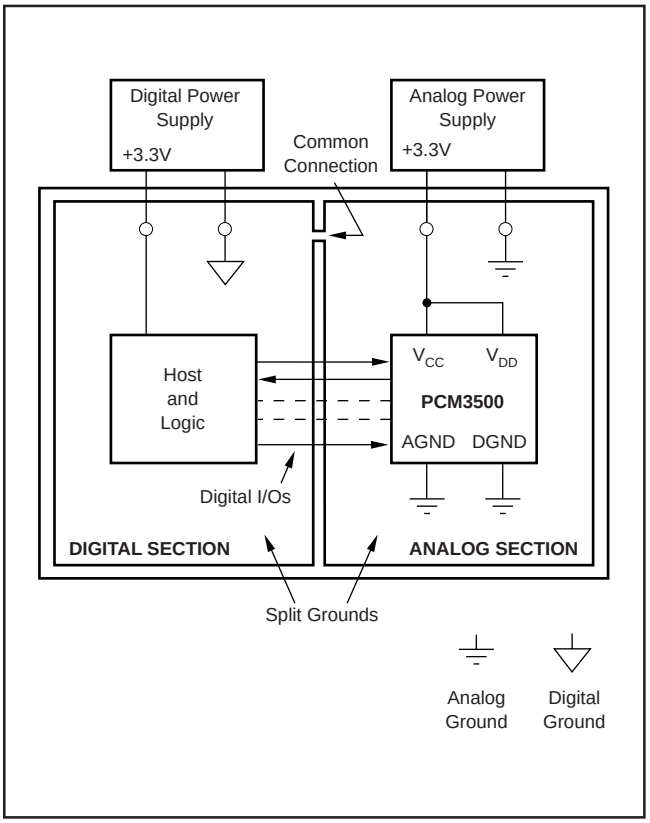



FIGURE 18. Recommended PCB Layout Technique.

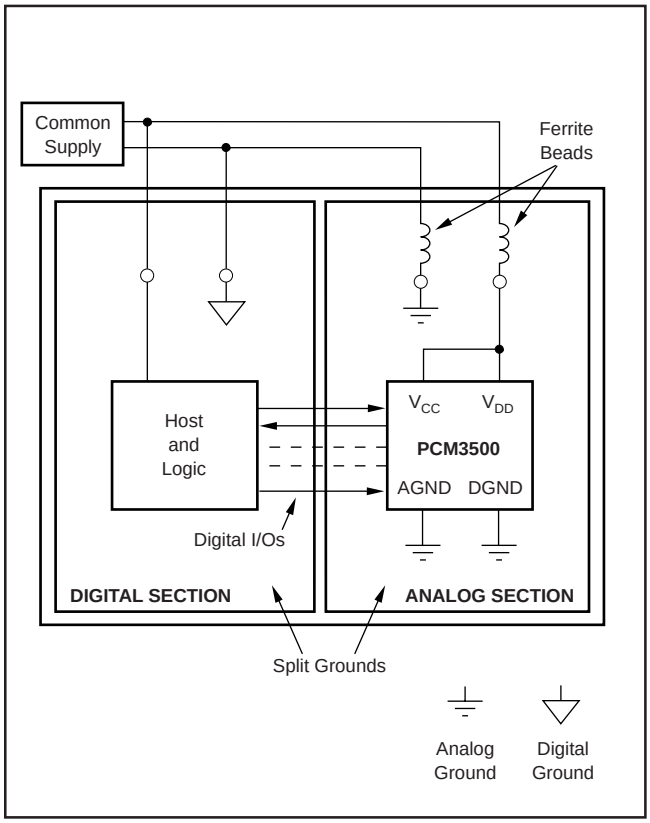



FIGURE 19. PCB Layout Using a Single-Supply or Battery.

## OUTPUT FILTER CIRCUITS FOR THE DAC

The PCM3500's DAC uses delta-sigma conversion techniques. It uses oversampling and noise shaping to improve in-band ($f = f_S/2$) signal-to-noise performance at the expense of increased out-of-band noise. The DAC output must be low-pass filtered to attenuate the out-of-band noise to a reasonable level.

The PCM3500 includes a low-pass filter in the on-chip output amplifier circuit. The frequency response for this filter is shown in Figure 20. Although this filter helps to lower the out-of-band noise, it is not adequate for many applications. This is especially true for applications where the sampling frequency is below 16kHz, since the out-of-band noise above $f_S/2$ is in the audio spectrum. An external filter circuit, either passive or active, is required to provide additional attenuation of the out-of-band noise. The low-pass filter order will be dependent upon the out-of-band noise requirements for a particular system. Generally, a 2nd-order or better low-pass circuit will be required, with the cut-off frequency set to $f_S/2$ or less.

Burr-Brown Application Bulletin AB-034 provides information for designing both Multiple Feedback and Sallen-Key active filter circuits using software available from Burr-Brown's web site. Another excellent reference for both passive and active filter design is the *"Electronic Filter Design Handbook, Third Edition"* by Williams and Taylor, published by McGraw-Hill.

## ON-CHIP ANALOG FRONT END FOR THE ADC

The PCM3500 A/D converter includes a fully differential input delta-sigma modulator. In order to simplify connection for single-ended applications, an analog front end (AFE) circuit has been included on the PCM3500 just prior to the modulator. The AFE circuit is shown in Figure 21.

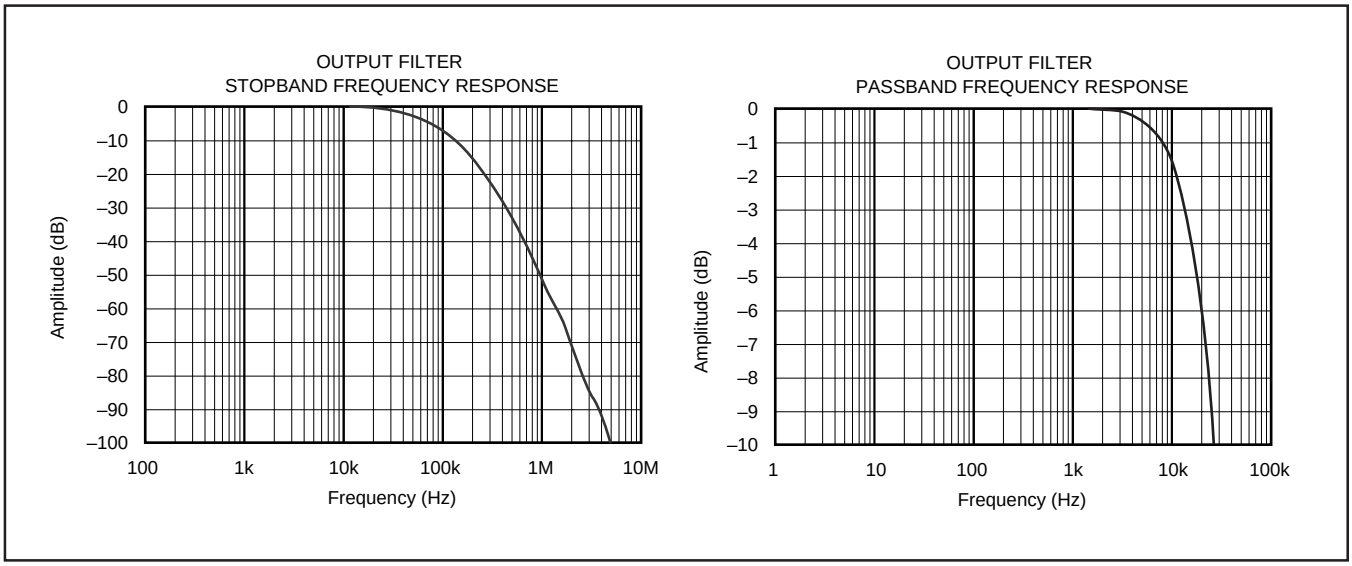



FIGURE 20. DAC Output Amplifier Filter Response.

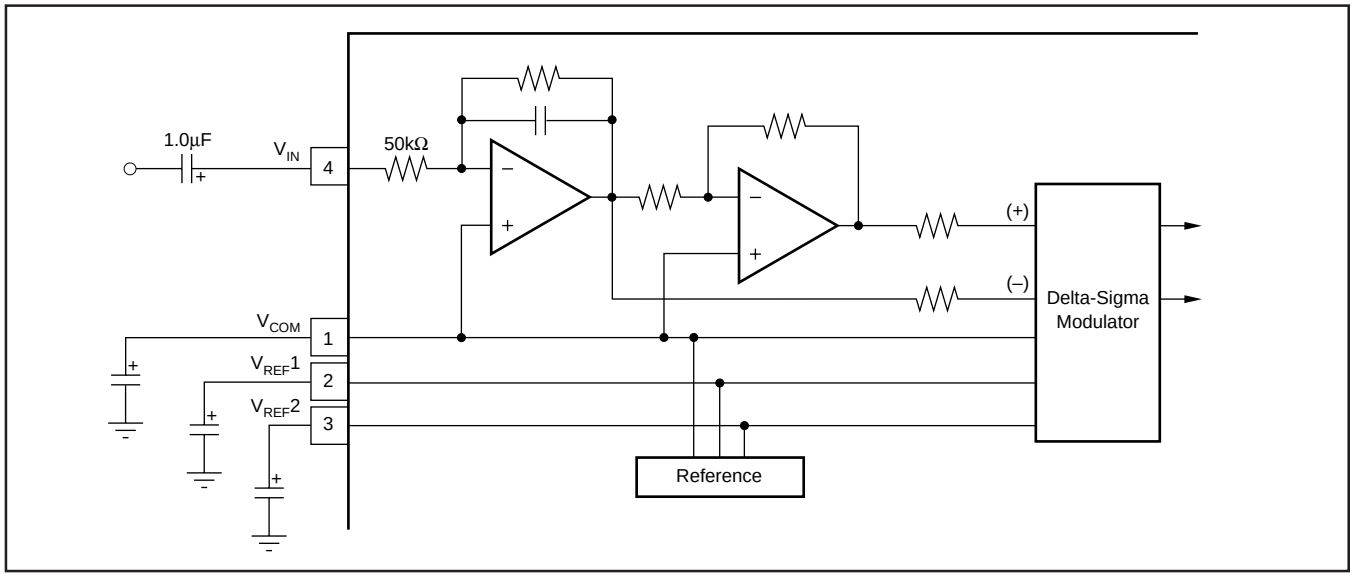



FIGURE 21. On-Chip AFE Circuit for the ADC.

The AFE circuit consists of a single-ended-to-differential converter, with the first stage of the circuit doubling as a low-pass, anti-alias filter. The frequency response for the filter is shown in Figure 22. Since the delta-sigma modulator oversamples the input at $64f_S$, the anti-alias filter requirements are relaxed, with only a single-pole filter being required. If an application requires further band limiting of the input signal, a simple RC filter at the $V_{IN}$ input (pin 4) can be used, as shown in Figure 23.

## SOFTWARE MODEM APPLICATIONS

The PCM3500 was designed to meet the requirements for software-based analog modems, supporting up to 56kbps(1). In a software modem application, the PCM3500 is paired with a Data Access Arrangement (DAA) and a host CPU to provide the complete modem function. Figure 24 shows a simplified block diagram of a software modem using the PCM3500.

The DAA provides the interface between the CODEC and two-wire telephone line. The DAA provides numerous functions, including two-to-four wire conversion, modem-side to line-side isolation, ring detection, hook switch control, line current compensation, and overvoltage protection.

The host CPU provides the data pump and supervisory functions for the software modem application. The host executes modem software code, which includes the necessary routines for transmit and receive functions, error detection and correction, echo cancellation, and CODEC/DAA control and supervision.

NOTE: (1) Data transmission is limited to 53kbps over standard telephone lines. Actual transmission rates vary depending upon the quality of the lines and switching equipment for a given connection.

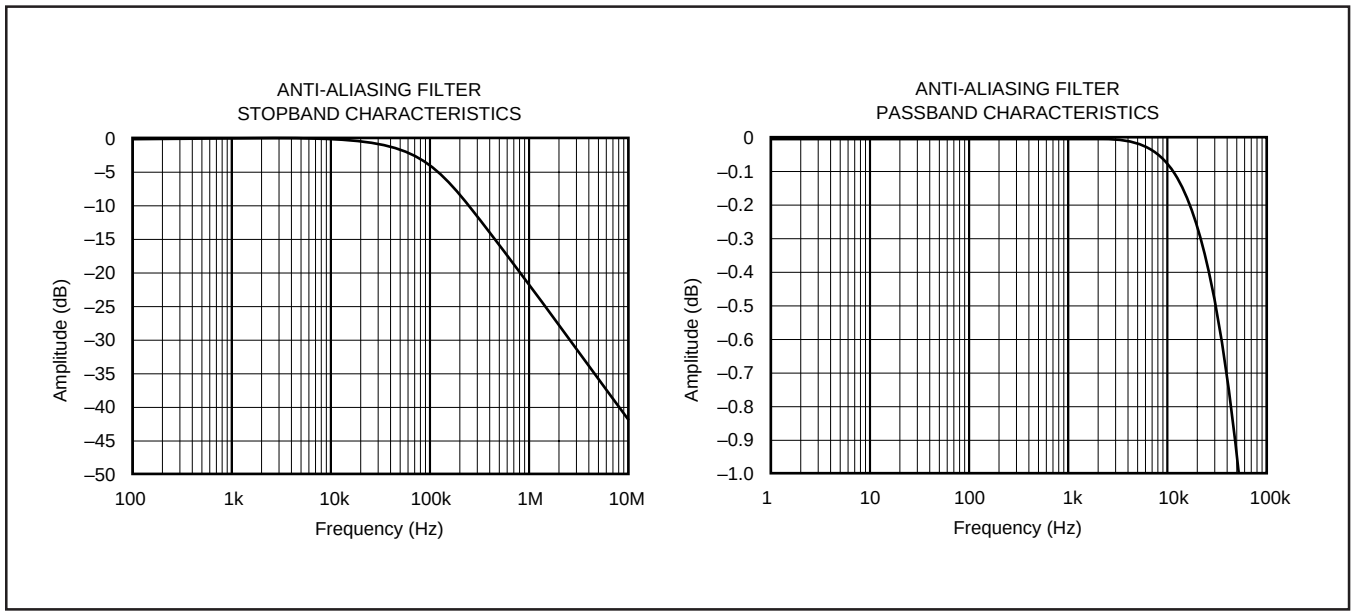



FIGURE 22. Anti-Alias Filter Frequency Response.

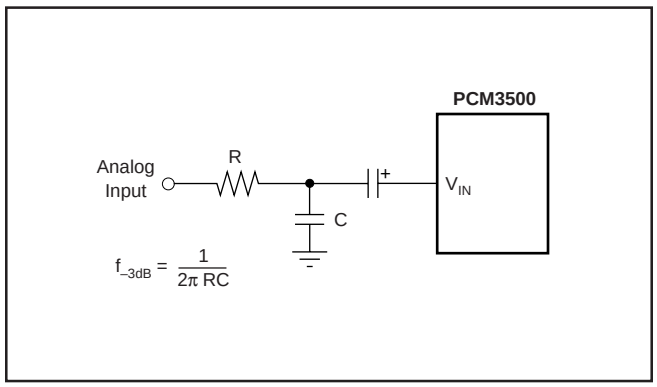



FIGURE 23. Optional External Low-Pass Filter for the ADC.

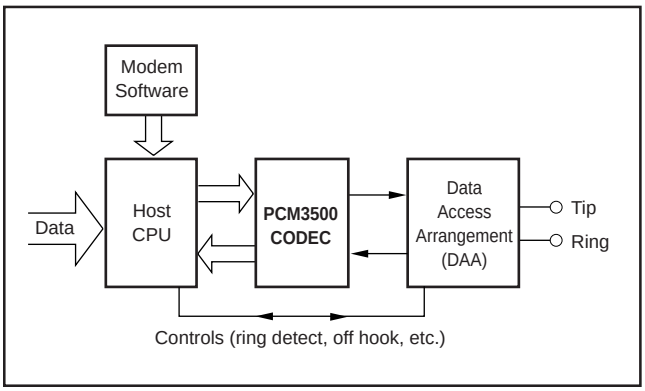



FIGURE 24. Software Modem Block Diagram.

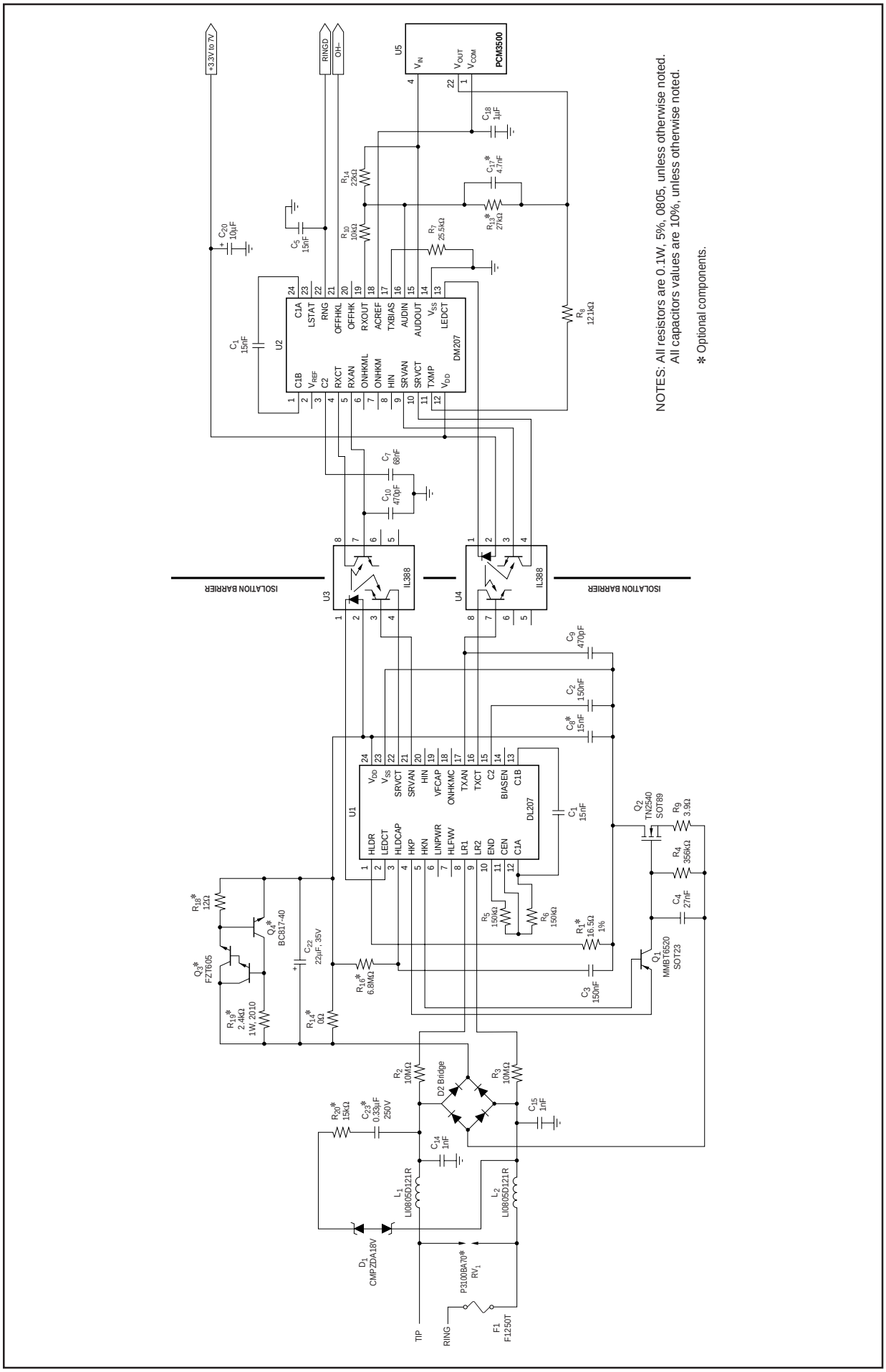



FIGURE 25. Modem AFE Application Circuit.

### Software Modem AFE Application Circuit

Figure 25 shows an applications circuit which utilizes the PCM3500 and the DAA2000 from Infineon Technologies (Siemens) to implement a complete modem AFE. The DAA2000 provides modem-side (DM207) and line-side (DL207) interfaces, with optical isolation separating the functions. The PCM3500 is connected to the modem-side of the DAA2000. The PCM3500's serial interface and hardware mode controls are connected to the host CPU.

# THEORY OF OPERATION

## ADC SECTION

The PCM3500 A/D converter consists of two reference circuits, a mono single-to-differential converter, a fully differential 5th-order delta-sigma modulator, a decimation filter (including digital high pass), and a serial interface circuit. The block diagram on the front page of this data sheet illustrates the architecture of the ADC section, Figure 21 shows the single-to-differential converter, and Figure 26 illustrates the architecture of the 5th-order delta-sigma modulator and transfer functions.

An internal reference circuit with three external capacitors provides all reference voltages which are required by the ADC, which defines the full-scale range for the converter. The internal single-to-differential voltage converter saves the design, space and extra parts needed for external circuitry required by many delta-sigma converters. The internal full-differential signal processing architecture provides a wide dynamic range and excellent power supply rejection performance. The input signal is sampled at a 64x oversampling rate, eliminating the need for a sample-and-hold circuit, and simplifying anti-alias filtering requirements. The 5th-order delta-sigma noise shaper consists of five integrators which use a switched-capacitor topology, a comparator, and a feedback loop consisting of a one-bit DAC. The delta-sigma modulator shapes the quantization noise, shifting it out of the audio band in the frequency domain. The high order of the modulator enables it to randomize the modulator outputs, reducing idle tone levels.

The $64f_S$ one-bit data stream from the modulator is converted to $1f_S$, 16-bit data words by the decimation filter, which also acts as a low-pass filter to remove the shaped quantization noise. The DC components can be removed by a high-pass filter function contained within the decimation filter.

## DAC SECTION

The delta-sigma DAC section of PCM3500 is based on a 5-level amplitude quantizer and a 3rd-order noise shaper. This section converts the oversampled input data to 5-level delta-sigma format. A block diagram of the 5-level delta-sigma modulator is shown in Figure 27. This 5-level delta-sigma modulator has the advantage of stability and clock jitter sensitivity over the typical one-bit (2 level) delta-sigma modulator. The combined oversampling rate of the delta-sigma modulator and the internal 8x interpolation filter is $64f_S$ for a $512f_S$ system clock. The theoretical quantization noise performance of the 5-level delta-sigma modulator is shown in Figure 28.

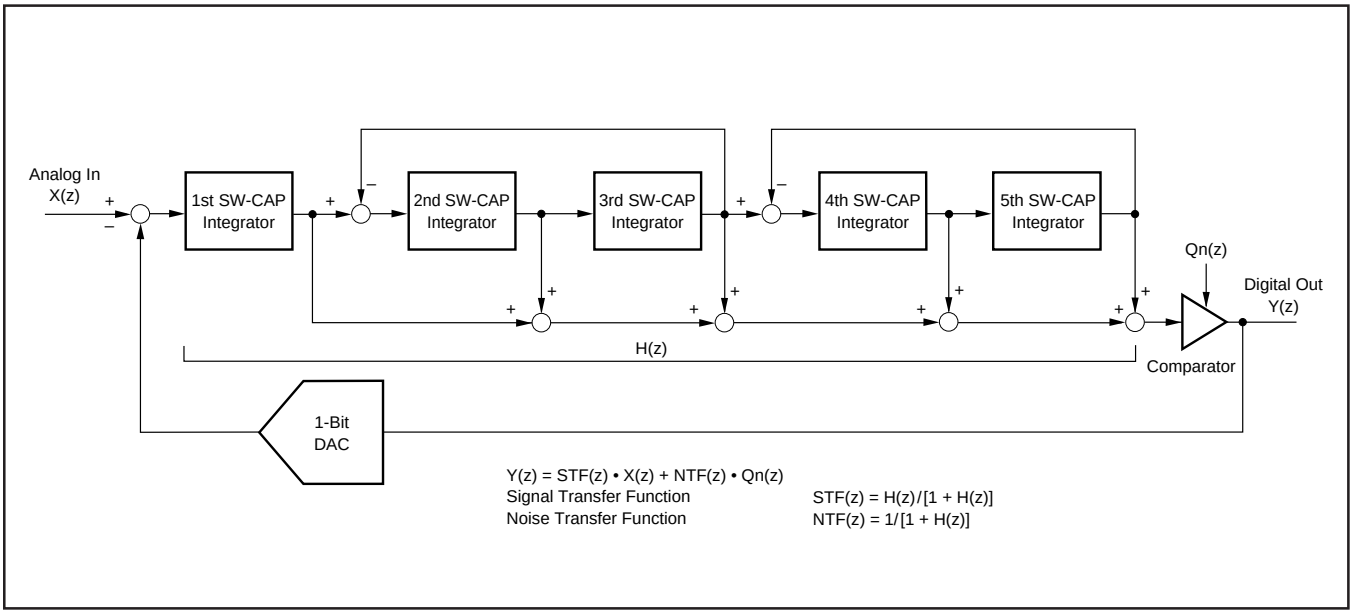



FIGURE 26. Simplified 5th-Order Delta-Sigma Modulator.

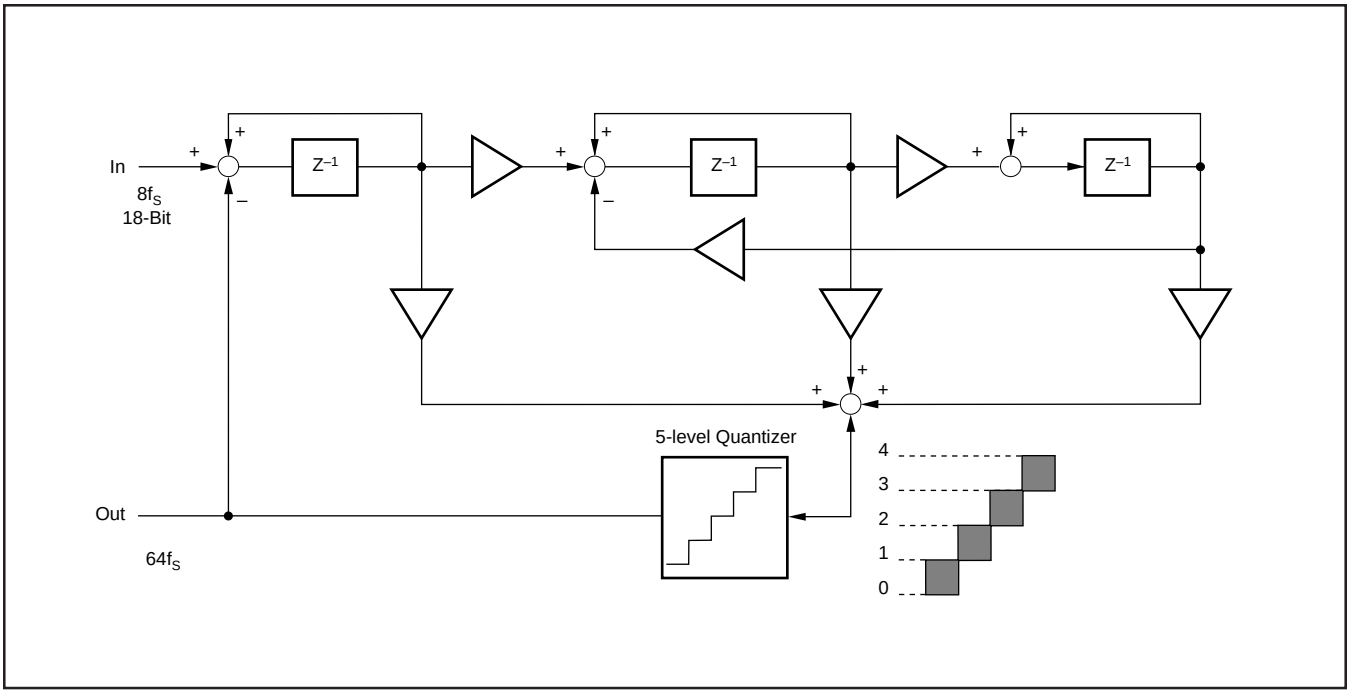



FIGURE 27. 5-Level Delta-Sigma Modulator Block Digram.

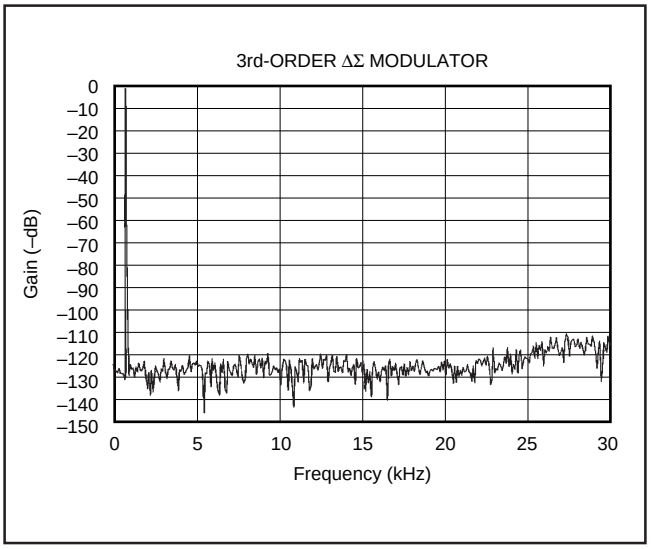



FIGURE 28. Quantization Noise Spectrum.

Multi Level Delta Sigma

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| PCM3500E | Last Time Buy | Production | SSOP (DB) \| 24 | 58 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -25 to 85 | PCM3500E |
| PCM3500E.B | Last Time Buy | Production | SSOP (DB) \| 24 | 58 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -25 to 85 | PCM3500E |
| PCM3500E/2K | Last Time Buy | Production | SSOP (DB) \| 24 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -25 to 85 | PCM3500E |
| PCM3500E/2K.B | Last Time Buy | Production | SSOP (DB) \| 24 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -25 to 85 | PCM3500E |
| PCM3500EG4 | Last Time Buy | Production | SSOP (DB) \| 24 | 58 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | See PCM3500E | PCM3500E |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

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(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

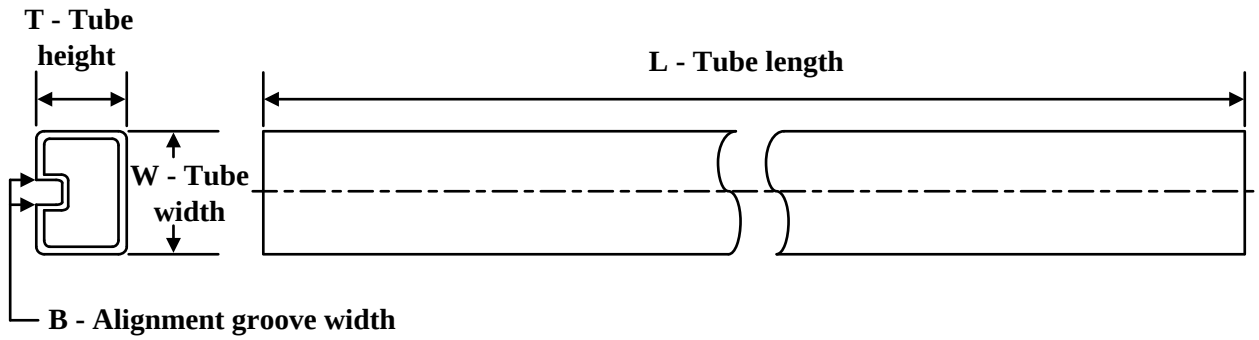
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| PCM3500E | DB | SSOP | 24 | 58 | 500 | 10.6 | 500 | 9.6 |
| PCM3500E.B | DB | SSOP | 24 | 58 | 500 | 10.6 | 500 | 9.6 |
| PCM3500EG4 | DB | SSOP | 24 | 58 | 500 | 10.6 | 500 | 9.6 |

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