Burr-Brown Products
from Texas Instruments

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High-Performance, 24-Bit, 216kHz Sampling, Four-Channel Audio Digital-to-Analog Converter

FEATURES

- Four High-Performance, Multi-Level, Delta-Sigma Digital-to-Analog Converters
- Differential Voltage Outputs
  - Full-Scale Output (Differential): 6.15V_{PP}
- Supports Sampling Frequencies up to 216kHz
- Typical Dynamic Performance (24-Bit Data)
  - Dynamic Range (A-Weighted): 118dB
  - THD+N: −100dB
- Linear Phase, 8x Oversampling Digital Interpolation Filter
- Digital De-Emphasis Filters for 32kHz, 44.1kHz, and 48kHz Sampling Rates
- Soft Mute Function
  - All-Channel Mute via the MUTE Input Pin
  - Per-Channel Mute Available in Software Mode
- Digital Attenuation (Software Mode Only)
  - Attenuation Range: 0dB to −119.5dB
  - 256 Steps with 0.5dB per Step
- Output Phase Inversion (Software Mode Only)
- Zero Data Mute (Software Mode Only)
- Audio Serial Port
  - Supports Left-Justified, Right-Justified, I^2S™, and TDM Data Formats
  - Accepts 16-, 18-, 20, and 24-Bit Two's Complement PCM Audio Data
- Standalone or Software-Controlled Configuration Modes
- Four-Wire Serial Peripheral Interface (SPI™) Port Provides Control Register Access in Software Mode
- Power Supplies: +5V Analog, +3.3V Digital
- Power Dissipation
  - 203mW typical with f_S = 48kHz
  - 220mW typical with f_S = 96kHz
  - 236mW typical with f_S = 192kHz
- Power-Down Modes
- Small 48-Lead TQFP Package

APPLICATIONS

- Digital Mixing Consoles
- Digital Audio Workstations
- Digital Audio Effects Processors
- Broadcast Studio Equipment
- Surround-Sound Processors
- High-End A/V Receivers

DESCRIPTION

The PCM4104 is a high-performance, four-channel digital-to-analog (D/A) converter designed for use in professional audio applications. The PCM4104 supports 16- to 24-bit linear PCM input data, with sampling frequencies up to 216kHz. The PCM4104 features lower power consumption than most comparable stereo audio D/A converters, making it ideal for use in high channel count applications by lowering the overall power budget required for the D/A conversion sub-system.

The PCM4104 features delta-sigma architecture, employing a high-performance multi-level modulator combined with a switched capacitor output filter. This architecture yields lower out-of-band noise and a high tolerance to system clock phase jitter. Differential voltage outputs are provided for each channel and are well-suited to high-performance audio applications. The differential outputs are easily converted to a single-ended output using an external op amp IC.

The PCM4104 includes a flexible audio serial port interface, which supports standard and time division multiplexed (TDM) formats. Support for TDM formats simplifies interfacing to DSP serial ports, while supporting a cascade connection for two PCM4104 devices. In addition, the PCM4104 offers two configuration modes: Standalone and Software-Controlled. The Standalone mode provides dedicated control pins for configuring a subset of the available PCM4104 functions, while Software mode utilizes a serial peripheral interface (SPI) port for accessing the complete feature set via internal control registers.

The PCM4104 operates from a +5V analog power supply and a +3.3V digital power supply. The digital I/O is compatible with +3.3V logic families. The PCM4104 is available in a TQFP-48 package.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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ORDERING INFORMATION(1)

PRODUCT	PACKAGE−LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
PCM4104	TQFP-48	PFB	−10°C to +70°C	PCM4104PFB	PCM4104PFBT	Tape and Reel, 250
					PCM4104PFBR	Tape and Reel, 2000

(1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet, or refer to our web site at www.ti.com.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

		PCM4104	UNIT
Supply voltage	V_{CC}	+6.0	V
	V_{DD}	+3.6	V
Ground voltage difference	Any AGND-to-AGND and AGND-to-DGND	±0.1	V
Digital input voltage	FS0, FS1, FMT0, FMT1, FMT2, CDOUT, CDIN, CCLK, $\overline{CS}$, DATA0, DATA1, BCK, LRCK, SCKI, SUB, DEM0, DEM1, MUTE, $\overline{RST}$, MODE	−0.3 to (V_{DD} + 0.3)	V
Input current (any pin except supplies)		±10	mA
Operating temperature range		−10 to +70	°C
Storage temperature range, T_{STG}		−65 to +150	°C

(1) Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

ELECTRICAL CHARACTERISTICS

All parameters are specified at T_A = +25°C with V_{CC} = +5V, V_{DD} = +3.3V, and a measurement bandwidth from 10Hz to 20kHz, unless otherwise noted. System clock frequency is equal to 256f_S for Single and Dual Rate sampling modes, and 128f_S for Quad Rate sampling mode.

PARAMETER		CONDITIONS	PCM4104 MIN	PCM4104 TYP	PCM4104 MAX	UNITS
RESOLUTION				24		Bits
DATA FORMAT						
Audio data formats			Left or Right Justified, I²S, and TDM			
Audio data word length			16		24	Bits
Binary data format			Two's Complement Binary, MSB First			
CLOCK RATES AND TIMING						
System clock frequency	f_{SCKI}	Single rate sampling mode	6.144		36.864	MHz
		Dual rate sampling mode	13.824		36.864	MHz
		Quad rate sampling mode	13.824		36.864	MHz
Sampling frequency	f_S	Single rate sampling mode	24		54	kHz
		Dual rate sampling mode	54		108	kHz
		Quad rate sampling mode	108		216	kHz
SPI port data clock	f_{CCLK}				24	MHz
SPI port data clock high time	t_{CCLKH}		15			ns
SPI port data clock low time	t_{CCLKL}		15			ns
DIGITAL INPUT/OUTPUT						
Input logic level	V_{IH}		2.0			V
	V_{IL}				0.8	V
Input logic current	I_{IH}	$V_{IN} = V_{DD}$		1	10	µA
	I_{IL}	V_{IN} = 0V		1	−10	µA
Output logic level	V_{OH}	I_{OH} = −2mA	2.4			V
	V_{OL}	I_{OH} = +2mA			0.4	V
ANALOG OUTPUTS						
Full-scale output voltage, differential		R_L = 600Ω		6.15		V_{PP}
Bipolar zero voltage				2.5		V
Output impedance				5		Ohms
Switched capacitor filter frequency response		f = 20kHz, all sampling modes		−0.2		dB
Gain error				0.5		% FSR
Gain mismatch, channel-to-channel				0.6		% FSR
Bipolar zero error				1		mV
$V_{COM}1$ and $V_{COM}2$ output voltage		V_{CC} = +5V		2.5		V
$V_{COM}1$ and $V_{COM}2$ output current					200	µA

ELECTRICAL CHARACTERISTICS (continued)

All parameters are specified at T_A = +25°C with V_{CC} = +5V, V_{DD} = +3.3V, and a measurement bandwidth from 10Hz to 20kHz, unless otherwise noted. System clock frequency is equal to 256f_S for Single and Dual Rate sampling modes, and 128f_S for Quad Rate sampling mode.

PARAMETER		CONDITIONS	PCM4104 MIN	PCM4104 TYP	PCM4104 MAX	UNITS
DYNAMIC PERFORMANCE WITH 24-BIT DATA(1)						
f_S = 48kHz						
Total harmonic distortion + noise	THD+N	f = 1kHz at 0dBFS		−100	−94	dB
		f = 1kHz at −60dBFS		−56		dB
Dynamic range, A-weighted		f = 1kHz at −60dBFS	112	118		dB
Idle channel SNR, A-weighted		All zero input data		119		dB
Idle channel SNR, unweighted		All zero input data		116		dB
Channel separation		f = 1kHz at 0dBFS for active channel	100	110		dB
f_S = 96kHz						
Total harmonic distortion + noise	THD+N	f = 1kHz at 0dBFS, BW = 10Hz to 40kHz		−100		dB
		f = 1kHz at −60dBFS, BW = 10Hz to 40kHz		−53		dB
Dynamic range, A-weighted		f = 1kHz at −60dBFS		118		dB
Idle channel SNR, A-weighted		All zero input data		119		dB
Idle channel SNR, unweighted		All zero input data, BW = 10Hz to 40kHz		113		dB
Channel separation		f = 1kHz at 0dBFS for active channel		110		dB
fs = 192kHz						
Total harmonic distortion + noise	THD+N	f = 1kHz at 0dBFS, BW = 10Hz to 40kHz		−97		dB
		f = 1kHz at −60dBFS, BW = 10Hz to 40kHz		−53		dB
Dynamic range, A-weighted		f = 1kHz at −60dBFS		118		dB
Idle channel SNR, A-weighted		All zero input data		118		dB
Idle channel SNR, unweighted		All zero input data, BW = 10Hz to 40kHz		113		dB
Channel separation		f = 1kHz at 0dBFS for active channel		110		dB
DYNAMIC PERFORMANCE WITH 16-BIT DATA						
fs = 44.1kHz						
Total harmonic distortion + noise	THD+N	f = 1kHz at 0dBFS		−92		dB
		f = 1kHz at −60dBFS		−33		dB
Dynamic Range, A-weighted		f = 1kHz at −60dBFS		96		dB
Idle channel SNR, A-weighted(2)		All zero input data		118		dB
Idle channel SNR, unweighted(2)		All zero input data		115		dB

(1) Dynamic performance parameters are measured using an Audio Precision System Two Cascade or Cascade Plus test system. Input data word length is 24 bits with triangular PDF dither added for dynamic range and THD+N tests. Idle channel SNR is measured with both the soft and zero data mute functions disabled and 0% full-scale input data with no dither applied. The measurement bandwidth is limited by using the Audio Precision 10Hz high-pass filter in combination with either the AES17 20kHz low-pass filter or AES17 40kHz low-pass filter. All A-weighted measurements are performed using the Audio Precision A-weighting filter in combination with either the 22kHz or 80kHz low-pass filter. Measurement mode is set to RMS for all parameters. The AVERAGE measurement mode will yield better typical performance numbers.

(2) Idle Channel SNR is not limited by word length.

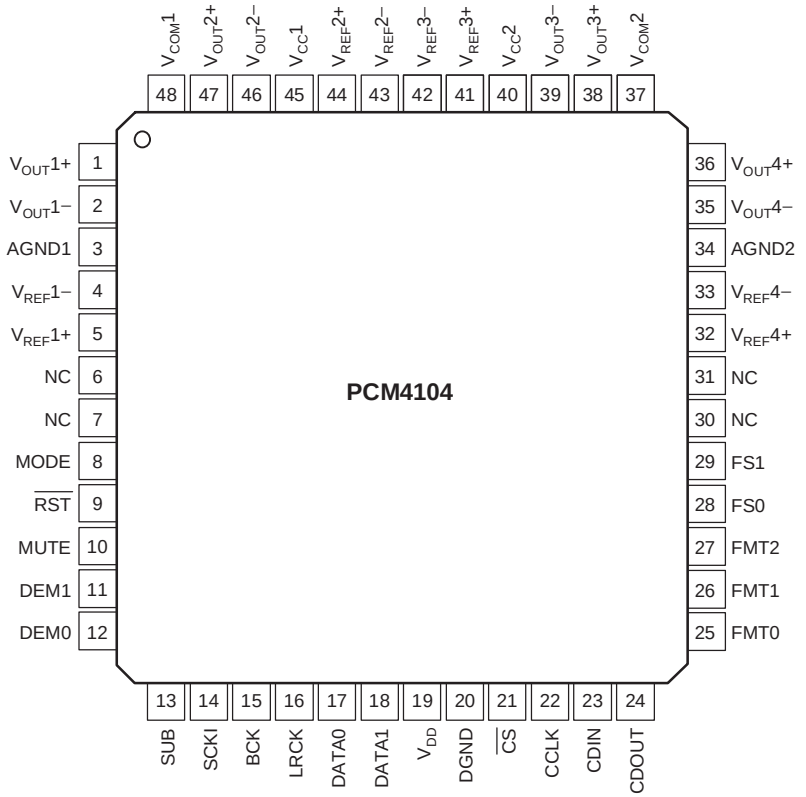
ELECTRICAL CHARACTERISTICS (continued)

All parameters are specified at T_A = +25°C with V_{CC} = +5V, V_{DD} = +3.3V, and a measurement bandwidth from 10Hz to 20kHz, unless otherwise noted. System clock frequency is equal to 256f_S for Single and Dual Rate sampling modes, and 128f_S for Quad Rate sampling mode.

PARAMETER	CONDITIONS	PCM4104			UNITS
		MIN	TYP	MAX	
DIGITAL FILTERS					
Passband	±0.002dB			0.454f_S	Hz
	−3dB			0.487f_S	Hz
Stop Band		0.546fs			Hz
Passband ripple				±0.002	dB
Stopband attenuation	0.546fs	−75			dB
	0.567fs	−82			dB
Group delay			29/f_S		sec
De-emphasis filter error				0.1	dB
POWER SUPPLY					
Supply Range					
Analog supply, V_{CC}		+4.75	+5.0	+5.25	V
Digital supply, V_{DD}		+3.0	+3.3	+3.6	V
Power down current	**V_{CC} = +5V, VDD = +3.3V**				
Power-down supply current, I_{CC} + I_{DD}	$\overline{RST}$ = low, system and audio clocks off		1		mA
Quiescent current	**System and audio clocks applied, all 0s data**				
Analog supply, I_{CC}	V_{CC} = +5V, f_S =48kHz		32	40	mA
	V_{CC} = +5V, f_S =96kHz		32		mA
	V_{CC} = +5V, f_S =192kHz		32		mA
Digital supply, I_{DD}	V_{DD} = +3.3V, f_S =48kHz		13	17	mA
	V_{DD} = +3.3V, f_S =96kHz		18		mA
	V_{DD} = +3.3V, f_S =192kHz		23		mA
Total power dissipation	V_{CC} = +5V, V_{DD} = +3.3V				
	f_S = 48kHz		203	256	mW
	f_S = 96kHz		220		mW
	f_S = 192kHz		236		mW

PIN ASSIGNMENTS

TQFP PACKAGE
(TOP VIEW)



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
$V_{OUT}1+$	1	Output	Channel 1 Analog Output, Noninverted
$V_{OUT}1-$	2	Output	Channel 1 Analog Output, Inverted
AGND1	3	Ground	Analog Ground
$V_{REF}1-$	4	Input	Channel 1 Low Reference Voltage; Connect to AGND
$V_{REF}1+$	5	Input	Channel 1 High Reference Voltage; Connect to V_{CC}
NC	6		No Internal Connection
NC	7		No Internal Connection
MODE	8	Input	Operating Mode (0 = Standalone, 1= Software Controlled)
$\overline{RST}$	9	Input	Reset/Power Down (Active Low)
MUTE	10	Input	All−Channel Soft Mute (Active High)
DEM1	11	Input	Digital De-Emphasis Filter Configuration
DEM0	12	Input	Digital De-Emphasis Filter Configuration
SUB	13	Input	Sub-Frame Assignment (TDM Formats Only)
SCKI	14	Input	System Clock

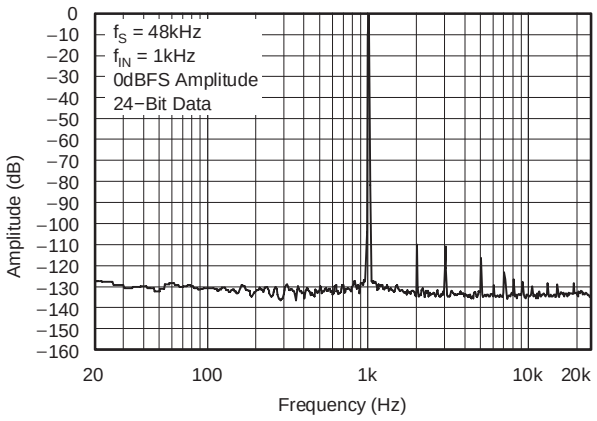
Terminal Functions (continued)

TERMINAL NAME	NO.	I/O	DESCRIPTION
BCK	15	Input	Audio Bit (or Data) Clock
LRCK	16	Input	Audio Left/Right (or Word) Clock
DATA0	17	Input	Audio Data for Channels 1 and 2 (I^2S, Left/Right Justified formats) or Audio Data for Channels 1 Through 4 for TDM Formats
DATA1	18	Input	Audio Data for Channels 3 and 4 (I^2S, Left/Right Justified formats)
V_{DD}	19	Power	Digital Power Supply, +3.3V
DGND	20	Ground	Digital Ground
$\overline{CS}$	21	Input	Serial Peripheral Interface (SPI) Chip Select (Active Low)
CCLK	22	Input	Serial Peripheral Interface (SPI) Data Clock
CDIN	23	Input	Serial Peripheral Interface (SPI) Data Input
CDOUT	24	Output	Serial Peripheral Interface (SPI) Data Output
FMT0	25	Input	Audio Data Format Configuration
FMT1	26	Input	Audio Data Format Configuration
FMT2	27	Input	Audio Data Format Configuration
FS0	28	Input	Sampling Mode Configuration
FS1	29	Input	Sampling Mode Configuration
NC	30		No Internal Connection
NC	31		No Internal Connection
$V_{REF}4+$	32	Input	Channel 4 High Reference Voltage; Connect to V_{CC}
$V_{REF}4-$	33	Input	Channel 4 Low Reference Voltage; Connect to AGND
AGND2	34	Ground	Analog Ground
$V_{OUT}4-$	35	Output	Channel 4 Analog Output, Inverted
$V_{OUT}4+$	36	Output	Channel 4 Analog Output, Noninverted
$V_{COM}2$	37	Output	DC Common-Mode Voltage for Channels 3 and 4, +2.5V nominal
$V_{OUT}3+$	38	Output	Channel 3 Analog Output, Noninverted
$V_{OUT}3-$	39	Output	Channel 3 Analog Output, Inverted
$V_{CC}2$	40	Power	Analog Power Supply, +5V
$V_{REF}3+$	41	Input	Channel 3 High Reference Voltage; Connect to V_{CC}
$V_{REF}3-$	42	Input	Channel 3 Low Reference Voltage,; Connect to AGND
$V_{REF}2-$	43	Input	Channel 2 Low Reference Voltage; Connect to AGND
$V_{REF}2+$	44	Input	Channel 2 High Reference Voltage; Connect to V_{CC}
$V_{CC}1$	45	Power	Analog Power Supply, +5V
$V_{OUT}2-$	46	Output	Channel 2 Analog Output, Inverted
$V_{OUT}2+$	47	Output	Channel 2 Analog Output, Noninverted
$V_{COM}1$	48	Output	DC Common-Mode Voltage for Channels 1 and 2, +2.5V nominal

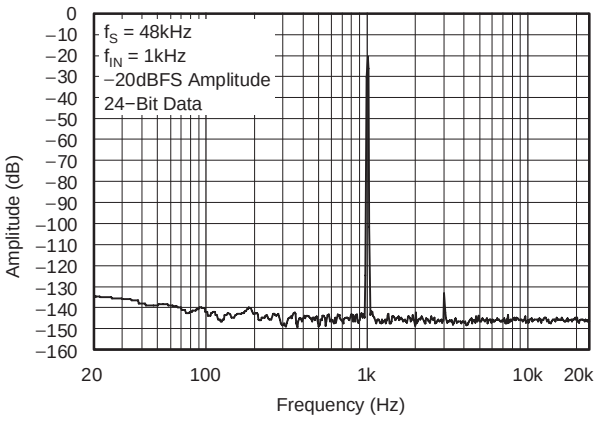
TYPICAL CHARACTERISTICS

All parameters are specified at T_A = +25°C with V_{CC} = +5V, V_{DD} = +3.3V, and a measurement bandwidth from 10Hz to 20kHz, unless otherwise noted. System clock frequency is equal to 256f_S for Single and Dual Rate sampling modes, and 128f_S for Quad Rate sampling mode.

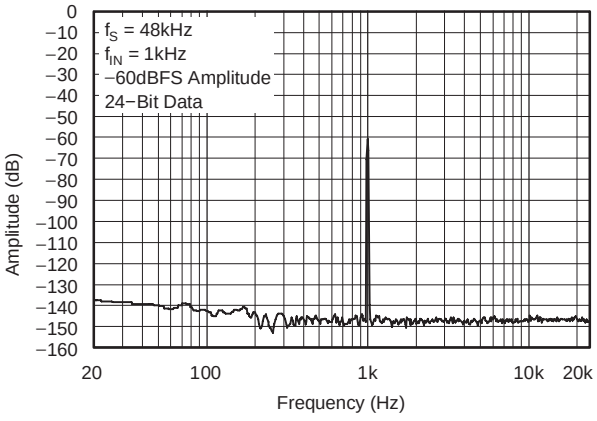
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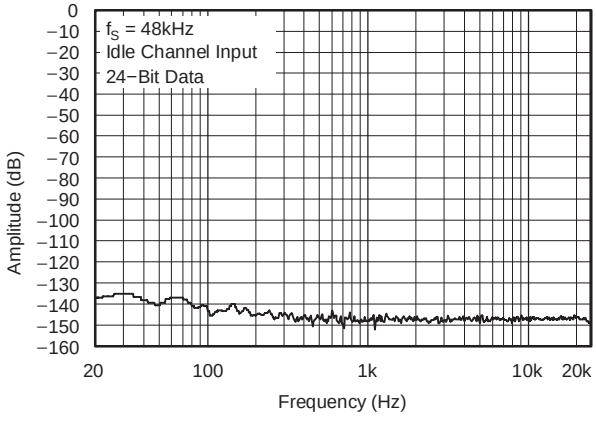
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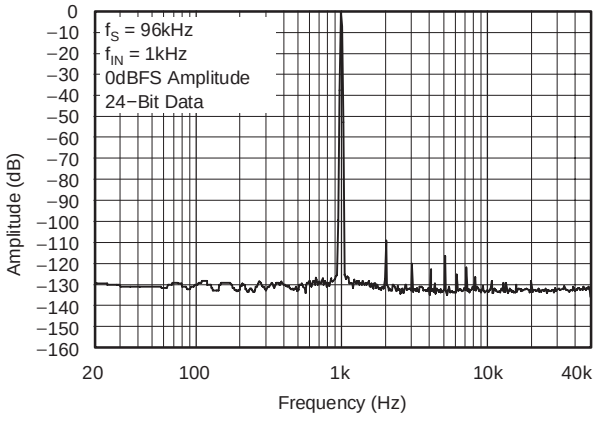
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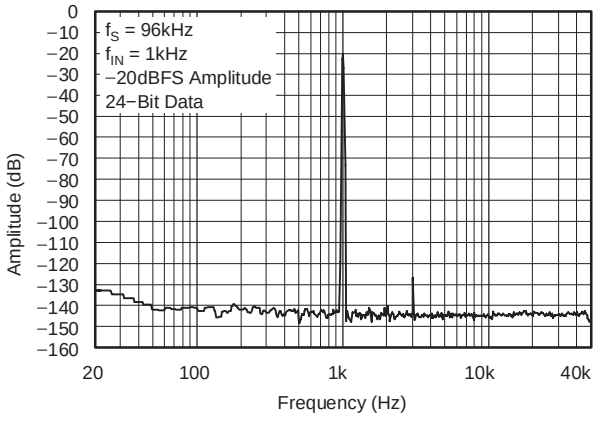
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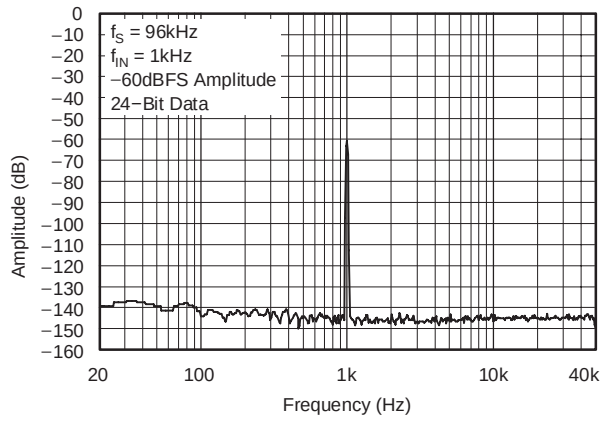
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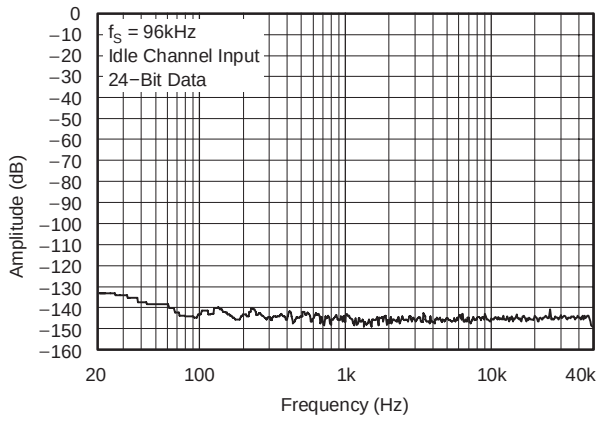
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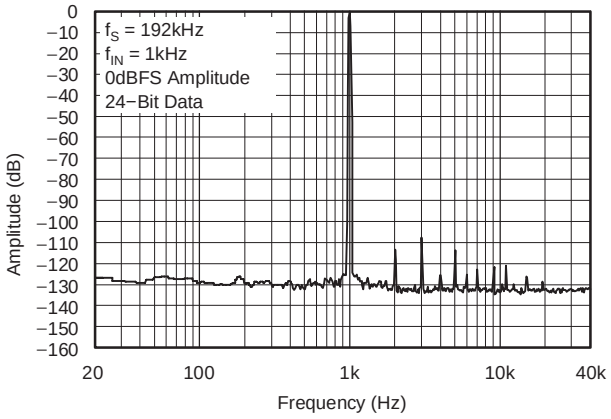
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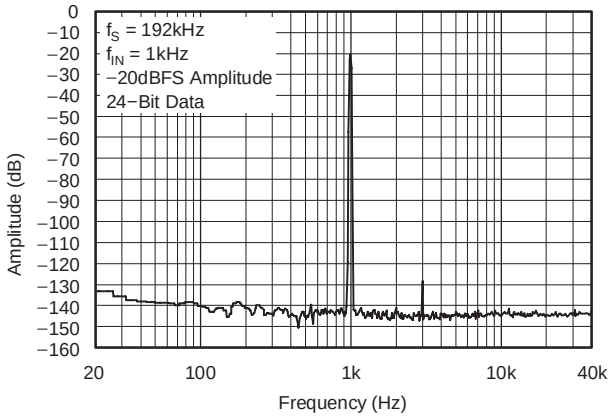
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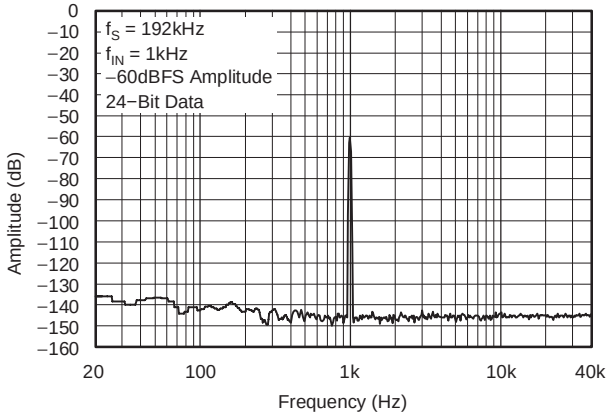
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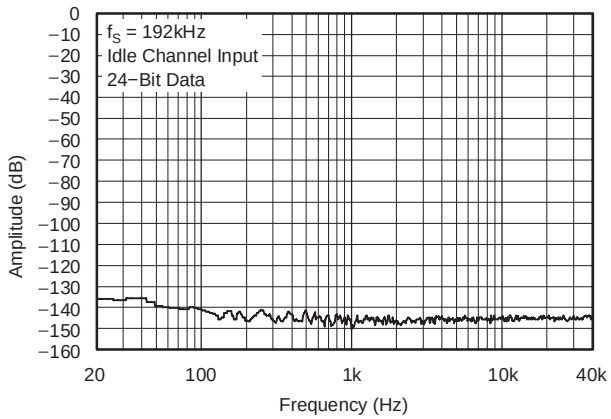
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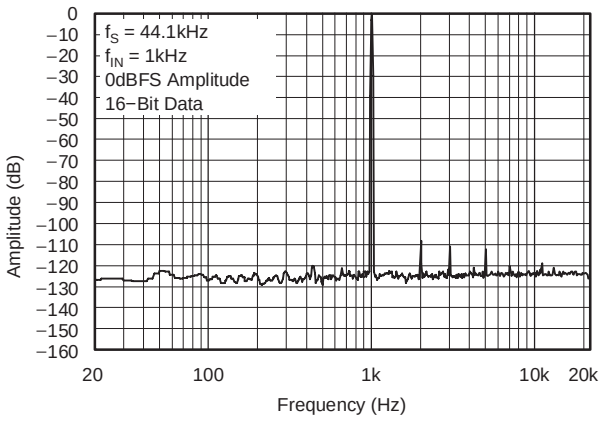
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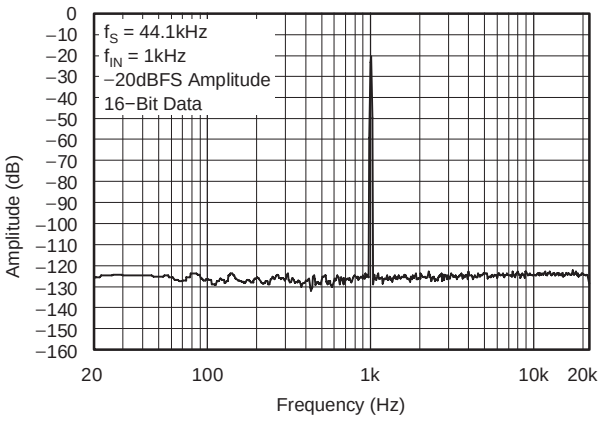
TYPICAL CHARACTERISTICS (continued)

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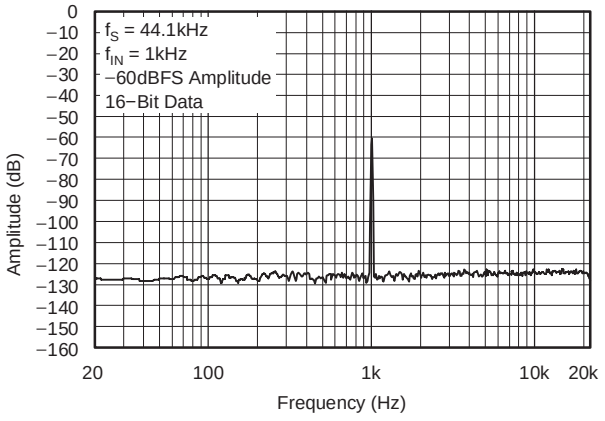
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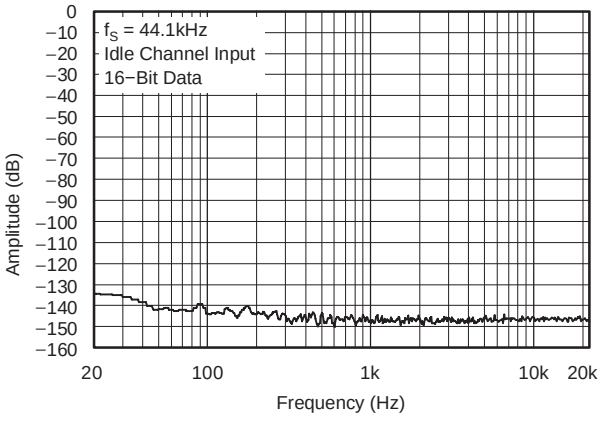
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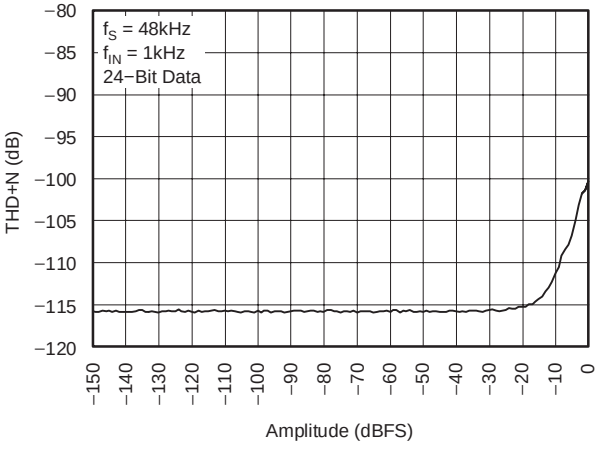
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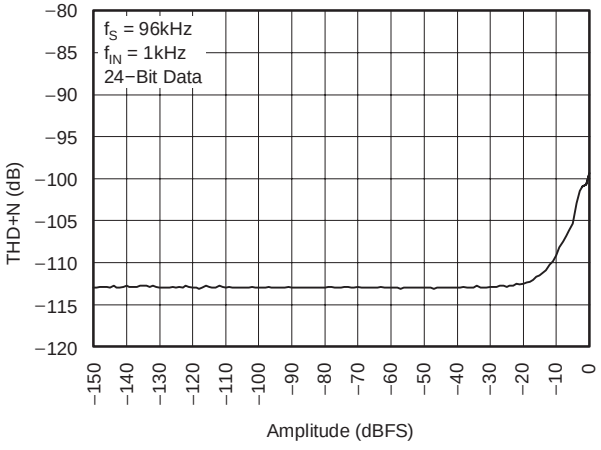
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THD+N vs AMPLITUDE



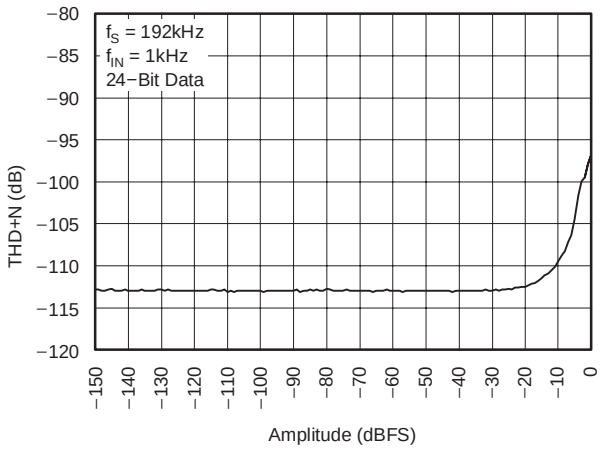
THD+N vs AMPLITUDE



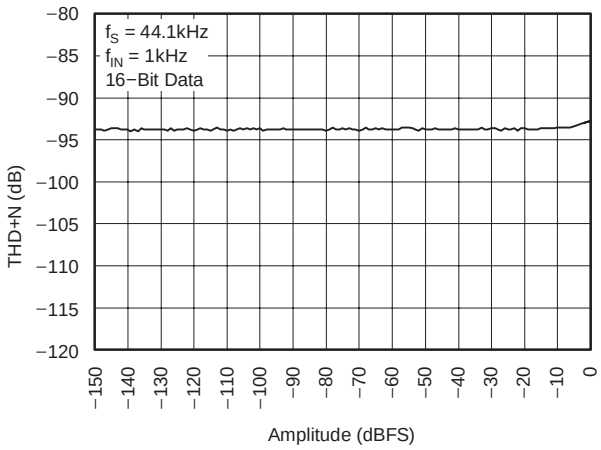
TYPICAL CHARACTERISTICS (continued)

All parameters are specified at T_A = +25°C with V_{CC} = +5V, V_{DD} = +3.3V, and a measurement bandwidth from 10Hz to 20kHz, unless otherwise noted. System clock frequency is equal to 256f_S for Single and Dual Rate sampling modes, and 128f_S for Quad Rate sampling mode.

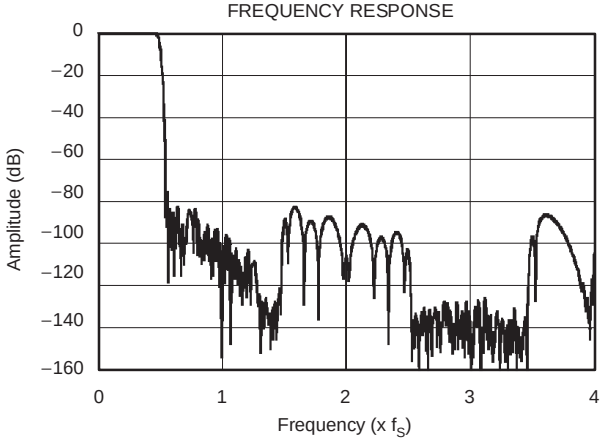
THD+N vs AMPLITUDE



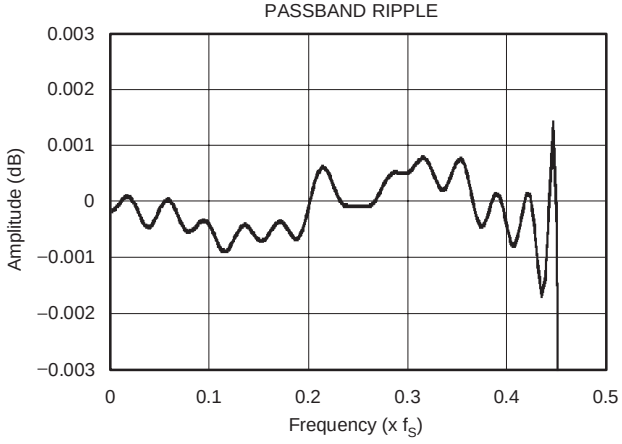
THD+N vs AMPLITUDE



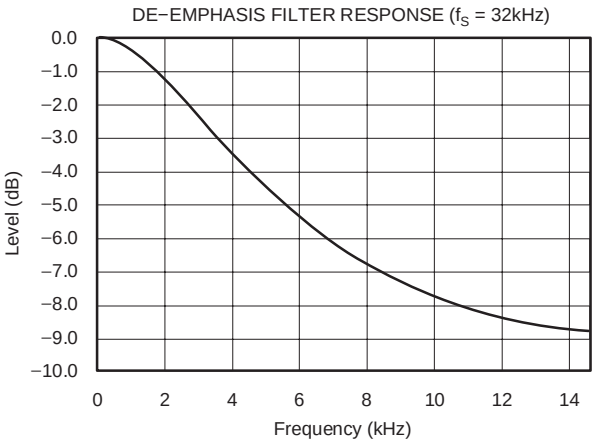
FREQUENCY RESPONSE



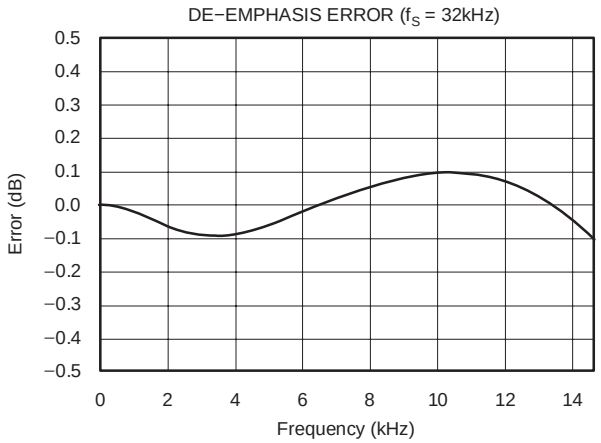
PASSBAND RIPPLE



DE−EMPHASIS FILTER RESPONSE (f_S = 32kHz)



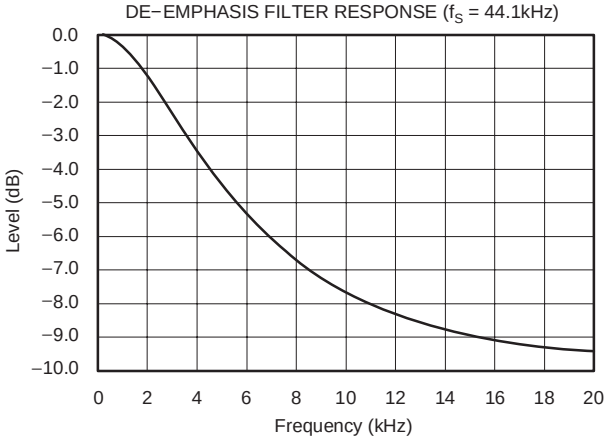
DE−EMPHASIS ERROR (f_S = 32kHz)



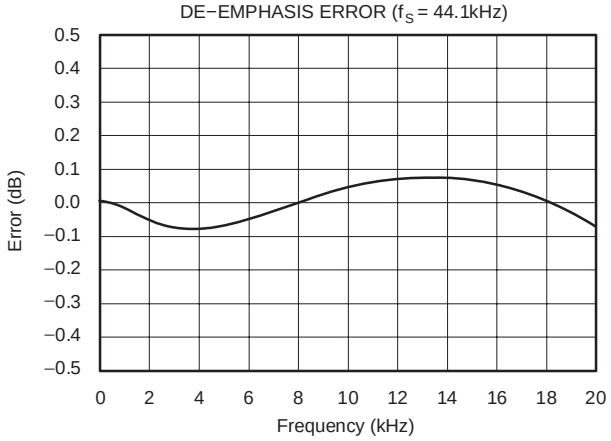
TYPICAL CHARACTERISTICS (continued)

All parameters are specified at T_A = +25°C with V_{CC} = +5V, V_{DD} = +3.3V, and a measurement bandwidth from 10Hz to 20kHz, unless otherwise noted. System clock frequency is equal to 256f_S for Single and Dual Rate sampling modes, and 128f_S for Quad Rate sampling mode.

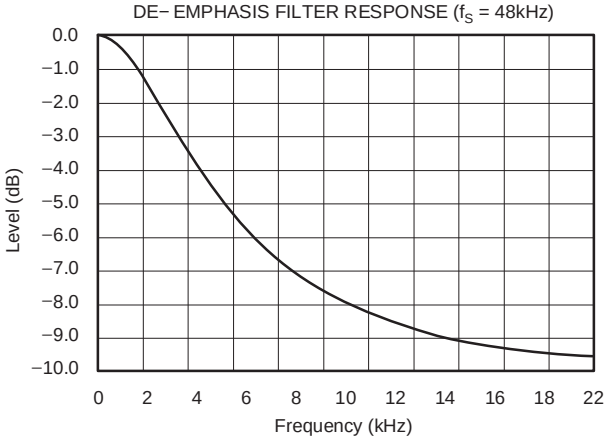
DE−EMPHASIS FILTER RESPONSE (f_S = 44.1kHz)



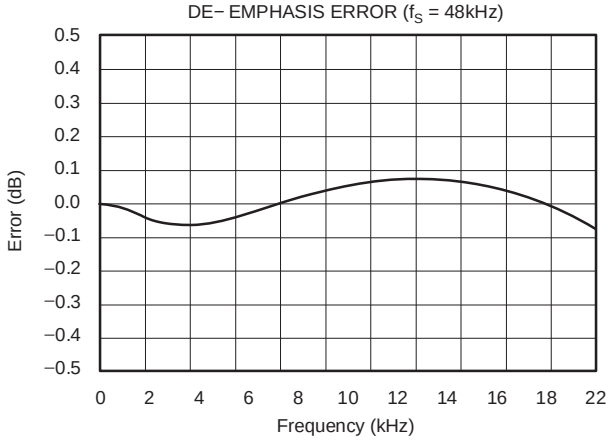
DE−EMPHASIS ERROR (f_S = 44.1kHz)



DE− EMPHASIS FILTER RESPONSE (f_S = 48kHz)



DE− EMPHASIS ERROR (f_S = 48kHz)



PRODUCT OVERVIEW

The PCM4104 is a high-performance, four-channel D/A converter designed for professional audio systems. The PCM4104 supports 16- to 24-bit linear PCM input data and sampling frequencies up to 216kHz. The PCM4104 utilizes an 8x oversampling digital interpolation filter, followed by a multi-level delta-sigma modulator with a single pole switched capacitor output filter. This architecture provides excellent dynamic and sonic performance, as well as high tolerance to clock phase jitter. Functional block diagrams, showing both Standalone and Software modes, are shown in Figure 1 and Figure 2.

The PCM4104 incorporates a flexible audio serial port, which accepts 16- to 24-bit PCM audio data in both standard audio formats (Left Justified, Right Justified, and Philips I^2S) and TDM data formats. The TDM formats are especially useful for interfacing to the synchronous serial ports of digital signal processors. The TDM formats support daisy-chaining of two PCM4104 devices on a single three-wire serial interface (for sampling frequencies up to 108kHz), forming a high-performance eight-channel D/A conversion system.

The PCM4104 offers two modes for configuration control: Software and Standalone. Software mode makes use of a four-wire SPI port to access internal control registers, allowing configuration of the full PCM4104 feature set. Standalone mode offers a more limited subset of the functions available in Software mode, while allowing for a simplified pin-programmed configuration mode.

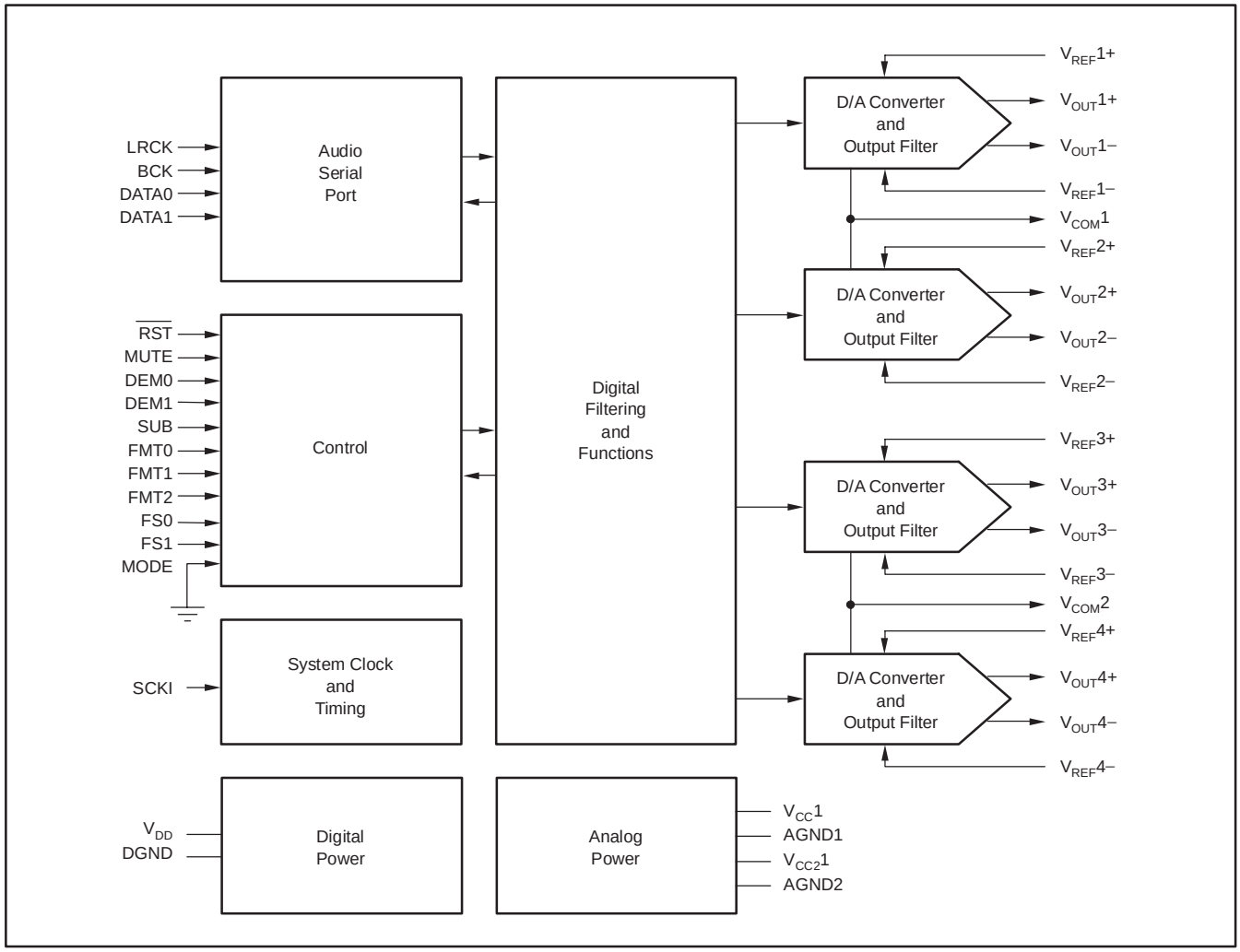


Figure 1. Functional Block Diagram for Standalone Mode

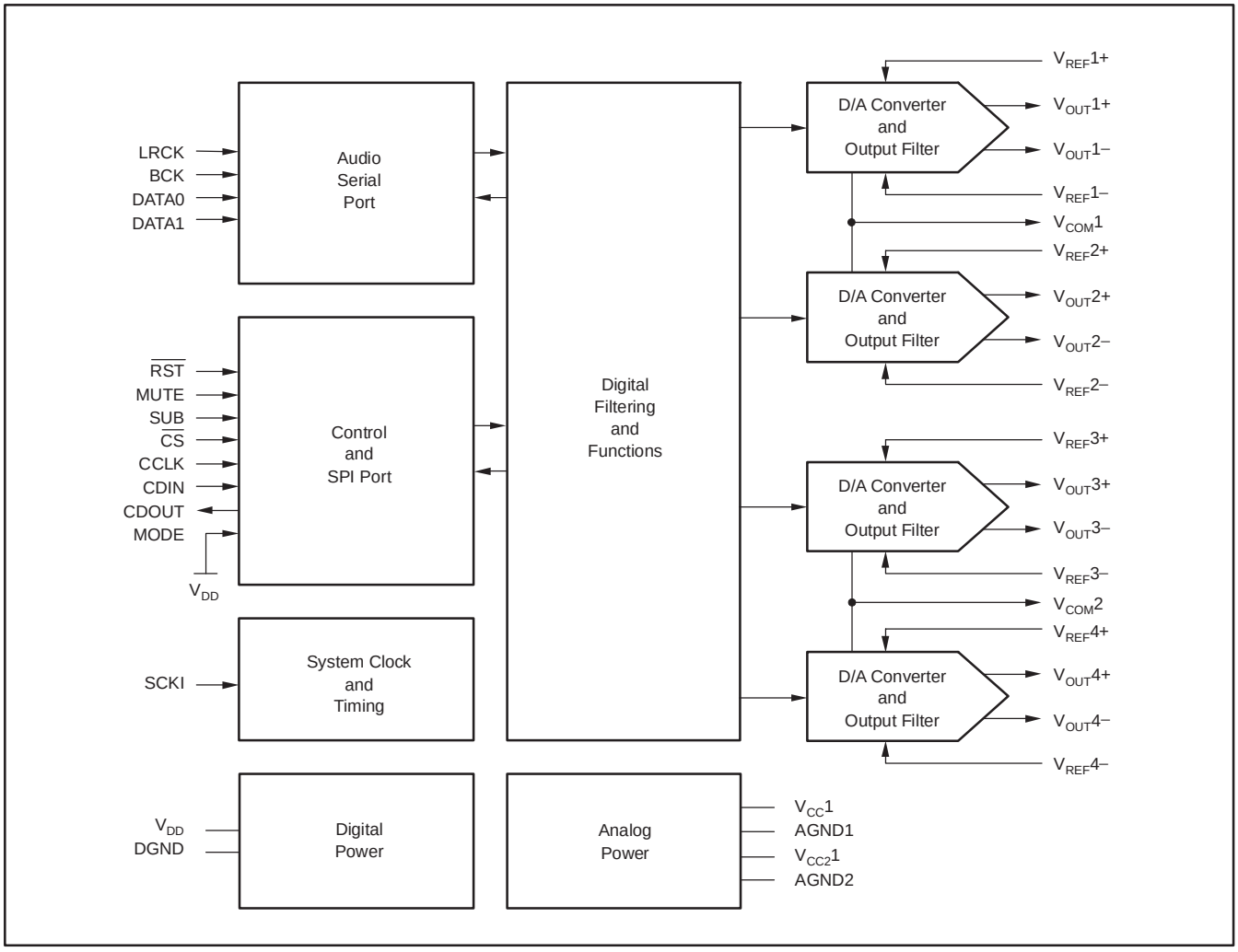


Figure 2. PCM4104 Functional Block Diagram for Software Mode

ANALOG OUTPUTS

The PCM4104 provides four differential voltage outputs, corresponding to audio channels 1 through 4. $V_{OUT}1+$ (pin 1) and $V_{OUT}1-$ (pin 2) correspond to Channel 1. $V_{OUT}2+$ (pin 47) and $V_{OUT}2-$ (pin 46) correspond to Channel 2. $V_{OUT}3+$ (pin 38) and $V_{OUT}3-$ (pin 39) correspond to Channel 3. $V_{OUT}4+$ (pin 36) and $V_{OUT}4-$ (pin 35) correspond to Channel 4.

Each differential output is typically capable of providing 6.15V full-scale (differential) into a 600Ω output load. The output pins are internally biased to the common-mode (or bipolar zero) voltage, which is nominally $V_{CC}/2$. The output section of each D/A converter channel includes a single-pole, switched capacitor low-pass filter circuit. The switched capacitor filter response tracks with the sampling frequency of the D/A converter and provides attenuation of the out-of-band noise produced by the delta-sigma modulator. An external two-pole continuous time filter is recommended to further reduce the out-of-band noise energy and to band limit the output spectrum to frequencies suitable for audio reproduction. Refer to the Applications Information section of this data sheet for recommended output filter circuits.

VOLTAGE REFERENCES

The PCM4104 includes high and low reference pins for each output channel. $V_{REF}1+$ (pin 5) and $V_{REF}1-$ (pin 4) correspond to Channel 1. $V_{REF}2+$ (pin 44) and $V_{REF}2-$ (pin 43) correspond to Channel 2. $V_{REF}3+$ (pin 41) and $V_{REF}3-$ (pin 42) correspond to Channel 3. $V_{REF}4+$ (pin 32) and $V_{REF}4-$ (pin 33) correspond to Channel 4.

The high reference (+) pin may be connected to the corresponding V_{CC} supply or an external +5.0V reference, while the low reference (−) pin is connected to analog ground. A 0.01µF bypass capacitor should be placed

between the corresponding high and low reference pins. An X7R ceramic chip capacitor is recommended for this purpose. In some cases, a larger capacitor may need to be placed in parallel with the 0.01µF capacitor, with the value of the larger capacitor being dependent upon the low-frequency power-supply noise present in the system. Typical values may range from 1µF to 10µF. Low ESR tantalum or multilayer ceramic chip capacitors are recommended. Figure 3 illustrates the recommended connections for the reference pins.

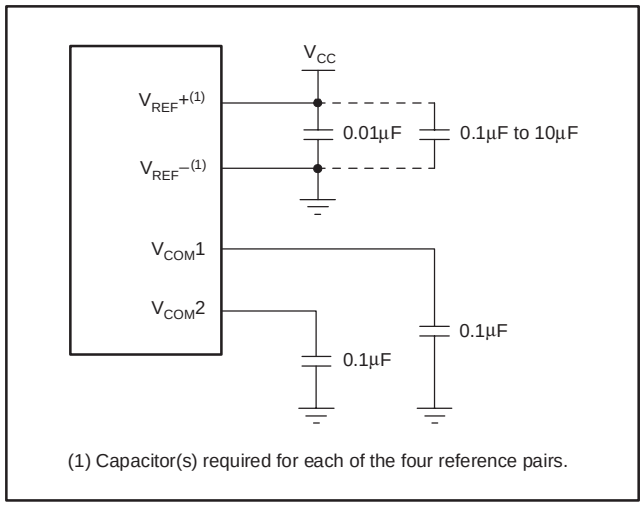


Figure 3. Recommended Connections for Voltage Reference and Common-Mode Output Pins

In addition to the reference pins, there are two common-mode voltage output pins, $V_{COM}1$ (pin 48) and $V_{COM}2$ (pin 37). These pins are nominally set to a value equal to $V_{CC}/2$ by internal voltage dividers. The $V_{COM}1$ pin is common to both Channels 1 and 2, while the $V_{COM}2$ pin is common to Channels 3 and 4. A 0.1µF X7R ceramic chip capacitor should be connected between the common-mode output pin and analog ground. The common-mode outputs are used primarily to bias external output circuitry.

SAMPLING MODES

The PCM4104 can operate in one of three sampling modes: Single Rate, Dual Rate, or Quad Rate. Sampling modes are selected by using the FS[1:0] bits in Control Register 6 in Software mode, or by using the FS0 (pin 28) and FS1 (pin 29) inputs in Standalone mode.

The Single Rate mode allows sampling frequencies up to and including 54kHz. The D/A converter performs 128x oversampling of the input data in Single Rate mode.

The Dual Rate mode allows sampling frequencies greater than 54kHz, up to and including 108kHz. The D/A converter performs 64x oversampling of the input data in Dual Rate mode.

The Quad Rate mode allows sampling frequencies greater than 108kHz, up to and including 216kHz. The D/A converter performs 32x oversampling of the input data in Quad Rate mode.

Refer to Table 1 for examples of system clock requirements for common sampling frequencies.

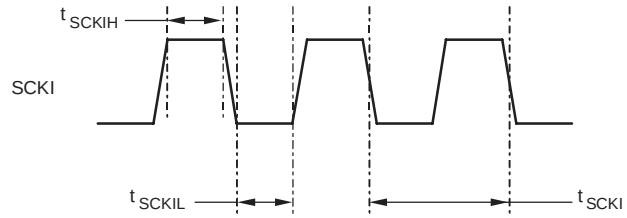
SYSTEM CLOCK REQUIREMENTS

The PCM4104 requires a system clock, applied at the SCKI (pin 14) input. The system clock operates at an integer multiple of the input sampling frequency, or f_S. The multiples supported include $128f_S$, $192f_S$, $256f_S$, $384f_S$, $512f_S$, or $768f_S$. The system clock frequency is dependent upon the sampling mode. Table 1 shows the required system clock frequencies for common audio sampling frequencies. Figure 4 shows the system clock timing requirements.

Although the architecture of the PCM4104 is tolerant to phase jitter on the system clock, it is recommended that the user provide a low jitter clock (100 picoseconds or less) for optimal performance.

Table 1. Sampling Modes and System Clock Frequencies for Common Audio Sampling Rates

SAMPLING MODE	SAMPLING FREQUENCY, f_S (kHz)	SYSTEM CLOCK FREQUENCY (MHz)					
		$128f_S$	$192f_S$	$256f_S$	$384f_S$	$512f_S$	$768f_S$
Single Rate	32	n/a	n/a	8.192	12.288	16.384	24.576
Single Rate	44.1	n/a	n/a	11.2896	16.9344	22.5792	33.8688
Single Rate	48	n/a	n/a	12.288	18.432	24.576	36.864
Dual Rate	88.2	n/a	n/a	22.5792	33.8688	n/a	n/a
Dual Rate	96	n/a	n/a	24.576	36.864	n/a	n/a
Quad Rate	176.4	22.5792	33.8688	n/a	n/a	n/a	n/a
Quad Rate	192	24.576	36.864	n/a	n/a	n/a	n/a



PARAMETER	DESCRIPTION	MIN	MAX	UNITS
t_{SCKI}	System Clock Period	26		ns
t_{SCKIH}	System Clock High Pulse Time	12		ns
t_{SCKIL}	System Clock Low Pulse Time	12		ns

Figure 4. System Clock Timing Requirements

RESET OPERATION

The PCM4104 includes three reset functions: power-on, external, and software-controlled. This section describes each of the three reset functions.

On power up, the internal reset signal is forced low, forcing the PCM4104 into a reset state. The power-on reset circuit monitors the V_{DD}, $V_{CC}1$, and $V_{CC}2$ power supplies. When V_{DD} exceeds +2.0V (margin of error is ±400mV) and $V_{CC}1$ and $V_{CC}2$ exceed +4.0V (margin of error is ±400mV), the internal reset signal is forced high. The PCM4104 then waits for the system clock input (SCKI) to become active. Once the system clock has been detected, the initialization sequence begins. The initialization sequence requires 1024 system clock periods for completion. When the initialization sequence is completed, the PCM4104 is ready to accept audio data at the audio serial port. Figure 5 shows the power-on reset sequence timing.

If the PCM4104 is configured for Software mode control via the SPI port, all control registers will be reset to their default state during the initialization sequence. In both Standalone and Software modes, the analog outputs for all four channels are muted during the reset and initialization sequence. While in mute state, the analog output pins are driven to the bipolar zero voltage, or $V_{CC}/2$.

The user may force a reset initialization sequence at any time while the system clock input is active by utilizing the $\overline{RST}$ input (pin 9). The $\overline{RST}$ input is active low, and requires a minimum low pulse width of 40 nanoseconds. The low-to-high transition of the applied reset signal will force an initialization sequence to begin. As in the case of the power-on reset, the initialization sequence requires 1024 system clock periods for completion. Figure 6 illustrates the reset sequence initiated when using the $\overline{RST}$ input.

A reset initialization sequence is available in Software mode, using the RST bit in Control Register 6. The RST bit is active high. When RST is set to 1, a reset sequence is initiated in the same fashion as an external reset applied at the $\overline{RST}$ input.

Figure 7 shows the state of the analog outputs for the PCM4104 before, during and after the reset operations.

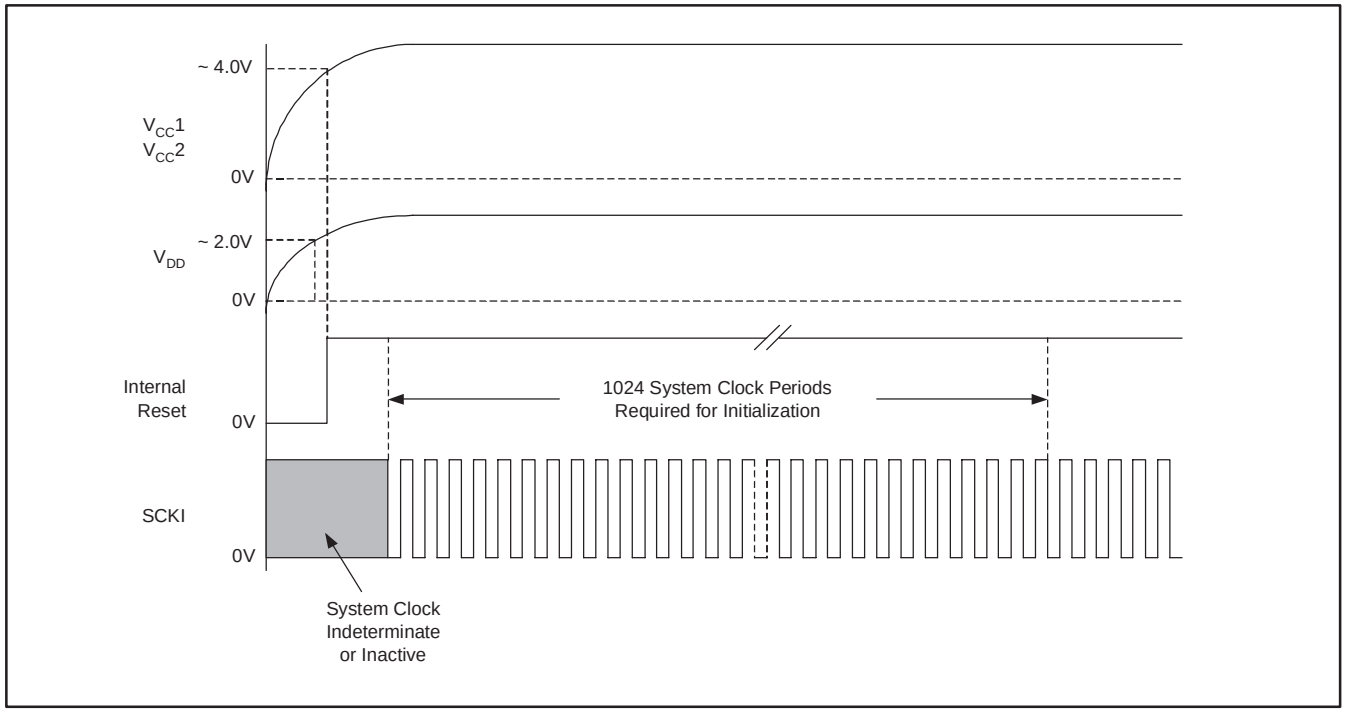


Figure 5. Power-Up Reset Timing

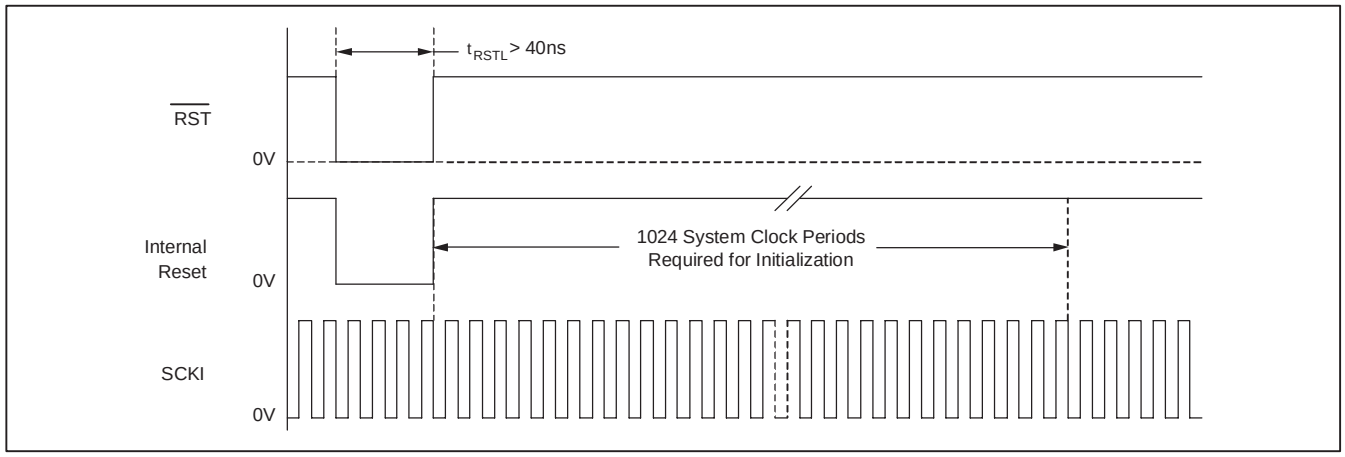


Figure 6. External Reset Timing

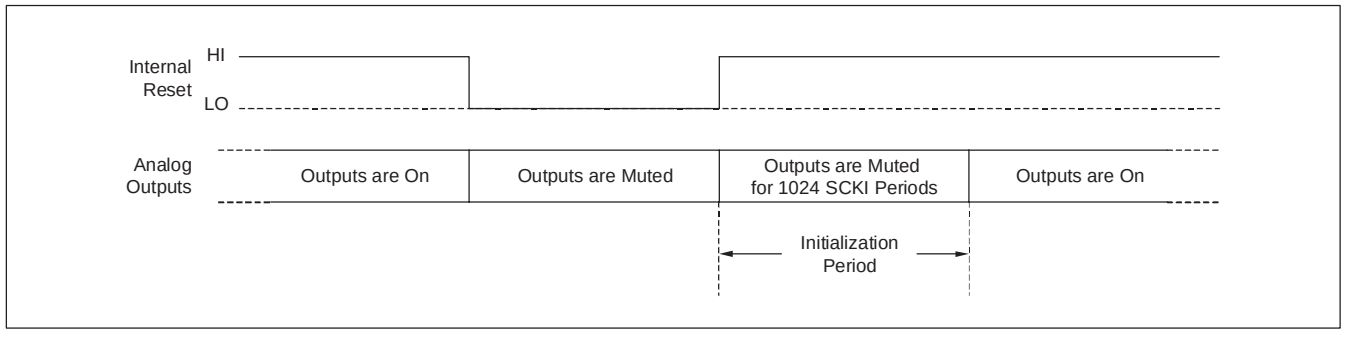


Figure 7. Analog Output State for Reset Operations

POWER-DOWN OPERATION

The PCM4104 can be forced to a power-down state by applying a low level to the $\overline{RST}$ input for a minimum of 65,536 system clock cycles. In power-down mode, all internal clocks are stopped, and analog outputs are set to a high-impedance state. The system clock can then be removed to conserve additional power. In the case of system clock restart when exiting the power-down state, the clock should be restarted prior to a low-to-high transition of the reset signal at the $\overline{RST}$ input. The low-to-high transition of the reset signal initiates a reset sequence, as described in the Reset Operation section of this data sheet.

In Software mode, two additional power-down controls are provided. The PDN12 and PDN34 bits are located in Control Register 6 and may be used to power-down channel pairs, with PDN12 corresponding to channels 1 and 2, and PDN34 corresponding to channels 3 and 4. This allows the user to conserve power when a channel pair is not in use. The power-down function is the same as described in the previous paragraph for the corresponding channel pair. Unlike the power-down function implemented using the $\overline{RST}$ input, setting a power-down bit will immediately power down the corresponding channel pair.

When exiting power-down mode, either by forcing the $\overline{RST}$ input high or by setting the PDN12 or PDN34 bits low, the analog outputs will transition from the high-impedance state to the mute state, with the output level set to the bipolar zero voltage. There may be a small transient created by this transition, since internal capacitor charge can initially force the output to a voltage above or below bipolar zero, or external circuitry can pull the outputs to some other voltage level. Figure 8 illustrates the state of the analog outputs before, during, and after a power-down event.

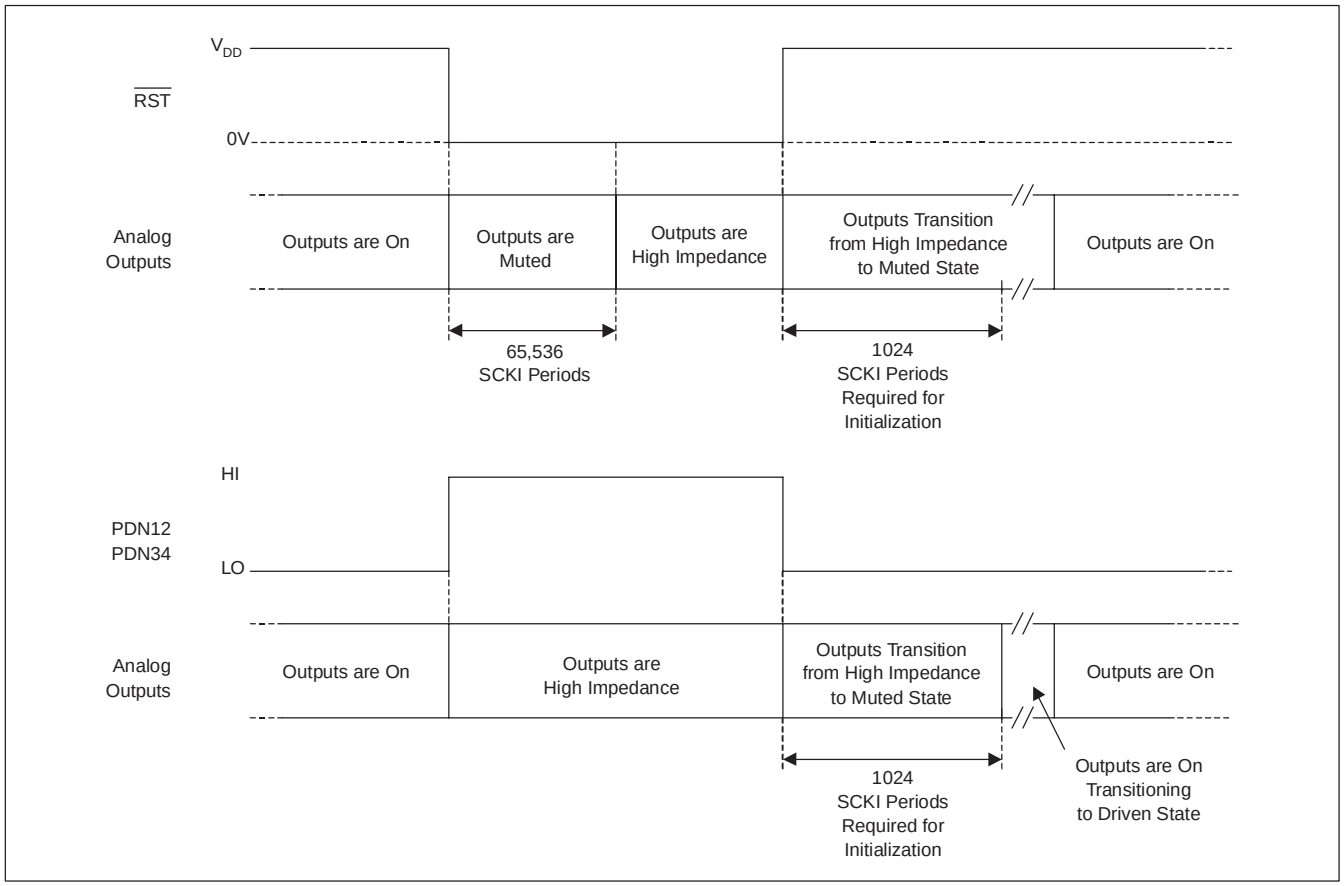


Figure 8. Analog Output State for Power-Down Operations

AUDIO SERIAL PORT

The audio serial port provides a common interface to digital signal processors, digital interface receivers (AES3, S/PDIF), and other digital audio devices. The port operates as a slave to the processor, receiver, or other clock generation circuitry. Figure 9 illustrates a typical audio serial port connection to a processor or receiver. The audio serial port is comprised of four signal pins: BCK (pin 15), LRCK (pin 16), DATA0 (pin 17), and DATA1 (pin 18).

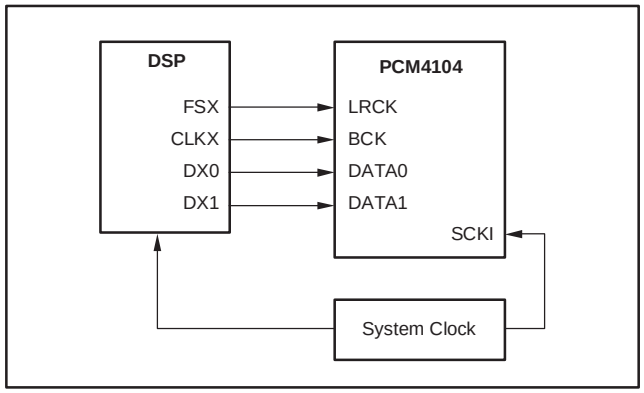


Figure 9. Audio Serial Port Connections for Left Justified, Right Justified, and I^2S Formats.

The LRCK pin functions as either the left/right word clock or the frame synchronization clock, depending upon the data format selected. The LRCK frequency is equal to the input sampling frequency (44.1kHz, 48kHz, 96kHz, etc.).

The BCK pin functions as the serial data clock input. This input is referred to as the bit clock. The bit clock runs at an integer multiple of the input sampling frequency. Typical multiples include 32, 48, 64, 96, 128, 192, and 256, depending upon the data format, word length, and system clock frequency selected.

The DATA0 and DATA1 pins are the audio data inputs. When using Left Justified, Right Justified, or I^2S data formats, the DATA0 pin carries the audio data for channels 1 and 2, while the DATA1 pin carries the audio data for channels 3 and 4. When using TDM data formats, DATA0 carries the audio data for all four channels, while the DATA1 input is ignored.

The audio serial port data formats are shown in Figure 10, Figure 13, and Figure 14. Data formats are selected by using the FMT[2:0] bits in Control Register 7 in Software mode, or by using the FMT0 (pin 25), FMT1 (pin 26), and FMT2 (pin 27) inputs in Standalone mode. In Software mode, the user may also select the phase (normal or inverted) for the LRCK input, as well as the data sampling edge for the BCK input (either rising or falling edge). The reset default conditions for the Software mode are normal phase for LRCK and rising edge data sampling for BCK.

The Left Justified, Right Justified, and I^2S data formats are similar to one another, with differences in data justification and word length. The PCM audio data must be two's complement binary, MSB first. Figure 10 provides illustrations for these data formats.

The TDM formats carry the information for four or eight channels on a single data line. The DATA0 input (pin 17) is used as the data input for the TDM formats. The data is carried in a time division multiplexed fashion; hence, the *TDM* acronym used to describe this format. Figure 12 shows the TDM connection of two PCM4104 devices. The data for each channel is assigned one of the time slots in the TDM frame, as shown in Figure 13 and Figure 14. The sub−frame assignment for each PCM4104 is determined by the state of the SUB input (pin 13). When SUB is forced low, the device is assigned to sub-frame 0. When SUB is forced high, the device is assigned to sub-frame 1.

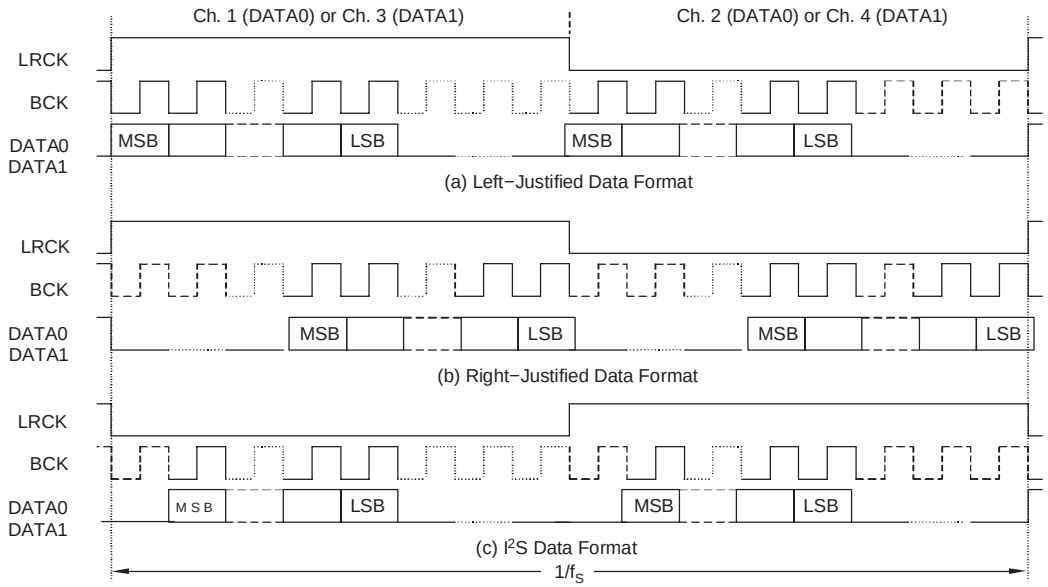
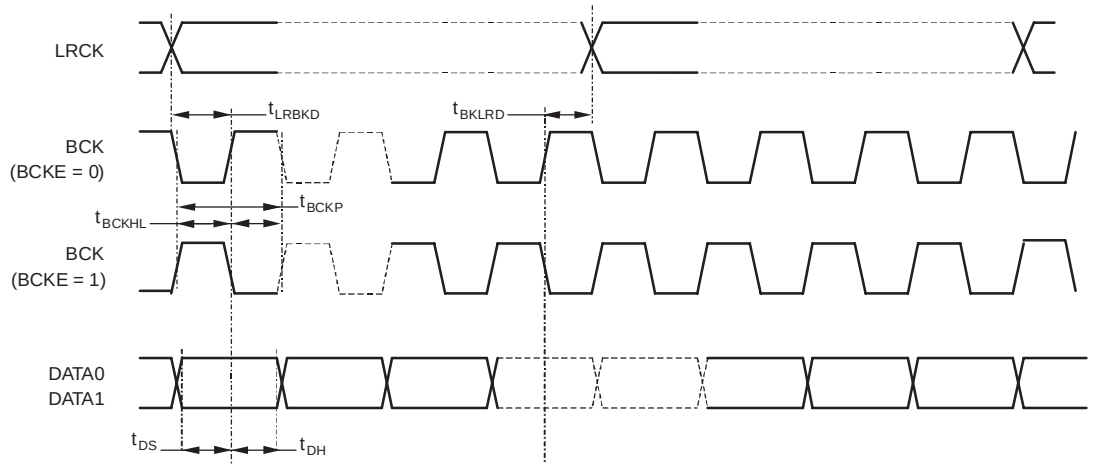


Figure 10. Left Justified, Right Justified, and I²S Data Formats



PARAMETER	DESCRIPTION	MIN	MAX	UNITS
t_{BCKP}	BCK Cycle Time	70		ns
t_{BCKHL}	BCK High/Low Time	30		ns
t_{LRBKD}	LRCK Edge to BCK Sampling Edge Delay	10		ns
t_{BKLRD}	BCK Sampling Edge to LRCK Edge Delay	10		ns
t_{DS}	Data Setup Time	10		ns
t_{DH}	Data Hold Time	10		ns
–	LRCK Duty Cycle	50		%

Figure 11. Audio Serial Port Timing for Left Justified, Right Justified, and I²S Data Formats.

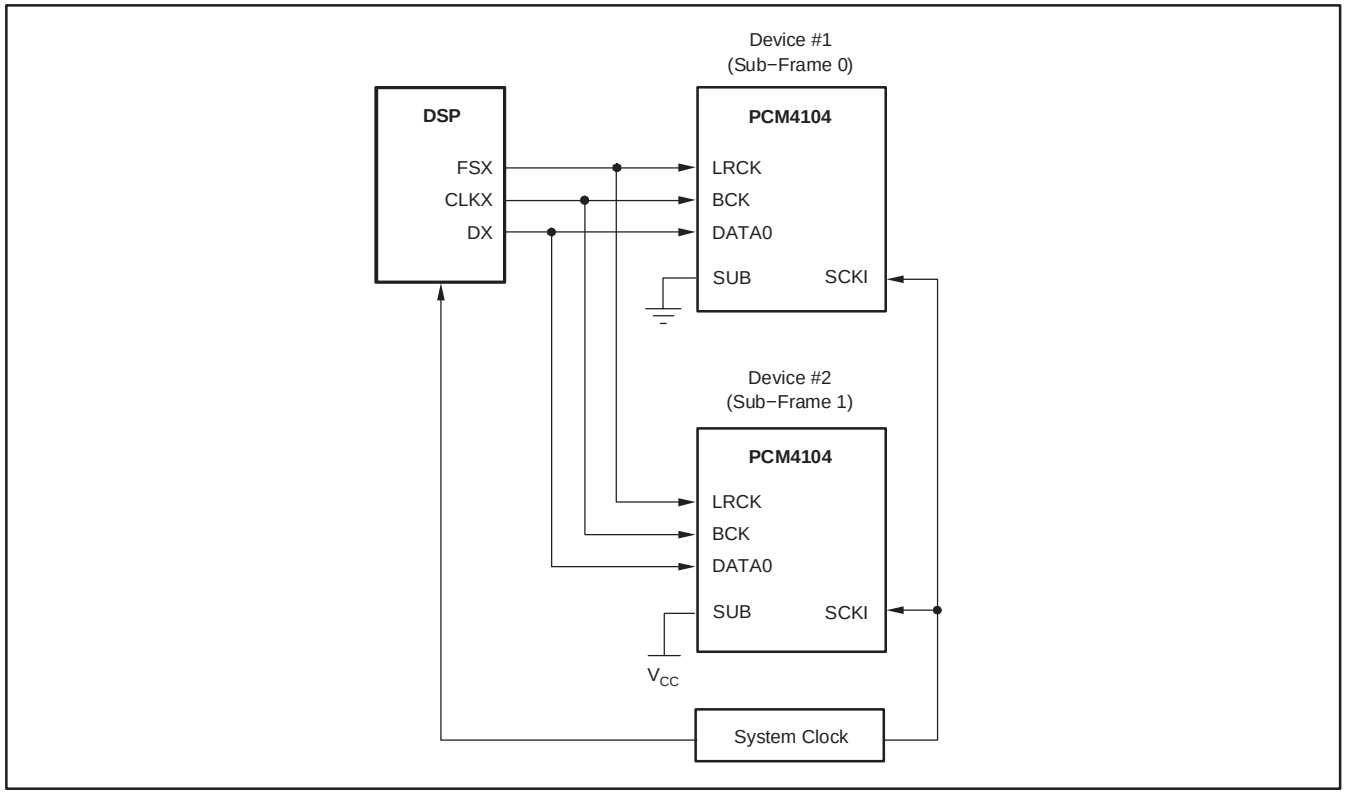
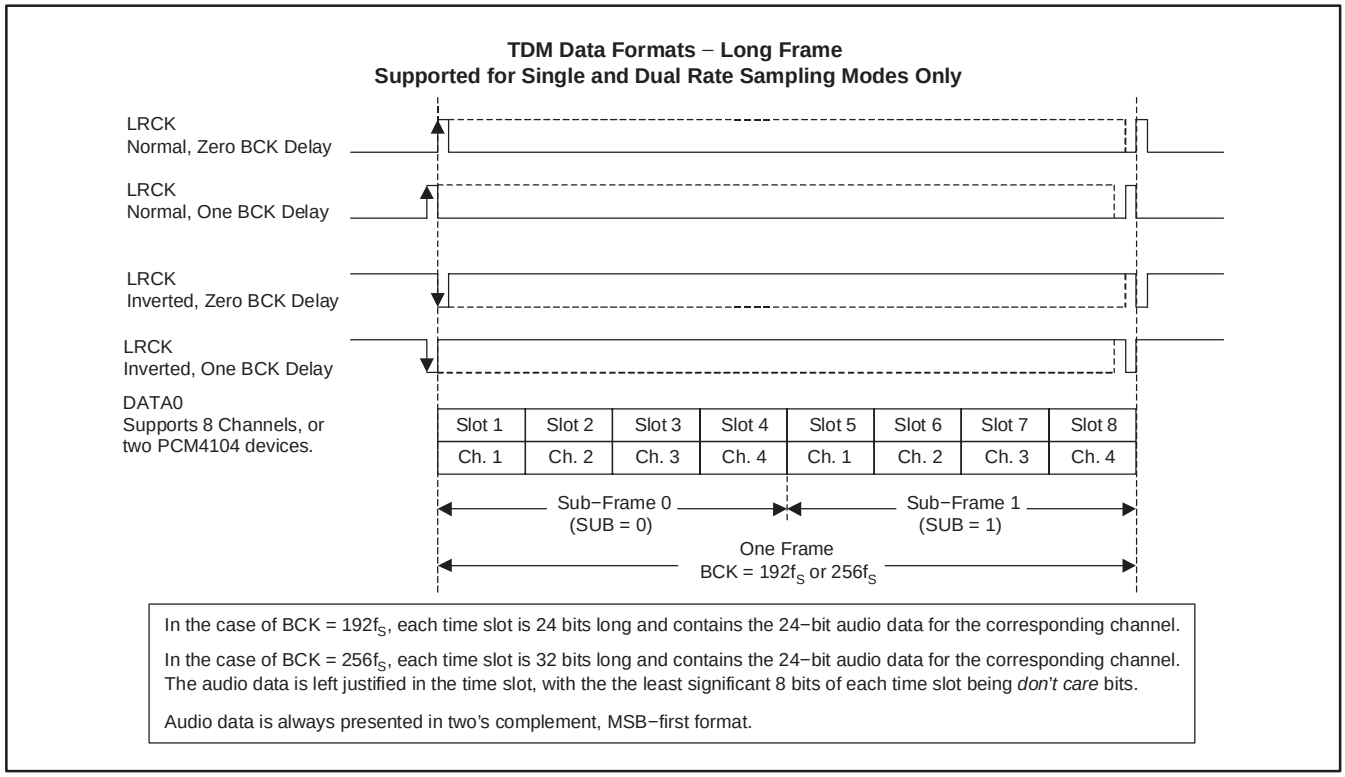


Figure 12. TDM Connection



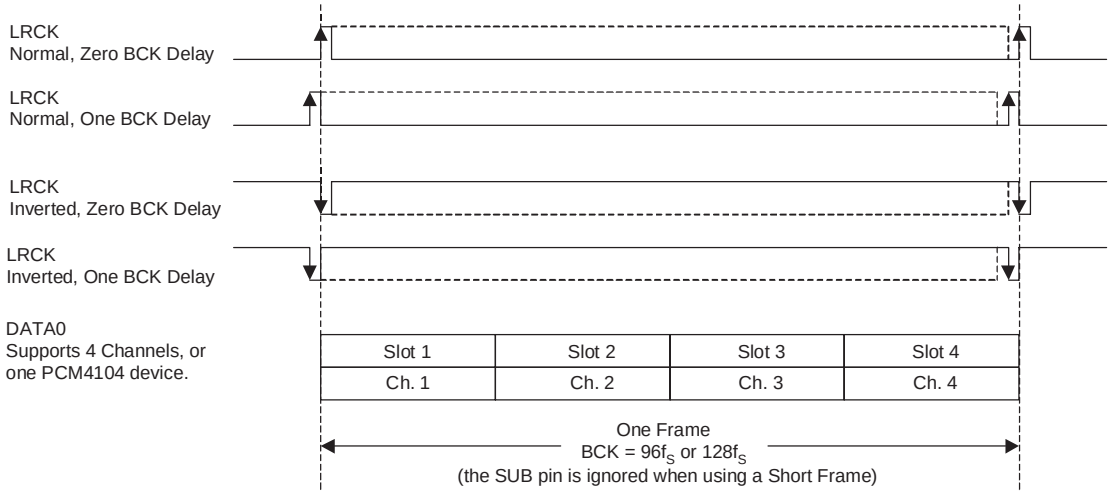
In the case of BCK = $192f_S$, each time slot is 24 bits long and contains the 24−bit audio data for the corresponding channel.

In the case of BCK = $256f_S$, each time slot is 32 bits long and contains the 24−bit audio data for the corresponding channel. The audio data is left justified in the time slot, with the the least significant 8 bits of each time slot being *don't care* bits.

Audio data is always presented in two's complement, MSB−first format.

Figure 13. TDM Data Formats: Long Frame

TDM Data Formats − Short Frame
All Sampling Modes Supported

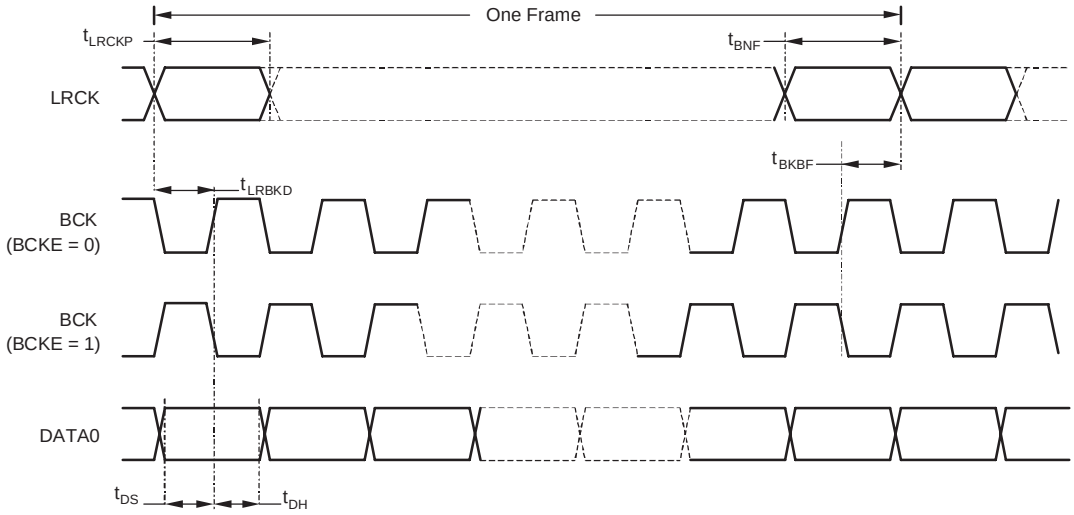


In the case of BCK = $96f_S$, each time slot is 24 bits long and contains the 24−bit audio data for the corresponding channel.

In the case of BCK = $128f_S$, each time slot is 32 bits long and contains the 24−bit audio data for the corresponding channel. The audio data is left justified in the time slot, with the the least significant 8 bits of each time slot being *don't care* bits.

Audio data is always presented in two's complement, MSB−first format.

Figure 14. TDM Data Formats: Short Frame



PARAMETER	DESCRIPTION	MIN	MAX	UNITS
t_{LRCKP}	LRCK pulse width	$1/f_{BCK}$		ns
t_{LRBKD}	LRCK active edge to BCK sampling edge delay	12		ns
t_{DS}	Data setup time	10		ns
t_{DH}	Data hold time	10		ns
t_{BNF}	LRCK transition before new frame	$1/f_{BCK}$		ns
t_{BKBF}	BCK sampling edge to new frame delay	12		ns

Figure 15. TDM Timing

STANDALONE MODE CONFIGURATION

Standalone mode is selected by forcing the MODE input (pin 8) low. Standalone mode operation provides a subset of the functions available in Software mode, while providing an option for a simplified control model. Standalone configuration is accomplished by either hardwiring or driving a small set of input pins with external logic or switches. Standalone mode functions include sampling mode and audio data format selection, an all-channel soft mute function, and digital de-emphasis filtering. The following paragraphs provide a brief description of each function available when using Standalone mode.

Sampling Mode

The sampling mode is selected using the FS0 (pin 28) and FS1 (pin 29) inputs. A more detailed discussion of the sampling modes was provided in an earlier section of this data sheet. Table 2 summarizes the sampling mode configuration for Standalone mode.

Table 2. Sampling Mode Configuration

FS1	FS0	SAMPLING MODE
0	0	Single Rate
0	1	Dual Rate
1	0	Quad Rate
1	1	− Not Used −

Audio Data Format

The audio data format is selected using the FMT0 (pin 25), FMT1 (pin 26), and FMT2 (pin 27) inputs. A detailed discussion of the audio serial port operation and the corresponding data formats was provided in the Audio Serial Port section on page 19. For Standalone mode, the LRCK polarity is always normal, while the serial audio data is always sampled on the rising edge of the BCK clock. Table 3 shows the audio data format configuration for Standalone mode.

Table 3. Audio Data Format Configuration

FMT2	FMT1	FMT0	AUDIO DATA FORMAT
0	0	0	24-bit left justified
0	0	1	24-bit I^2S
0	1	0	TDM with zero BCK delay
0	1	1	TDM with one BCK delay
1	0	0	24-bit right justified
1	0	1	20-bit right justified
1	1	0	18-bit right justified
1	1	1	16-bit right justified

Soft Mute Function

The MUTE input (pin 10) may be used in either the Standalone or Software modes to simultaneously mute the four output channels. The soft mute function slowly ramps the digital output attenuation from its current setting to the mute level, minimizing or eliminating audible artifacts. Table 4 summarizes MUTE function operation.

Table 4. Mute Function Configuration

MUTE	ANALOG OUTPUTS
0	On (mute disabled)
1	Muted

Digital De-Emphasis

This is a global digital function (common to all four channels) and provides de-emphasis of the higher frequency content within the 20kHz audio band. De-emphasis is required when the input audio data has been pre-emphasized. Pre-emphasis entails increasing the amplitude of the higher frequency components in the 20kHz audio band using a standardized filter function in order to enhance the high-frequency response. The PCM4104 de-emphasis filters implement the standard 50/15µs de-emphasis transfer function commonly used in digital audio applications.

De-emphasis filtering is available for three input sampling frequencies in Single Rate sampling mode: 32kHz, 44.1kHz, and 48kHz. De-emphasis is not available when operating in Dual or Quad Rate sampling modes. The de-emphasis filter is selected using the DEM0 (pin 12) and DEM1 (pin 11) inputs. Table 5 illustrates the de-emphasis filter configuration for Standalone mode.

Table 5. Digital De-Emphasis Configuration

DEM1	DEM0	DIGITAL DE-EMPHASIS MODE
0	0	Off (de-emphasis disabled)
0	1	48kHz
1	0	44.1kHz
1	1	32kHz

SOFTWARE MODE CONFIGURATION

Software mode is selected by forcing the MODE input (pin 8) high. Software mode operation provides full access to the features of the PCM4104 by allowing the writing and reading of on-chip control registers. This is accomplished using the four-wire SPI port. The following paragraphs provide a brief description of each function available when using Software mode.

Digital Attenuation

The audio signal for each channel can be attenuated in the digital domain using this function. Attenuation settings from 0dB (unity gain) to −119.5dB are provided in 0.5dB steps. In addition, the attenuation level may be set to the mute state. The rate of change for the digital attenuation function is one 0.5dB step for every eight LRCK periods. Each channel has its own independent attenuation control, accessed using control registers 1 through 4. The reset default setting for all channels is 0dB, or unity gain (no attenuation applied).

Digital De-Emphasis

The de-emphasis function is accessed through Control Register 5 using the DEM[1:0] bits. The reset default setting is that the de-emphasis is disabled for all four channels. De-emphasis filter operation is described in the Standalone Mode Configuration section of this data sheet.

Soft Mute

Each of the four D/A converter channels has its own independent soft mute control, located in Control Register 5.

The reset default is normal output for all four channels with the soft mute function disabled. The MUTE input (pin 10) also functions in Software mode, with a high input forcing soft mute on all four channels.

Zero Data Mute

The PCM4104 includes a zero data detection and mute function in Software mode. This function automatically mutes a given channel when 1024 consecutive LRCK periods of all zero data are detected for that channel. The zero data mute function is enabled and disabled using the ZDM bit in Control Register 5. The zero data mute function is disabled by default on power up or reset.

Output Phase Reversal

The PCM4104 includes an output phase reversal function, which provides the ability to invert the output phase for all four channels, either for testing or for matching various output circuit configurations. This function is controlled using the PHASE bit, located within Control Register 5. The output phase is set to noninverted by default on power up or reset.

Sampling Mode

Sampling mode configuration was discussed earlier in this data sheet, with Table 1 providing a reference for common sampling and system clock frequencies. The FS0 and FS1 bits located in Control Register 6 are used to set the sampling mode. The sampling mode defaults to Single Rate on power up or reset.

Power-Down Modes

The power-down control bits are located in Control Register 6. These bits are used to power down pairs of D/A converters within the PCM4104. The PDN12 bit is used to power down channels 1 and 2, while the PDN34 bit is used to power down channels 3 and 4. When a channel pair is powered down, it ignores the audio data inputs and sets its outputs to a high-impedance state. By default, the power-down bits are disabled on power up or reset.

Software Reset

This reset function allows a reset sequence to be initiated under software control. All control registers are reset to their default state. The reset bit, RST, is located in Control Register 6. Setting this bit to 1 initiates a one-time reset sequence. The RST bit is cleared by the initialization sequence.

Audio Data Formats, LRCK Polarity, and BCK Sampling Edge

Control Register 7 is used to configure the PCM4104 audio serial port. Audio serial port operation was discussed previously in this data sheet; refer to that section for more details regarding the functions controlled by this register. The control register definitions provide additional information regarding the register functions and their default settings.

SERIAL PERIPHERAL INTERFACE (SPI) PORT OPERATION

The SPI port is a four-wire synchronous serial interface that is used to access the on-chip control registers when the PCM4104 is configured for Software mode operation. The CDIN input (pin 23) is the serial data input for the port, while CDOUT (pin 24) is used for reading back control register contents in a serial fashion. The $\overline{CS}$ input (pin 21) functions as the chip select input, and must be forced low for register write or read access. The CCLK input (pin 22) functions as the serial data clock, used to clock data in and out of the port. Data is clocked into the port on the rising edge of CCLK, while data is clocked out of the port on the falling edge of CCLK.

There are three modes of operation supported for the SPI port: Single Register, Continuous, and Auto-Increment.

The Single Register and Continuous modes are similar to one another. In Continuous mode, instead of bringing the $\overline{CS}$ input high after writing or reading a single register, the $\overline{CS}$ input is held low and a new control byte is issued with a new address for the next write or read operation. Continuous mode allows multiple, sequential or nonsequential register addresses to be read or written in succession, as shown in Figure 16.

Auto-Increment mode is designed for writing or reading multiple sequential register addresses. After the first register is written or read, the register address is automatically incremented by 1, so the next write or read operation is performed without issuing another control byte, as shown in Figure 17.

Control Byte (or Byte 0)

The control byte, or byte 0, is the first byte written to the PCM4104 SPI port when performing a write or read operation. The control byte includes bits that define the operation to be performed (read or write), the auto-increment mode status, and the control register address.

The Read/Write bit, R/$\overline{W}$, is set to 0 to indicate a register write operation, or set to 1 for a register read operation.

The Increment bit, INC, enables or disables the Auto-Increment mode of operation. When this bit is set to a 0, auto-increment operation is disabled, and the operation performed is either Single Register or Continuous. Setting the INC bit to 1 enables Auto-Increment operation.

A two-bit key code, 10_B, follows the INC bit and must be present in order for any operation to take place on the control port. Any other combination for these bits will result in the port ignoring the write or read request.

The four-bit address field, A[3:0], is used to specify the control register address for the read or write operation, or the starting address for an Auto-Increment write or read operation.

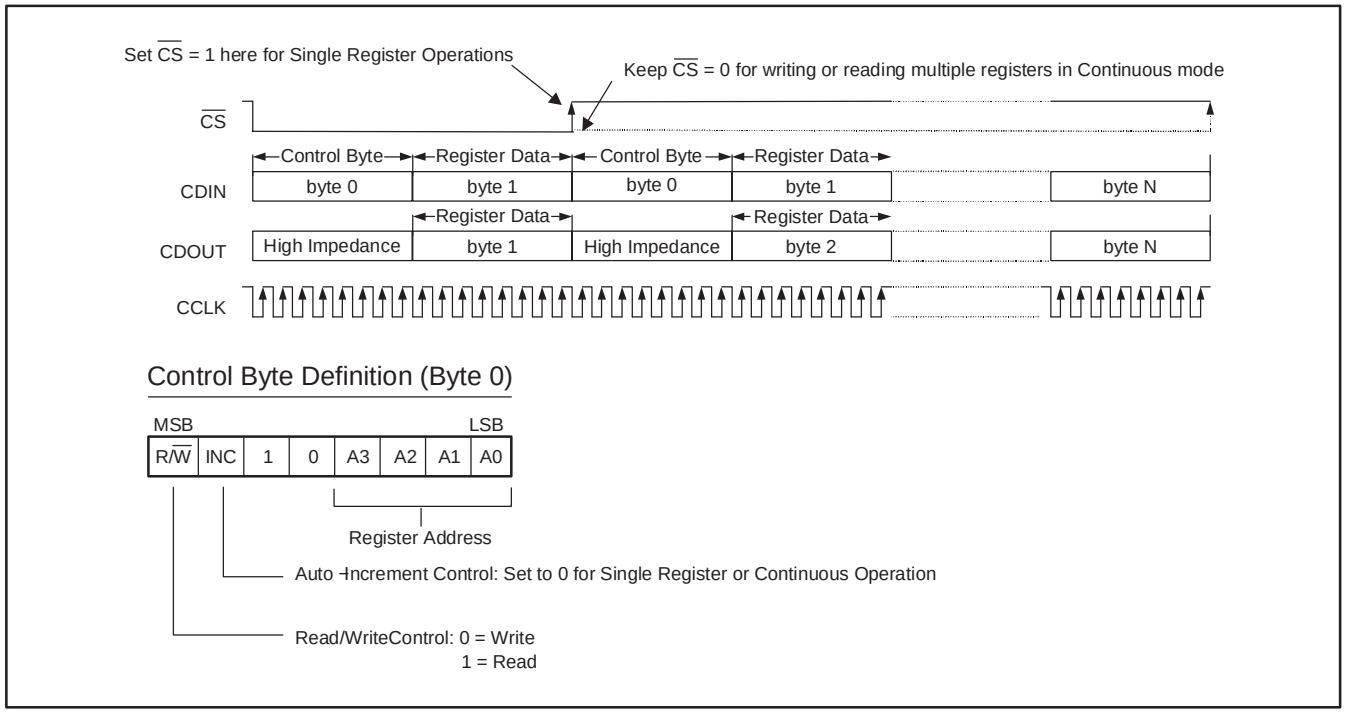


Figure 16. Single Register and Continuous Write or Read Operation

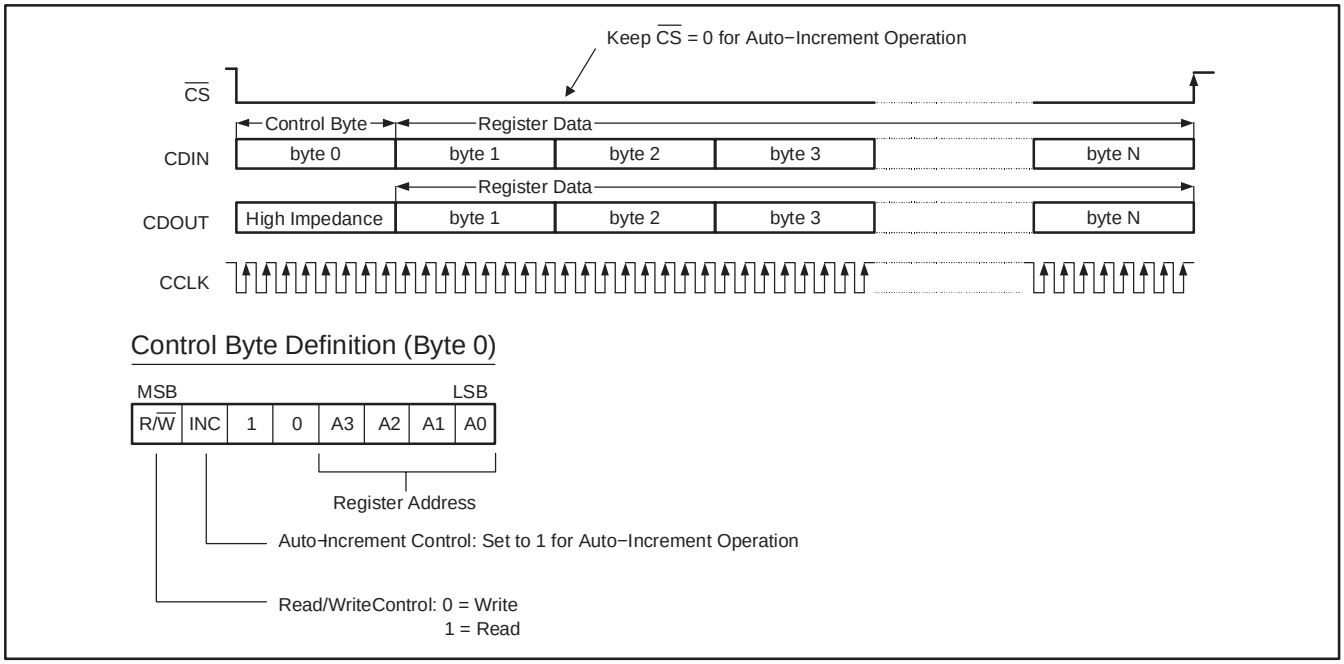
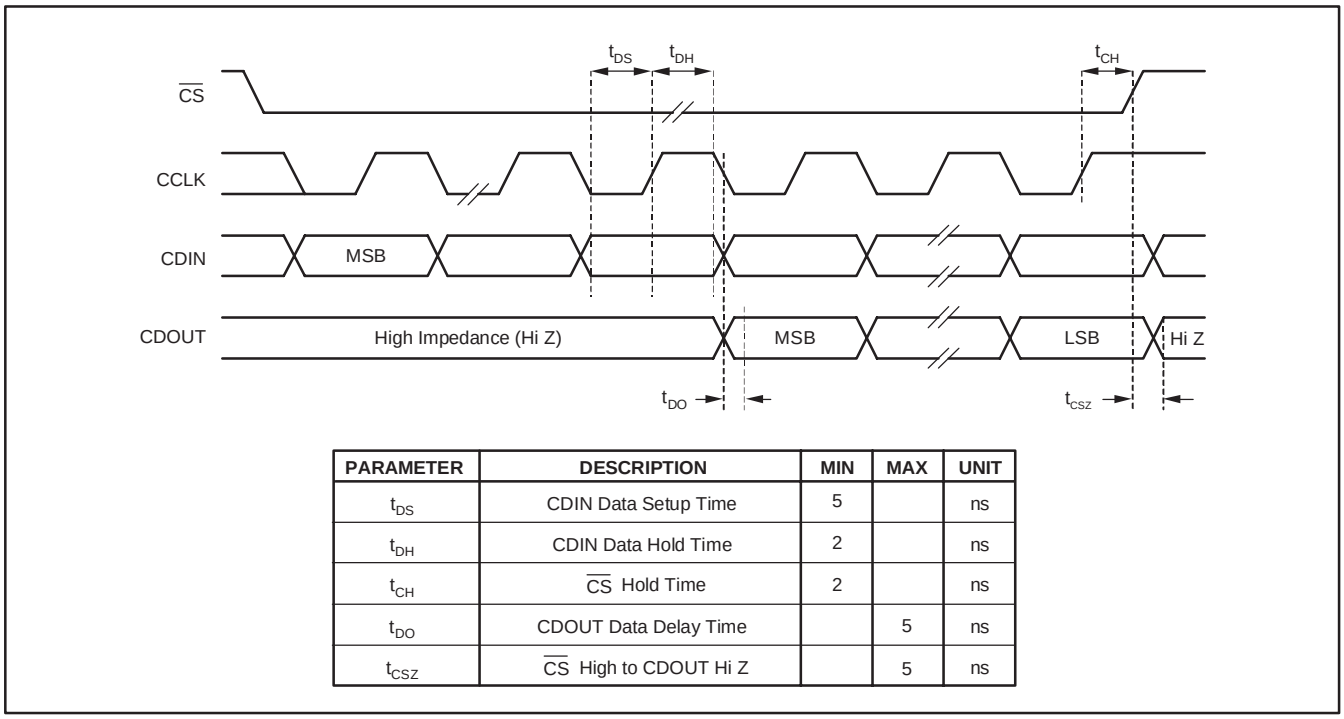


Figure 17. Auto-Increment Write or Read Operation



PARAMETER	DESCRIPTION	MIN	MAX	UNIT
t_{DS}	CDIN Data Setup Time	5		ns
t_{DH}	CDIN Data Hold Time	2		ns
t_{CH}	$\overline{CS}$ Hold Time	2		ns
t_{DO}	CDOUT Data Delay Time		5	ns
t_{CSZ}	$\overline{CS}$ High to CDOUT Hi Z		5	ns

Figure 18. SPI Port Timing

CONTROL REGISTER DEFINITIONS (SOFTWARE MODE ONLY)

The PCM4104 includes a small set of control registers, which are utilized to configure the full set of on-chip functions in Software mode. The register map is shown in Table 6. Register 0 is reserved for factory use and should not be written to for normal operation. Register 0 defaults to all zero data on power up or reset.

Table 6. Control Register Map

CONTROL REGISTER ADDRESS (HEX)	MSB BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	LSB BIT 0
0	0	0	0	0	0	0	0	0
1	AT17	AT16	AT15	AT14	AT13	AT12	AT11	AT10
2	AT27	AT26	AT25	AT24	AT23	AT22	AT21	AT20
3	AT37	AT36	AT35	AT34	AT33	AT32	AT31	AT30
4	AT47	AT46	AT45	AT44	AT43	AT42	AT41	AT40
5	MUT4	MUT3	MUT2	MUT1	ZDM	PHASE	DEM1	DEM0
6	RST	0	0	0	PDN34	PDN12	FS1	FS0
7	0	0	BCKE	LRCKP	0	FMT2	FMT1	FMT0

Register 1: Attenuation Control Register − Channel 1

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
AT17	AT16	AT15	AT14	AT13	AT12	AT11	AT10

This register controls the digital output attenuation for Channel 1.

Default: AT1[7:0] = 255, or 0dB

Let N = AT1[7:0].

For N = 16 to 255, Attenuation (dB) = 0.5 x (255 – N)

For N = 0 to 15, Attenuation (dB) = Infinite (Muted)

Register 2: Attenuation Control Register – Channel 2

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
AT27	AT26	AT25	AT24	AT23	AT22	AT21	AT20

This register controls the digital output attenuation for Channel 2.

Default: AT2[7:0] = 255, or 0dB

Let N = AT2[7:0].

For N = 16 to 255, Attenuation (dB) = 0.5 x (255 – N)

For N = 0 to 15, Attenuation (dB) = Infinite (Muted)

Register 3: Attenuation Control Register – Channel 3

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
AT37	AT36	AT35	AT34	AT33	AT32	AT31	AT30

This register controls the digital output attenuation for Channel 3.

Default: AT3[7:0] = 255, or 0dB

Let N = AT3[7:0].

For N = 16 to 255, Attenuation (dB) = 0.5 x (255 – N)

For N = 0 to 15, Attenuation (dB) = Infinite (Muted)

Register 4: Attenuation Control Register – Channel 4

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
AT47	AT46	AT45	AT44	AT43	AT42	AT41	AT40

This register controls the digital output attenuation for Channel 4.

Default: AT4[7:0] = 255, or 0dB

Let N = AT4[7:0].

For N = 16 to 255, Attenuation (dB) = 0.5 x (255 – N)

For N = 0 to 15, Attenuation (dB) = Infinite (Muted)

Register 5: Function Control Register

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
MUT4	MUT3	MUT2	MUT1	ZDM	PHASE	DEM1	DEM0

This register controls various D/A converter functions, including de-emphasis filtering, output phase reversal, zero data mute, and per-channel soft muting.

DEM[1:0] Digital De-Emphasis

De-emphasis is available for Single Rate mode only.

De-emphasis is disabled for Dual and Quad Rate modes.

DEM1	DEM0	De-Emphasis Selection
0	0	De-emphasis disabled (default)
0	1	De-emphasis for f_S = 48kHz
1	0	De-emphasis for f_S = 44.1kHz
1	1	De-emphasis for f_S = 32kHz

PHASE Output Phase

PHASE	Output Phase
0	Noninverted (default)
1	Inverted

ZDM Zero Data Mute

ZDM	Zero Mute
0	Disabled (default)
1	Enabled

MUT[4:1] Soft Mute

MUTx	D/A Converter Output
0	On (default)
1	Muted

NOTE: x = channel number.

Register 6: System Control Register

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
RST	0	0	0	PDN34	PDN12	FS1	FS0

This register controls various system level functions of the PCM4104, including sampling mode, power down, and soft reset.

FS[1:0] Sampling Mode

FS1	FS0	Sampling Mode
0	0	Single Rate (default)
0	1	Dual Rate
1	0	Quad Rate
1	1	− Not Used −

PDN12 Power-Down for Channels 1 and 2

PDN12	Power Down for Channels 1 and 2
0	Disabled (default)
1	Enabled

PDN34 Power Down for Channels 3 and 4

PDN34	Power Down for Channels 3 and 4
0	Disabled (default)
1	Enabled

RST Software Reset (value defaults to 0)

Setting this bit to 1 will initiate a logic reset of the PCM4104. This bit functions the same as an external reset applied at the $\overline{RST}$ input (pin 9).

Register 7: Audio Serial Port Control Register

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
0	0	BCKE	LRCKP	0	FMT2	FMT1	FMT0

This register is used to control the data format and clock polarity for the PCM4104 audio serial port.

FMT[2:0] Audio Data Format

FMT2	FMT1	DEM0	Data Format
0	0	0	24-bit left justified (default)
0	0	1	24-bit I^2S
0	1	0	TDM with zero BCK delay
0	1	1	TDM with one BCK delay
1	0	0	24-bit right justified
1	0	1	20-bit right justified
1	1	0	18-bit right justified
1	1	1	16-bit right justified

LRCKP LRCK Polarity (0 = Normal, 1 = Inverted). Defaults to 0.

BCKE BCK Sampling Edge (0 = Rising Edge, 1 = Falling Edge), Defaults to 0.

APPLICATIONS INFORMATION

This section provides practical information for system and hardware engineers that are designing in the PCM4104.

BASIC CIRCUIT CONFIGURATIONS

Figure 19 and Figure 20 show typical circuit configurations for the PCM4104 operated in Standalone and Software modes. Power supply bypass and reference decoupling capacitors should be placed as close to the corresponding PCM4104 pins as possible. A common ground is shown in both figures, with the analog and digital ground pins connected to a common plane. Separate power supplies are utilized for the analog and digital sections, with +5V required for the PCM4104 analog supplies and +3.3V required for the digital supply.

The +5V analog supply may be derived from a higher valued, positive analog power supply using a linear voltage regulator, such as the REG103 available from Texas Instruments. The +3.3V digital supply can be derived from a primary +5V digital supply using a linear voltage regulator, such as the REG1117, also from TI. The PCM4104EVM evaluation module provides an example of how the common ground with separate supply approach can be successfully implemented. The PCM4104EVM User's Guide includes schematics and PCB layout plots for reference. The evaluation module is available through Texas Instruments' distributors and sales representatives, or may be ordered online through the TI eStore, which can be accessed through the TI home page at http://www.ti.com.

The master clock generator supplies the system clock for the PCM4104, as well as the audio data source, such as a digital signal processor. The LRCK and BCK audio clocks should be derived from the system clock, in order to ensure synchronous operation.

ANALOG OUTPUT FILTER CIRCUITS

An external output filter is recommended for each differential output pair. The external output filter further reduces the out-of-band noise energy produced by the delta-sigma modulator, while providing band limiting suitable for audio reproduction. A 2nd-order Butterworth low-pass filter circuit with a −3dB corner frequency from 50kHz to 180kHz is recommended.

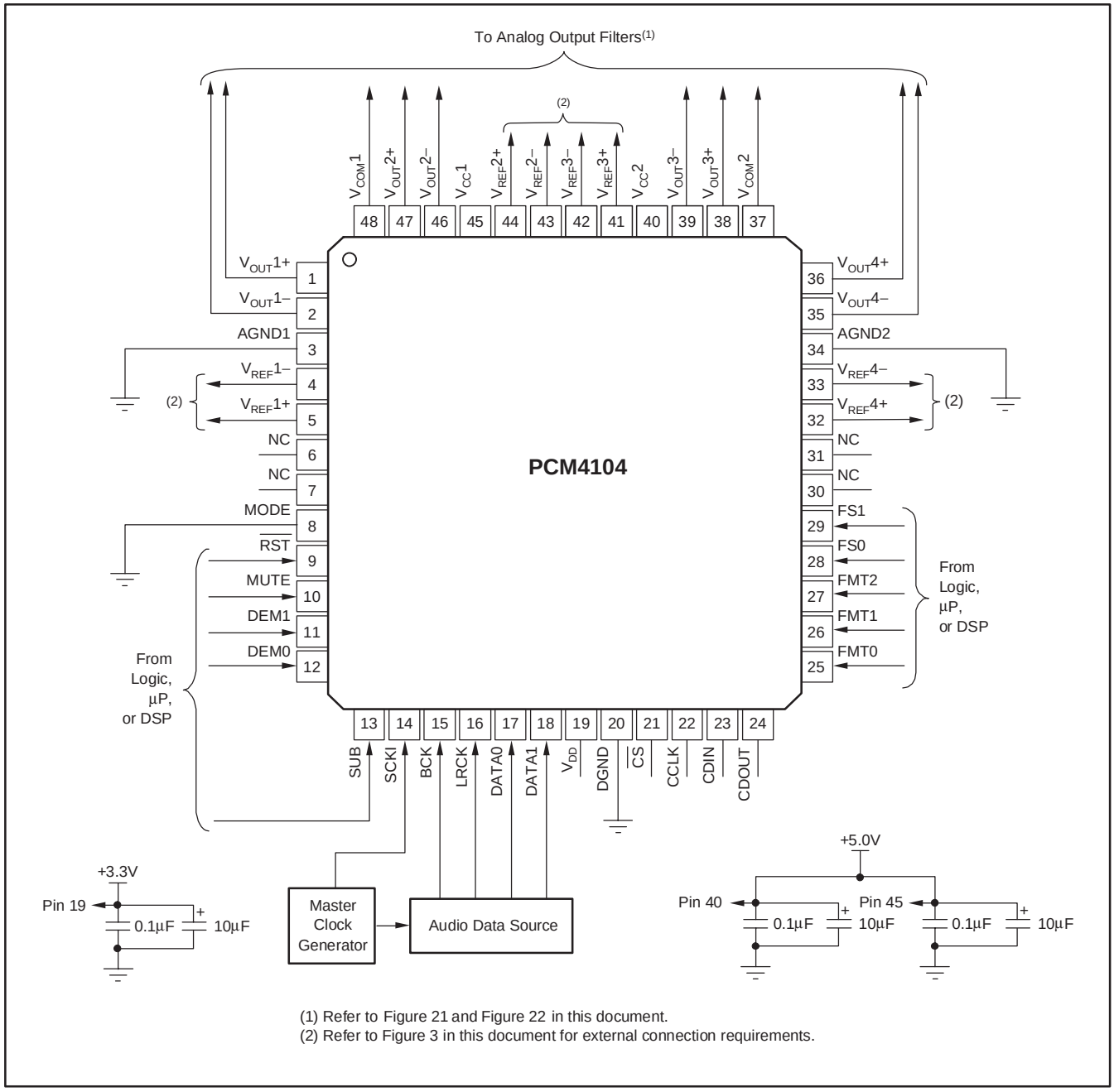
The configuration of the output filter circuit is dependent upon whether a single-ended or differential output is required. Single-ended outputs are commonly used in consumer playback systems, while differential or balanced outputs are used in many professional audio applications, such as recording or broadcast studios and live sound systems.

Figure 21 illustrates an active filter circuit that uses a single op amp to provide both 2nd-order low-pass filtering and differential to single-ended signal conversion. This circuit is used on the PCM4104EVM evaluation circuit and meets the published typical Electrical Characteristics for dynamic performance. The single-ended output is convenient for connecting to both headphone and power amplifiers when used for listening tests.

The quality of the op amp used is this circuit is important, as many devices will degrade the dynamic range and/or total harmonic distortion plus noise (THD+N) specifications for the PCM4104. An NE5534A is shown in Figure 21 and provides both low noise and distortion. Bipolar input op amps with equivalent specifications should produce similar measurement results. Devices that exhibit higher equivalent input noise voltage, such as the Texas Instruments OPA134 or OPA604 families, will produce lower dynamic range measurements (approximately 1dB to 2dB lower than the typical PCM4104 specification), while having little or no impact on the THD+N specification when measuring a full-scale output level.

Figure 22 illustrates a fully-differential output filter circuit suitable for use with the PCM4104. The OPA1632 from Texas Instruments provides the fully differential signal path in this circuit. The OPA1632 features very low noise and distortion, making it suitable for high-end audio applications.

Texas Instruments provides a free software tool, FilterPro™, used to assist in the design of active filter circuits. The software supports design of multiple feedback (MFB), Sallen-Key, and fully differential filter circuits. FilterPro is available from the TI web site. Additionally, TI document number SBAF001A, also available from the TI web site, provides pertinent application information regarding the proper usage of the FilterPro program.



(1) Refer to Figure 21 and Figure 22 in this document.
(2) Refer to Figure 3 in this document for external connection requirements.

Figure 19. Typical Standalone Mode Configuration

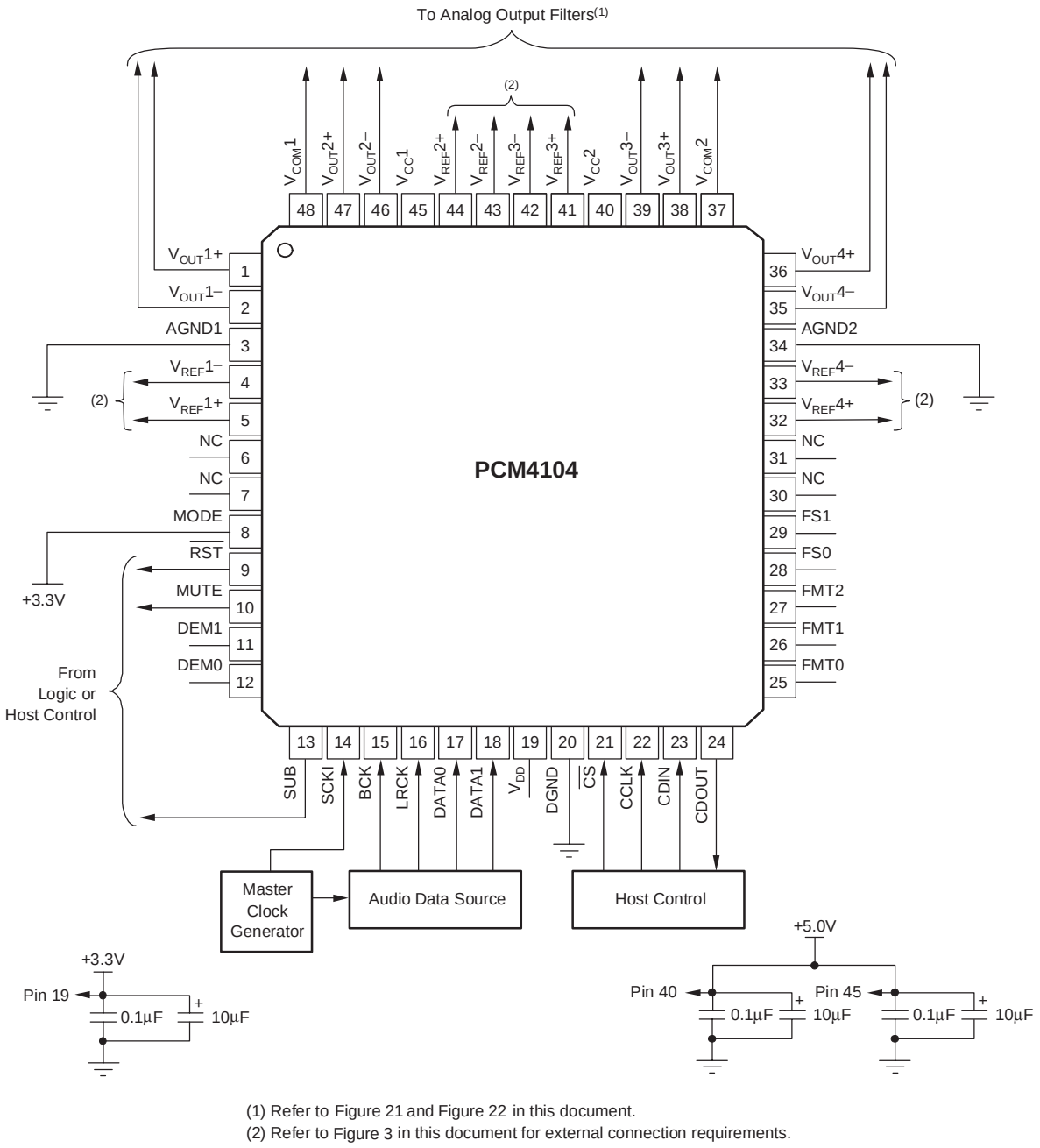


Figure 20. Typical Software Mode Configuration

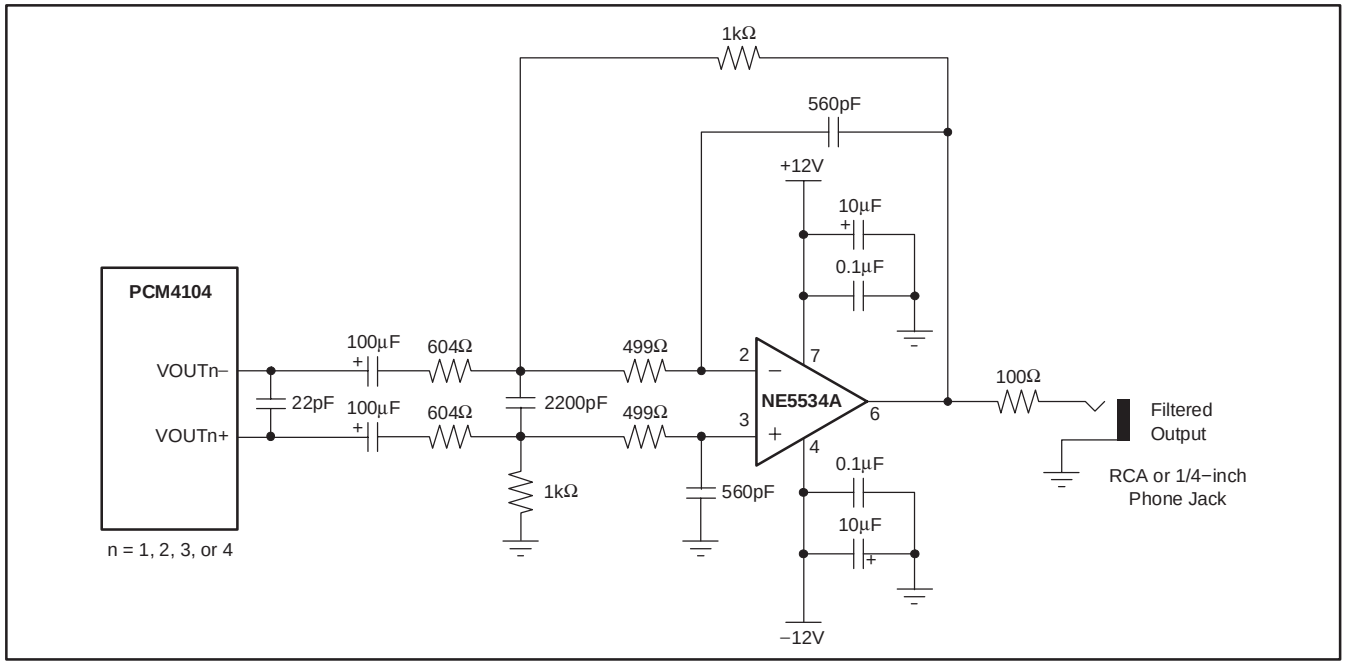


Figure 21. Single-Ended Output Filter Circuit

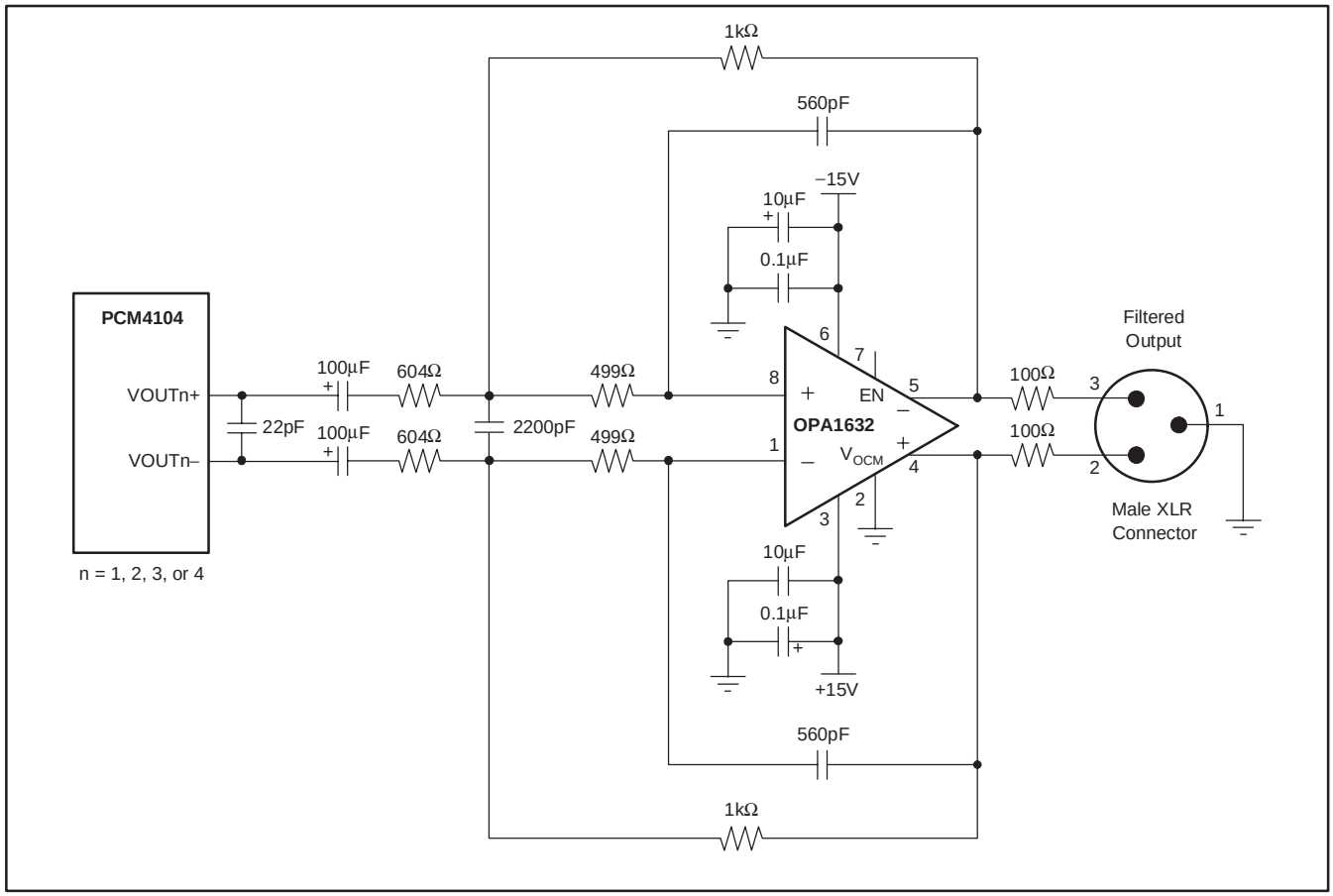


Figure 22. Differential Output Filter Circuit

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PCM4104PFBR	Active	Production	TQFP (PFB) | 48	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-10 to 70	PCM4104
PCM4104PFBR.B	Active	Production	TQFP (PFB) | 48	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-10 to 70	PCM4104
PCM4104PFBT	Active	Production	TQFP (PFB) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-10 to 70	PCM4104
PCM4104PFBT.B	Active	Production	TQFP (PFB) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-10 to 70	PCM4104
PCM4104PFBTG4	Active	Production	TQFP (PFB) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-10 to 70	PCM4104

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

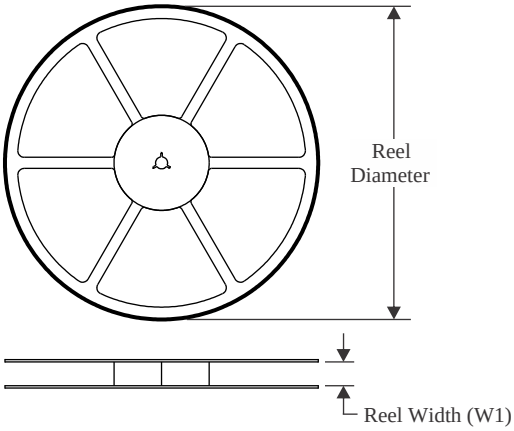
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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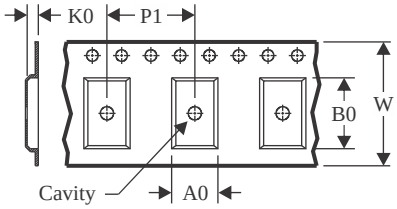
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

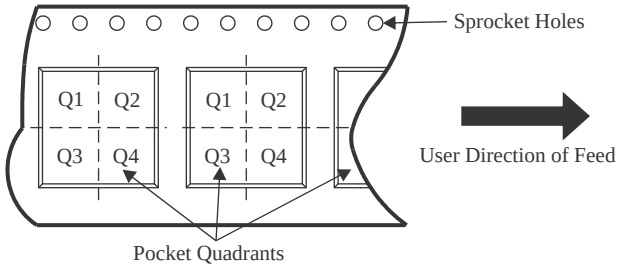


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

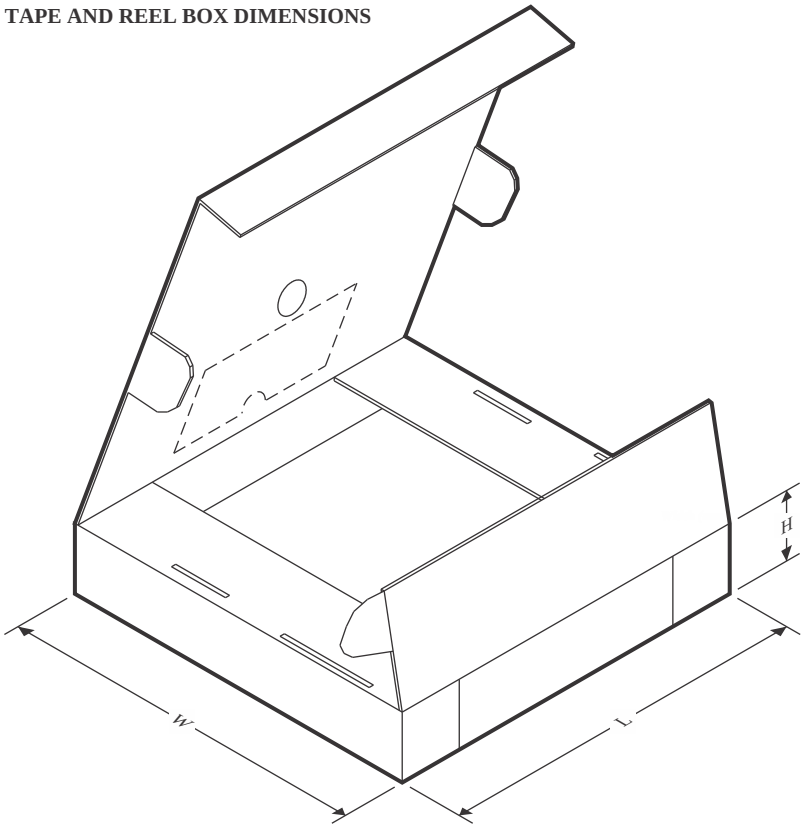
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCM4104PFBR	TQFP	PFB	48	2000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

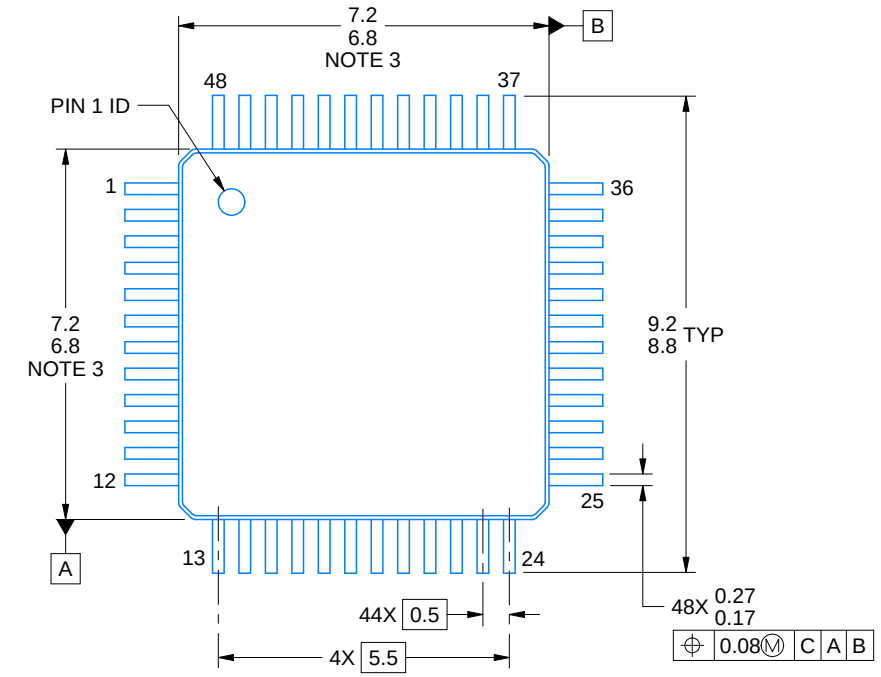
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCM4104PFBR	TQFP	PFB	48	2000	350.0	350.0	43.0

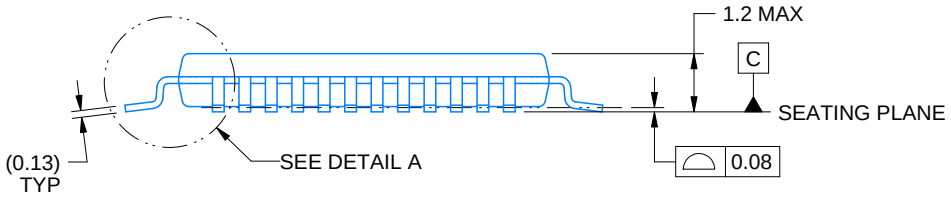
PACKAGE OUTLINE

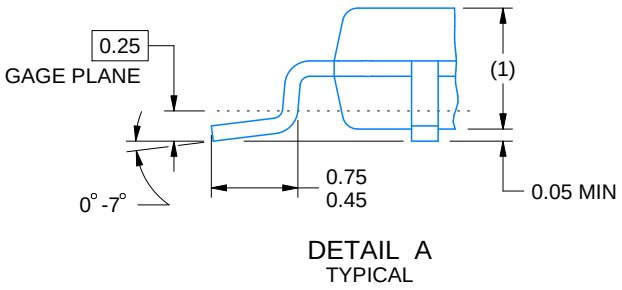
PFB0048A

TQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK





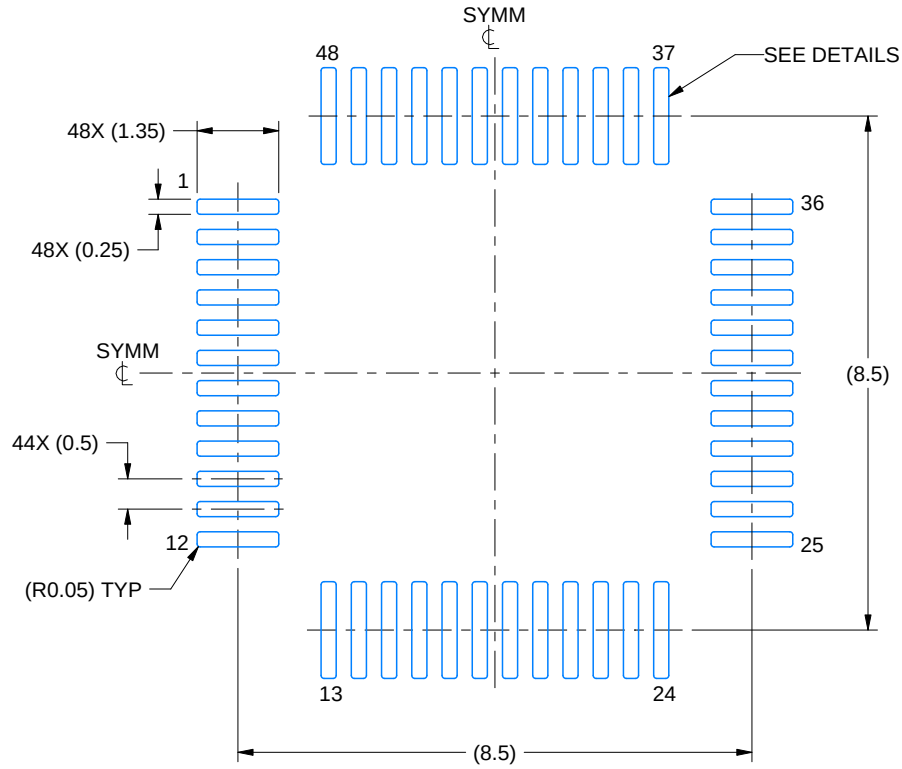


DETAIL A
TYPICAL

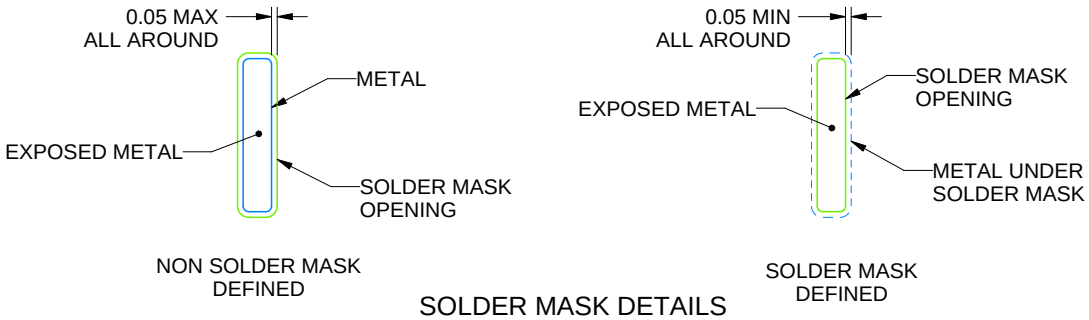
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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

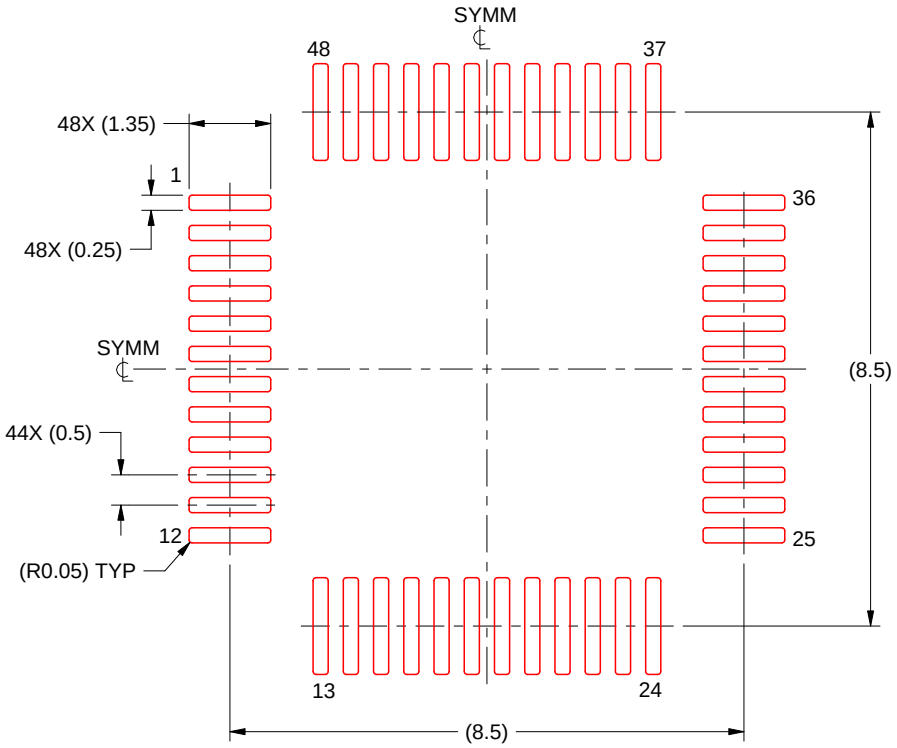


SOLDER MASK DETAILS

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NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
SCALE:8X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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