2V_{RMS} DirectPath™, 112/106/100dB Audio Stereo DAC with 32-bit, 384kHz PCM Interface

Check for Samples: PCM5100, PCM5101, PCM5102

FEATURES

- **Market-Leading Low Out-of-Band Noise**
- **Selectable Digital-Filter Latency and Performance**
- **No DC Blocking Capacitors Required**
- **Integrated Negative Charge Pump**
- **Internal Pop-Free Control For Sample-Rate Changes Or Clock Halts**
- **Intelligent Muting System; Soft Up or Down Ramp and Analog Mute For 120dB Mute SNR With Popless Operation.**
- **Integrated High-Performance Audio PLL With BCK Reference To Generate SCK Internally**
- **Small 20-pin TSSOP Package**

Typical Performance (3.3V Power Supply)

Parameter	PCM5102 / PCM5101 / PCM5100
SNR	112 / 106 / 100dB
Dynamic Range	112 / 106 / 100dB
THD+N @ - 1dBFS	–93 / –92 / –90dB
Full Scale Output	2.1V_{RMS} (GND center)
Normal 8× Oversampling Digital Filter Latency: 20/f_S	
Low Latency 8× Oversampling Digital Filter Latency: 3.5/f_S	
Sampling Frequency	8kHz to 384kHz
System Clock Multiples (f_{SCK}): 64, 128, 192, 256, 384, 512, 768, 1024, 1152, 1536, 2048, 3072; up to 50 MHz	

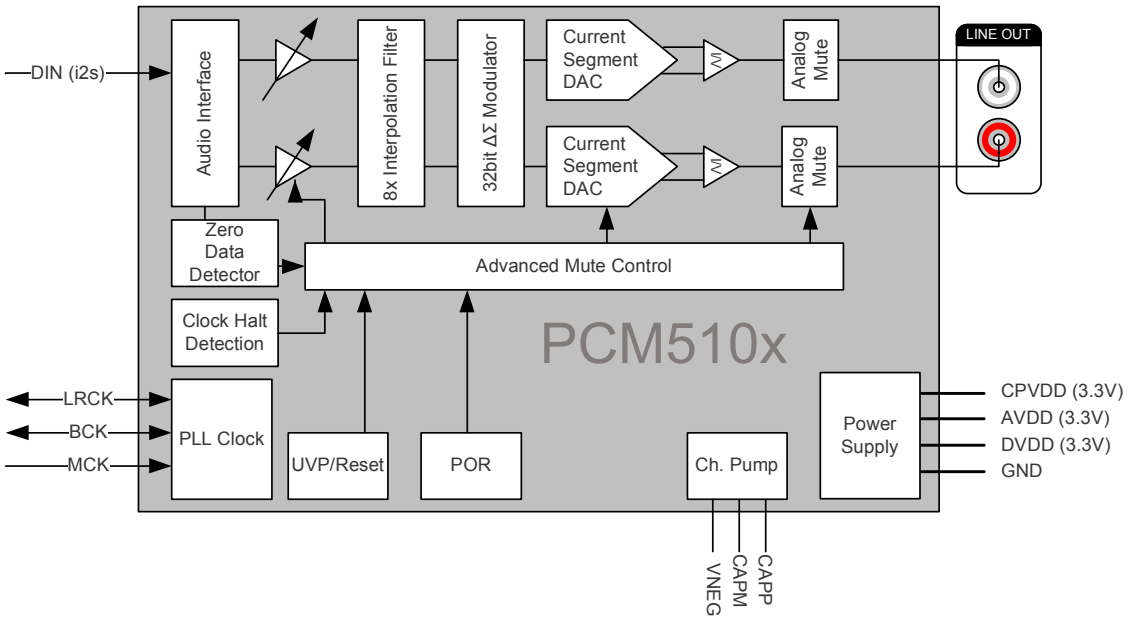


Figure 1. PCM510x Functional Block Diagram

OTHER KEY FEATURES

- **Accepts 16-, 24-, And 32-Bit Audio Data**
- **PCM Data Formats: I^2S, Left-Justified**
- **Automatic Power-Save Mode When LRCK And BCK Are Deactivated.**
- **3.3V Failsafe LVCMOS Digital Inputs**
- **Hardware Configuration**
- **Single Supply Operation:**
  - **3.3V Analog, 3.3V Digital**
- **Integrated Power-On Reset**

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ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

APPLICATIONS

- **A/V Receivers**
- **DVD, BD Players**
- **HDTV Receivers**
- **Applications Requiring $2V_{RMS}$ Audio Output**

DESCRIPTION

The PCM510x devices are a family of monolithic CMOS integrated circuits that include a stereo digital-to-analog converter and additional support circuitry in a small TSSOP package. The PCM510x uses the latest generation of TI's advanced segment-DAC architecture to achieve excellent dynamic performance and improved tolerance to clock jitter.

The PCM510x provides $2.1V_{RMS}$ ground centered outputs, allowing designers to eliminate DC blocking capacitors on the output, as well as external muting circuits traditionally associated with single supply line drivers.

The integrated line driver surpasses all other charge-pump based line drivers by supporting loads down to 1kΩ. By supporting loads down to 1kΩ, the PCM510x can essentially drive up to 10 products in parallel, such as an LCD TV, DVDR, AV Receivers and other devices.

The integrated PLL on the device removes the requirement for a system clock (commonly known as master clock), allowing a 3-wire I^2S connection and reducing system EMI.

Intelligent clock error and PowerSense under voltage protection utilizes a two level mute system for pop-free performance. Upon clock error or system power failure, the device digitally attenuates the data (or last known good data), then mutes the analog circuit

Compared with existing DAC technology, the PCM510x family offers up to 20dB lower out-of-band noise, reducing EMI and aliasing in downstream amplifiers/ADCs. (from traditional 100kHz OBN measurements all the way to 3MHz)

The PCM510x accepts industry-standard audio data formats with 16- to 32-bit data. Sample rates up to 384kHz are supported.

Table 1. Differences Between PCM510x Devices

Part Number	Dynamic Range	SNR	THD
PCM5102	112dB	112dB	–93dB
PCM5101	106dB	106dB	–92dB
PCM5100	100dB	100dB	–90dB

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ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DEVICE INFORMATION

TERMINAL FUNCTIONS, PCM510x

PCM510x (top view)

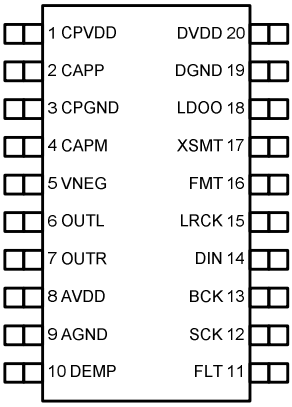


Table 2. TERMINAL FUNCTIONS, PCM510x

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
CPVDD	1	—	Charge pump power supply, 3.3V
CAPP	2	O	Charge pump flying capacitor terminal for positive rail
CPGND	3	—	Charge pump ground
CAPM	4	O	Charge pump flying capacitor terminal for negative rail
VNEG	5	O	Negative charge pump rail terminal for decoupling, -3.3V
OUTL	6	O	Analog output from DAC left channel
OUTR	7	O	Analog output from DAC right channel
AVDD	8	-—	Analog power supply, 3.3V
AGND	9	—	Analog ground
DEMP	10	I	De-emphasis control for 44.1kHz sampling rate(1): Off (Low) / On (High)
FLT	11	I	Filter select : Normal latency (Low) / Low latency (High)
SCK	12	I	System clock input(1)
BCK	13	I	Audio data bit clock input(1)
DIN	14	I	Audio data input(1)
LRCK	15	I	Audio data word clock input(1)
FMT	16	I	Audio format selection : I^2S (Low) / Left justified (High)
XSMT	17	I	Soft mute control(1): Soft mute (Low) / soft un-mute (High)
LDOO	18	—	Internal logic supply rail terminal for decoupling
DGND	19	—	Digital ground
DVDD	20	—	Digital power supply, 3.3V

(1) Failsafe LVCMOS Schmitt trigger input

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ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
Supply Voltage	AVDD, CPVDD, DVDD	–0.3 to 3.9	V
Digital Input Voltage		–0.3 to 3.9	
Analog Input Voltage		–0.3 to 3.9	
Operating Temperature Range		–25 to 85	°C
Storage Temperature Range		–65 to 150	

THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ_{JA}	Theta JA	High K		91.2		ºC/W
ψ_{JT}	Psi JT			1.0		
ψ_{JB}	Psi JB			41.5		
θ_{JC}	Theta JC	Top		25.3		
θ_{JB}	Theta JB			42.0		

ELECTRICAL CHARACTERISTICS

All specifications at T_A = 25°C, AV_{DD} = CPV_{DD} = DV_{DD} = 3.3V, f_S = 48kHz, system clock = 512 f_S and 24-bit data unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution		16	24	32	Bits
Data Format (PCM Mode)						
	Audio data interface format		I^2S, left justified			
	Audio data bit length		16, 24, 32-bit acceptable			
	Audio data format		MSB First, 2's Complement			
f_S (1)	Sampling frequency		8		384	kHz
	System clock frequency		64, 128, 192, 256, 384, 512, 768, 1024, 1152, 1536, 2048, or 3072 f_{SCK}, up to 50Mhz			
Digital Input/Output						
	Logic Family: 3.3V LVCMOS compatible					
V_{IH}	Input logic level		0.7×DV_{DD}			V
V_{IL}					0.3×DV_{DD}	
I_{IH}	Input logic current	V_{IN} = V_{DD}			10	µA
I_{IL}		V_{IN} = 0V			–10	
V_{OH}	Output logic level	I_{OH} = –4mA	0.8×DV_{DD}			V
V_{OL}		I_{OL} = 4mA			0.22×DV_{DD}	

(1) One sample time si defined as the reciprocal of the sampling frequency. $1t_S = 1/f_S$

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ELECTRICAL CHARACTERISTICS (continued)

All specifications at T_A = 25°C, AV_{DD} = CPV_{DD} = DV_{DD} = 3.3V, f_S = 48kHz, system clock = 512 f_S and 24-bit data unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Dynamic Performance (PCM Mode)(2)(3) (Values shown for three devices PCM5102/PCM5101/PCM5100)						
	THD+N at –1 dBFS(3)	f_S = 48kHz		–93/–92/–90	-83/ -82/ -80	dB
		f_S = 96kHz		–93/–92/–90		
		f_S = 192kHz		–93/–92/–90		
	Dynamic range(3)	EIAJ, A-weighted, f_S = 48kHz	106/ 100/ 95	112/106/100		
		EIAJ, A-weighted, f_S = 96kHz		112/106/100		
		EIAJ, A-weighted, f_S = 192kHz		112/106/100		
	Signal-to-noise ratio(3)	EIAJ, A-weighted, f_S = 48kHz		112/106/100		
		EIAJ, A-weighted, f_S = 96kHz		112/106/100		
		EIAJ, A-weighted, f_S = 192kHz		112/106/100		
	Signal to noise ratio with analog mute(3)(4)	EIAJ, A-weighted, f_S = 48kHz	113	123		
		EIAJ, A-weighted, f_S = 96kHz		123		
		EIAJ, A-weighted, f_S = 192kHz		123		
	Channel Separation	f_S = 48 kHz	100/ 95/ 90	109/103/97		
		f_S = 96kHz		109/103/97		
		f_S = 192kHz		109/103/97		
Analog Output						
	Output voltage			2.1		V_{RMS}
	Gain error		–6	±2.0	6	% of FSR
	Gain mismatch, channel-to-channel		–6	±2.0	6	% of FSR
	Bipolar zero error	At bipolar zero	–5	±1.0	5	mV
	Load impedance		1			kΩ
Filter Characteristics–1: Normal						
	Pass band				0.45f_S	
	Stop band		0.55f_S			
	Stop band attenuation		–60			dB
	Pass-band ripple				±0.02	
	Delay time			20/f_S		s
Filter Characteristics–2: Low Latency						
	Pass band				0.47f_S	
	Stop band		0.55f_S			
	Stop band attenuation		–52			dB
	Pass-band ripple				±0.0001	
	Delay time			3.5/f_S		s

(2) Filter condition: THD+N: 20Hz HPF, 20kHz AES17 LPF Dynamic range: 20Hz HPF, 20kHz AES17 LPF, A-weighted Signal-to-noise ratio: 20Hz HPF, 20kHz AES17 LPF, A-weighted Channel separation: 20Hz HPF, 20kHz AES17 LPF Analog performance specifications are measured using the System Two Cascade™ audio measurement system by Audio Precision™ in the RMS mode.
(3) Output load is 10kΩ, with 470Ω output resistor and a 2.2nF shunt capacitor (see recommended output filter).
(4) Assert XSMT or both L-ch and R-ch PCM data are BPZ

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ELECTRICAL CHARACTERISTICS (continued)

All specifications at T_A = 25°C, AV_{DD} = CPV_{DD} = DV_{DD} = 3.3V, f_S = 48kHz, system clock = 512 f_S and 24-bit data unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply Requirements						
DV_{DD}	Digital supply voltage	Target DV_{DD} = 3.3V	3.0	3.3	3.6	VDC
AV_{DD}	Analog supply voltage		3.0	3.3	3.6	
CPV_{DD}	Charge-pump suply voltage		3.0	3.3	3.6	
I_{DD}	DV_{DD} supply current at 3.3V(5)	f_S = 48kHz		7	12	mA
		f_S = 96kHz		8		
		f_S = 192kHz		9		
I_{DD}	DV_{DD} supply current at 3.3V(6)	f_S = 48kHz		8	13	mA
		f_S = 96kHz		9		
		f_S = 192kHz		10		
I_{DD}	DV_{DD} supply current at 3.3V(7)			0.5	0.8	mA
I_{CC}	AV_{DD} / CPV_{DD} Supply Current(5)	f_S = 48kHz		11	16	mA
		f_S = 96kHz		11		
		f_S = 192kHz		11		
I_{CC}	AV_{DD} / CPV_{DD} Supply Current(6)	f_S = 48kHz		22	32	mA
		f_S = 96kHz		22		
		f_S = 192kHz		22		
I_{CC}	AV_{DD} / CPV_{DD} Supply Current(7)	f_S = n/a		0.2	0.4	mA
	Power Dissipation, DV_{DD} = 3.3V(5)	f_S = 48kHz		59.4	92.4	mW
		f_S = 96kHz		62.7		
		f_S = 192kHz		66.0		
	Power Dissipation, DV_{DD} = 3.3V(6)	f_S = 48kHz		99.0	148.5	mW
		f_S = 96kHz		102.3		
		f_S = 192kHz		105.6		
	Power Dissipation, DV_{DD} = 3.3V(7)	f_S = n/a (Power Down Mode)		2.3	4.0	mW

(5) Input is Bipolar Zero data.
(6) Input is 1kHz -1dBFS data
(7) Power Down Mode

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TYPICAL CHARACTERISTICS

All specifications at T_A = 25°C, AV_{DD} = CPV_{DD} = DV_{DD} = 3.3V, f_S = 48kHz, system clock = 512 f_S and 24-bit data unless otherwise noted.

PCM5100 THD+N vs Input Level

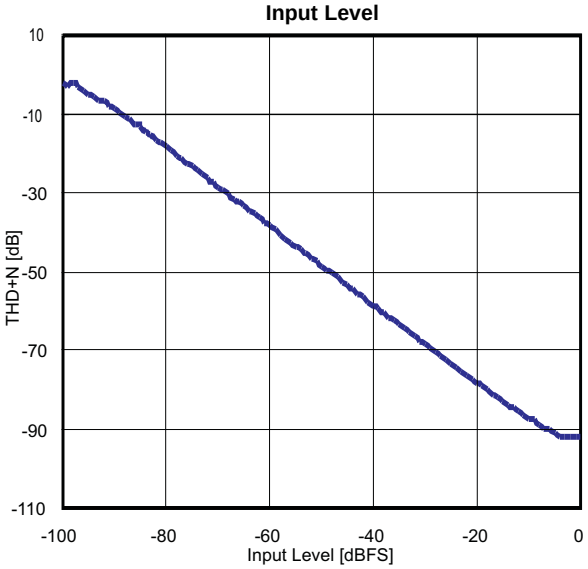


Figure 2.

PCM5101 THD+N vs Input Level

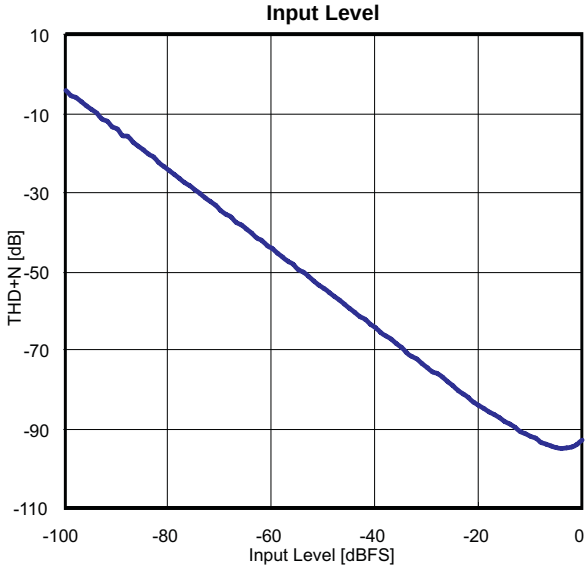


Figure 3.

PCM5102 THD+N vs Input Level

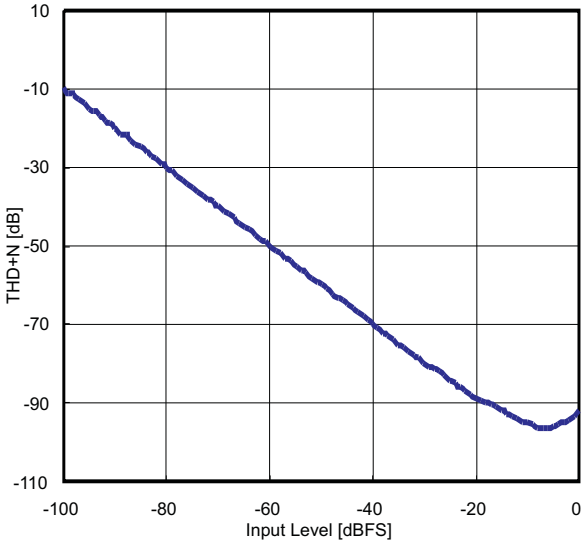


Figure 4.

TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = 25°C, AV_{DD} = CPV_{DD} = DV_{DD} = 3.3V, f_S = 48kHz, system clock = 512 f_S and 24-bit data unless otherwise noted.

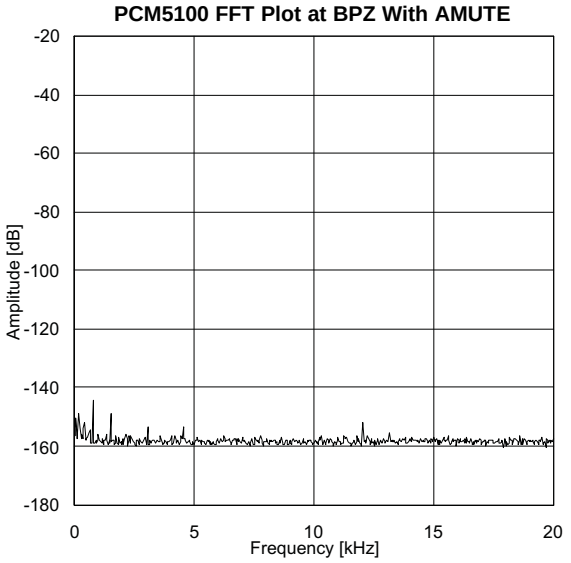


Figure 5.

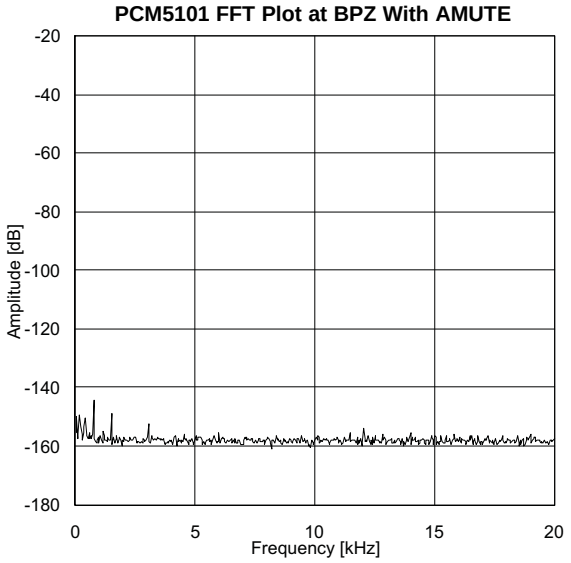


Figure 6.

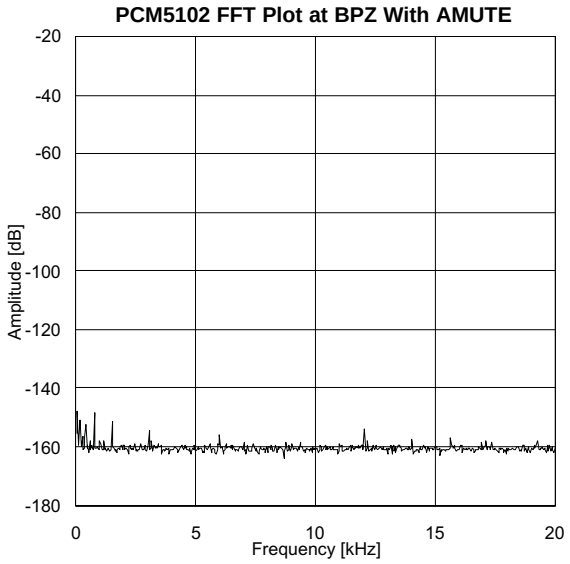


Figure 7.

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TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = 25°C, AV_{DD} = CPV_{DD} = DV_{DD} = 3.3V, f_S = 48kHz, system clock = 512 f_S and 24-bit data unless otherwise noted.

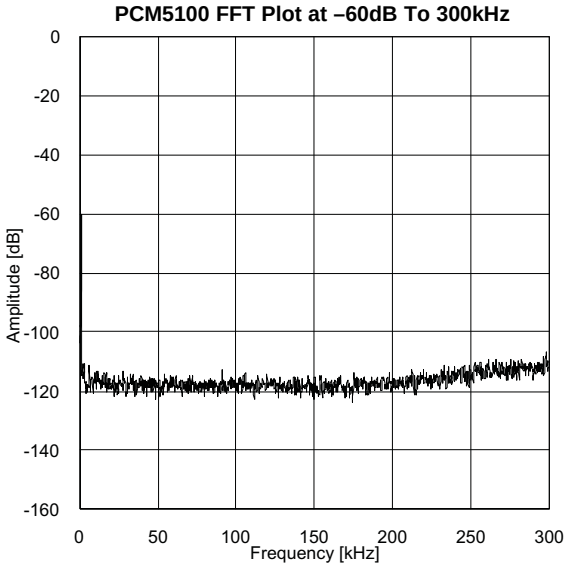


Figure 8.

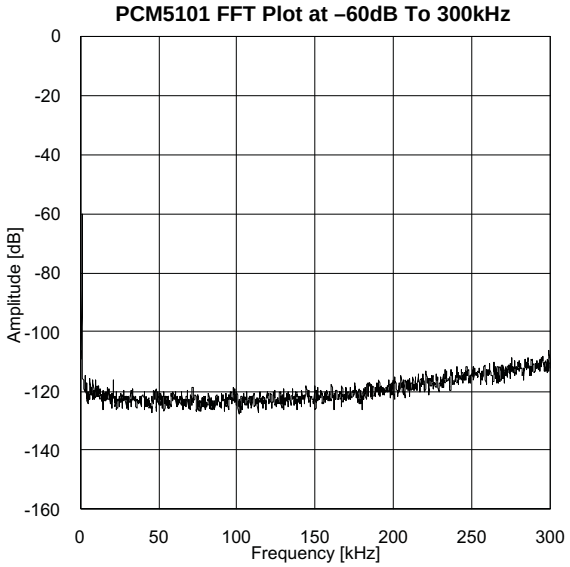


Figure 9.

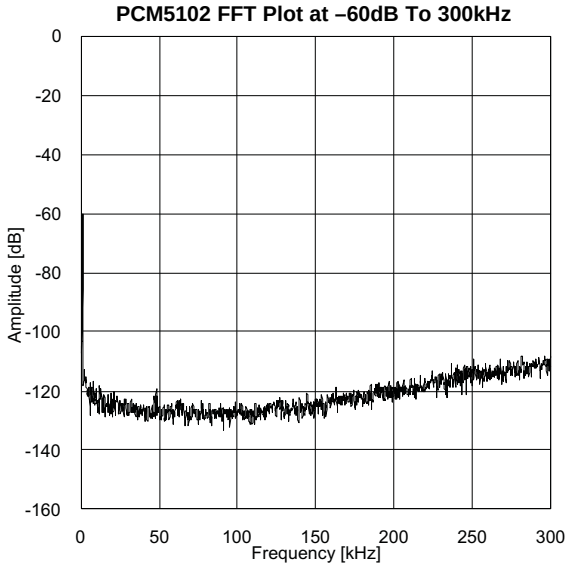


Figure 10.

APPLICATION INFORMATION

Reset and System Clock Functions

Power-On Reset Function

The PCM510x includes a power-on reset function shown in Figure 11. With V_{DD} > 2.8V, the power-on reset function is enabled. After the initialization period, the PCM510x is set to its default reset state.

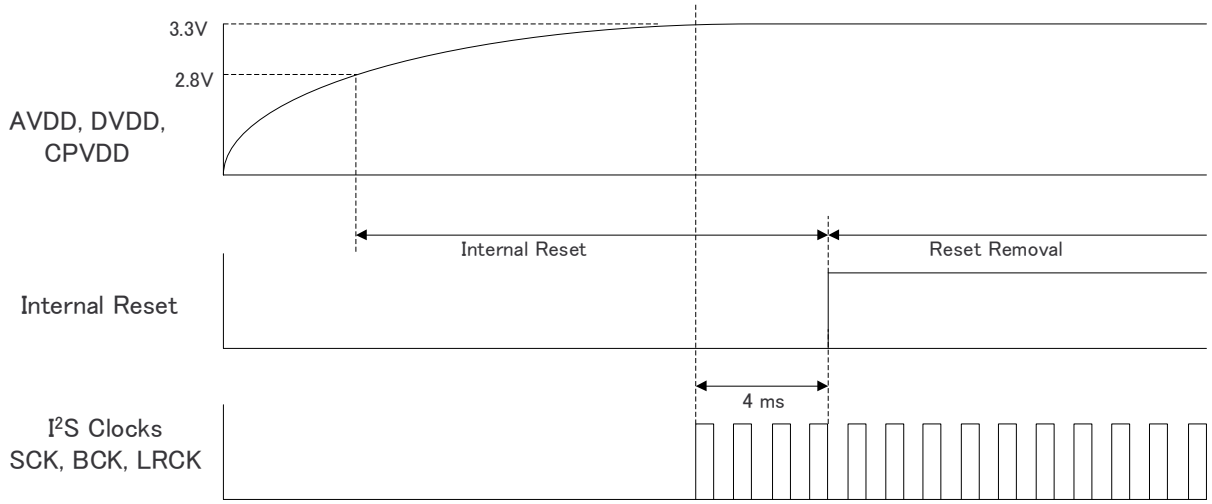


Figure 11. Power-On Reset Timing, DVDD = 3.3V

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System Clock Input

The PCM510x requires a system clock to operate the digital interpolation filters and advanced segment DAC modulators. The system clock is applied at the SCK input (pin 12) and supports up to 50MHz. The PCM510x system-clock detection circuit automatically senses the system-clock frequency. Common audio sampling frequencies of 8kHz, 16kHz, 32kHz - 44.1kHz - 48kHz, 88.2kHz - 96kHz, 176.4kHz -192kHz, and 384kHz with ±4% tolerance are supported. The sampling frequency detector sets the clock for the digital filter, Delta Sigma Modulator (DSM) and the Negative Charge Pump (NCP) automatically. Table 3 shows examples of system clock frequencies for common audio sampling rates.

SCK rates that are not common to standard audio clocks, between 1MHz and 50MHz, are only supported in software mode, available only in the PCM512x and PCM514x devices, by configuring various PLL and clock-divider registers. Software mode allows the device to become a clock master and drive the host serial port with LRCK and BCK, from a non-audio related clock; for example, using 12MHz to generate 44.1kHz (LRCK) and 2.8224MHz (BCK).

Figure 12 shows the timing requirements for the system clock input. For optimal performance, it is important to use a clock source with low phase jitter and noise.

Table 3. System Master Clock Inputs for Audio Related Clocks

Sampling Frequency	System Clock Frequency (f_{SCK}) (MHz)											
	64 f_S	128 f_S	192 f_S	256 f_S	384 f_S	512 f_S	768 f_S	1024 f_S	1152 f_S	1536 f_S	2048 f_S	3072 f_S
8 kHz	–(1)	1.0240(2)	1.5360(2)	2.0480	3.0720	4.0960	6.1440	8.1920	9.2160	12.2880	16.3840	24.5760
16 kHz	–(1)	2.0480(2)	3.0720(2)	4.0960	6.1440	8.1920	12.2880	16.3840	18.4320	24.5760	36.8640	49.1520
32 kHz	–(1)	4.0960(2)	6.1440(2)	8.1920	12.2880	16.3840	24.5760	32.7680	36.8640	49.1520	–(1)	–(1)
44.1 kHz	–(1)	5.6488(2)	8.4672(2)	11.2896	16.9344	22.5792	33.8688	45.1584	–(1)	–(1)	–(1)	–(1)
48 kHz	–(1)	6.1440(2)	9.2160(2)	12.2880	18.4320	24.5760	36.8640	49.1520	–(1)	–(1)	–(1)	–(1)
88.2 kHz	–(1)	11.2896(2)	16.9344	22.5792	33.8688	45.1584	–(1)	–(1)	–(1)	–(1)	–(1)	–(1)
96 kHz	–(1)	12.2880(2)	18.4320	24.5760	36.8640	49.1520	–(1)	–(1)	–(1)	–(1)	–(1)	–(1)
176.4 kHz	–(1)	22.5792	33.8688	45.1584	–(1)	–(1)	–(1)	–(1)	–(1)	–(1)	–(1)	–(1)
192 kHz	–(1)	24.5760	36.8640	49.1520	–(1)	–(1)	–(1)	–(1)	–(1)	–(1)	–(1)	–(1)
384 kHz	24.5760	49.1520	–(1)	–(1)	–(1)	–(1)	–(1)	–(1)	–(1)	–(1)	–(1)	–(1)

(1) This system clock rate is not supported for the given sampling frequency.
(2) This system clock rate is supported by PLL mode.

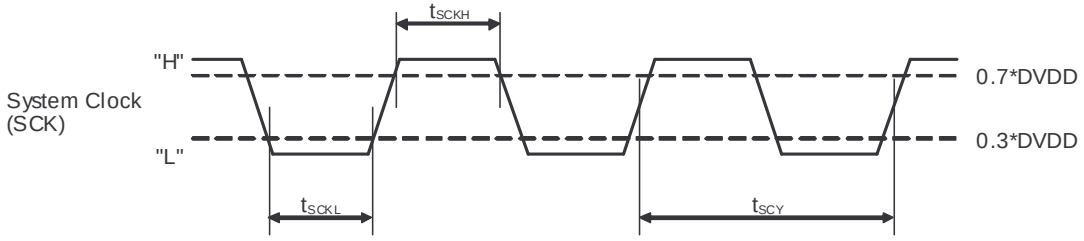


Figure 12. Timing Requirements for SCK Input

Table 4. Timing Requirements for SCK Input

	Parameters	Min	Max	Unit
t_{SCY}	System clock pulse cycle time	20	1000	ns
t_{SCKH}	System clock pulse width, High	9		ns
t_{SCKL}	System clock pulse width, Low	9		ns

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System Clock PLL Mode

The system clock PLL mode allows designers to use a simple 3-wire I^2S audio source when driving the DAC. The 3-wire source reduces the need for a high frequency SCK, making PCB layout easier, and reduces high frequency electromagnetic interference.

The device starts up expecting an external SCK input, but if BCK and LRCK start correctly while SCK remains at ground level for 16 successive LRCK periods, then the internal PLL starts, automatically generating an internal SCK from the BCK reference. The PCM510x disables the internal PLL when an external SCK is supplied; specific BCK rates are required to generate an appropriate master clock. Table 5 describes the minimum and maximum BCK per LRCK for the integrated PLL to automatically generate an internal SCK.

Table 5. BCK Rates (MHz) by LRCK Sample Rate for PCM510x PLL Operation

	BCK (f_S)	
Sample f (kHz)	32	64
8	-	-
16	-	1.024
32	1.024	2.048
44.1	1.4112	2.8224
48	1.536	3.072
96	3.072	6.144
192	6.144	12.288
384	12.288	24.576

Audio Data Interface

Audio Serial Interface

The audio interface port is a 3-wire serial port, including LRCK (pin 15), BCK (pin 13), and DIN (pin 14). BCK is the serial audio bit clock, used to clock the serial data present on DIN into the serial shift register of the audio interface. Serial data is clocked into the PCM510x on the rising edge of BCK. LRCK is the serial audio left/right word clock.

Table 6. PCM510x Audio Data Formats, Bit Depths and Clock Rates

CONTROL MODE	FORMAT	DATA BITS	MAX LRCK FREQUENCY [f_S]	SCK RATE [x f_S]	BCK RATE [x f_S]
Hardware Control	I^2S/LJ	32, 24, 20, 16	Up to 192kHz	128 – 3072 (≤50MHz)	64, 48, 32
			384kHz	64, 128	64, 48, 32

The PCM510x requires the synchronization of LRCK and system clock, but does not need a specific phase relation between LRCK and system clock.

If the relationship between LRCK and system clock changes more than ±5 SCK, internal operation is initialized within one sample period and analog outputs are forced to the bipolar zero level until resynchronization between LRCK and system clock is completed.

If the relationship between LRCK and BCK are invalid more than 4 LRCK periods, internal operation is initialized within one sample period and analog outputs are forced to the bipolar zero level until resynchronization between LRCK and BCK is completed.

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PCM Audio Data Formats and Timing

The PCM510x supports industry-standard audio data formats, including standard I^2S and left-justified. Data formats are selected using the FMT (pin 16), Low for I^2S, and High for Left-justified.

All formats require binary 2s complement, MSB-first audio data. Figure 13 shows a detailed timing diagram for the serial audio interface.

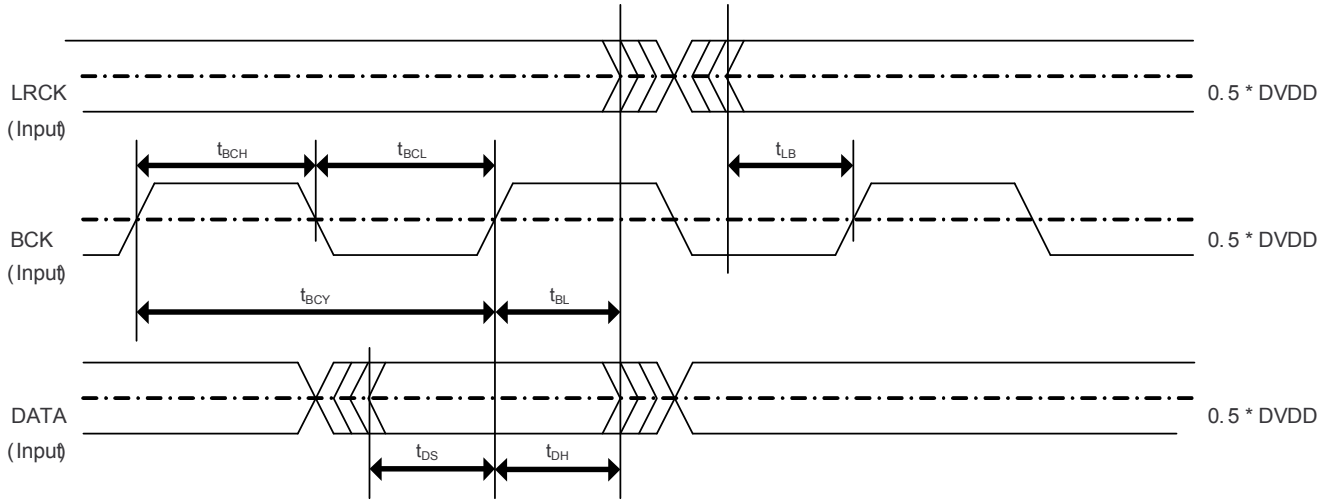
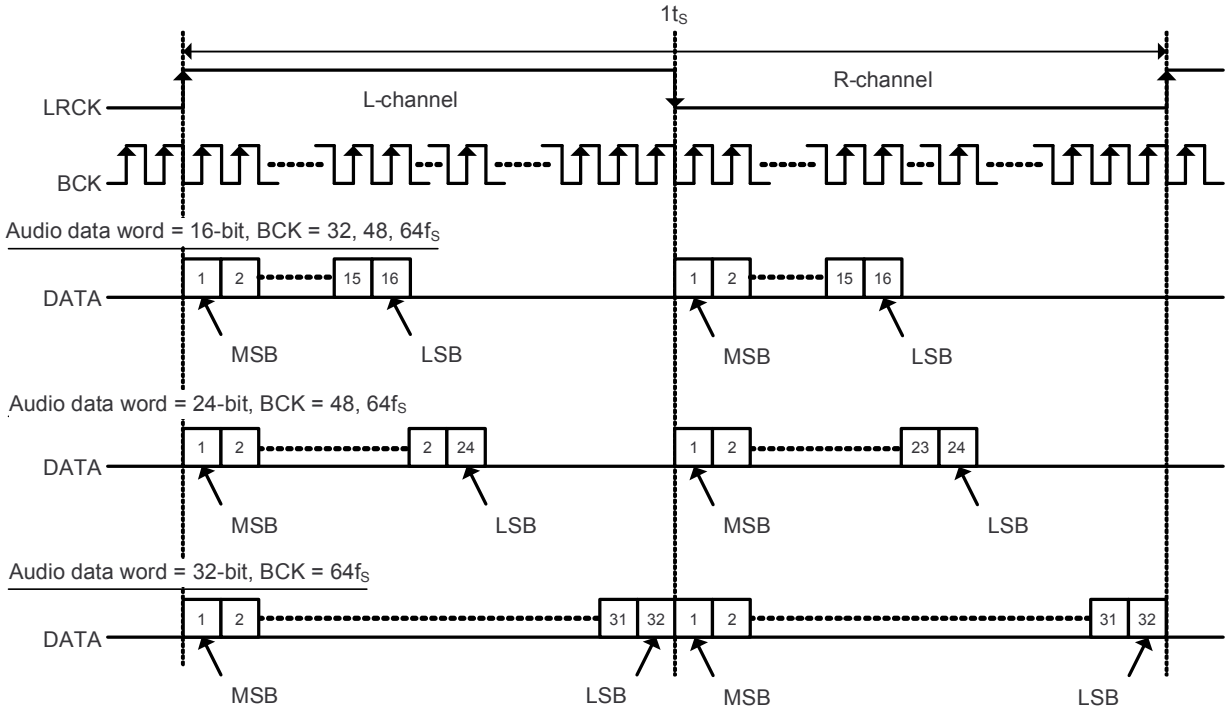


Figure 13. PCM510x Serial Audio Timing - Slave

Table 7. Audio Interface Slave Timing

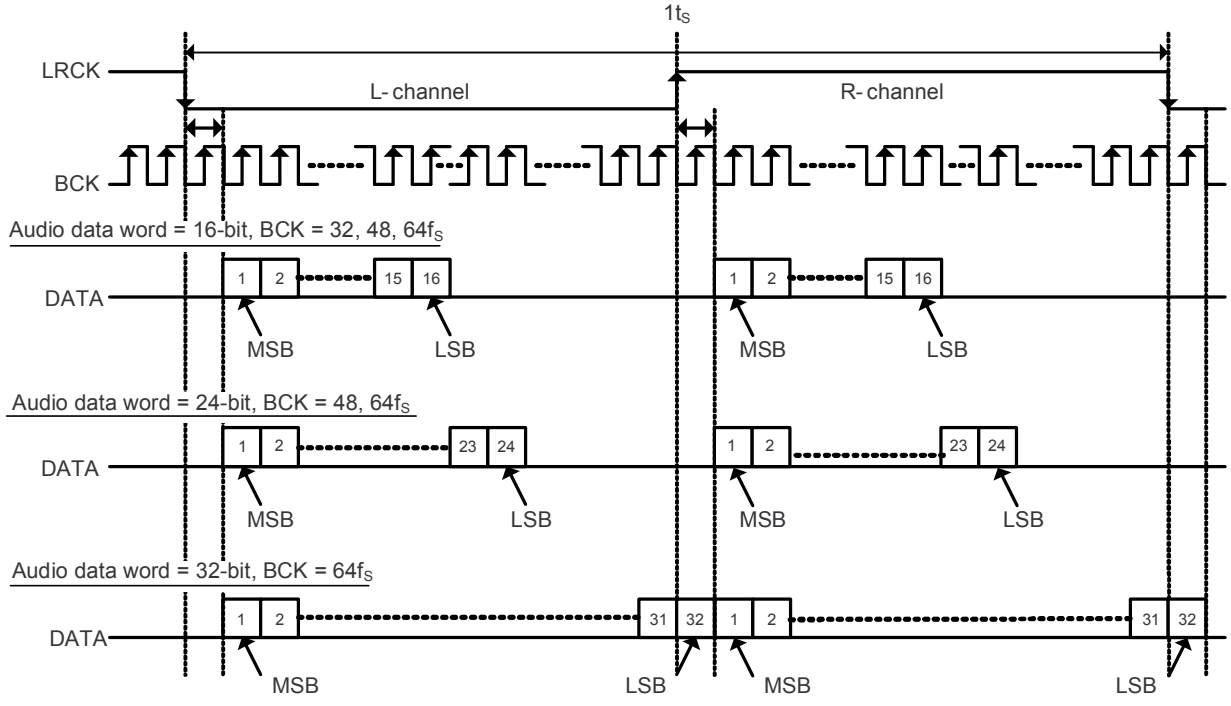
	Parameters	Min	Max	Units
t_{BCY}	BCK Pulse Cycle Time	40		ns
t_{BCL}	BCK Pulse Width LOW	16		ns
t_{BCH}	BCK Pulse Width HIGH	16		ns
t_{BL}	BCK Rising Edge to LRCK Edge	8		ns
t_{LB}	LRCK Edge to BCK Rising Edge	8		ns
t_{DS}	DATA Set Up Time	8		ns
t_{DH}	DATA Hold Time	8		ns
f_{BCK}	BCK frequency @ DVDD=3.3V		24.576	MHz

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Left Justified Data Format; L-channel = HIGH, R-channel = LOW

Figure 14. Left Justified Audio Data Format



I²S Data Format; L-channel = LOW, R-channel = HIGH

Figure 15. I²S Audio Data Format

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Function Descriptions

Interpolation Filter

The PCM510x provides 2 types of interpolation filter. Users can select which filter to use by using the FLT pin (pin11)

Table 8. Digital Interpolation Filter Options

FLT Pin	Description
0	FIR Normal x8/x4/x2/x1 Interpolation Filters
1	IIR Low Latency x8/x4/x2/x1 Interpolation Filters

The Normal x8/x4/x2/x1(bypass) Interpolation filter is programmed in 256 cycles in 1 sample time (t_S) for sample rates from 8kHz to 384kHz.

Table 9. Normal x8 Interpolation Filter

Parameter	Condition	Value (Typ)	Value (Max)	Units
Filter Gain Pass Band	0 ……. $0.45f_S$		±0.02	dB
Filter Gain Stop Band	$0.55f_S$ ….. $7.455f_S$	–60		dB
Filter Group Delay		$22t_S$		s

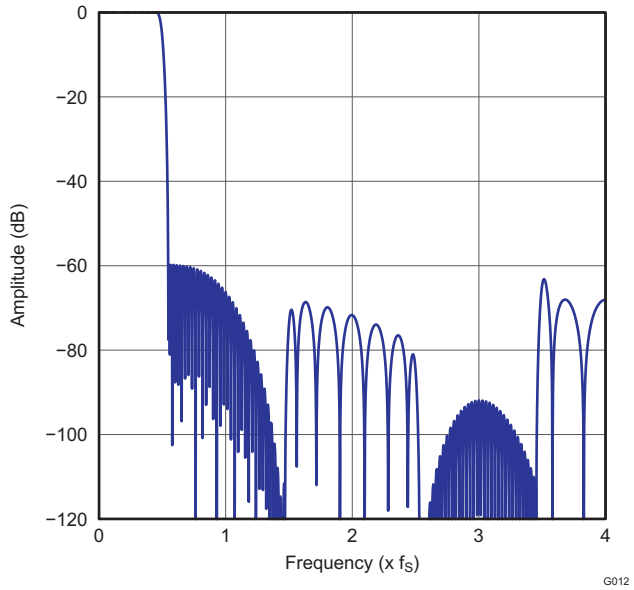


Figure 16. Normal x8 Interpolation Filter Frequency Response

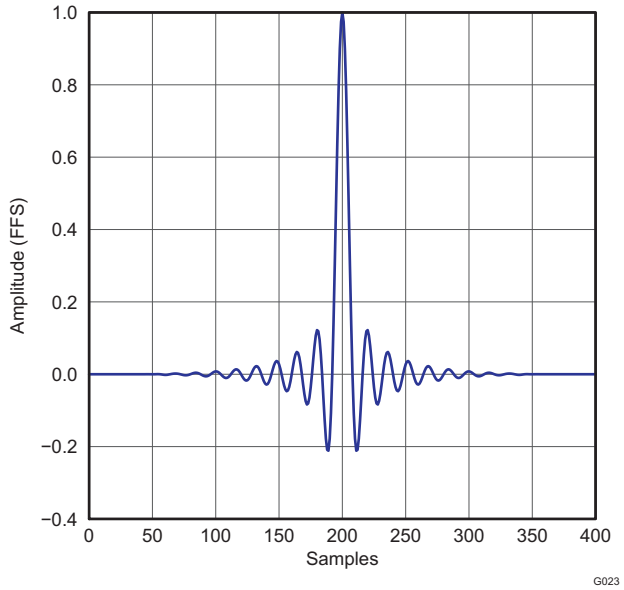


Figure 17. Normal x8 Interpolation Filter Impulse Response

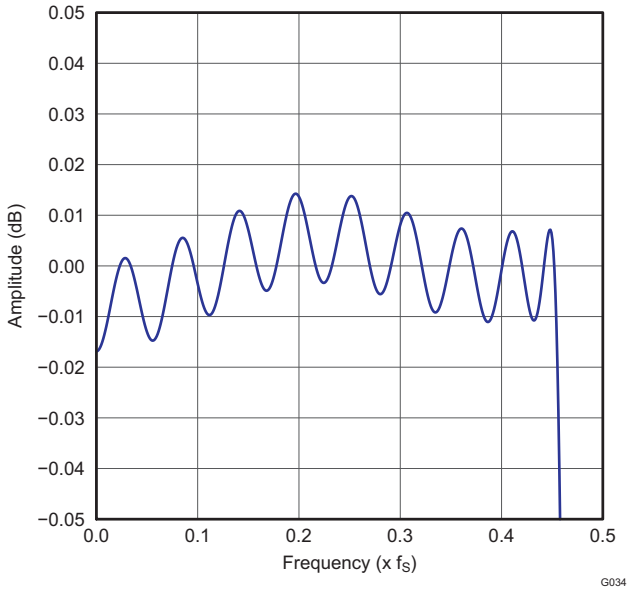


Figure 18. Normal x8 Interpolation Filter Passband Ripple

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The Normal x4/x2/x1(bypass) Interpolation filter is programmed in 256 cycles in 1 sample time (t_S) for sample rates from 8kHz to 384kHz.

Table 10. Normal x4 Interpolation Filter

Parameter	Condition	Value (Typ)	Value (Max)	Units
Filter Gain Pass Band	0 ……. $0.45f_S$		±0.02	dB
Filter Gain Stop Band	$0.55f_S$ ….. $7.455f_S$	–60		dB
Filter Group Delay		$22t_S$		s

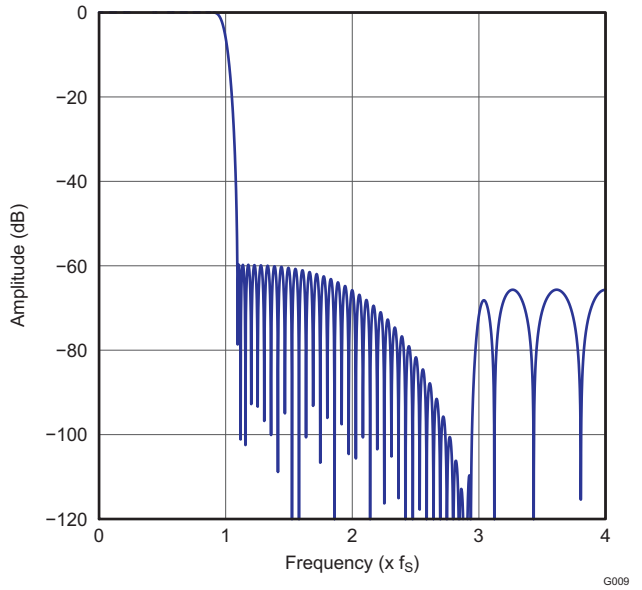


Figure 19. Normal x4 Interpolation Filter Frequency Response

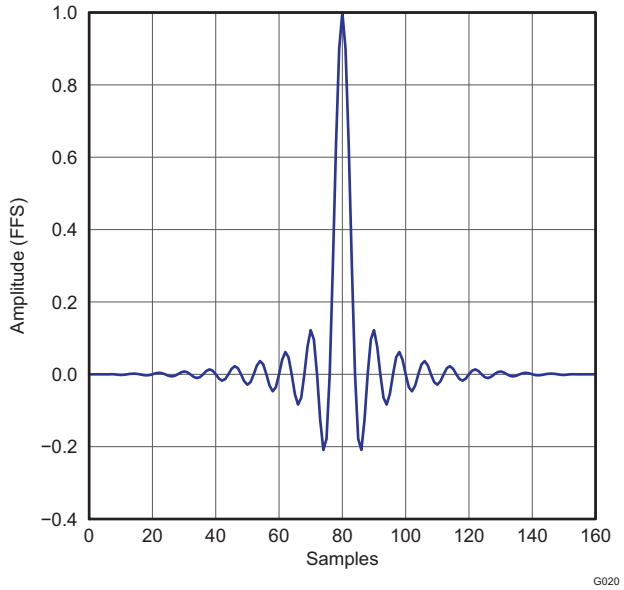


Figure 20. Normal x4 Interpolation Filter Impulse Response

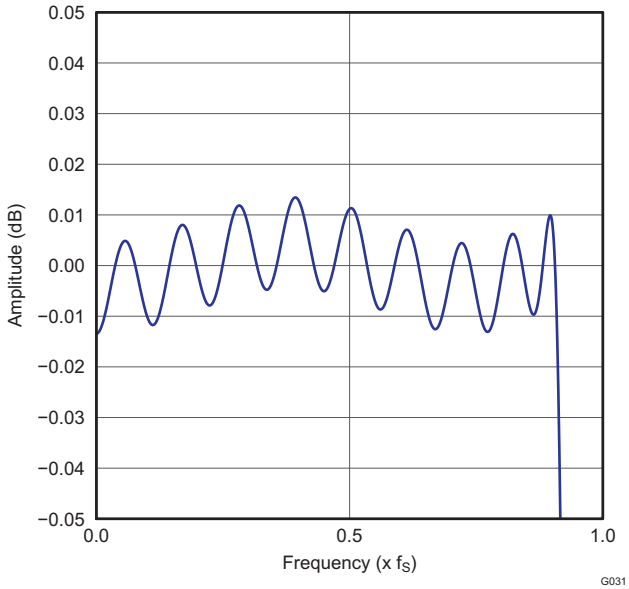


Figure 21. Normal x4 Interpolation Filter Passband Ripple

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Normal x2 / x1(bypass) Interpolation filter is programmed in 256 cycles in 1 sample time (t_S) for sample rates from 8kHz to 384kHz.

Table 11. Normal x2 Interpolation Filter

Parameter	Condition	Value (Typ)	Value (Max)	Units
Filter Gain Pass Band	0 ……. $0.45f_S$		±0.02	dB
Filter Gain Stop Band	$0.55f_S$ ….. $7.455f_S$	–60		dB
Filter Group Delay		$22t_S$		s

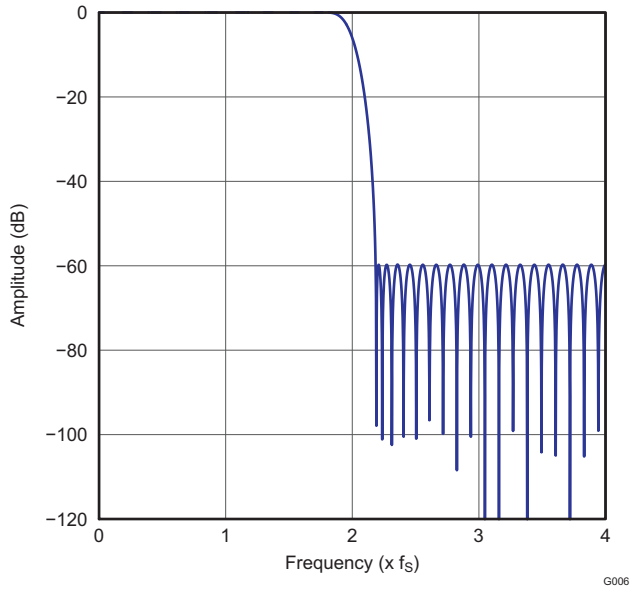


Figure 22. Normal x2 Interpolation Filter Frequency Response

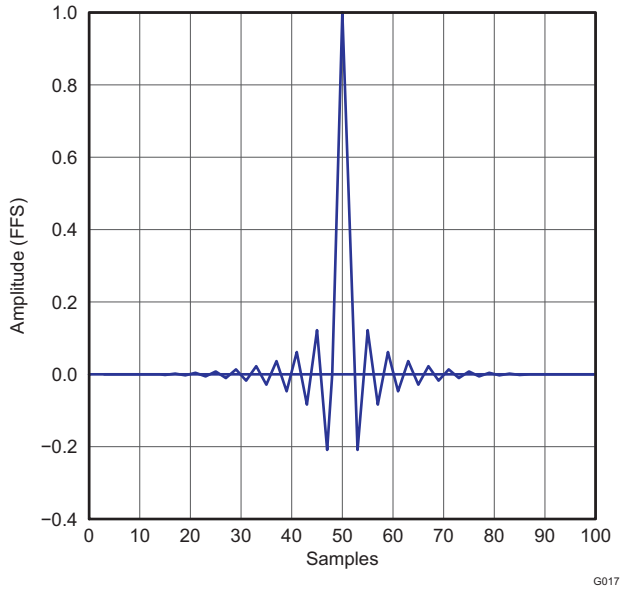


Figure 23. Normal x2 Interpolation Filter Impulse Response

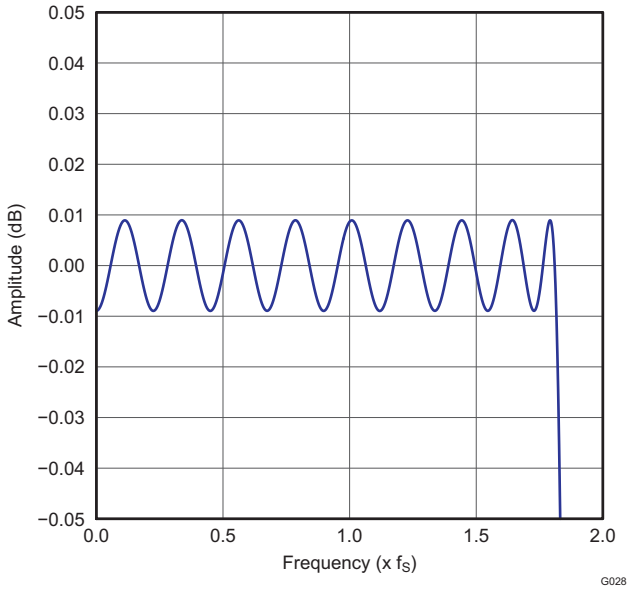


Figure 24. Normal x2 Interpolation Filter Passband Ripple

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The low-latency x8 / x4 / x2 / x1(bypass) Interpolation filter is programmed in 256 cycles 1 sample time (t_S) for sample rates from 8kHz to 384kHz.

Table 12. Low latency x8 Interpolation Filter

Parameter	Condition	Value (Typ)	Units
Filter Gain Pass Band	0 ……. $0.45f_S$	±0.0001	dB
Filter Gain Stop Band	$0.55f_S$ ….. $7.455f_S$	–52	dB
Filter Group Delay		$3.5t_S$	s

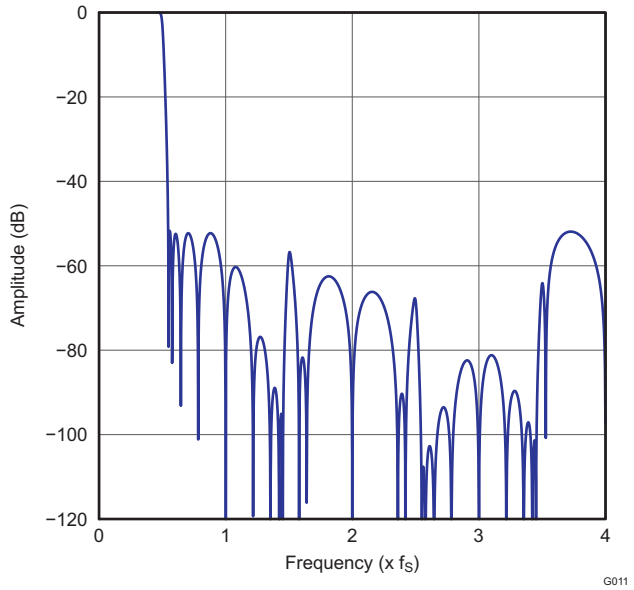


Figure 25. Low latency x8 Interpolation Filter Frequency Response

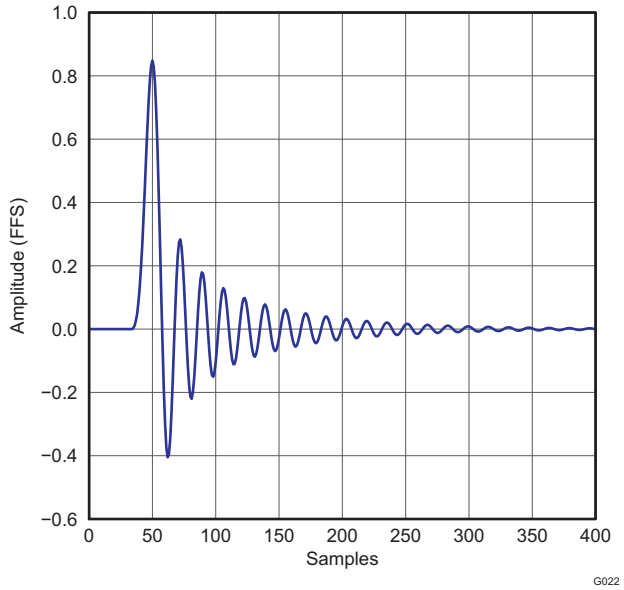


Figure 26. Low latency x8 Interpolation Filter Impulse Response

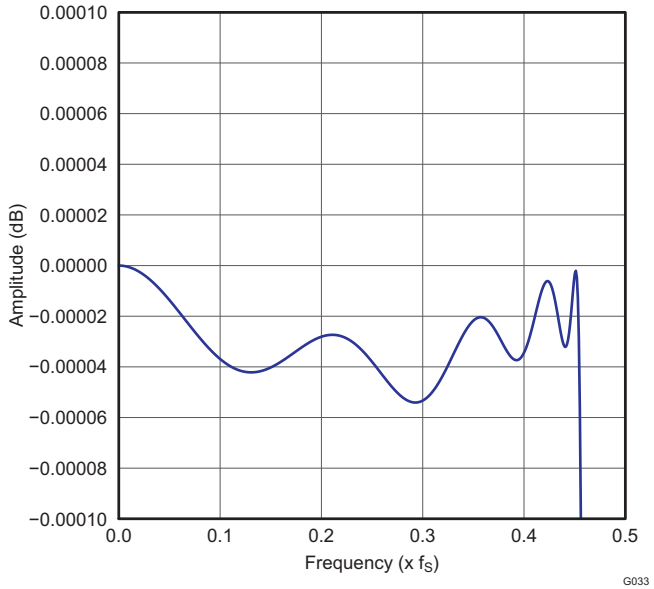


Figure 27. Low latency x8 Interpolation Filter Passband Ripple

Table 13. Low latency x4 Interpolation Filter

Parameter	Condition	Value (Typ)	Units
Filter Gain Pass Band	0 ……. $0.45f_S$	±0.0001	dB
Filter Gain Stop Band	$0.55f_S$ ….. $3.455f_S$	–52	dB
Filter Group Delay		$3.5t_S$	s

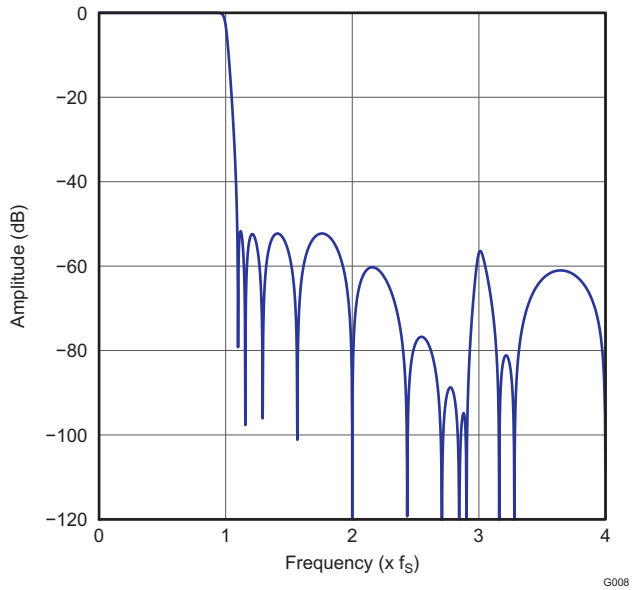


Figure 28. Low latency x4 Interpolation Filter Frequency Response

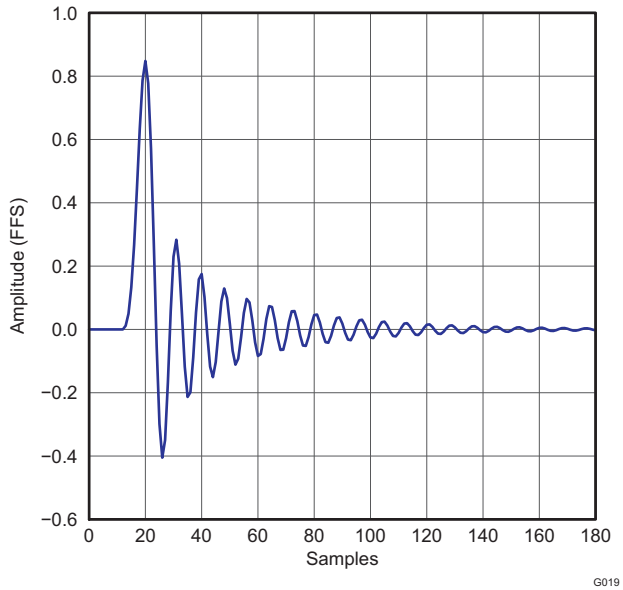


Figure 29. Low latency x4 Interpolation Filter Impulse Response

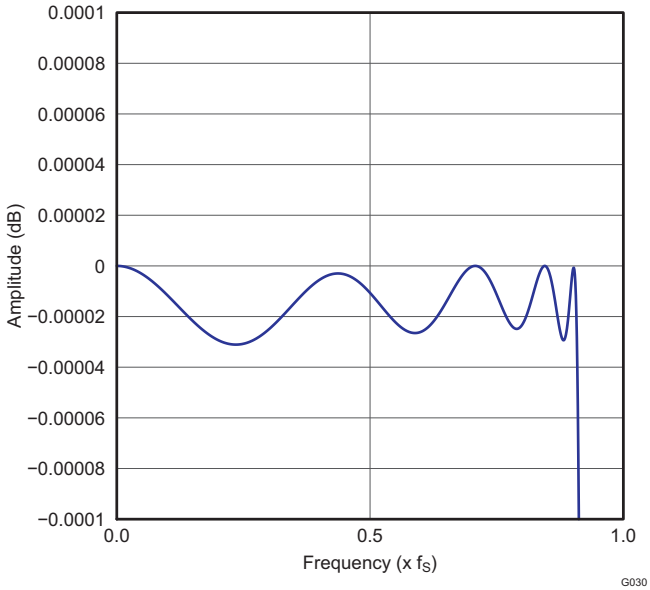


Figure 30. Low latency x4 Interpolation Filter Passband Ripple

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Table 14. Low latency x2 Interpolation Filter

Parameter	Condition	Value (Typ)	Units
Filter Gain Pass Band	0 ……. $0.45f_S$	±0.0001	dB
Filter Gain Stop Band	$0.55f_S$ ….. $1.455f_S$	–52	dB
Filter Group Delay		$3.5t_S$	s

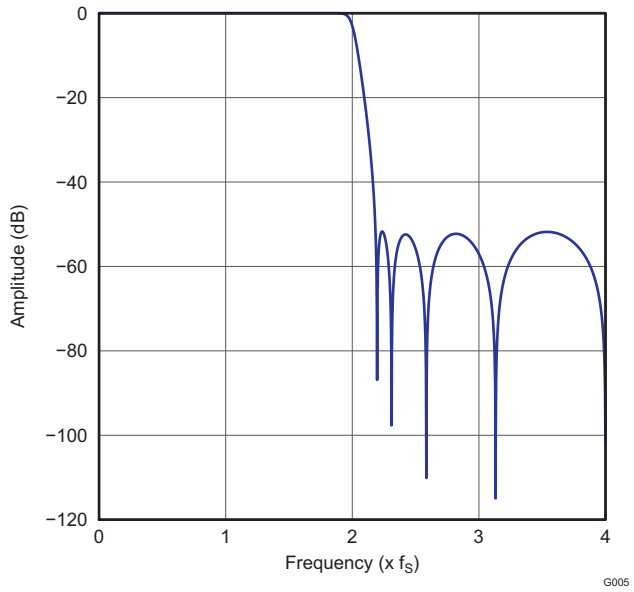


Figure 31. Low latency x2 Interpolation Filter Frequency Response

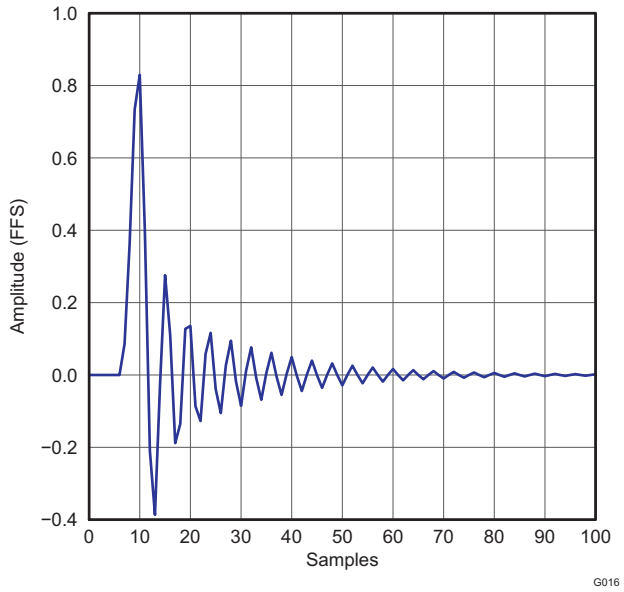


Figure 32. Low latency x2 Interpolation Filter Impulse Response

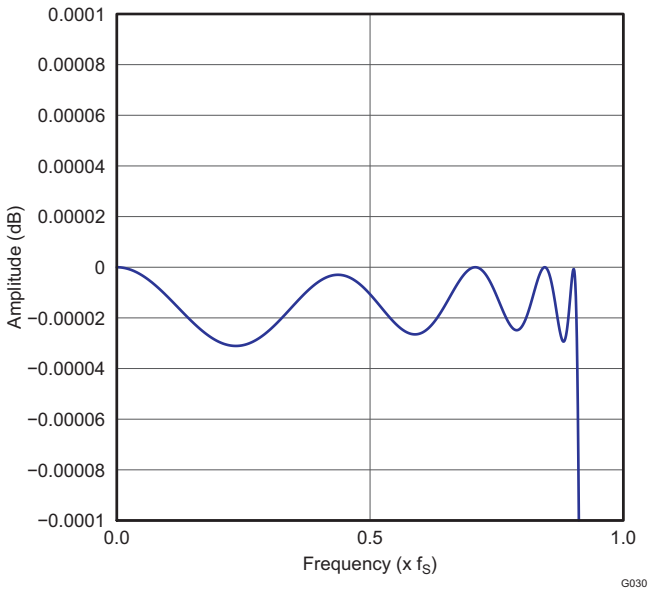


Figure 33. Low latency x2 Interpolation Filter Passband Ripple

Zero Data Detect

The PCM510x has a zero-data detect function. When the device detects continuous zero data, it enters a full analog mute condition.

The PCM510x counts zero data over 1024LRCKs (21ms @ 48kHz) before setting analog mute.

Power Save Mode

When any kind of clock error (SCK, BCK, and LRCK) or clock halt is detected, the PCM510x enters Stand-by mode automatically. The current-segment DAC and Line driver are also powered down.

When BCK and LRCK halt to a low level for more than 1 second, the PCM510x enters Power down mode automatically. Power-down mode includes the negative charge pump and Bias/Reference circuit power-down in addition to stand-by.

Whenever expected Audio clocks (SCK, BCK, LRCK) are applied to the PCM510x, the device starts its powerup sequence automatically.

XSMT Pin (Soft Mute and Soft Un-Mute)

For external digital control of the PCM510x, the XSMT pin must be driven by an external digital host with a specific/minimum rise time (t_r) and fall time (t_f) for soft mute and soft un-mute. The PCM510x requires t_r/t_f times of less than 20ns. In the majority of applications, this shouldn't be a problem, however, traces with high capacitance may have issues.

When the XSMT pin is shifted from high to low (3.3V to 0V), a soft digital attenuation ramp is started. –1dB attenuation will be applied every $1t_S$ from 0dBFS to –∞. This attenuation takes 104 sample times.

When the XSMT pin is shifted from low to high (0V to 3.3V), a soft digital "un-mute" is started. 1dB gain steps are applied every t_S from –∞ to 0dBFS. This ramp-up takes 104 sample times.

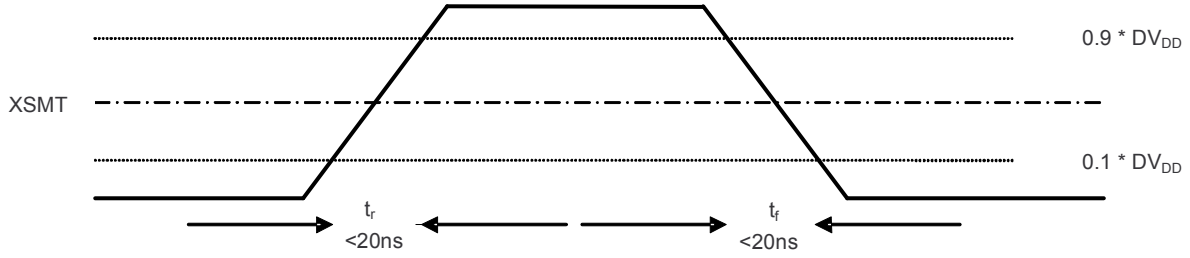


Figure 34. XSMT Timing for Soft Mute and Soft Un-Mute

Table 15. XSMT Timing Parameters

Parameters	Min	Max	Unit
Rise time (t_r)		20	ns
Fall time (t_f)		20	ns

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External Power Sense Undervoltage Protection mode (supported only when DVDD = 3.3V)

The XSMT pin can also be used to monitor a system voltage, such as the 24VDC LCD TV backlight, or 12VDC system supply using a potential divider created with two resistors. (See Figure 35)

- If the XSMT pin makes a transition from 1 to 0 over 6ms or more, the device will switch into external under-voltage protection mode. In this mode, two trigger levels are used.
- When XSMT pin level reaches 2V, soft mute process begins.
- When XSMT pin level reaches 1.2V, analog mute will engage, regardless of digital audio level, and analog shut down will begin. (For example, DAC circuitry powers down).

A timing diagram to show this is shown in Figure 36.

NOTE

The XSMT input pins voltage range is from –0.3V to DVDD + 0.3V.The ratio of external resistors must be considered within this input range. Any increase in power supply (such as power supply positive noise/ripple) can pull the XSMT pin higher than DVDD+0.3V.

For example, if the PCM510x is monitoring a 12V input, and dividing the voltage by 4, then the voltage at XSMT during ideal power supply conditions will be 3V. If the voltage spikes any higher than 14.4V, then XSMT will see a voltage in excess of 3.6V (DVDD+0.3), potentially damaging the device.

Providing the divider is set appropriately, any DC voltage can be monitored.

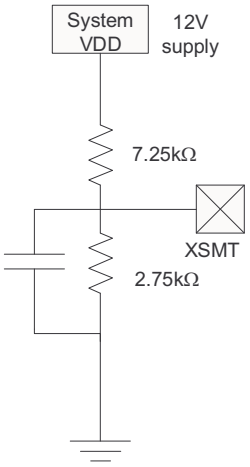


Figure 35. XSMT in External UVP Mode

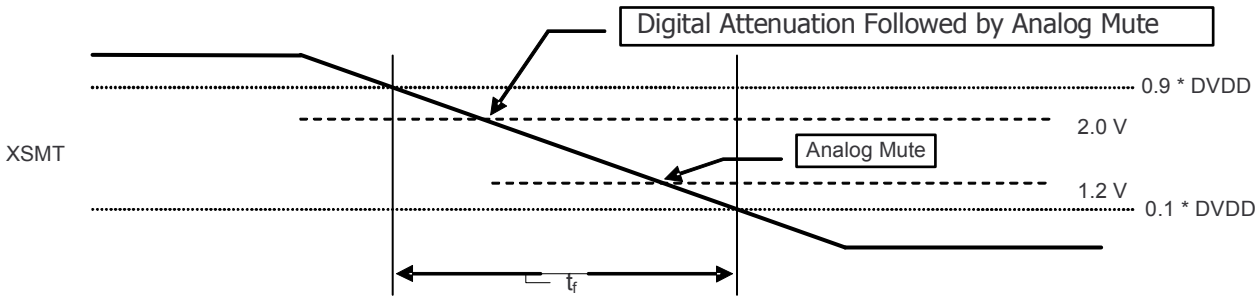


Figure 36. XSMT Timing for Undervoltage Protection

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Recommended Powerdown Sequence

With inadequate system design, the PCM510x can exhibit some pop on power down. Pops are caused by the device not having enough time to detect power loss and start the muting process.

The PCM510x evaluation board avoids audible pop with an electrolytic decoupling capacitor. This capacitor provides enough time between data loss from USB or S/PDIF and power supply loss for the muting process to take place.

The PCM510x has two auto-mute functions to mute the device upon power loss (intentional or unintentional).

XSMT = 0

When the XSMT pin is pulled low, the incoming PCM data is attenuated to 0, closely followed by a hard analog mute. This process takes 150 sample times (t_S) + 0.2mS.

As this mute time is mainly dominated by the sampling frequency, systems sampling at 192kHz will mute much faster than a 48kHz system.

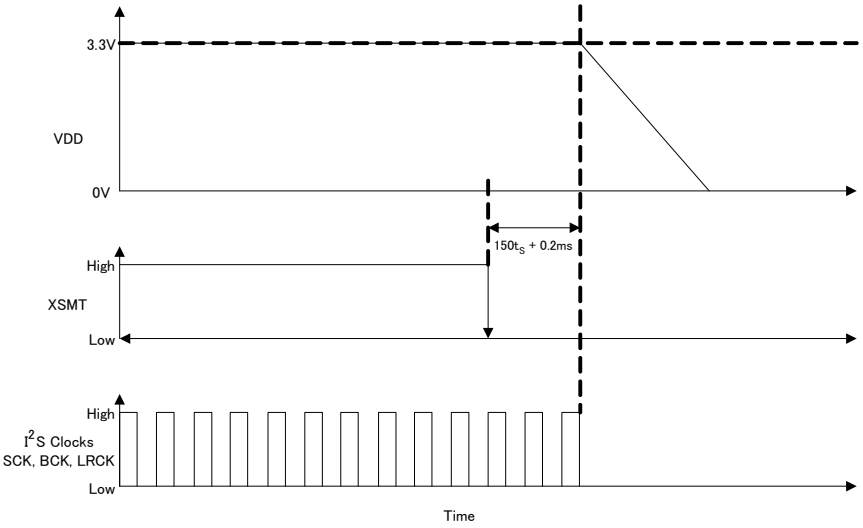
Clock Error Detect

When clock error is detected on the incoming data clock, the PCM510x family switches to an internal oscillator, and continues to the drive the DAC, while attenuating the data from the last known value. Once this process is complete, the PCM510x outputs will be hard muted to ground.

Planned Shutdown

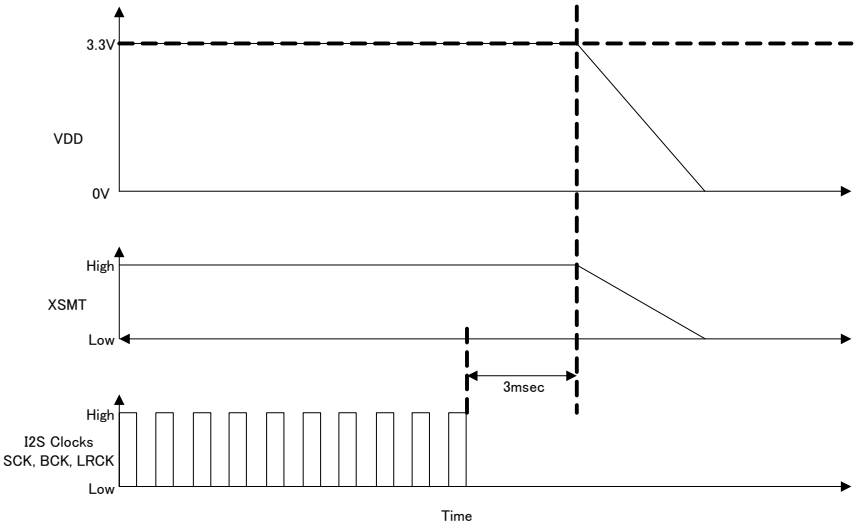
These auto-muting processes can be manipulated by system designs to mute before power loss in the following ways:

1. Assert XSMT low $150t_S$ + 0.2mS before power is removed.



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2. Stop I^2S clocks (SCK, BCK, LRCK) 3ms before powerdown as shown below:



Unplanned Shutdown

Many systems use a low-noise regulator to provide an AVDD 3.3V supply for the DAC. The XSMT Pin can take advantage of such a feature to measure the pre-regulated output from the system SMPS to mute the DAC before the entire SMPS discharges. Figure 37 shows how to configure such a system to use the XSMT pin. The XSMT pin can also be used in parallel with a GPIO pin from the system microcontroller/DSP or Power Supply.

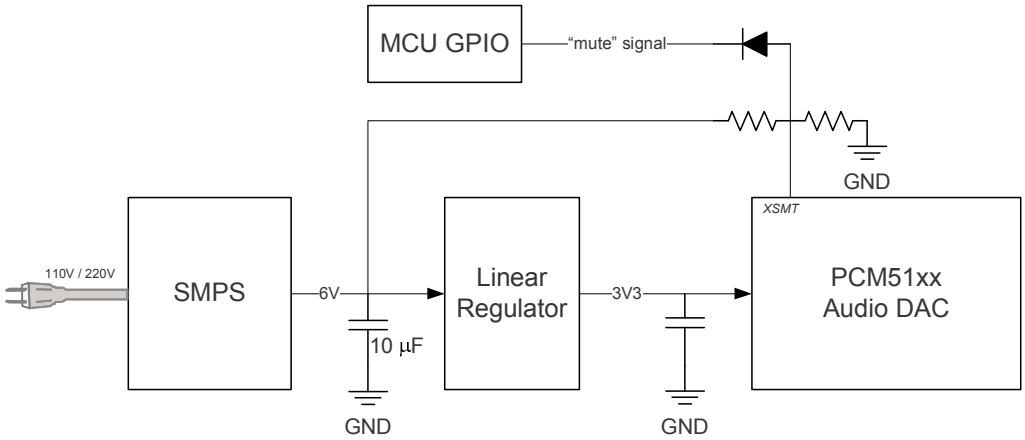


Figure 37. Using the XSMT Pin

Typical Application Circuits

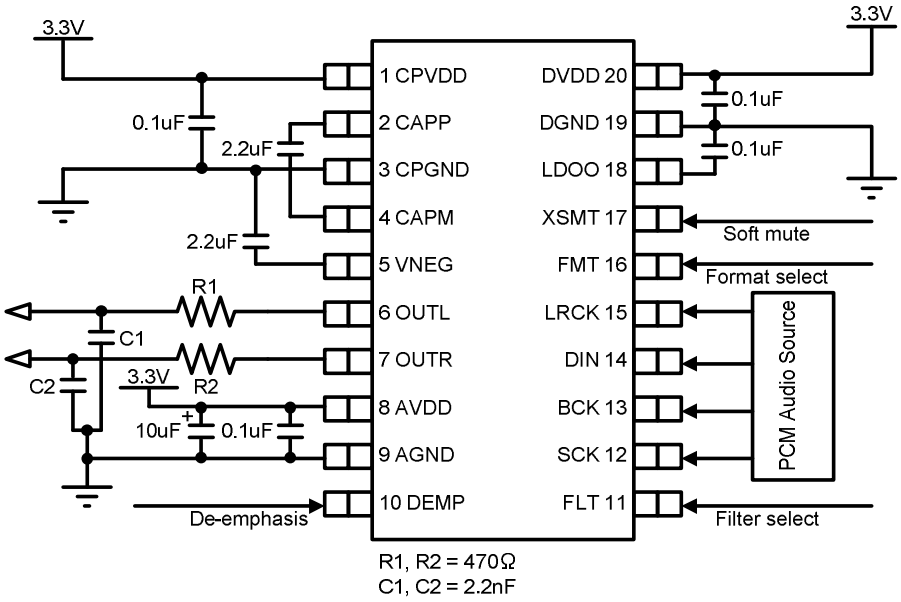


Figure 38. PCM510x Standard PCM Audio Operation, 3.3V

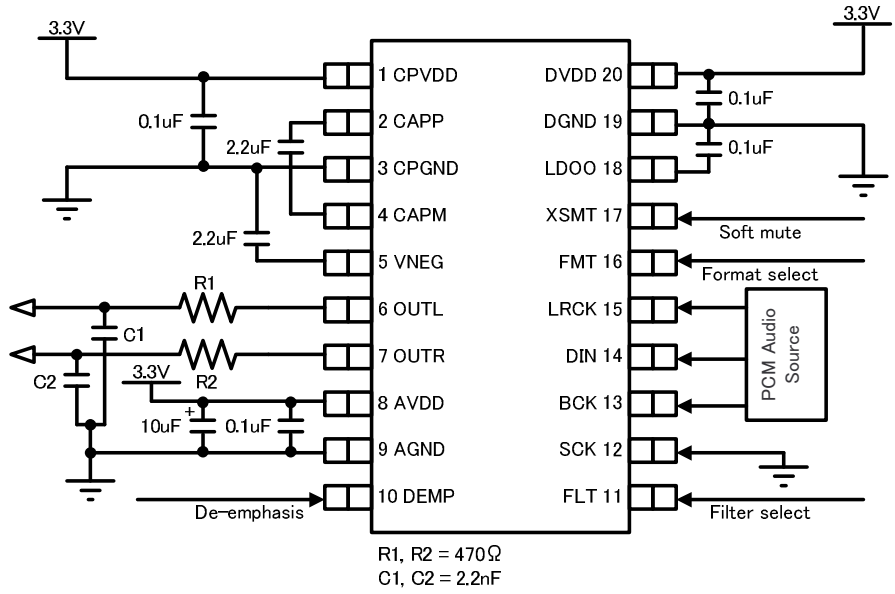


Figure 39. PCM510x PLL Operation, 3.3V

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Recommended Output Filter for the PCM510x

The diagram in Figure 40 shows the recommended output filter for the PCM510x. The new PCM510x next generation current segment architecture offers excellent out of band noise, making a traditional 20kHz low pass filter a thing of the past.

The RC settings below offer a –3dB filter point at 153kHz (approx), giving the DAC the ability to reproduce virtually all frequencies through to it's maximum sampling rate of 384kHz.

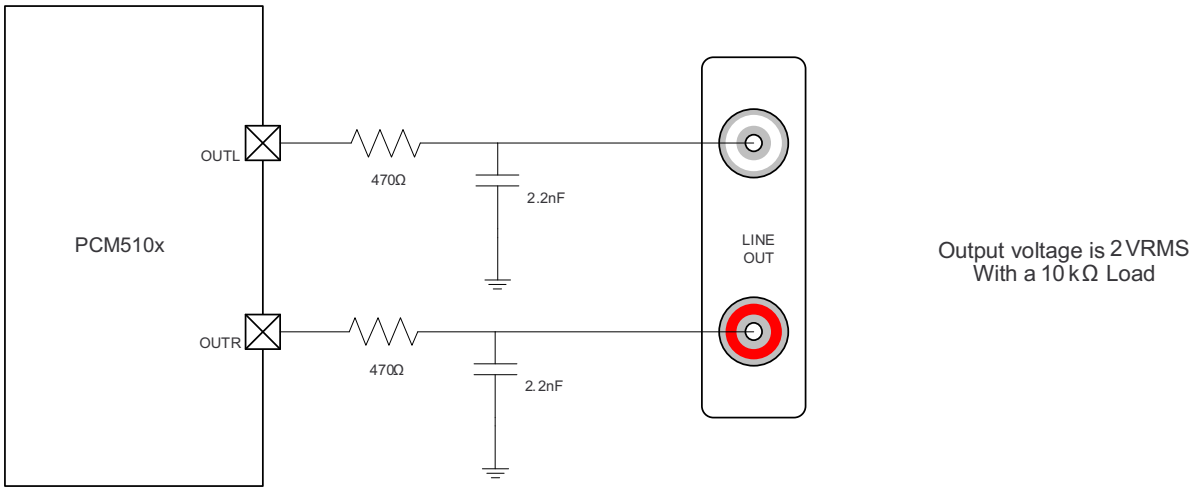


Figure 40. Recommended Output Lowpass Filter for 10kΩ Operation

REVISION HISTORY

Changes from Revision Initial Release (May 2011) to Revision A	Page
• Changed layout of first two pages	1
• Deleted "Device Power Dissipation" row	4
• Changed "VOUT = -1 dB" to " -1 dBFS" in THD+N	5
• Changed reference to correct footnote	6
• Changed Updated plot	7
• Changed t_{SCKH} and t_{SCKL} values to 9ns.	11
• Removed 48kHz sample rate with PLL-generated clock	12
• Added BCK frequency max for convenience	13
• Added PCM510x application diagram, PLL Operation	26

REVISION HISTORY

Changes from Revision A (March 2012) to Revision B	Page
• fixed typos associated with the term "sample frequency"	1

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PCM5100PW	NRND	Production	TSSOP (PW) | 20	70 | BULK	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM5100
PCM5100PW.A	NRND	Production	TSSOP (PW) | 20	70 | BULK	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM5100
PCM5100PWR	NRND	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM5100
PCM5100PWR.A	NRND	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM5100
PCM5101PW	NRND	Production	TSSOP (PW) | 20	70 | BULK	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM5101
PCM5101PW.A	NRND	Production	TSSOP (PW) | 20	70 | BULK	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM5101
PCM5101PWR	NRND	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM5101
PCM5101PWR.A	NRND	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM5101
PCM5102PW	NRND	Production	TSSOP (PW) | 20	70 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM5102
PCM5102PW.A	NRND	Production	TSSOP (PW) | 20	70 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM5102
PCM5102PWR	NRND	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM5102
PCM5102PWR.A	NRND	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM5102

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF PCM5102 :

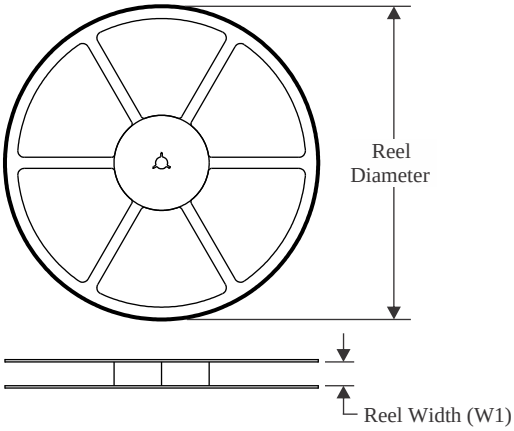
- Automotive : PCM5102-Q1

NOTE: Qualified Version Definitions:

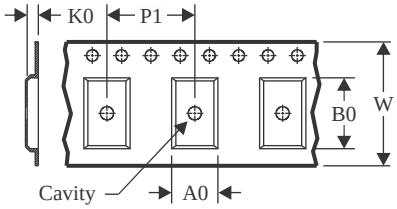
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

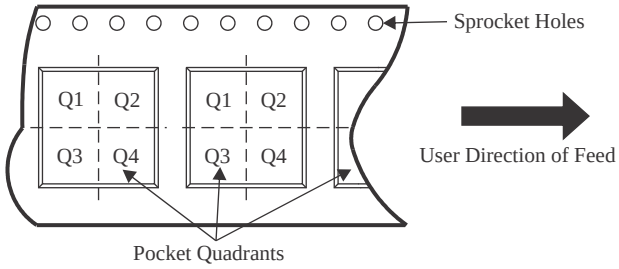


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

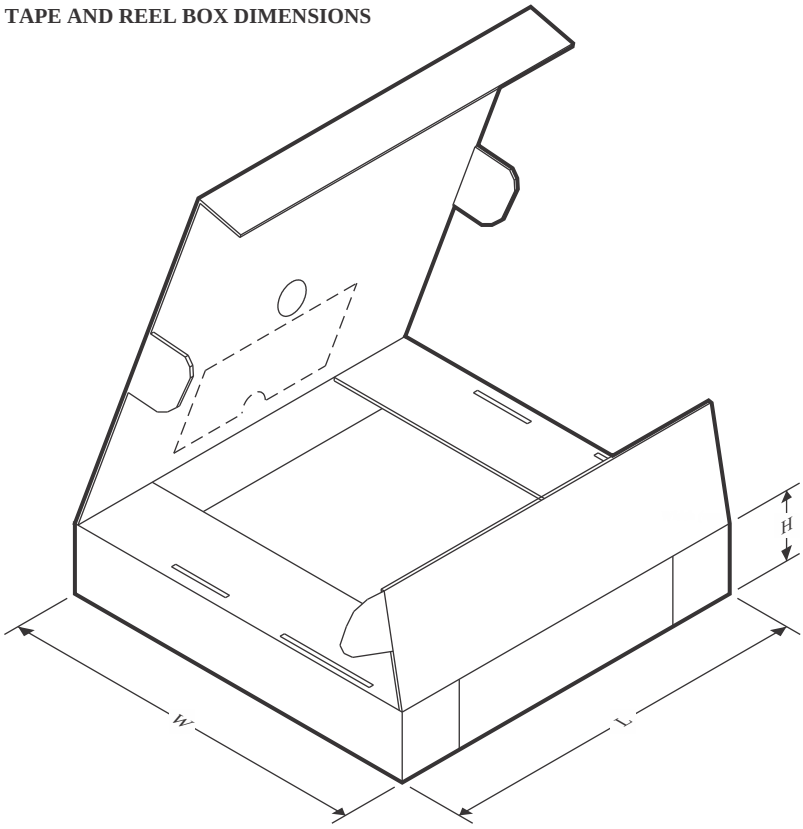
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCM5100PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
PCM5101PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
PCM5102PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

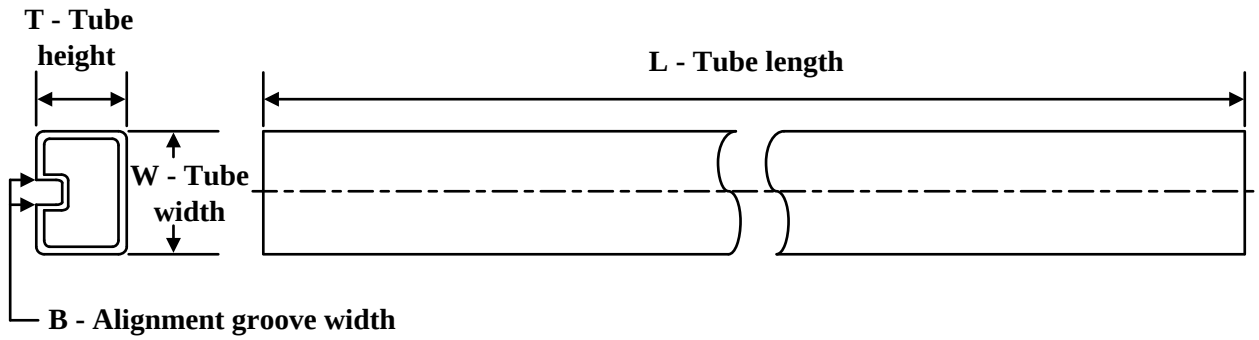
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCM5100PWR	TSSOP	PW	20	2000	350.0	350.0	43.0
PCM5101PWR	TSSOP	PW	20	2000	350.0	350.0	43.0
PCM5102PWR	TSSOP	PW	20	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

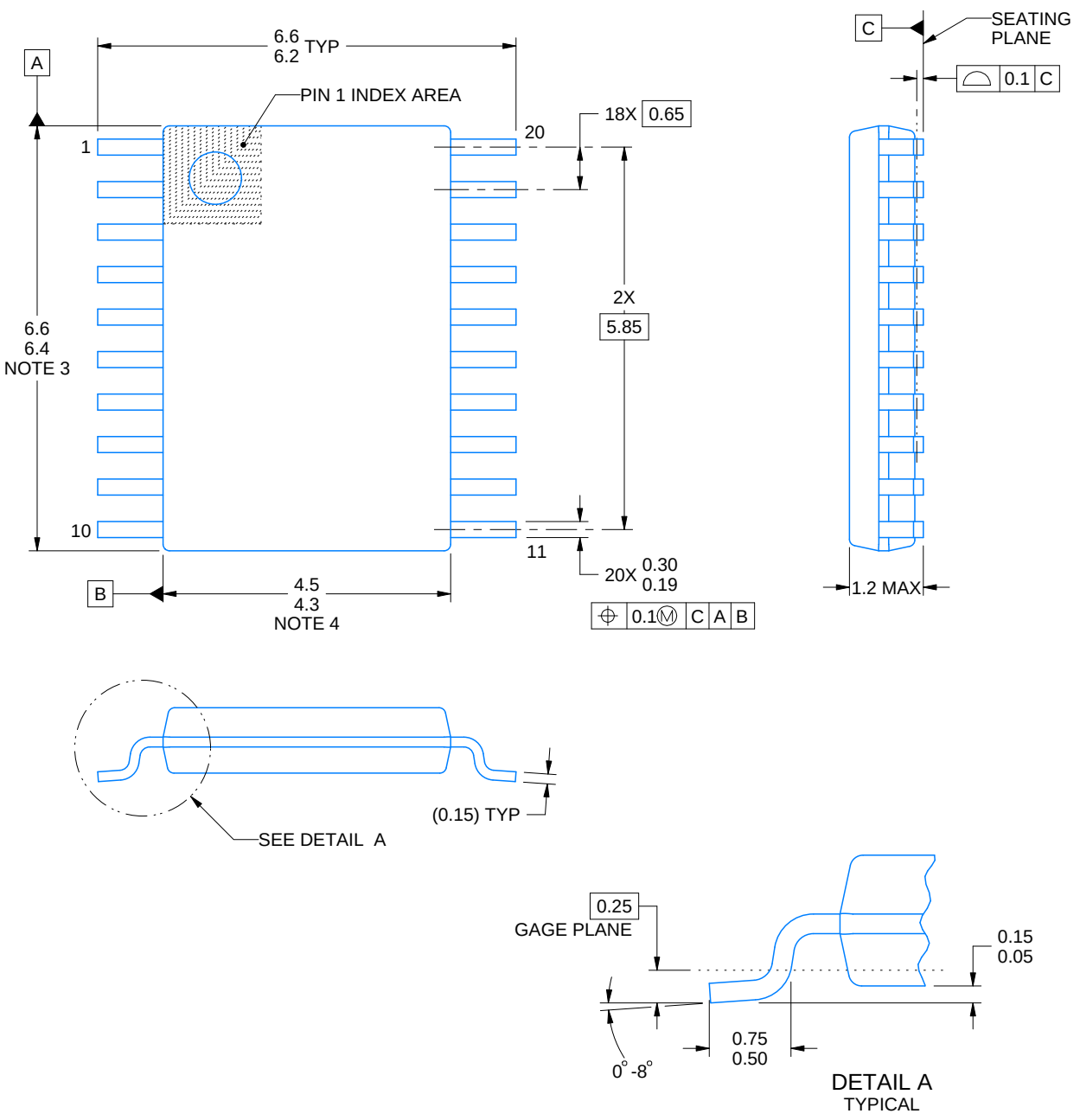
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
PCM5100PW	PW	TSSOP	20	70	530	10.2	3600	3.5
PCM5100PW.A	PW	TSSOP	20	70	530	10.2	3600	3.5
PCM5101PW	PW	TSSOP	20	70	530	10.2	3600	3.5
PCM5101PW.A	PW	TSSOP	20	70	530	10.2	3600	3.5
PCM5102PW	PW	TSSOP	20	70	530	10.2	3600	3.5
PCM5102PW.A	PW	TSSOP	20	70	530	10.2	3600	3.5

PACKAGE OUTLINE

PW0020A

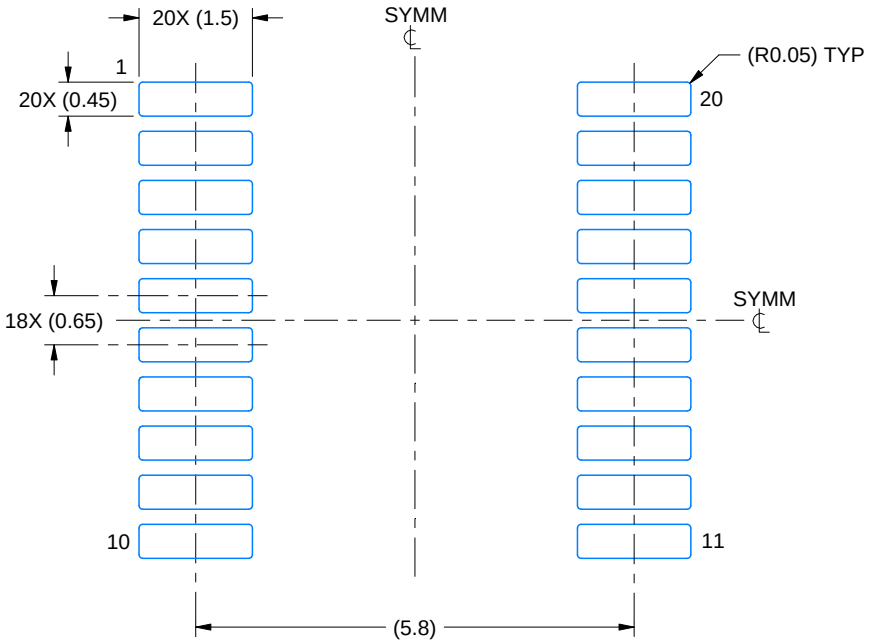
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

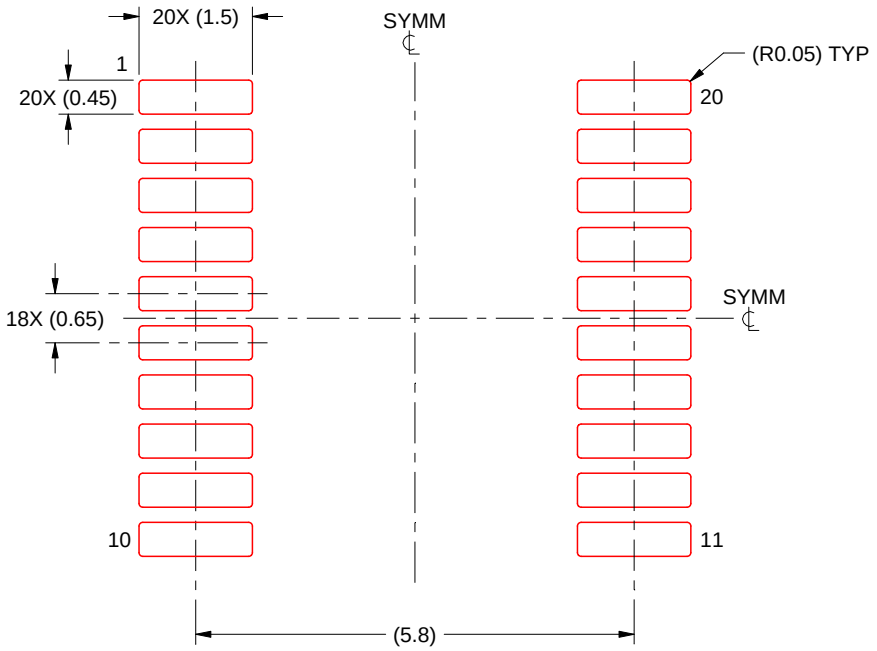


SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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