PE4259

Product Specification

UltraCMOS® High-power SPDT RF Switch, 10 MHz–3.0 GHz

Features

- Single-pin or complementary CMOS logic control inputs
- Low insertion loss:
  - 0.35 dB at 1000 MHz
  - 0.5 dB at 2000 MHz
- Isolation: 30 dB at 1000 MHz
- High ESD tolerance: 2 kV HBM
- Typical input 1 dB compression point: +33.5 dBm
- Minimum power supply voltage: 1.8V
- Packaging: Ultra-small 6-lead SC-70

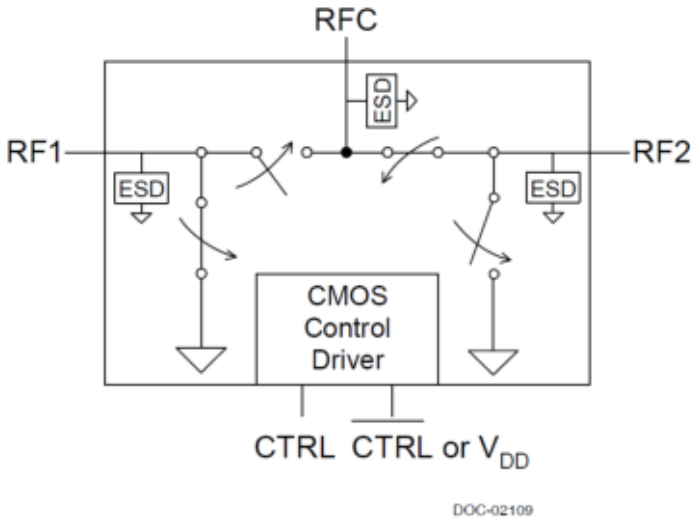


Figure 1. PE4259 functional diagram

Product description

The PE4259 UltraCMOS® RF switch is designed to cover a broad range of applications from 10–3000 MHz. This reflective switch integrates on-board CMOS control logic with a low-voltage CMOS-compatible control interface and can be controlled using either single-pin or complementary control inputs. Using a nominal +3V power supply voltage, a typical input 1 dB compression point of +33.5 dBm can be achieved.

The PE4259 is manufactured on pSemi's UltraCMOS process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.

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Absolute maximum ratings

Exceeding the absolute maximum ratings listed in Table 1 could cause permanent damage. Restrict operation to the limits in Table 2. Operation between the operating range maximum and the absolute maximum for extended periods could reduce reliability.

ESD precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, do not exceed the rating listed in Table 1.

Latch-up immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 1. Absolute maximum ratings

Parameter or condition	Symbol	Min	Max	Unit
Power supply voltage	V_{DD}	-0.3	4.0	V
Voltage on any DC input	V_I	-0.3	V_{DD} + 0.3	V
Storage temperature range	T_{ST}	-65	150	°C
Operating temperature range	T_{OP}	-40	85	°C
Input power (50Ω)(*)	P_{IN}	–	+34	dBm
ESD Voltage (HBM, ML_STD 883 Method 3015.7)	V_{ESD}	–	2000	V
ESD Voltage (MM, JEDEC, JESD22-A114-B)		–	100	V
Note: * To maintain optimum device performance, do not exceed the maximum input power (P_{IN}) at the preferred operating frequency. For details, see Figure 3.				

Recommended operating conditions

Table 2 lists the PE4259 recommended operating conditions. Do not operate devices outside the operating conditions listed below.

Table 2. Operating conditions

Parameter	Min	Typ	Max	Unit
Power supply voltage, V_{DD}	1.8	3.0	3.3	V
Power supply current, I_{DD} (V_{DD} = 3V and V_{CTRL} = 3V)	–	9	20	µA
Control voltage high	0.7 × V_{DD}	–	–	V
Control voltage low	–	–	0.3 × V_{DD}	V

Electrical specifications

Table 3 lists the PE4259 key electrical specifications at +25 °C and V_{DD} = 3V (Z_S = Z_L = 50Ω), unless otherwise specified.

Table 3. Electrical specifications

Parameter	Condition	Min	Typ	Max	Unit
Operating frequency(1)	–	10	–	3000	MHz
Insertion loss(2)	1000 MHz 2000 MHz	–	0.35 0.50	0.45 0.60	dB
Isolation	1000 MHz 2000 MHz	29 19	30 20	–	dB
Return loss(2)	1000 MHz 2000 MHz	21 24	22 27	–	dB
ON switching time(3)	50% CTRL to 0.1 dB of final value, 1 GHz	–	1.50	–	µs
OFF switching time(3)	50% CTRL to 25 dB isolation, 1 GHz	–	1.50	–	µs
Video feedthrough(4)	–	–	15	–	mV_{PP}
Input 1-dB compression point	1000 MHz at 2.3–3.3V 1000 MHz at 1.8–2.3V 2500 MHz at 2.3–3.3V 2500 MHz at 1.8–2.3V	31.5 29.5 28.5 28	33.5 30.5 30.5 29	–	dBm
Input IP3	1000 MHz, 20 dBm input power	–	55	–	dBm

Notes:
1. Device linearity begins to degrade below 10 MHz.
2. A tuning capacitor must be added to the application board to optimize the insertion loss and return loss performance. For details, see Figure 13.
3. The PE4259 has a maximum 25 kHz switching rate.
4. The DC transient at the output of any port of the switch when the control voltage is switched from low-to-high or high-to-low in a 50Ω test setup, measured with 1 ns risetime pulses and 500-MHz bandwidth.

Thermal data

The junction top-of-package, Psi-JT (Ψ_{JT}), is a thermal metric to estimate the junction temperature of the device in an application PCB, per JEDEC JESD51-2:

$$\Psi_{JT} = (T_J - T_T)/P$$

where:

- Ψ_{JT} = Junction-to-top of package characterization parameter in °C/W
- T_J = Die junction temperature in °C
- T_T = Package temperature (top surface, in the center) in °C
- P = Power dissipated by the device in Watts

Table 4. Thermal data

Parameter	Typ	Unit
Maximum junction temperature, T_{JMAX} (RF input power, CW = 31.5 dBm, +85 °C ambient)	99	°C
Junction top-of-package, Ψ_{JT}	37	°C/W
Junction-to-ambient thermal resistance, Θ_{JA}	104	°C/W

Control logic

Table 5. Single-pin control logic truth table

Control voltages	Signal path
Pin 6 (V_{DD}) = V_{DD} Pin 4 (CTRL) = High	RFC to RF1
Pin 6 (V_{DD}) = V_{DD} Pin 4 (CTRL) = Low	RFC to RF2

Table 6. Complementary-pin control logic truth table

Control voltages	Signal path
Pin 6 ($\overline{CTRL}$ or V_{DD}) = Low Pin 4 (CTRL) = High	RFC to RF1
Pin 6 ($\overline{CTRL}$ or V_{DD}) = High Pin 4 (CTRL) = Low	RFC to RF2

Control logic input

The PE4259 is a versatile RF switch that supports two operating control modes: single-pin control mode and complementary-pin control mode:

- *Single-pin control mode* enables the switch to operate with a single control pin (pin 4) supporting a +3V CMOS logic input and requires a dedicated +3V power supply connection on pin 6 (V_{DD}). This mode of operation reduces the number of control lines required and simplifies the switch control interface typically derived from a CMOS microprocessor I/O port.
- *Complementary-pin control mode* allows the switch to operate using complementary control pins CTRL and $\overline{CTRL}$ (pins 4 and 6, respectively), that can be directly driven by +3V CMOS logic or a suitable microprocessor I/O port. This enables the PE4259 to be used as a potential alternate source for SPDT RF switch products used in positive control voltage mode and operating within the PE4259 operating limits.

Power derating curve

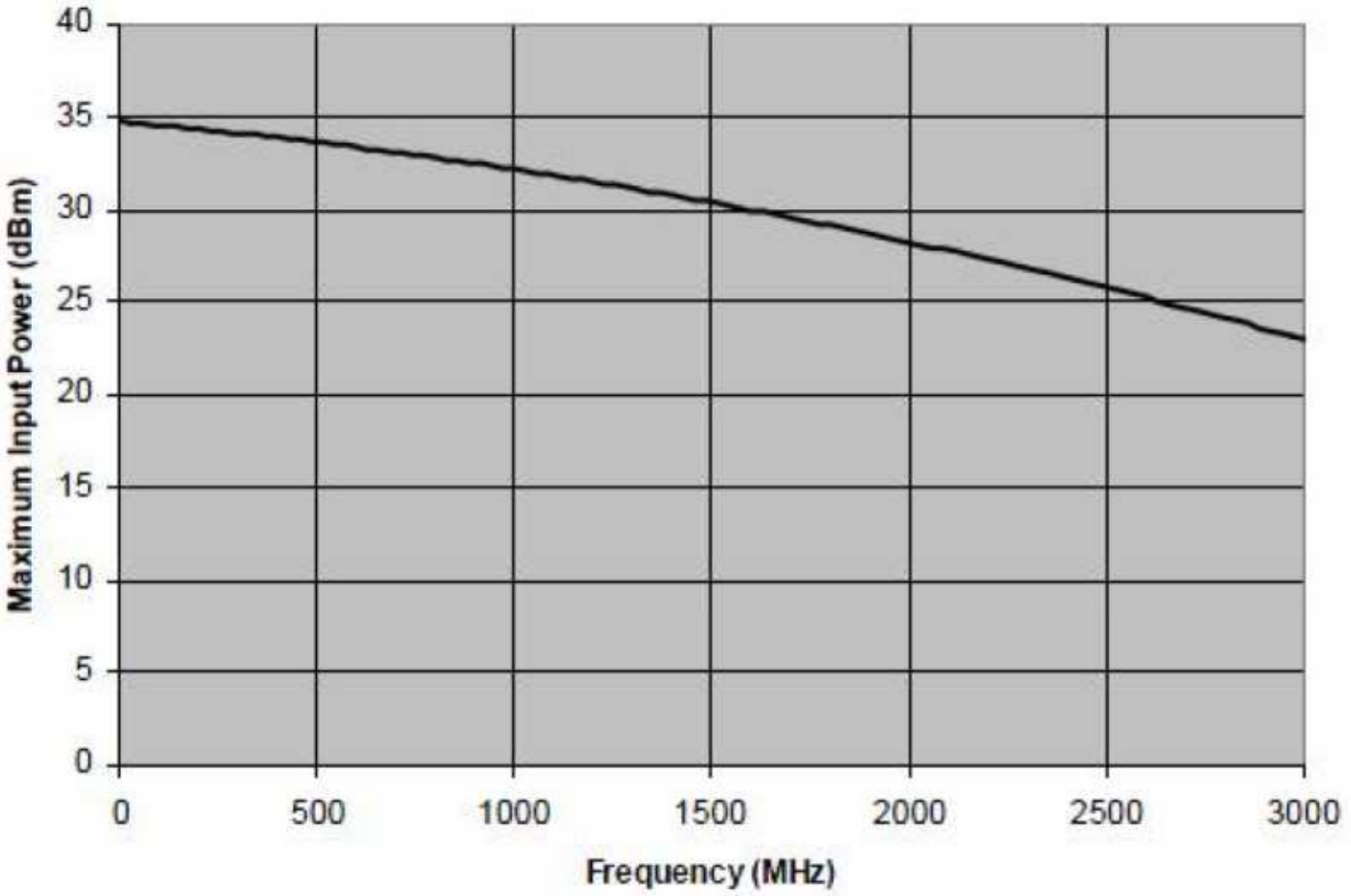


Figure 3. Power derating curve at 25 °C and 3.0V

Typical performance data

Figure 4–Figure 7 show the typical performance data at T = -40 °C to 85 °C and V_{DD} = 3V, unless otherwise specified.

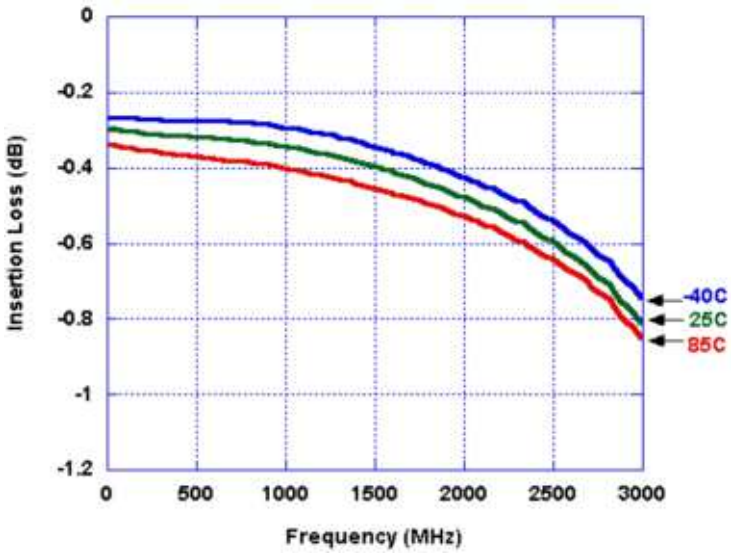


Figure 4. Insertion loss

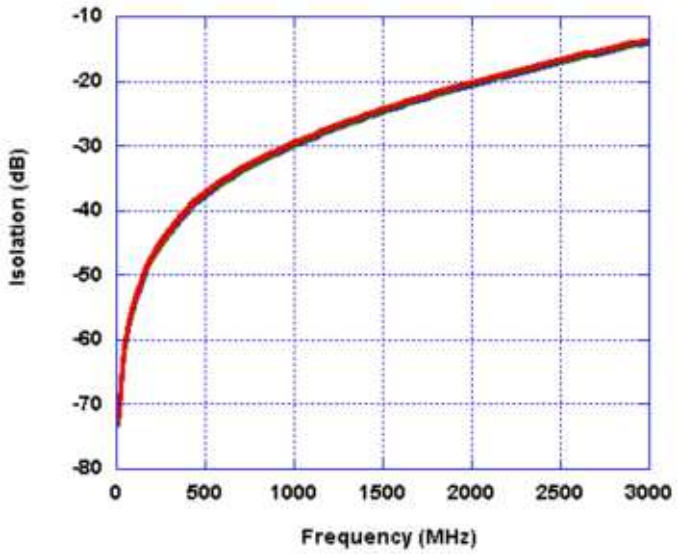


Figure 5. Isolation, input to output

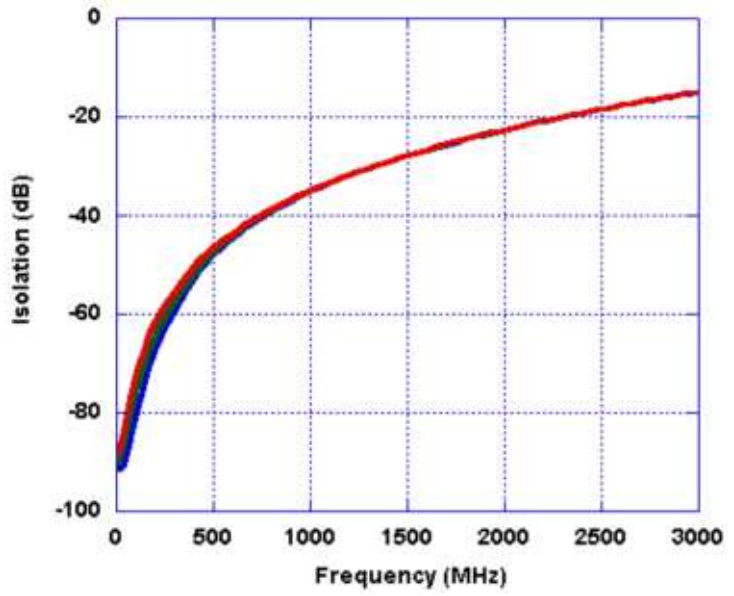


Figure 6. Isolation, output to output

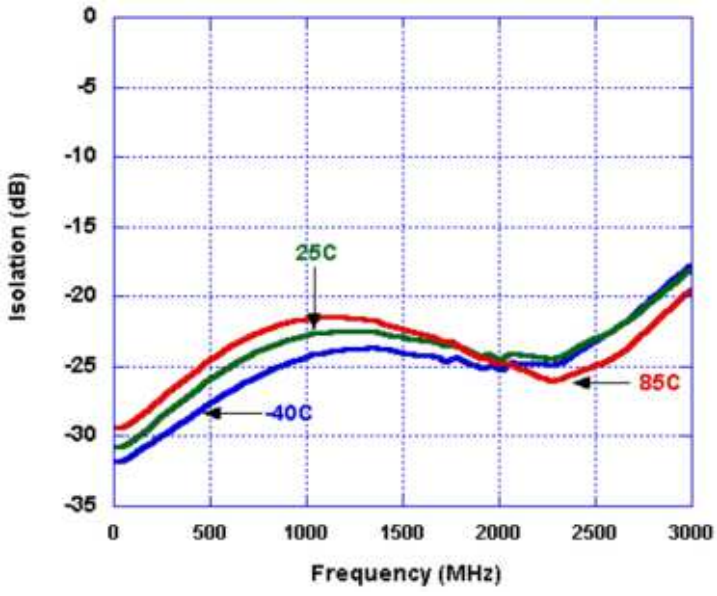


Figure 7. Return loss, input

Figure 8–Figure 11 show the typical performance data at T = 25 °C and V_{DD} = 2.3V, unless otherwise specified.

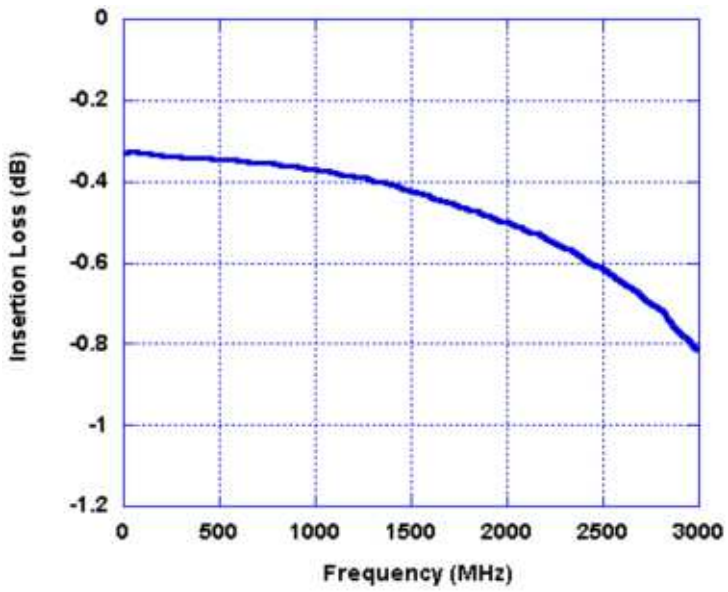


Figure 8. Insertion loss

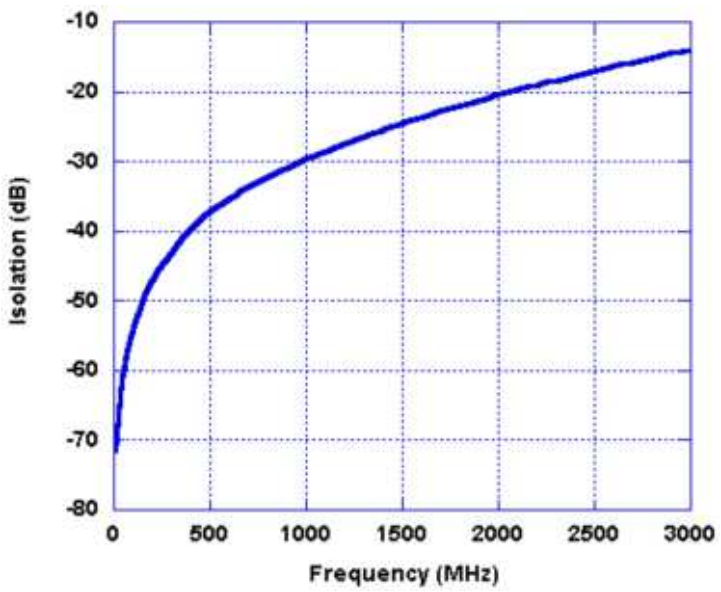


Figure 9. Isolation, input to output

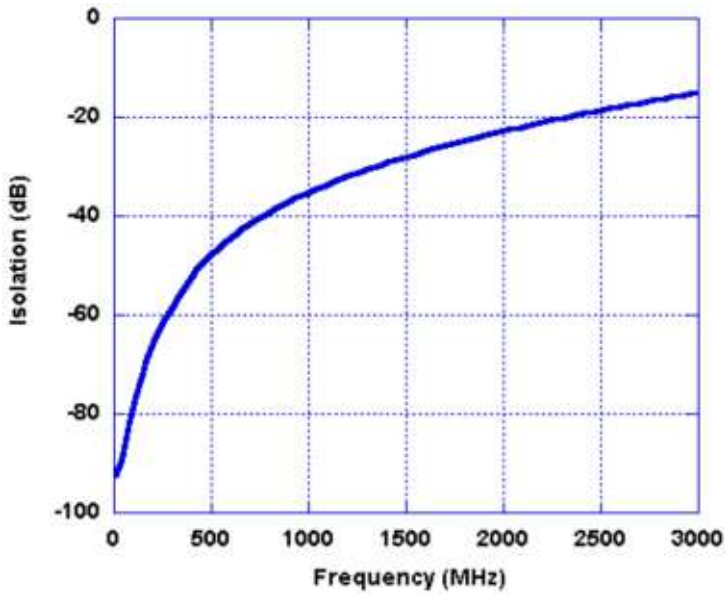


Figure 10. Isolation, output to output

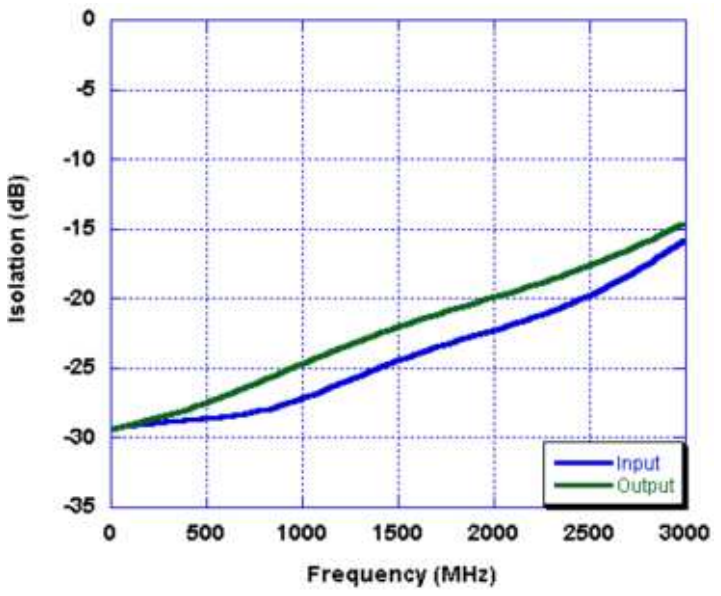


Figure 11. Return loss, input and output

Evaluation kit

pSemi designed the SPDT switch evaluation board to ease your evaluation of the PE4259. The RF common port connects through a 50Ω transmission line via the top SMA connector, J1. RF1 and RF2 connect through 50Ω transmission lines via SMA connectors J2 and J3, respectively. A through 50Ω transmission is available via SMA connectors J4 and J5. Use this transmission line to estimate the loss of the PCB over the environmental conditions being evaluated.

The board is constructed of a two-metal layer FR4 material with a total thickness of 0.031”. The bottom layer provides ground for the RF transmission lines. The transmission lines were designed using a coplanar waveguide with ground plane model using a trace width of 0.0476”, trace gaps of 0.030”, dielectric thickness of 0.028”, metal thickness of 0.0021”, and εr of 4.4.

J6 and J7 provide a means for controlling DC and digital inputs to the device. J6-1 is connected to the device VDD or $\overline{\text{CTRL}}$ input. J7-1 is connected to the device CTRL input.

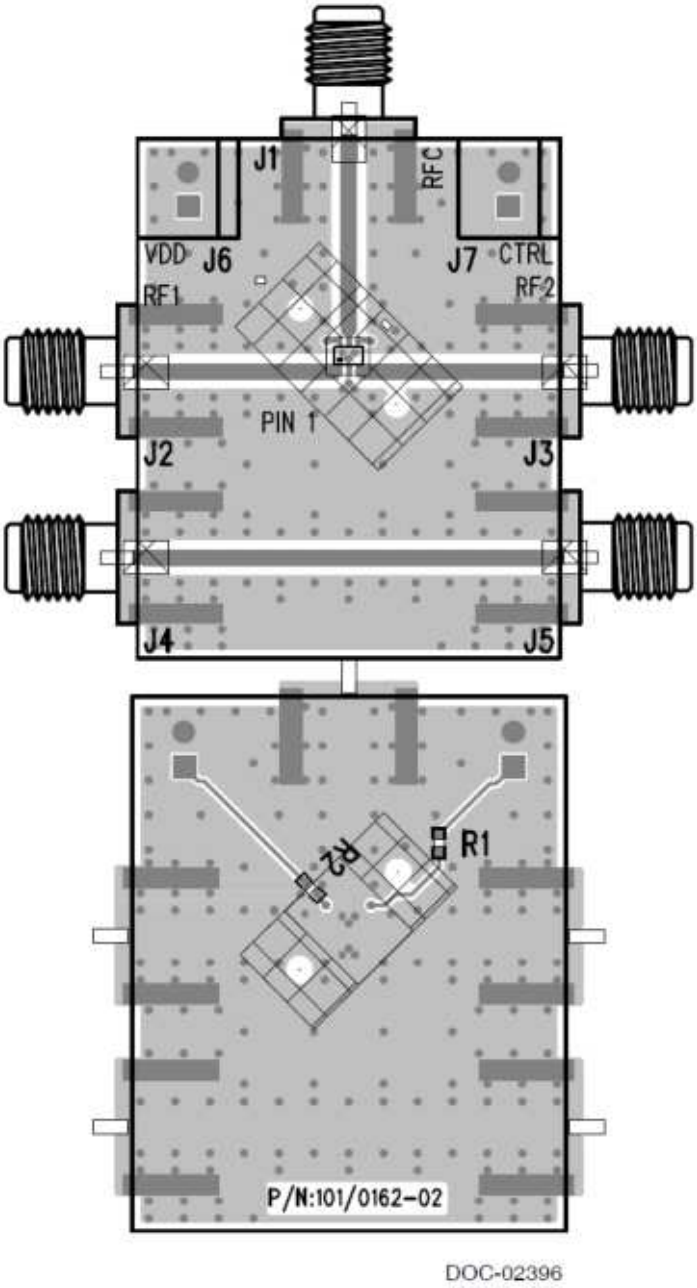


Figure 12. Evaluation board layout

Evaluation board schematic

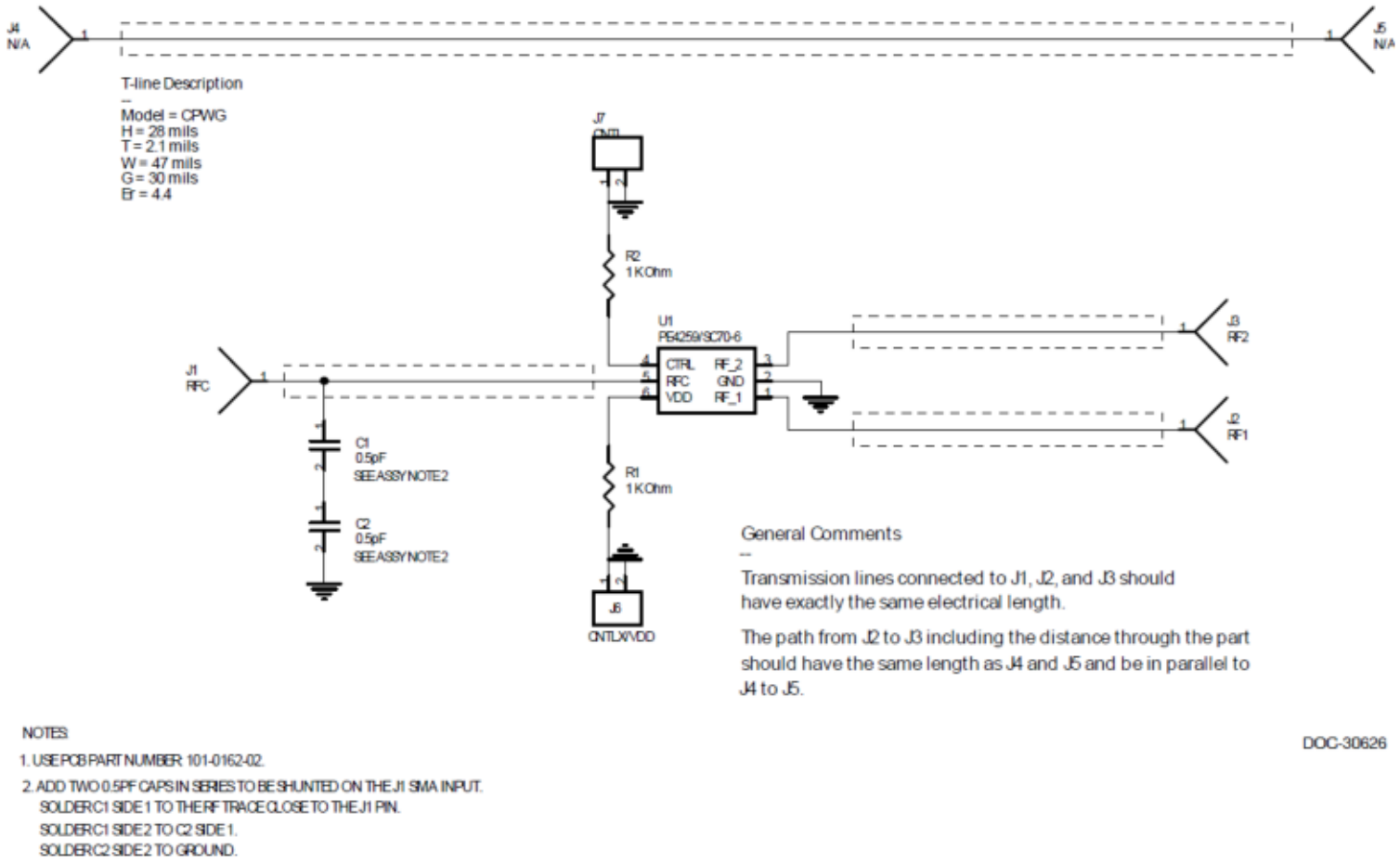


Figure 13. Evaluation board schematic

Pin configuration

Figure 14 shows the PE4259 pin configuration for the 6-lead SC-70 package, and Table 7 lists the description for each pin.

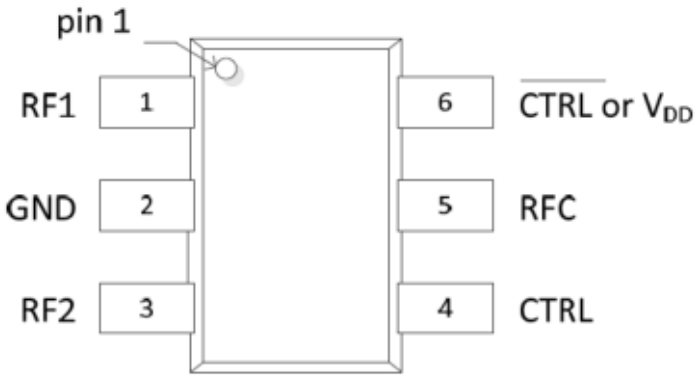


Figure 14. Pin configuration, top view

Table 7. Pin descriptions

Pin no.	Pin name	Description
1(*)	RF1	RF port 1
2	GND	Ground connection. Traces must be physically short and connected to ground plane for best performance.
3(*)	RF2	RF port 2
4	CTRL	Switch control input, CMOS logic level.
5(*)	RFC	RF common port
6	$\overline{CTRL}$ or V_{DD}	This pin supports two interface options: • *Single-pin control mode*: A nominal 3V supply connection is required. • *Complementary-pin control mode*: A complementary CMOS control signal to CTRL is supplied to this pin. Bypassing on this pin is not required in this mode.
Note: * RF pins 1, 3, and 5 must be DC blocked with an external series capacitor or held at 0 VDC.		

Packaging information

This section provides the following packaging data:

- Moisture sensitivity level
- Package drawing
- Package marking
- Tape-and-reel information

Moisture sensitivity level

The PE4259 moisture sensitivity level rating for the 6-lead SC-70 package is MSL1.

Package drawing

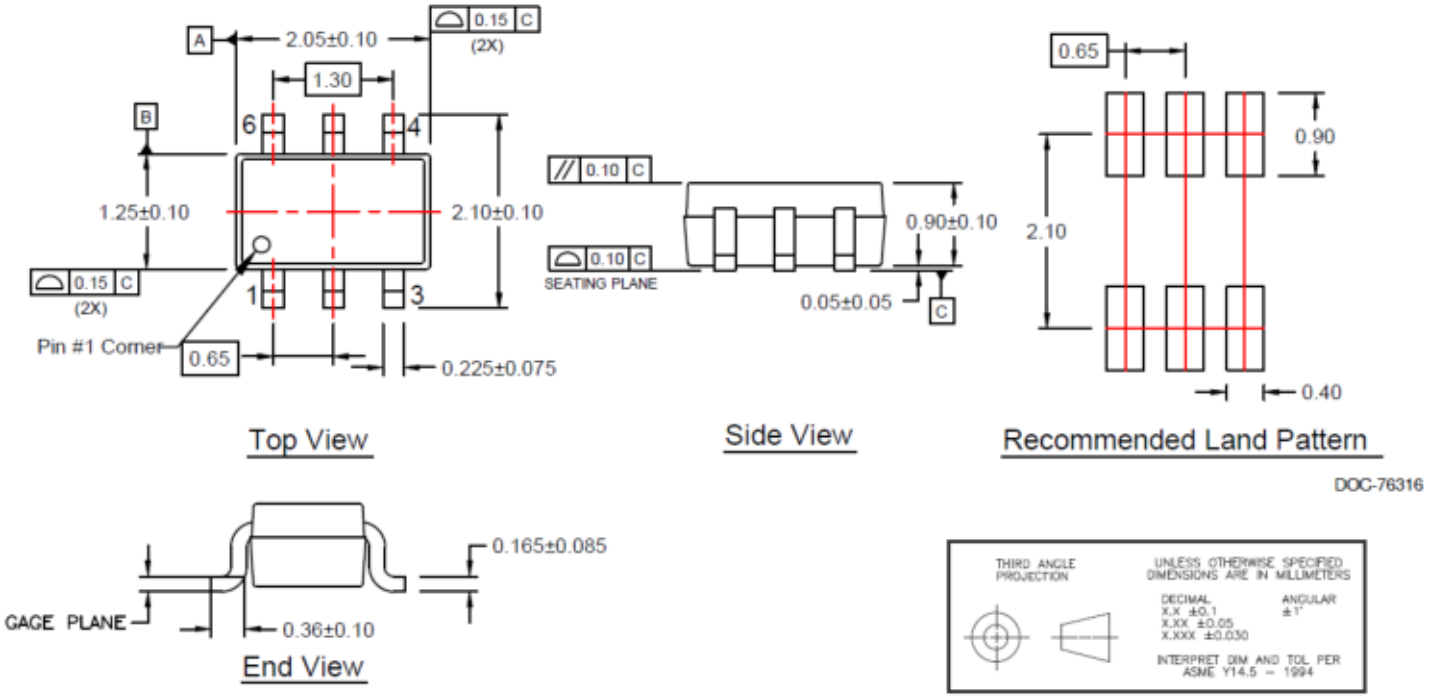


Figure 15. Package mechanical drawing for the 6-lead SC-70 package

Top-marking specification

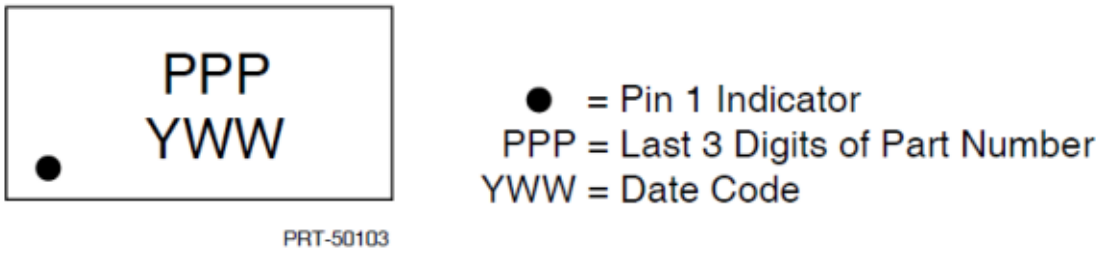
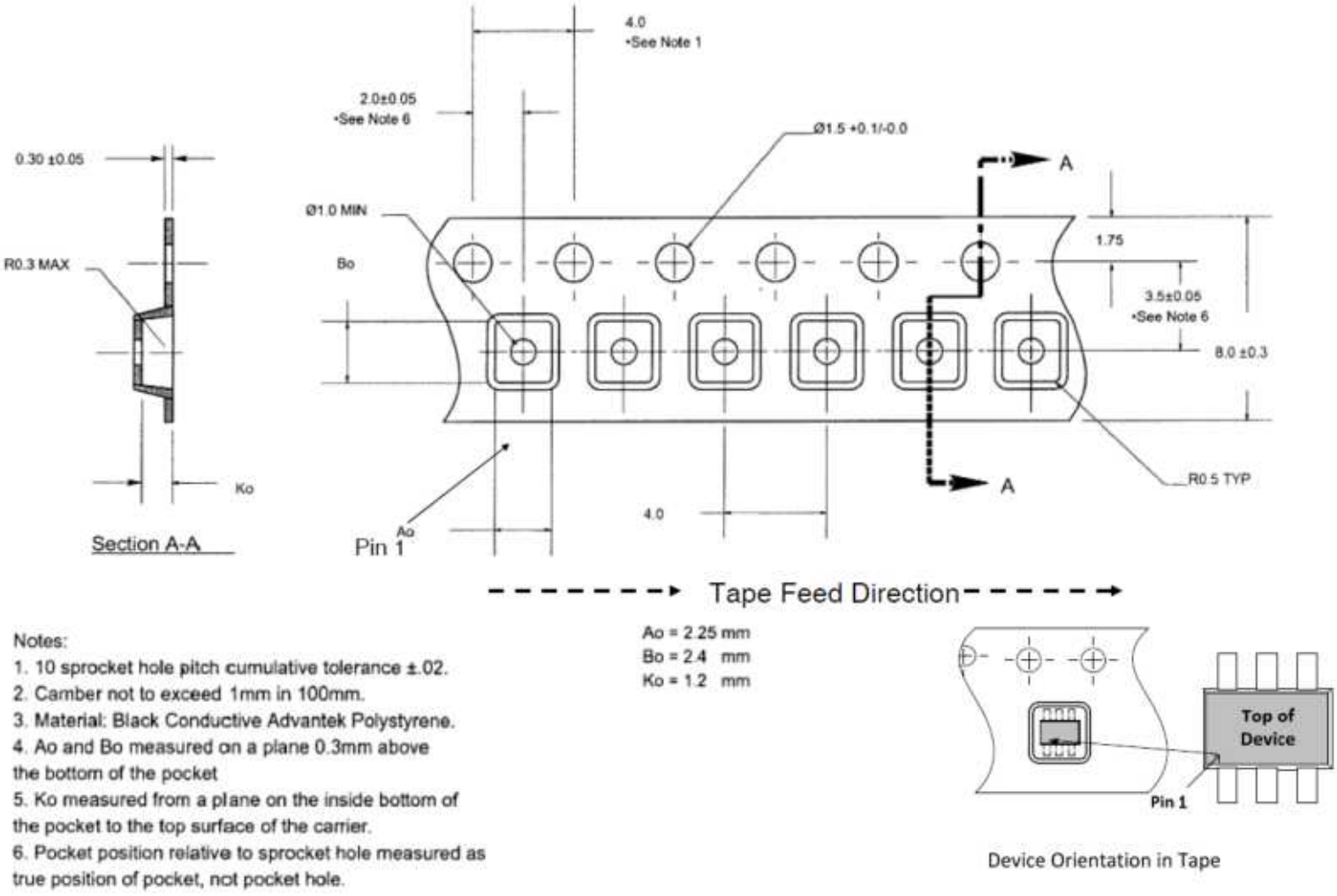


Figure 16. Package marking specification

Tape and reel specification



Notes:
1. 10 sprocket hole pitch cumulative tolerance ±.02.
2. Camber not to exceed 1mm in 100mm.
3. Material: Black Conductive Advantek Polystyrene.
4. Ao and Bo measured on a plane 0.3mm above the bottom of the pocket
5. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

Figure 17. Tape and reel specification for the 6-lead SC-70 package

Ordering information

Order code	Description	Packaging	Shipping method
4259-63	PE4259 SPDT RF switch	Green 6-lead SC-70	3000 units/T&R
EK4259-01	PE4259 evaluation kit	Evaluation kit	1/box

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