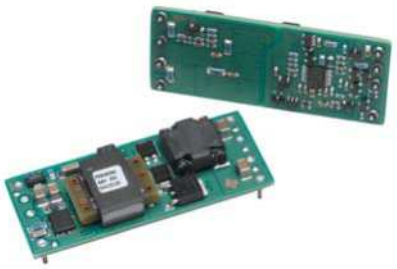
Not Recommended for New Designs

PTB48580 Series

Dual Complementary-Output DC/DC Converter for DSL

SLTS240 DECEMBER 2004



Features

- Dual Complementary Outputs (±5 V, ±12 V)
- Input Voltage Range: 36 V to 75 V
- On/Off Enable for Sequencing
- 1500 VDC Isolation
- Over-Current Protection
- Over-Temperature Shutdown
- Under-Voltage Lockout
- Temp Range: –40 to +85 °C
- Industry Standard Outline
- Fixed Frequency Operation
- Synchronizes with PTB48500
- Powers line driver ICs for AC-7 and other xDSL chipsets
- Safety Approvals: (Pending):
  EN60950
  UL/cUL60950

Description

The PTB48580 series of isolated DC/DC converter modules produce a complementary pair of regulated supply voltages for powering line-driver ICs in xDSL telecom applications. The modules operate from a standard telecom (-48 V) central office (CO) supply and can provide up to a 30 W of power in a balanced load configuration.

The A-suffix module (±5 V) is designed to power the line driver ICs for the AC-7 ADSL chipset. Other voltage options will power other analog applications requiring a complementary supply with relatively balanced loads. The outputs can also be easily configured for single-ended use.

The modules incorporate an On/Off enable control, output current limit, over-temperature protection, and input under-voltage lockout (UVLO) as standard features.

The control inputs, "Enable" and "Sync In," are compatible with the "EN Out" and "Sync Out" signals of the PTB48500 DC/DC converter. This allows the power-up and switching frequency of the PTB48580 series to be directly controlled from a PTB48500. Together a PTB48500 and a PTB48580A converter meet all the system power and sequencing requirements of an AC-7 ADSL chipset.

The PTB48580 series uses double-sided surface mount contruction. The package size is based on an industry standard outline and does not require a heatsink. Both through-hole and surface mount pin configurations are available.

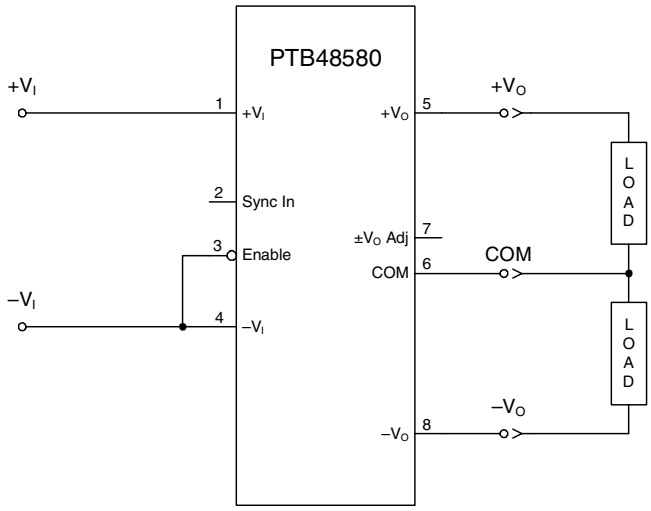
Pin Configuration

Pin	Function
1	$+V_I$
2	Sync In
3	Enable *
4	$-V_I$
5	$+V_O$
6	COM
7	V_O Adjust
8	$-V_O$

Shaded functions indicate signals that are referenced to $-V_I$.

* *Denotes negative logic:*
Open = Outputs Off
$-V_I$ = Normal operation

Stand-Alone Application



Ordering Information

Base Pt. No. (PTB48580xxx)

Order Prefix	Description
PTB48580xxx	Basic Model

Output Voltage (PTB48580❐xx)

Code	Voltage
A	±5 V
B	±12 V

Package Options (PT48580x❐❐)

Code	Description	Pkg Ref. (1)
AH	Horiz. T/H	(ERV)
AS	SMD, Standard (2)	(ERS)

Notes: *(1) Reference the applicable package reference drawing for the dimensions and PC board layout*
(2) "Standard" option specifies 63/37, Sn/Pb pin solder material.

Pin Descriptions

+V_I: The positive input supply for the module with respect to –V_I. When powering the module from a –48 V telecom central office supply, this input is connected to the primary system ground.

–V_I: The negative input supply for the module, and the 0 VDC reference for the '*Enable**', and '*Sync In*' signals. When the module is powered from a +48-V supply, this input is connected to the 48-V Return.

+V_O: The positive output supply voltage, which is referenced to the '*COM*' node. The voltage at '+V_O' has the same magnitude, but is the complement to that at '-V_O'.

–V_O: The negative output supply voltage, which is referenced to the '*COM*' node. The voltage at '-V_O' has the same magnitude, but is the complement to that at '+V_O'.

COM: The secondary return reference for the module's regulated output voltages. This node is dc isolated from the input supply pins.

±V_O Adjust: Using a single resistor, this pin allows the magnitude of both '+V_O' and '–V_O' to be adjusted together, either higher or lower than their preset value. If not used, this pin should be left open circuit.

Enable*: This is an open-collector (open-drain) negative logic input that enables the module output. This pin is referenced to -V_I. A logic '0' at this pin enables the module's outputs, and a high impedance disables the outputs. If this feature is not used the pin should be connected to –V_I. *Note: Connecting this input directly to the "EN Out" pin of the PTB4850x enables the output voltages from both converters (PTB4850x and PTB48580) to power up in sequence.*

Sync In: This pin is used when the PTB48580 and PTB4850x DC/DC converter modules are used together. Connecting this pin to the '*Sync Out*' of the PTB4850x module allows the PTB48580 to be synchronized to the same switch conversion frequency as the PTB4850x.

Environmental and General Specifications (Unless otherwise stated, all voltages are with respect to –V_I)

Characteristics	Symbols	Conditions		Min	Typ	Max	Units
Input Voltage Range	V_I	Over output load range		36	48	75	VDC
Isolation Voltage Capacitance Resistance		Input–output/input–case Input to output Input to output		1500 — 10	— 1500 —	— — —	V pF MΩ
Operating Temperature Range	T_A	Over V_I Range		–40	—	+85	°C
Over-Temperature Protection	OTP	Shutdown threshold Hysterisis		— —	115 (i) 10	— —	°C
Solder Reflow Temperature	T_{REFLOW}	Surface temperature of module body or pins				235 (ii)	°C
Storage Temperature	T_S	—		–40	—	125	°C
Mechanical Shock		Per Mil-STD-883D, Method 2002.3 1 msec, ½ Sine, mounted		—	500	—	G's
Mechanical Vibration		Mil-STD-883D, Method 2007.2 20-2000 Hz	T/H SMD	— —	20 5	— —	G's
Weight	—			—	13.5	—	grams
Flammability	—	Meets UL 94V-O					

Notes: *(i) This parameter is guaranteed be design*
(ii) During reflow of SMD package version do not elevate peak temperature of the module, pins or internal components above the stated maximum.

Specifications (Unless otherwise stated, T_A =25°C, V_I =48 V, C_I =0 µF, ±C_O =0 µF, $|+I_O| = |-I_O|$, and $|\pm I_O|$ =0.5 $|\pm I_O|$max)

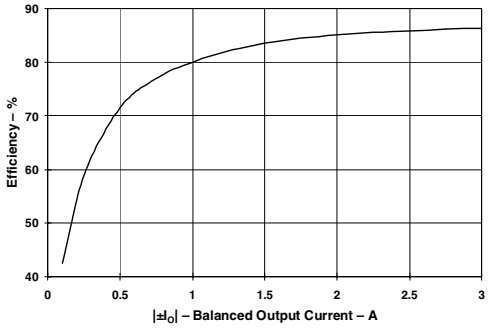
Characteristic	Symbol	Conditions	PTB48580A Min	Typ	Max	Units
Output Power	P_O	Total output power from $\pm V_O$	0	—	30 (1)	W
Output Current	$\|\pm I_O\|$	Over V_I range, $\|+I_O\| - \|-I_O\| \le 0.1$ A	0	—	3 (2)	A
Output Load Imbalance	$\|+I_O\| - \|-I_O\|$	$\|+I_O\| \ge 0.1$ A, $\|-I_O\| \ge 0.1$ A	0	—	1 (3)	A
Output Voltage	$\|\pm V_O\|$	Inlcudes set-point, line, $\|+I_O\| - \|-I_O\| \le 0.1$ A $-40 \le T_A \le +85$°C	4.75 (2)	5	5.25 (2)	V
Temperature Variation	ΔReg_{temp}	$-40 \le T_A \le +85$°C, $\|\pm I_O\|$ =0.1 A $\pm V_O$	—	±1	—	$\%V_O$
Line Regulation	ΔReg_{line}	Over V_I range, balanced load $\pm V_O$	—	±0.1	±0.4	$\%V_O$
Load Regulation	ΔReg_{load}	Over $\pm I_O$ range, balanced load $\pm V_O$	—	±0.2	±0.4	$\%V_O$
Efficiency	η	$P_O = P_O$ max	—	86	—	%
V_o Ripple (pk-pk)	±Vr	20 MHz bandwidth, C_O =10 µF tantalum capacitor	—	25	50 (4)	mV_{pp}
Transient Response	t_S	0.1 A/µs load step, 50% to 75% $\pm I_O$ max	—	30	—	µs
	ΔV_O pk	$\|\pm V_O\|$ over/undershoot	—	±1	—	$\%V_O$
Over Current Threshold	$I_O$trip	V_I =36 V reset followed by auto-recovery	3.3	4.3	5.3	A
Short Circuit Current		Continuous over-current trip, $\|\pm I_O\|_{PK}$	—	6.5	—	A
		$\|+I_O\| = \|-I_O\|$ Duty	—	10	—	%
Output Voltage Adjust Range	$\|\pm V_O\|$adj	$\|+V_O\|$ and $\|-V_O\|$ adjust simulataneously	3.5	—	6 (5)	V
Switching Frequency	f_S	Over V_I and I_O ranges	440	470 (6)	500	kHz
Under-Voltage Lockout	$V_I$on $V_I$off	V_I increasing V_I decreasing	— —	33 32	— —	V
On/Off Enable (pin 3) Input High Voltage Input Low Voltage	 V_{IH} V_{IL}	Referenced to $-V_I$ (pin 4)	 +3.6 –0.2	 — —	 +75 (7) +0.8	V
Input Low Current	I_{IL}		—	—	–1	mA
Standby Input Current	I_I standby	pin 3 open circuit	—	2	—	mA
Start-up Time	t_{ON}	$\|\pm I_O\|$ =1 A, $\|\pm V_O\|$ rising 0 to 0.95 $\|\pm V_O\|_{TYP}$	—	10	—	ms
Internal Input Capacitance	C_I		—	2	—	µF
External Output Capacitance	C_O	Capacitance from either output to COM (pin 6)	0	—	2,000 (8)	µF
Reliability	MTBF	Per Telcordia SR-332 50% stress, T_A =40°C, ground benign	2.8	—	—	10^6 Hrs

Notes: *(1) See Safe Operating Area curves or contact the factory for the appropriate derating.*
(2) Under balanced load conditions, load current flowing out of $+V_O$ is balanced to within ±0.1 A of that flowing into $-V_O$.
(3) A load imbalance is the difference in current flowing from $+V_O$ to $-V_O$. The module can operate with a higher imbalance but with reduced specifications.
(4) Output voltage ripple is measured with a 10 µF tantalum capacitor connected from $+V_O$ (pin 5) or $-V_O$ (pin 8), to COM (pin 6).
(5) When the output voltage is adjusted higher than the nominal output voltage the load current must not exceed the module's maximum power rating.
(6) This is the free-running frequency. The module can be made to synchronize with the PTB48500 when both modules are used together in a system.
(7) The On/Off Enable (pin 3) has an internal pull-up and may be controlled with an open-collector (or open-drain) transistor. The input is diode protected and may be connected to $+V_I$. The open-circuit voltage is 7 V max. If it is left open circuit the converter will operate when input power is applied.
(8) Electrolytic capacitors with very low equivalent series resistance (ESR) may induce instability when used on the output. Consult the factory before using capacitors with organic, or polymer-aluminum type electrolytes.

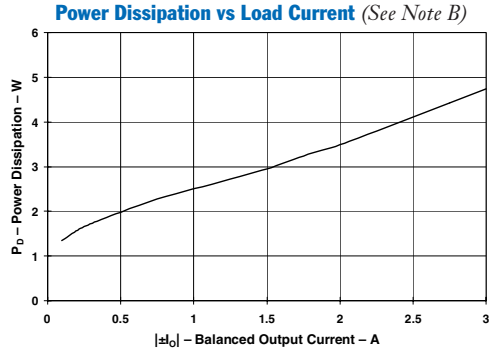
Typical Characteristics

PTB48580A Characteristic Data @V_I =48 V *(See Notes A)*

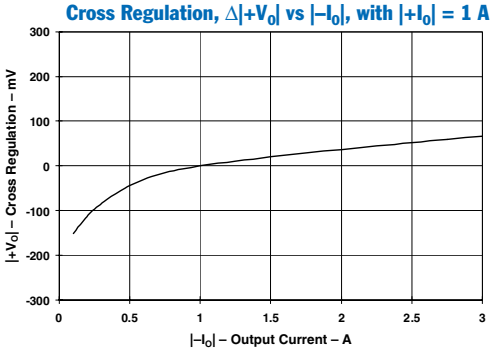
Efficiency vs Load Current *(See Note B)*



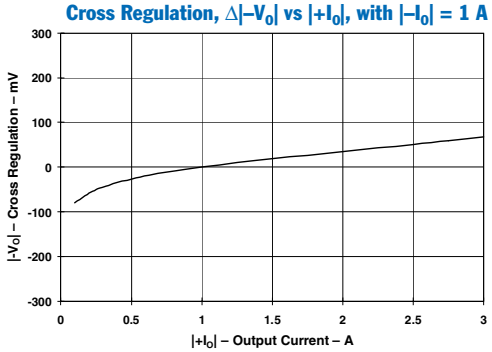
Power Dissipation vs Load Current *(See Note B)*



Cross Regulation, $\Delta|+V_O|$ vs $|-I_O|$, with $|+I_O|$ = 1 A

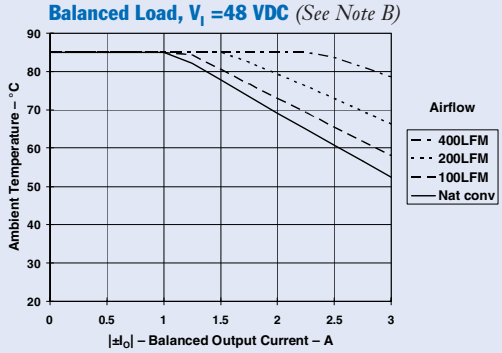


Cross Regulation, $\Delta|-V_O|$ vs $|+I_O|$, with $|-I_O|$ = 1 A



Safe Operating Area PTB48580A *(See Note C)*

Balanced Load, V_I =48 VDC *(See Note B)*



Note A: *Characteristic data has been developed from actual products tested at 25°C. This data is considered typical data for the converter.*
Note B: *Under a balanced load, current flowing out of $+V_O$ is equal to that flowing into $-V_O$.*
Note C: *SOA curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 4 in. × 4 in. double-sided PCB with 2 oz. copper.*

Specifications

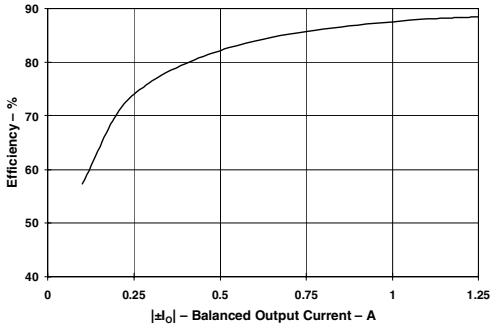
(Unless otherwise stated, T_A =25°C, V_I =48 V, C_I =0 µF, $\pm C_O$ =0 µF, $|+I_O| = |-I_O|$, and $|\pm I_O| = 0.5\ |\pm I_O|$max)

Characteristic	Symbol	Conditions	PTB48580B Min	PTB48580B Typ	PTB48580B Max	Units
Output Power	P_O	Total output power from $\pm V_O$	0	—	30 (1)	W
Output Current	$\|\pm I_O\|$	Over V_I range, $\|+I_O\| - \|-I_O\| \le 0.1$ A	0	—	1.25 (2)	A
Output Load Imbalance	$\|+I_O\| - \|-I_O\|$	$\|+I_O\| \ge 0.1$ A, $\|-I_O\| \ge 0.1$ A	0	—	0.5 (3)	A
Output Voltage	$\|\pm V_O\|$	Inlcudes set-point, line, $\|+I_O\| - \|-I_O\| \le 0.1$ A $-40 \le T_A \le +85$°C	11.6 (2)	12	12.4 (2)	V
Temperature Variation	ΔReg_{temp}	$-40 \le T_A \le +85$°C, $\|\pm I_O\|$ =0.1 A $\pm V_O$	—	±1	—	$\%V_O$
Line Regulation	ΔReg_{line}	Over V_I range, balanced load $\pm V_O$	—	±0.1	±0.5	$\%V_O$
Load Regulation	ΔReg_{load}	Over $\pm I_O$ range, balanced load $\pm V_O$	—	±0.1	±1	$\%V_O$
Efficiency	η	$P_O = P_O$ max	—	88	—	%
V_o Ripple (pk-pk)	±Vr	20 MHz bandwidth, C_O =10 µF tantalum capacitor	—	50	100 (4)	mV_{pp}
Transient Response	t_S	0.1 A/µs load step, 50% to 75% $\pm I_O$ max	—	30	—	µs
	ΔV_O pk	$\|\pm V_O\|$ over/undershoot	—	±1	—	$\%V_O$
Over Current Threshold	$I_O$trip	V_I =36 V reset followed by auto-recovery	1.4	1.9	2.4	A
Short Circuit Current		Continuous over-current trip, $\|\pm I_O\|_{PK}$	—	3	—	A
		$\|+I_O\| = \|-I_O\|$ Duty	—	10	—	%
Output Voltage Adjust Range	$\|\pm V_O\|$adj	$\|+V_O\|$ and $\|-V_O\|$ adjust simulataneously	6.5	—	13.4 (5)	V
Switching Frequency	f_S	Over V_I and I_O ranges	440	480 (6)	520	kHz
Under-Voltage Lockout	$V_I$on $V_I$off	V_I increasing V_I decreasing	— —	33 32	— —	V
On/Off Enable (pin 3) Input High Voltage Input Low Voltage	 V_{IH} V_{IL}	Referenced to $-V_I$ (pin 4)	 +3.6 –0.2	 — —	 +75 (7) +0.8	V
Input Low Current	I_{IL}		—	—	–1	mA
Standby Input Current	I_I standby	pin 3 open circuit	—	2	—	mA
Start-up Time	t_{ON}	$\|\pm I_O\|$ =1 A, $\|\pm V_O\|$ rising 0 to 0.95 $\|\pm V_O\|_{TYP}$	—	10	—	ms
Internal Input Capacitance	C_I		—	2	—	µF
External Output Capacitance	C_O	Capacitance from either output to COM (pin 6)	0	—	1,500 (8)	µF
Reliability	MTBF	Per Telcordia SR-332 50% stress, T_A =40°C, ground benign	2.8	—	—	10^6 Hrs

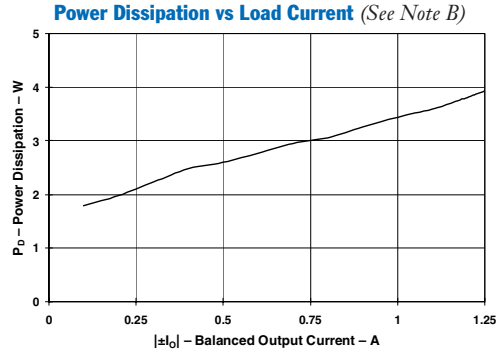
Notes: *(1) See Safe Operating Area curves or contact the factory for the appropriate derating.*
(2) Under balanced load conditions, load current flowing out of $+V_O$ is balanced to within ±0.1 A of that flowing into $-V_O$.
(3) A load imbalance is the difference in current flowing from $+V_O$ to $-V_O$. The module can operate with a higher imbalance but with reduced specifications.
(4) Output voltage ripple is measured with a 10-µF tantalum capacitor connected from $+V_O$ (pin 5) or $-V_O$ (pin 8), to COM (pin 6).
(5) When the output voltage is adjusted higher than the nominal output voltage the load current must not exceed the module's maximum power rating.
(6) This is the free-running frequency. The module can be made to synchronize with the PTB48500 when both modules are used together in a system.
(7) The On/Off Enable (pin 3) has an internal pull-up and may be controlled with an open-collector (or open-drain) transistor. The input is diode protected and may be connected to $+V_I$. The open-circuit voltage is 7 V max. If it is left open circuit the converter will operate when input power is applied.
(8) Electrolytic capacitors with very low equivalent series resistance (ESR) may induce instability when used on the output. Consult the factory before using capacitors with organic, or polymer-aluminum type electrolytes.

PTB48580B Characteristic Data @V_{IN} =48 V *(See Notes A)*

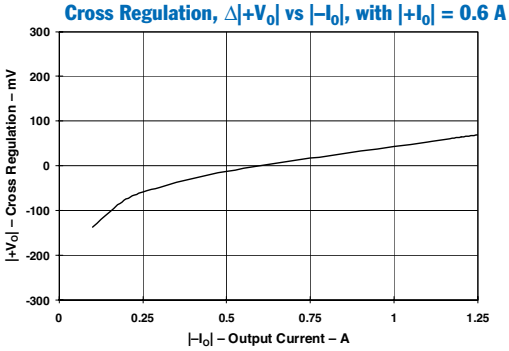
Efficiency vs Load Current *(See Note B)*



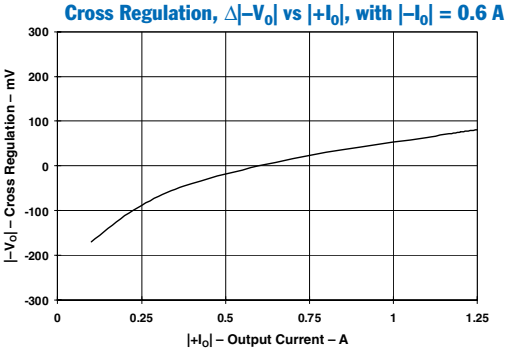
Power Dissipation vs Load Current *(See Note B)*



Cross Regulation, $\Delta|+V_O|$ vs $|-I_O|$, with $|+I_O|$ = 0.6 A

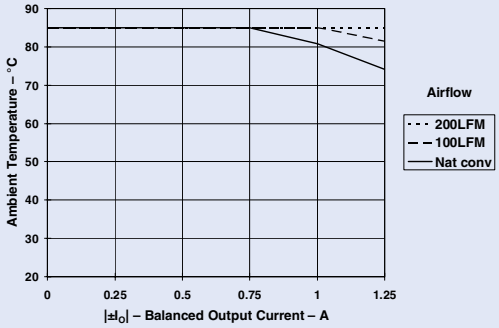


Cross Regulation, $\Delta|-V_O|$ vs $|+I_O|$, with $|-I_O|$ = 0.6 A



Safe Operating Area PTB48580B *(See Note C)*

Balanced Load, V_I =48 VDC *(See Note B)*



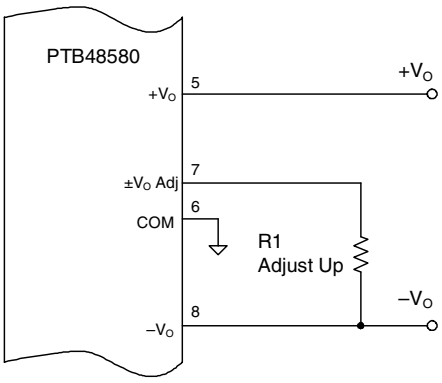
Note A: *Characteristic data has been developed from actual products tested at 25°C. This data is considered typical data for the converter.*
Note B: *Under a balanced load, current flowing out of $+V_o$ is equal to that flowing into $-V_o$.*
Note C: *SOA curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 4 in. × 4 in. double-sided PCB with 2 oz. copper.*

Adjusting the Output Voltages of the PTB48580 Series of DC/DC Converters

The PTB48580 series of DC/DC converters produce a balanced pair of complementary output voltages. They are identified $+V_O$ and $-V_O$, respectively. The magnitude of both output voltages can be adjusted together as a pair, higher or lower, by up to ±10% of their nominal. The adjustment method uses a single external resistor. [1] The value of the resistor determines the magnitude of the adjustment, and its placement determines whether the magnitude is increased or decreased. The resistor values can be calculated using the appropriate formula (see below). The formula constants are given in Table 1-1. The placement of each resistor is as follows.

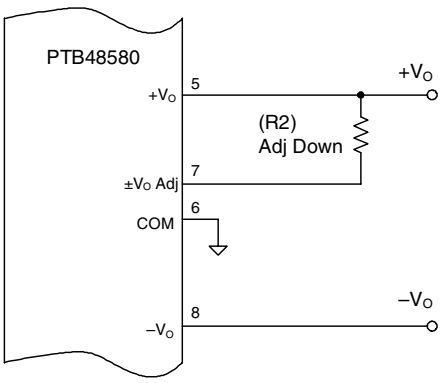
Adjust Up: To increase the magnitude [3] of both output voltages, place a resistor R1 between $\pm V_O\,Adj$ (pin 7) and the $-V_O$ (pin 8) voltage rail; see Figure 1-1(a).

Figure 1-1a



Adjust Down: To decrease the magnitude of both output voltages, add a resistor (R2), between $V_O\,Adj$ (pin 7) and the $+V_O$ (pin 5) voltage rail; see Figure 1-1(b).

Figure 1-1b



Calculation of Resistor Adjust Values

The value of the adjust resistor is calculated using one of the following equations. Use the equation for R1 to adjust up, or (R2) to adjust down.

$$R_1\ [\text{Adjust Up}] = \frac{V_R\,R_O}{2\,(V_A - V_O)} - R_S \quad k\Omega$$

$$(R_2)\ [\text{Adjust Down}] = \frac{R_O\,(2\,V_A - V_R)}{2\,(V_O - V_A)} - R_S \quad k\Omega$$

Where: V_O = Magitude of the original $\pm V_O$
V_A = Magnitude of the adjusted voltage
V_R = The reference voltage from Table 1-1
R_O = The resistance value in Table 1-1
R_S = The series resistance from Table 1-1

Table 1-1

ADJUSTMENT RANGE AND FORMULA PARAMETERS

Series Pt. No.	PTB48580A	PTB48580B
V_O (nom)	5 V	12 V
V_A (min)	3.5 V	6.5 V
V_A (max) [3]	6 V	13.4 V
V_R	2.495 V	2.495 V
R_O (kΩ)	7.5	18.2
R_S (kΩ)	9.09	16.9

Notes:

1. A 0.05-W rated resistor may be used. The tolerance should be 1%, with a temperature stability of 100 ppm/°C or better. Place the resistor in either the R1 or (R2) location, as close to the converter as possible.
2. Never connect capacitors to the $\pm V_O\,Adj$ pin. Capacitance added to this pin can affect the stability of the regulated output.
3. When the output voltage is adjusted higher than the nominal output voltage the load current must not exceed the module's maximum power rating of 30 W. For example, when the PTB48580A is adjusted to ±6 V (12 V in the single output configuration), the load current is limited to 2.5 A.

Configuring the PTB48580 Series of DC/DC Converters for DSL Applications

When operated as a pair, the PTB4850x and PTB48580 converters are specifically designed to provide all the required supply voltages for powering xDSL chipsets. The PTB4850x produces two logic voltages. They include a 3.3-V source for logic and I/O, and a low-voltage for powering a digital signal processor core. The PTB48580 produces a balanced pair of complementary supply voltages that is required for the xDSL transceiver ICs. When used together in these types of applications, the PTB4850x and PTB48580 may be configured for power-up sequencing, and also synchronized to a common switch conversion frequency. Figure 2-1 shows the required cross-connects between the two converters to enable these two features.

Switching Frequency Synchronization

Unsynchronized, the difference in switch frequency introduces a beat frequency into the input and output AC ripple components from the converters. The beat frequency can vary considerably with any slight variation in either converter's switch frequency. This results in a variable and undefined frequency spectrum for the ripple waveforms, which would normally require separate filters at the input of each converter. When the switch frequency of the converters are synchronized, the ripple components are constrained to the fundamental and higher. This simplifies the design of the output filters, and allows a common filter to be specified for the treatment of input ripple.

Power-Up Sequencing

The desired power-up sequence for the AC7 supply voltages requires that the two logic-level voltages from the PTB4850x converter rise to regulation prior to the two complementary voltages that power the transceiver ICs. This sequence cannot be guaranteed if the PTB4850x and PTB48580 are allowed to power up independently, especially if the 48-V input voltage rises relatively slowly. To ensure the desired power-up sequence, the "EN Out" pin of the PTB4850x is directly connected to the active-low "Enable" input of the PTB48580 (see Figure 2-1). This allows the PTB4850x to momentarily hold off the outputs from the PTB48580 until the logic-level voltages have risen first. Figure 2-2 shows the power-up waveforms of all four supply voltages from the schematic of Figure 2-1.

Figure 2-2; Power-Up Sequencing Waveforms

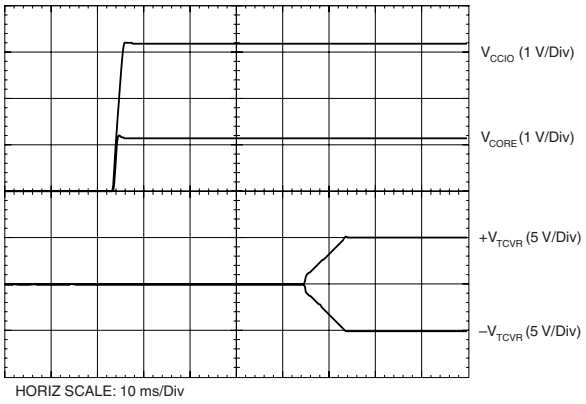
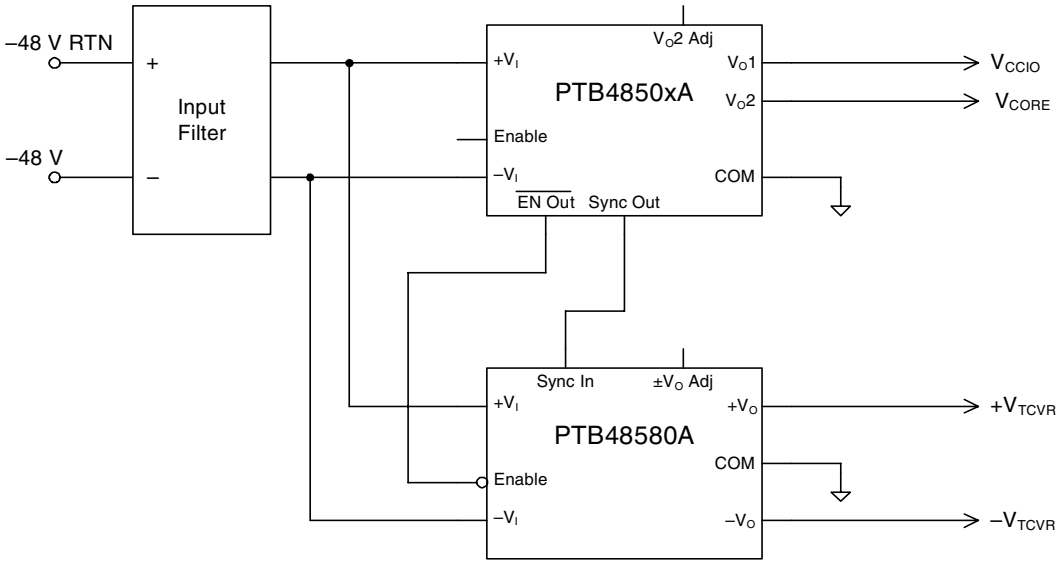


Figure 2-1; Example of PTB4850x & PTB48580A Modules Configured for DSL Applications



PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTB48580AAH	NRND	Production	Through-Hole Module (ERV) | 8	15 | TIW TRAY	In-Work	SN	N/A for Pkg Type	-40 to 85	
PTB48580AAH.B	NRND	Production	Through-Hole Module (ERV) | 8	15 | TIW TRAY	In-Work	SN	N/A for Pkg Type	-40 to 85	
PTB48580AAS	NRND	Production	Surface Mount Module (ERS) | 8	15 | TIW TRAY	No	SNPB	Level-1-235C-UNLIM/ Level-3-260C-168HRS	-40 to 85	
PTB48580AAS.B	NRND	Production	Surface Mount Module (ERS) | 8	15 | TIW TRAY	No	SNPB	Level-1-235C-UNLIM/ Level-3-260C-168HRS	-40 to 85	
PTB48580AAZ	NRND	Production	Surface Mount Module (ERS) | 8	15 | TIW TRAY	In-Work	SNAGCU	Level-3-260C-168 HR	-40 to 85	
PTB48580BAH	NRND	Production	Through-Hole Module (ERV) | 8	15 | TIW TRAY	In-Work	SN	N/A for Pkg Type	-40 to 85	
PTB48580BAH.B	NRND	Production	Through-Hole Module (ERV) | 8	15 | TIW TRAY	In-Work	SN	N/A for Pkg Type	-40 to 85	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

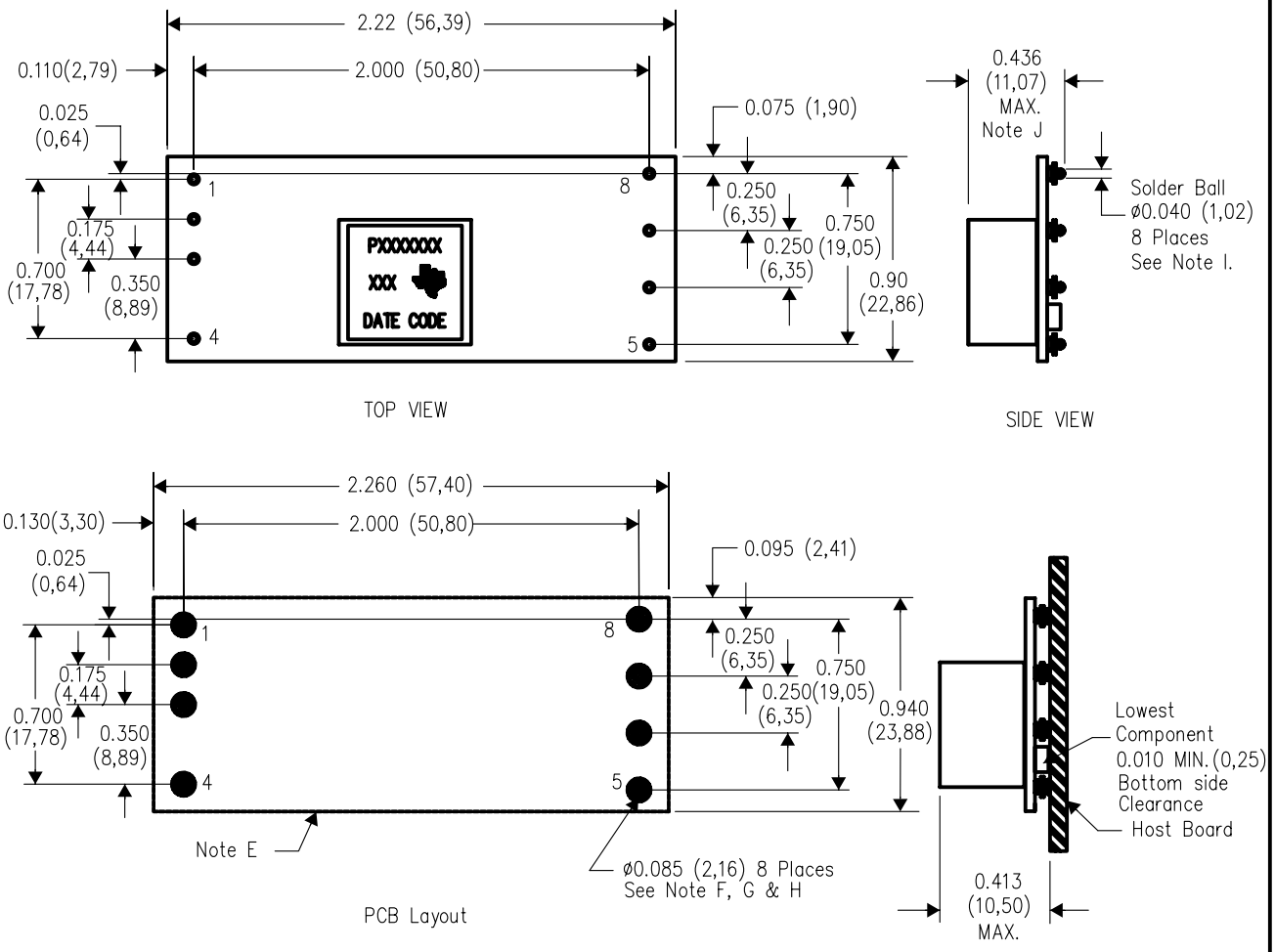
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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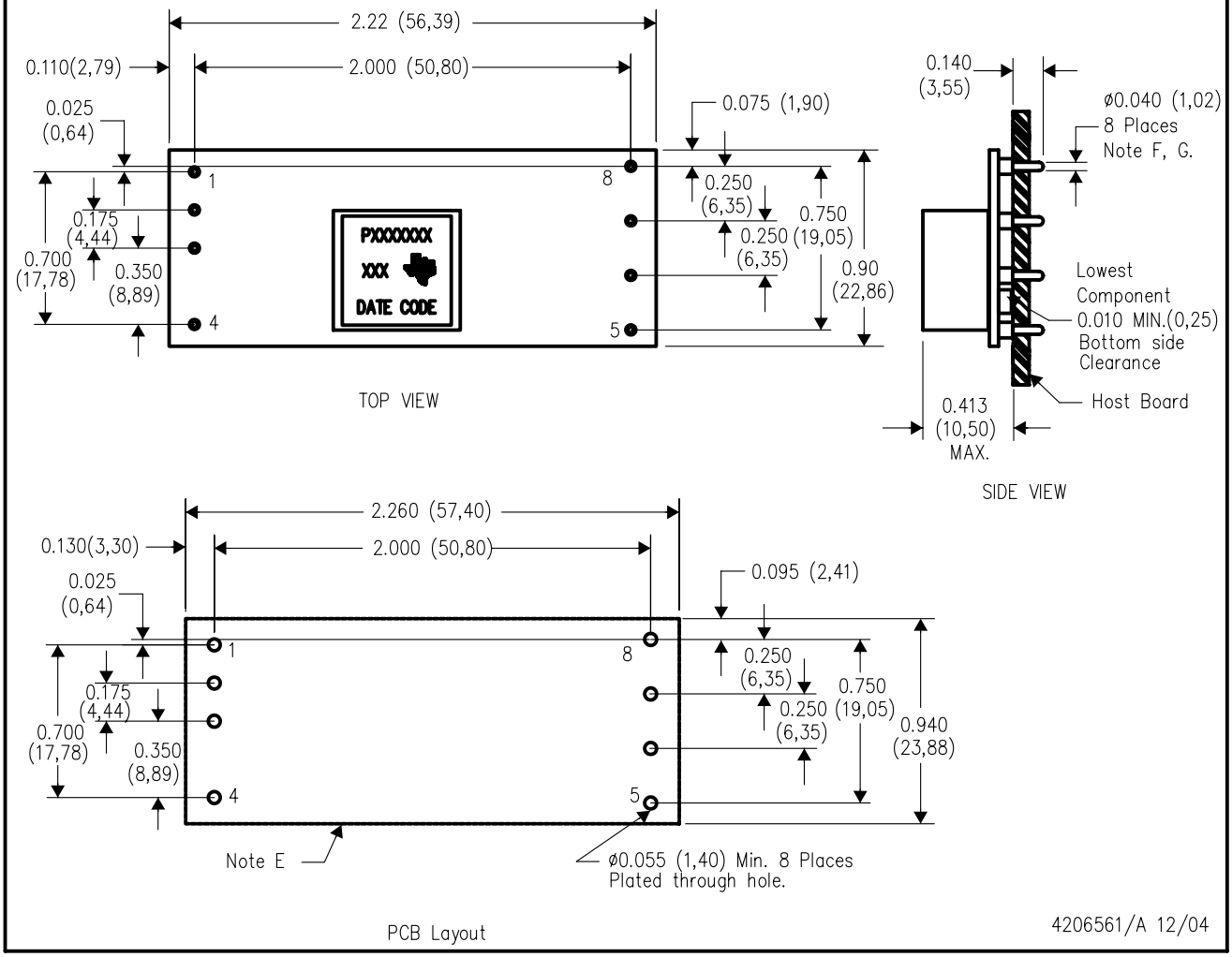
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ERS (R–PDSS–T8) DOUBLE SIDED MODULE



NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.020 (±0,51mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Power pin connection should utilize four or more vias to the interior power plane of 0.025 (0,63) I.D. per input, ground and output pin (or the electrical equivalent).
G. Paste screen opening: 0.080 (2,03) to 0.085 (2,16). Paste screen thickness: 0.006 (0,15).
H. Pad type: Solder mask defined.
I. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate
Solder Ball – See product data sheet.
J. Dimension prior to reflow solder.

ERV (R–PDSS–T8) DOUBLE SIDED MODULE



NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.020 (±0,51mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Pins are 0.040" (1,02) diameter with 0.070" (1,78) diameter standoff shoulder.
G. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate

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