# 60-A, 3.3/5-V INPUT, NONISOLATED WIDE-OUTPUT ADJUST POWER MODULE

**Check for Samples: PTH04040W**

## FEATURES

- **60-A Output Current**
- **3.3-V and 5-V Input Voltage**
- **Wide-Output Voltage Adjust (0.8 V to 2.5 V)**
- **Efficiencies up to 93%**
- **On/Off Inhibit**
- **Differential Output Sense**
- **Output Overcurrent Protection (Nonlatching, Auto-Reset)**
- **Overtemperature Protection**
- **Auto-Track™ Sequencing**
- **Start Up Into Output Prebias**
- **Margin Up/Down Controls**
- **Operating Temperature: –40°C to 85°C**
- **Multi-Phase, Switch-Mode Topology**
- **Programmable Undervoltage Lockout (UVLO)**
- **Safety Agency Approvals: UL/IEC/CSA-22.2 60950-1**

## APPLICATIONS

- **Advanced Computing and Server Applications**






NOMINAL SIZE = 2.05 in x 1.05 in (52 mm x 26,7 mm)

## DESCRIPTION

The PTH04040W is a high-performance 60-A rated, nonisolated, power module, which uses the latest multi-phase switched-mode topology. This provides a small, ready-to-use module, that can power the most densely populated multiprocessor systems.

The PTH04040W operates over an input voltage range of 2.95 V to 5.5 V, and can be set to any output voltage over the range, 0.8 V to 2.5 V, using a single external resistor. The combination of a wide input voltage and wide-output adjust range allows the PTH04040W to be used in many of high-performance applications. These include advanced computing platforms and servers that utilize either a 3.3-V or 5-V distribution bus.

These modules incorporate a comprehensive list of features. They include an on/off inhibit and margin up/down controls. A differential remote output voltage sense ensures tight load regulation, and an output overcurrent and overtemperature shutdown protect against most load faults. A programmable undervoltage lockout allows the turn-on threshold to be customized.

The PTH04040W incorporates Auto-Track™. Auto-Track is a popular feature of the PTH family that allows the outputs of multiple modules to track a common voltage during power-up and power-down transitions. This greatly simplifies the sequencing of voltages for VLSI ICs that operate off multiple power rails.

The double-sided surface mount construction has a low profile and compact footprint. It is available in both throughhole and surface-mount packages.

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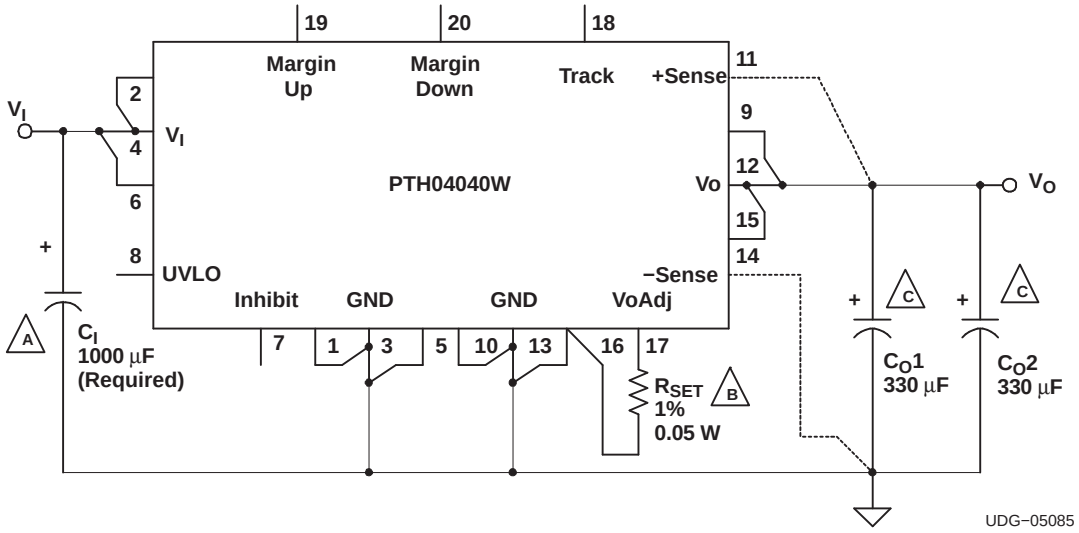
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## STANDARD APPLICATION




A. For $C_I$, a minimum of 1,000 µF (or 2 × 470 µF) of input capacitance is required for proper operation.

B. $R_{SET}$ is required to set the desired output voltage from the module higher than the minimum value.

C. For $C_O1$ and $C_O2$, a minimum of 660 µF (or 2 × 330 µF) of output capacitance is required for load transient regulation.

### ORDERING INFORMATION

**For the most current package and ordering information, see the Package Option Addendum at the end of this datasheet, or see the TI website at www.ti.com.**

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

| | | | | UNIT |
|---|---|---|---|---|
| | Signal input voltages | Track control (pin 18) | | –0.3 V to $V_I$ + 0.3 V |
| $T_A$ | Operating temperature range over $V_I$ range | | | –40°C to 85°C |
| $T_{wave}$ | Wave solder temperature | Surface temperature of module body or pins **(5 seconds)** | PTH04040WAH PTH04040WAD | 260°C (1) |
| $T_{reflow}$ | Solder reflow temperature | Surface temperature of module body or pins | PTH04040WAS | 235°C (1) |
| | | | PTH04040WAZ | 260°C (1) |
| $T_S$ | Storage temperature | | | –55°C to 125°C |
| | Mechanical shock | Per Mil-STD-883D, Method 2002.3, 1 msec, ½ Sine, mounted | | 500 G (2) |
| | Mechanical vibration | Mil-STD-883D, Method 2007.2, 20–2000 Hz | | 10 G (2) |
| | Weight | | | 22.5 grams |
| | Flammability | Meets UL94V-O | | |

(1) During soldering of package version, do not elevate peak temperature of the module, pins or internal components above the stated maximum.

(2) Qualification limits


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## ELECTRICAL CHARACTERISTICS

$T_A$ = 25°C, $V_I$ = 5 V, $V_O$ = 2.5 V, $C_I$ = 1000 µF, $C_O$ = 660 µF, and $I_O$ = $I_O$max (unless otherwise stated)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_O$ | Output current | 60°C, 200 LFM airflow | | 0 | | 60 (1) | A |
| $V_I$ | Input voltage range | Over $I_O$ range | | 2.95 (2) | | 5.5 | V |
| $V_O$tol | Set-point voltage tolerance | | | | | ±2 (3) | %$V_O$ |
| $\Delta Reg_{temp}$ | Temperature variation | –40°C < $T_A$ < 85°C | | | ±0.5 | | %$V_O$ |
| $\Delta Reg_{line}$ | Line regulation | Over $V_I$ range | | | ±5 | | mV |
| $\Delta Reg_{load}$ | Load regulation | Over $I_O$ range | | | ±5 | | mV |
| $\Delta Reg_{tot}$ | Total output variation | Includes set-point, line, load, –40°C ≤ $T_A$ ≤ 85°C | | | | ±3 (3) | %$V_O$ |
| $V_{O, ADJ}$ | Output adjust range | | 2.95 ≤ $V_I$ ≤ 4.5 V (3) | 0.8 | - | 1.65 | V |
| | | | 4.5 < $V_I$ ≤ 5.5 V (3) | 0.8 | - | 2.5 | |
| η | Efficiency | $V_I$ = 5 V, $I_O$ = 45 A | $R_{SET}$ = 2.21 kΩ, $V_O$ = 2.5 V | | 93% | | |
| | | | $R_{SET}$ = 5.49 kΩ, $V_O$ = 1.8 V | | 90% | | |
| | | | $R_{SET}$ = 8.87 kΩ, $V_O$ = 1.5 V | | 88% | | |
| | | | $R_{SET}$ = 17.4 kΩ, $V_O$ = 1.2 V | | 86% | | |
| | | $V_I$ = 3.3 V, $I_O$ = 45 A | $R_{SET}$ = 6.92 kΩ, $V_O$ = 1.65 V | | 92% | | |
| | | | $R_{SET}$ = 8.87 kΩ, $V_O$ = 1.5 V | | 91% | | |
| | | | $R_{SET}$ = 36.5 kΩ, $V_O$ = 1 V | | 87% | | |
| $V_R$ | $V_O$ ripple (peak-to-peak) | 20-MHz bandwidth | All voltages | | 15 | | $mV_{PP}$ |
| $I_O$trip | Overcurrent threshold | Reset, followed by auto-recovery | | | 90 | | A |
| $t_{rr}$ | Transient response | 1 A/µs load step, 50 to 100% $I_O$max, $C_O$=660µF | Recovery time | | 100 | | µS |
| $\Delta V_{tr}$ | | | $V_O$ over/undershoot | | 200 | | mV |
| | Margin up down adjust | From a given set-point voltage | | | ±5% | | % |
| $I_{IL}$margin | Margin input current | Pin to GND | | | –8 (4) | | µA |
| $I_{IL}$track | Track input current (pin 18) | Pin to GND | | | | –0.11 (5) | mA |
| dV/dt | Track slew rate capability | $\lvert V_{TRACK} - V_O \rvert$ ≤ 50 mV and $V_{(TRACK)}$ < $V_O$(nom) | | | | 1 | V/ms |
| UVLO | Undervoltage lockout | Pin 8 open | On-threshold | | 2.6 (6) | | V |
| | | | Hysterisis | | 0.6 (6) | | |
| | Inhibit control (pin 7) | Input high voltage ($V_{IH}$), Referenced to GND | | 2.5 | | Open (7) | V |
| | | Input low voltage ($V_{IL}$), Referenced to GND | | –0.2 | | 0.5 | |
| | | Input low current ($I_{IL}$), Pin to GND | | | 0.5 | | mA |
| $I_I$inh | Input standby current | Inhibit (pin 7) to GND | | | 60 | | mA |
| $f_s$ | Switching frequency | Over $V_I$ and $I_O$ ranges | | 675 | 825 | 975 | kHz |

(1) See SOA curves or consult factory for appropriate derating.
(2) The nominal input voltage must be at least 2 × $V_O$. Output voltage regulation is specified with an input voltage within ±10% from nominal 3.3 V or 5 V. For example, for $V_I$ = 5 V and $V_O$ = 2.5 V, the input can vary between 4.5 V and 5.5 V.
(3) The set-point voltage tolerance is affected by the tolerance of $R_{SET}$. The stated limit is unconditionally met if $R_{SET}$ has a tolerance of 1% with 100 ppm/°C or better temperature stability.
(4) A small, low-leakage (<100 nA) MOSFET is recommended to control this pin. The open-circuit voltage is less than 1 Vdc.
(5) This control pin has an internal pull-up to $V_I$. If it is left open-circuit the module operates when input power is applied. A small, low-leakage (<100 nA) MOSFET or open-drain/collector voltage supervisor IC is recommended for control. See the *Auto-Track Application Information* section for further guidance.
(6) These are the default voltages. They may be adjusted using the *UVLO Prog* control input. See the *UVLO Application Information* section for further guidance.
(7) This control pin has an internal pull-up to $V_I$. If it is left open-circuit the module operates when input power is applied. A small, low-leakage (<100 nA) MOSFET or open-drain/collector voltage supervisor IC is recommended for control. Do not place an external pull-up on this pin. See the *Inhibit Application Information* section for further guidance.

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## ELECTRICAL CHARACTERISTICS (continued)

$T_A$ = 25°C, $V_I$ = 5 V, $V_O$ = 2.5 V, $C_I$ = 1000 µF, $C_O$ = 660 µF, and $I_O$ = $I_O$max (unless otherwise stated)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $C_I$ | External input capacitance | | | 940(8) | | | µF |
| $C_O$ | External output capacitance | Capacitance value | Nonceramic | 660(9) | | 14000(10) | µF |
| | | | Ceramic | | | 400 | |
| | | Equivalent series resistance (nonceramic) | | 2(11) | | | mΩ |
| MTBF | Reliability | Per Bellcore TR-332 50% stress, $T_A$ = 40°C, ground benign | | 2.1 | | | $10^6$Hrs |

(8) A minimum capacitance of 940 µF is required at the input for proper operation. The capacitance must be rated for a minimum of 400 mArms of ripple current.
(9) 660 µF of output capacitance is required for proper operation. Additional capacitance at the load will improve transient response.
(10) This is the calculated maximum. The minimum ESR requirement often results in a lower value. See the *Capacitor Application Information* section for further guidance.
(11) This is the typical ESR for all the electrolytic (nonceramic) output capacitance. Use 4 mΩ as the minimum when using max-ESR values to calculate.

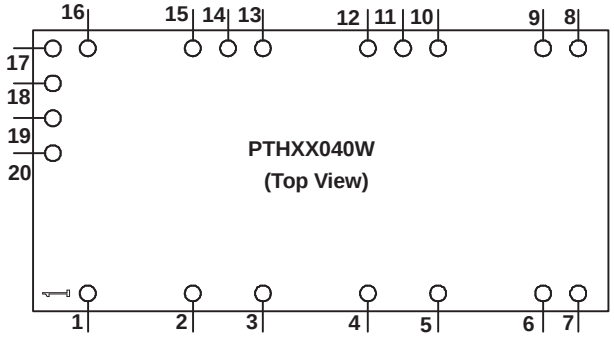

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# DEVICE INFORMATION

## TERMINAL FUNCTIONS

| TERMINAL | | DESCRIPTION |
|---|---|---|
| NAME | NO. | |
| GND | 1, 3, 5, 10, 13, 16 | This is the common ground connection for the $V_I$ and $V_O$ power connections. It is also the 0 Vdc reference for the control inputs. |
| $V_I$ | 2, 4, 6 | The positive input voltage power node to the module, which is referenced to common GND. |
| $V_O$ | 9, 12, 15 | The regulated positive power output with respect to the *GND* node. |
| Inhibit(1) | 7 | The Inhibit pin is an open-collector/drain negative logic input that is referenced to GND. Applying a low level ground signal to this input disables the module's output and turns off the output voltage. When the Inhibit control is active, the input current drawn by the regulator is significantly reduced. If the Inhibit pin is left open-circuit, the module produces an output whenever a valid input source is applied. Do not place an external pull-up on this pin. |
| $V_O$ Adjust | 17 | A 1%, 0.05-W resistor must be connected between this pin and GND to set the output voltage higher than the minimum value. The set-point range for the output voltage is from 0.8 V to 2.5 V. The resistor required for a given output voltage may be calculated from the following formula. If left open circuit, the module output defaults to its lowest output voltage value. For further information on the adjustment and/or trimming of the output voltage, see the related Application Information section. *Note: The specification table gives the preferred resistor values for a number of standard output voltages*. |
| +Sense | 11 | The sense inputs allow the regulation circuit to compensate for voltage drop between the module and the load. For optimal voltage accuracy, +Sense should be connected to $V_O$. If it is left open, a low-value internal resistor ensures that the output remains in regulation. |
| –Sense | 14 | For optimal voltage accuracy, –Sense should be connected to the ground return at the load. If it is left open, a low-value internal resistor ensures that the output remains in regulation. |
| UVLO Prog | 8 | Connecting a resistor from this pin to signal ground allows the *on* threshold of the input undervoltage lockout (UVLO) to be adjusted higher than the default value. The hysterisis can also be independently reduced by connecting a second resistor from this pin to $V_I$. For further information, see the Application Information section. |
| Track | 18 | This is an analog control input that allows the output voltage to follow another voltage during power up and power down sequences. The pin is active from 0 V, up to the nominal set-point voltage. Within this range, the module output follows the voltage at the Track pin on a volt-for-volt basis. When the control voltage is raised above this range, the module regulates at its nominal output voltage. If unused, this input should be connected to $V_I$ for a faster power up. For further information, see the related Application Information section. |
| Margin Down(1) | 20 | When this input is asserted to GND, the output voltage is decreased by 5% from the nominal. The input requires an open-collector (open-drain) interface. It is **not** TTL compatible. A lower percent change can be accommodated with a series resistor. For further information, see the related Application Information section. |
| Margin Up(1) | 19 | When this input is asserted to GND, the output voltage is increased by 5%. The input requires an open collector (open-drain) interface. It is **not** TTL compatible. The percent change can be reduced with a series resistor. For further information, see the related Application Information section. |

(1) Denotes negative logic: Open = Normal operation; Ground = Function active




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## TYPICAL CHARACTERISTICS ($V_I$ = 3.3 V)(1) (2)

## CHARACTERISTIC DATA

**EFFICIENCY vs LOAD CURRENT**

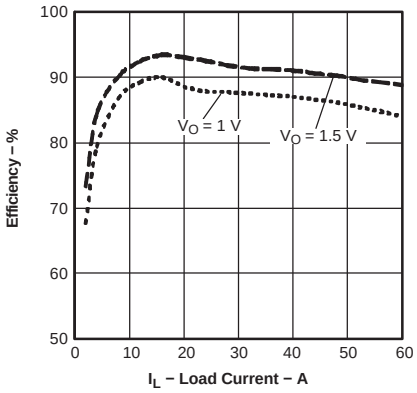



**Figure 1.**

**OUTPUT RIPPLE vs LOAD CURRENT**

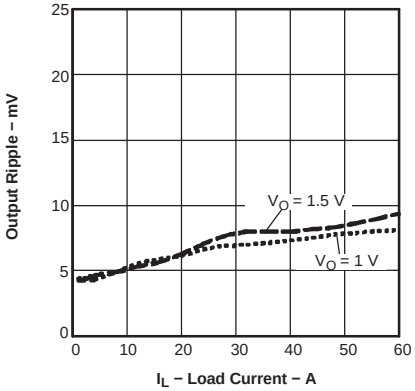



**Figure 2.**

**POWER DISSIPATION vs LOAD CURRENT**

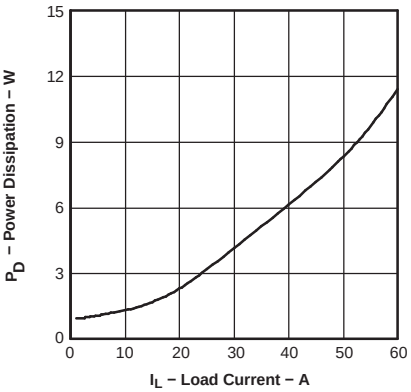



**Figure 3.**

**TEMPERATURE DERATING vs LOAD CURRENT**

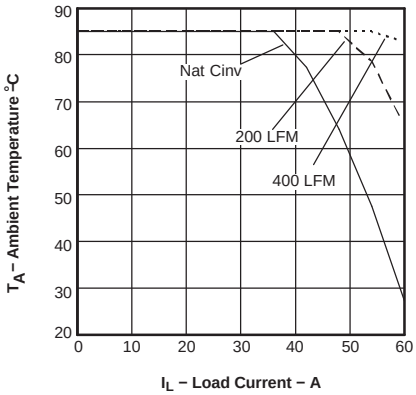



**Figure 4. Safe Operating Area**

(1) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to Figure 1, Figure 2, and Figure 3.

(2) SOA curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 4 inches × 4 inches double-sided PCB with 1 oz. copper. Applies to Figure 4.


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## TYPICAL CHARACTERISTICS ($V_I$ = 5 V)(1) (2)

**EFFICIENCY vs LOAD CURRENT**

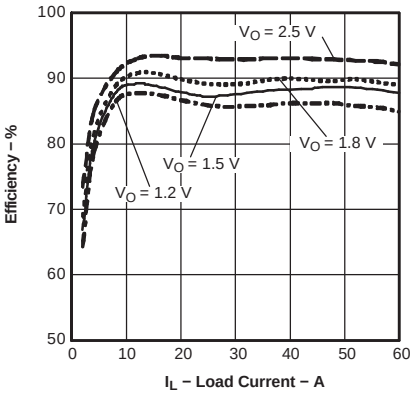



**Figure 5.**

**OUTPUT RIPPLE vs LOAD CURRENT**

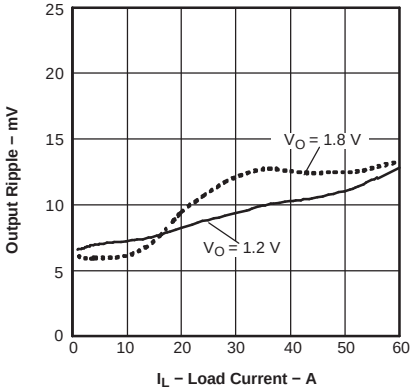



**Figure 6.**

**POWER DISSIPATION vs LOAD CURRENT**

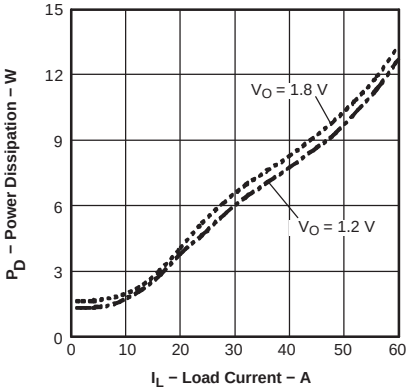



**Figure 7.**

**TEMPERATURE DERATING vs LOAD CURRENT**

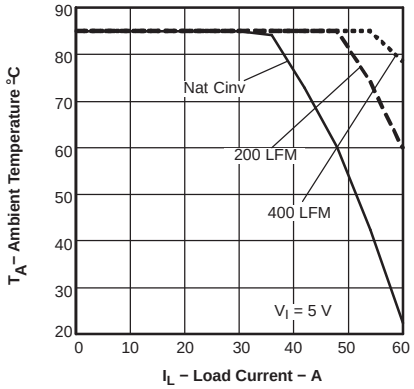



**Figure 8. Safe Operating Area**

(1) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to Figure 5, Figure 6, and Figure 7.

(2) SOA curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 4 inches × 4 inches double-sided PCB with 1 oz. copper. Applies to Figure 8.

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# APPLICATION INFORMATION

## CAPACITOR RECOMMENDATIONS FOR THE PTH04040W POWER MODULE

The PTH04040W uses state-of-the-art multi-phase power converter topology that employs multiple parallel switching and filter inductor paths between the input and output capacitors. The PTH04040W uses three switching paths. The three paths share the total load current, operate at the same frequency, and are evenly displaced in phase. With multiple switching paths the transient output current capability is significantly increased. This reduces the amount of external output capacitance required to support a load transient. The ripple current, as seen by the input and output capacitors, is reduced in magnitude and effectively tripled in frequency.

### INPUT CAPACITOR

The improved transient response of a multi-phase converter places a bigger burden on the transient capability of the input source. The size and value of the input capacitor is therefore determined by this converter's transient performance capability. The minimum amount of input capacitance required is 940 μF (2 × 470 μF or 3 × 330 μF), with an RMS ripple current rating of 400 mA. This minimum value assumes that the converter is supplied with a responsive, low-inductance input source. This source should have ample capacitive decoupling and be distributed the converter via PCB power and ground planes. For high performance applications, or wherever the transient capability of the input source is limited, 2,200 μF of input capacitance is recommended.

Ripple current and less than 100 mΩ equivalent series resistance (ESR) values are the major considerations, along with temperature, when designing with different types of capacitors. Unlike polymer tantalum, conventional tantalum capacitors have a recommended minimum voltage rating of 2 × (maximum dc voltage + ac ripple). This is standard practice to ensure reliability.

For improved ripple reduction on the input bus, ceramic capacitors may be used to complement electrolytic types and achieve the minimum required capacitance.

### OUTPUT CAPACITORS RECOMMENDED

In order to respond with load transients (sudden changes in load current) the regulator requires external output capacitance. The minimum output capacitance is 660 μF (2 × 330 μF or 1 × 680 μF) with an ESR of at least 2 mΩ. This output capacitance is required for the module to meet its transient response specification. For most applications, a high quality computer grade aluminum electrolytic capacitor is suitable. These capacitors provide adequate decoupling over the frequency range, 2 kHz to 150 kHz, and when ambient temperatures are above 0°C. For operation below 0°C, tantalum, ceramic, or Os-Con type capacitors are recommended.

When using one or more nonceramic capacitors, the calculated equivalent ESR should be no lower than 4 mΩ 7 mΩ using the manufacturer's maximum ESR for a single capacitor. A list of preferred low-ESR type capacitors are identified in Table 1.

### CERAMIC CAPACITORS

Above 150 kHz, the performance of aluminum electrolytic capacitors becomes less effective. To further improve, the reflected input ripple current or the output transient response, multilayer ceramic capacitors can also be added. Ceramic capacitors have very low ESR and their resonant frequency is higher than the bandwidth of the regulator. When used on the output their combined ESR is not critical as long as the total value of ceramic capacitance does not exceed 300 μF. Also, to prevent the formation of local resonances, do not place more than five identical ceramic capacitors in parallel with values of 10 μF or greater.

### TANTALUM CAPACITORS

Tantalum type capacitors can be used at both the input and output, and are recommended for applications where the ambient operating temperature can be less than 0°C. The AVX TPS, Sprague 593D/594/595, and Kemet T495/ T510 capacitor series are suggested over many other tantalum types due to their higher rated surge, power dissipation, and ripple current capability. As a caution, many general-purpose tantalum capacitors have considerably higher ESR, reduced power dissipation and lower ripple current capability. These capacitors are also less reliable when determining their power dissipation and surge current capability. Tantalum capacitors that do not have a stated ESR or surge current rating are not recommended for power applications. When specifying Os-Con and polymer tantalum capacitors for the output, the minimum ESR limit is encountered before the maximum capacitance value is reached.


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## CAPACITOR TABLE

Table 1 identifies the characteristics of capacitors from a number of vendors with acceptable ESR and ripple current (rms) ratings. The recommended number of capacitors required at both the input and output buses is identified for each capacitor type.

*Note: This is not an extensive capacitor list. Capacitors from other vendors are available with comparable specifications. Those listed are for guidance. The RMS ripple current rating and ESR (at 100kHz) are critical parameters necessary to insure both optimum regulator performance and long capacitor life.*

## DESIGNING FOR VERY FAST LOAD TRANSIENTS

The transient response of the dc/dc converter has been characterized using a load transient with a di/dt of 1 A/μs. The typical voltage deviation for this load transient is given in the data sheet specification table using the minimum required value of output capacitance. As the di/dt of a transient is increased, the response of a converter's regulation circuit ultimately depends on its output capacitor decoupling network. This is an inherent limitation with any dc/dc converter once the speed of the transient exceeds its bandwidth capability. If the target application specifies a higher di/dt or lower voltage deviation, the requirement can only be met with additional output capacitor decoupling. In these cases special attention must be paid to the type, value and ESR of the capacitors selected. Additional input capacitance may be required to insure the stability of the input bus during higher current transient di/dt.

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## Table 1. Input/Output Capacitors(1)

| Capacitor Vendor, Type Series (Style) | Capacitor Characteristics | | | | | Quantity | | |
|---|---|---|---|---|---|---|---|---|
| | Working Voltage | Value (µF) | Max. ESR at 100 kHz | Max Ripple Current at 85°C (I rms) | Physical Size (mm) | Input Bus | Output Bus | Vendor Part No. |
| Panasonic | | | | | | | | |
| FC (Radial) | 10 V | 1000 | 0.068 Ω | >1050 mA | 10 × 16 | 1 | 1 | EEUFC1A102 |
| FC (Radial) | 10 V | 1000 | 0.0650 Ω | 1205 mA | 12.5 × 16.5 | 1 | 1 | EEVFC1A102LQ |
| FK (SMD) | 10 V | 1000 | 0.080 Ω | 850 mA | 10 × 10.2 | 1 | 1 | EEVFK1A102P |
| United Chemi-Con | | | | | | | | |
| FX, Oscon (Radial) | 6.3 V | 1000 | 0.013 Ω | 4935 mA | 10 × 10.5 | 1 | 1 | 6FX1000M |
| PXA, (Poly-Aluminum (SMD) | 6.3 V | 820 | 0.010 Ω | 5500 mA | 10 × 12.2 | 2 | 1 | PXA6.3VC820MJ12TP |
| PSA (Poly-Aluminum) | 10 V | 680 | 0.007 Ω | >5800 mA | 10 × 11.5 | 2 | ≤3 | PSA6.3VB680MJ11 |
| LXZ, Aluminum (Radial) | 10 V | 1000 | 0.068 Ω | 1050 mA | 10 × 16 | 1 | 1 | LXZ10VB102M10X16LL |
| Nichicon, Aluminum | | | | | | | | |
| HD (Radial) | 6.3 V | 1000 | 0.053 Ω | 1030 mA | 10 × 12.5 | 1 | 1 | UHD0J102MPR |
| PM (Radial) | 10 V | 1000 | 0.065 Ω | 1040 mA | 12.5 × 15 | 1 | 1 | UPM1A102MHH6 |
| Sanyo, Os-Con | | | | | | | | |
| SP, (Radial) | 10 V | 470 | 0.015 Ω | >4500 mA | 10x10.5 | 2(2) | ≤5 | 10SP470M |
| SVP, (SMD) | 6.3 V | 820 | 0.012 Ω | >5440 mA | 10x12.7 | 2 | ≤4 | 6SVP820M |
| Panasonic, Poly-Aluminum: S/SE (SMD) | 63 V | 180 | 0.005 Ω | 4000 mA | 7.3x4.3x4.2 | N/R | ≤2 | EEFSE0J181R |
| AVX, Tantalum, Series III | | | | | | | | |
| TPS (SMD) | 10 V | 470 | 0.045 Ω | 1723 mA | 7.3x5.7x4.1 | 2(2) | ≤7 | TPSE477M010R0045 |
| | 10 V | 470 | 0.060 Ω | 1826 mA | 7.3x5.7x4.1 | 2(2) | ≤7 | TPSV477M010R0060 |
| Kemet, Poly-Tantalum | | | | | | | | |
| T520 (SMD) | 6.3 V | 470 | 0.018 Ω | >1200 mA | 7.3x4.3x4 | 2(2) | ≤6 | T520X477M006SE018 |
| T530 (SMD) | 10 V | 330 | 0.015 Ω | >3800 mA | 7.3x4.3x4 | 3 | ≤4 | T530X337M010AS |
| | 6.3 V | 470 | 0.012 Ω | 4200 mA | 7.3x4.3x4 | 2(2) | ≤3 | T530X477M006AS |
| Vishay-Sprague | | | | | | | | |
| 595D, Tantalum (SMD) | 10 V | 470 | 0.100 Ω | 1440 mA | 7.2x6×4.1 | 2(2) | ≤7 | 595D477X0010R2T |
| 94SA, Os-con (Radial) | 16 V | 2200 | 0.015 Ω | 9740 mA | 16 × 25 | 1 | ≤4 | 94SA108X0016HBP |
| Kemet, Ceramic X5R (SMD) | 16 V | 10 | 0.002 Ω | – | 1210 case | 1(3) | ≤9 | C1210C106M4PAC |
| | 6.3 V | 47 | 0.002 Ω | | 3225 mm | 1(3) | ≤8 | C1210C476K9PAC |
| Murata, Ceramic X5R (SMD) | 6.3 V | 100 | 0.002 Ω | – | 1210 case | 1(3) | ≤4 | GRM32ER60J107M |
| | 6.3 V | 47 | | | 3225 mm | 1(3) | ≤ 8 | GRM32ER60J476M |
| | 16 V | 22 | | | | 1(3) | ≤ 8 | GRM32ER61C226K |
| | 16 V | 10 | | | | | ≤ 9 | GRM32DR61C106K |
| TDK, Ceramic X5R (SMD) | 6.3 V | 100 | 0.002 Ω | – | 1210 case | 1(3) | ≤4 | C3225X5R0J107MT |
| | 6.3 V | 47 | | | 3225 mm | 1(3) | ≤ 8 | C3225X5R0J476MT |
| | 16 V | 22 | | | | 1(3) | ≤ 8 | C3225X5R1C226MT |
| | 16 V | 10 | | | | | ≤ 9 | C3225X5R1C106MT |

(1) **Capacitor Supplier Verification**
1.Please verify availability of capacitors identified in this table. Capacitor suppliers may recommend alternative part numbers because of limited availability or obsolete products. In some instances, the capacitor product life cycle may be in decline and have short-term consideration for obsolescence.
**RoHS, Lead-free and Material Details**
2.Please consult capacitor suppliers regarding material composition, RoHS status, lead-free status, and manufacturing process requirements. Component designators or part number deviations can occur when material composition or soldering requirements are updated.

(2) The total capacitance is slightly lower than 1000 µF, but is acceptable based on the combined ripple current rating.

(3) Ceramic capacitors can be used to complement electrolytic types at the input to further reduce high-frequency ripple current.


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## ADJUSTING THE OUTPUT VOLTAGE OF THE PTH04040W

The $V_O$ *Adjust* control (pin 17) sets the output voltage of the PTH04040W to a value higher than 0.8 V. The adjustment range is from 0.8 V to 2.5 V. For an output voltage other than 0.8 V a single external resistor, $R_{SET}$ 1, must be connected directly between the $V_O$ *Adjust* (pin 17) and the output *GND* (pin 16)(2). Table 2 gives the preferred value of the external resistor for a number of standard voltages, along with the actual output voltage that this resistance value provides.

For other output voltages, the value of the required resistor is calculated using the following formula, or by selecting from the range of values given in Table 3. Figure 9 shows the placement of the required resistor.

$$R_{set} = 10\ k\Omega \times \frac{0.8\ V}{V_{out} - 0.8\ V} - 2.49\ k\Omega \quad (1)$$

**Table 2. Preferred Values of $R_{set}$ for Standard Output Voltages**

| $V_{OUT}$ (Standard) (1) | $R_{SET}$ (Preferred Value) | $V_{OUT}$ (Actual) |
|---|---|---|
| 2.5 V | 2.21 kΩ | 2.502 V |
| 2 V | 4.12 kΩ | 2.010 V |
| 1.8 V | 5.49 kΩ | 1.803 V |
| 1.5 V | 8.87 kΩ | 1.504 V |
| 1.2 V | 17.4 kΩ | 1.202 V |
| 1 V | 36.5 kΩ | 1.005 V |
| 0.8 V | Open | 0.8 V |

(1) The nominal input voltage must be at least 2 × $V_O$. Output voltage regulation is specified with an input voltage within ±10% from nominal 3.3 V or 5 V. For example, for $V_I$ = 5 V and $V_O$ = 2.5 V, the input can vary between 4.5 V and 5.5 V.

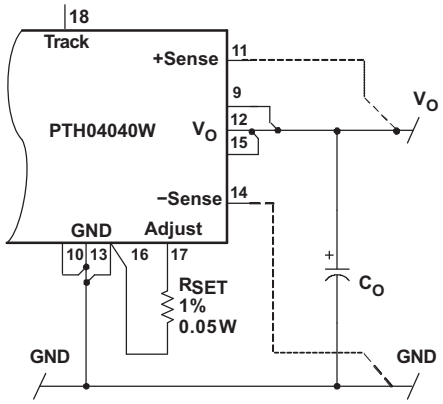



**Figure 9. $V_O$ Adjust Resistor Placement**

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**Table 3. Output Voltage Set-Point Resistor Values**

| $V_{OUT}$ | $R_{SET}$ | $V_{OUT}$ | $R_{SET}$ |
|---|---|---|---|
| 0.8 | Open | 1.425 | 10.3 kΩ |
| 0.825 | 318 kΩ | 1.45 | 9.82 kΩ |
| 0.85 | 158 kΩ | 1.475 | 9.36 kΩ |
| 0.875 | 104 kΩ | 1.5 | 8.94 kΩ |
| 0.9 | 77.5 kΩ | 1.55 | 8.18 kΩ |
| 0.925 | 61.5 kΩ | 1.6 | 7.51 kΩ |
| 0.95 | 50.8 kΩ | 1.65 | 6.92 kΩ |
| 0.975 | 43.2 kΩ | 1.7 | 6.4 kΩ |
| 1 | 37.5 kΩ | 1.75 | 5.93 kΩ |
| 1.025 | 33.1 kΩ | 1.8 | 5.51 kΩ |
| 1.05 | 29.5 kΩ | 1.85 | 5.13 kΩ |
| 1.075 | 26.6 kΩ | 1.9 | 4.78 kΩ |
| 1.1 | 24.2 kΩ | 1.95 | 4.47 kΩ |
| 1.125 | 22.1 kΩ | 2 | 4.18 kΩ |
| 1.15 | 20.4 kΩ | 2.05 | 3.91kΩ |
| 1.175 | 18.8 kΩ | 2.1 | 3.66 kΩ |
| 1.2 | 17.5 kΩ | 2.15 | 3.44 kΩ |
| 1.225 | 16.3 kΩ | 2.2 | 3.22 kΩ |
| 1.25 | 15.3 kΩ | 2.25 | 3.03 kΩ |
| 1.275 | 14.4 kΩ | 2.3 | 2.84 kΩ |
| 1.3 | 13.5 kΩ | 2.35 | 2.67 kΩ |
| 1.325 | 12.7 kΩ | 2.4 | 2.51 kΩ |
| 1.35 | 12.1 kΩ | 2.45 | 2.36 kΩ |
| 1.375 | 11.4 kΩ | 2.5 | 2.22 kΩ |
| 1.4 | 10.8 kΩ | | |

**NOTES:**

1. A 0.05-W rated resistor can be used. The tolerance should be 1%, with temperature stability of 100 ppm/°C (or better). Place the resistor as close to the regulator as possible. Connect the resistor directly between pins 17 and 16 using dedicated PCB traces.
2. Never connect capacitors from *$V_O$ Adjust* to either *GND or $V_O$* . Any capacitance added to the *$V_O$ Adjust* pin affects the stability of the regulator.


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## ADJUSTING THE UNDERVOLTAGE LOCKOUT (UVLO) OF THE PTH04040W

The PTH04040W power modules incorporate an input undervoltage lockout (UVLO). The UVLO feature prevents the operation of the module until there is sufficient input voltage to produce a valid output voltage. This enables the module to provide a monotonic powerup for the load circuit, and also limits the magnitude of current drawn from the module's input source during the power-up sequence.

The UVLO characteristic is defined by the on-threshold ($V_{THD}$) and hysterisis ($V_{HYS}$) voltages. Below the *on* threshold, the *Inhibit* control is overriden, and the module does not produce an output. Hysterisis voltage is the difference between the *on* and *off* threshold voltages. It ensures a clean power-up, even when the input voltage is rising slowly. The hysterisis prevents start-up oscillations, which can occur if the input voltage droops slightly when the module begins drawing current from the input source.

## UVLO ADJUSTMENT

The UVLO feature of the PTH04040W gives the user the option of adjusting the on-threshold voltage higher than the default value. This might be desirable if the module is powered from a 5-V input bus. This prevents the module from operating until the input bus has risen closer to its regulation voltage.

The adjustment method uses the *UVLO Prog* control (pin 8). If the *UVLO Prog* pin is left open circuit, the onthreshold voltage remains at its nominal value of 2.63 V (see electrical specification table). This ensures that the unadjusted module produces a regulated output when the minimum input voltage is applied. The hysterisis voltage is approximately 0.62 V, which correlates to an off-threshold voltage of about 2 V. The magnitude of the hysterisis is automatically set to about 22% of the onthreshold. So if the on-threshold voltage is increased, then the Hysterisis also increases.

## UVLO ADJUSTMENT METHOD

Figure 10 shows the placement of the resistor, $R_{THD}$, for adjusting the UVLO on-threshold voltage. It connects from the *UVLO Prog* control pin to *GND*. Equation 2 determines the value of $R_{THD}$ required to adjust $V_{THD}$ to a new value. The default value is 2.63 V, and it can only be adjusted higher. Once the value of $R_{THD}$ has been set, Equation 3 is used to determine the new hysterisis voltage.

$$R_{THD} = \frac{12.9}{V_{THD} - 2.63} \quad k\Omega \tag{2}$$

$$V_{HYS} = 2.191 \left( \frac{1}{R_{THD}} + 0.283 \right) V \tag{3}$$

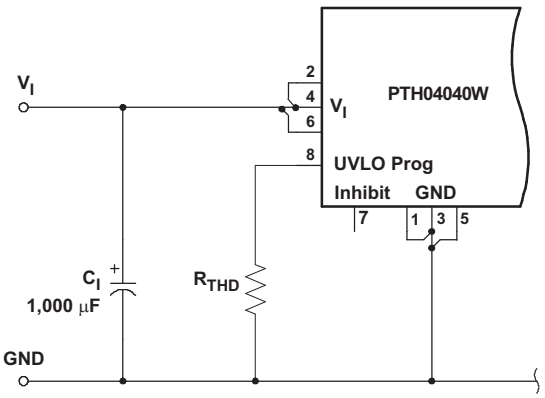



**Figure 10. UVLO Program Resistor Placement**

# FEATURES OF THE PTH FAMILY OF NONISOLATED WIDE OUTPUT ADJUST POWER MODULES

## POLA™ COMPATIBILITY

The PTH/PTV family of nonisolated, wide-output adjustable power modules are optimized for applications that require a flexible, high performance module that is small in size. Each of these products are POLA™ compatible. POLA-compatible products are produced by a number of manufacturers, and offer customers advanced, nonisolated modules with the same footprint and form factor. POLA parts are also assured to be interoperable, thereby providing customers with second-source availability.

Many of the POLA-compatible parts include a feature called Auto-Track™. Auto-Track was specifically designed to simplify the task of sequencing the supply voltages in a power system. This and other features are described the following sections.

## SOFT-START POWER UP

The Auto-Track feature allows the power-up of multiple PTH modules to be directly controlled from the *Track* pin. However in a stand-alone configuration, or when the Auto-Track feature is not being used, the *Track* pin should be directly connected to the input voltage, $V_{in}$ (see Figure 11).

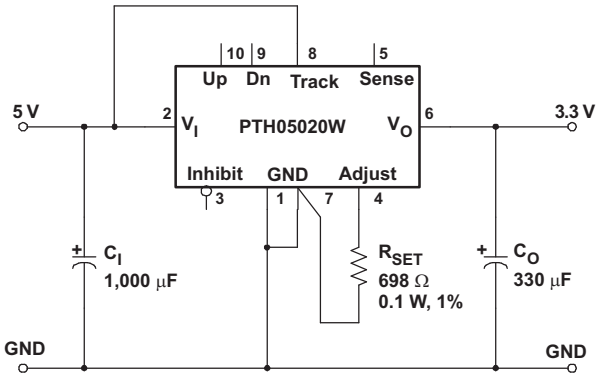



**Figure 11. Power-Up Application Circuit**

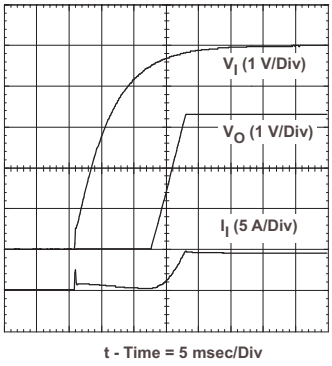



**Figure 12. Power-Up Waveforms**

When the *Track* pin is connected to the input voltage the Auto-Track function is permanently disengaged. This allows the module to power up entirely under the control of its internal soft-start circuitry. When power up is under soft-start control, the output voltage rises to the set-point at a quicker and more linear rate.

From the moment a valid input voltage is applied, the soft-start control introduces a short time delay (typically 5 ms–10 ms) before allowing the output voltage to rise. The output then progressively rises to the module's setpoint voltage. Figure 12 shows the soft-start power-up characteristic of the 22-A output product (PTH05020W), operating from a 5-V input bus and configured for a 3.3-V output. The waveforms were measured with a 5-A resistive load and the Auto-Track feature disabled. The initial rise in input current when the input voltage first starts to rise is the charge current drawn by the input capacitors. Power-up is complete within 15 ms.


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## OVERCURRENT PROTECTION

For protection against load faults, all modules incorporate output overcurrent protection. Applying a load that exceeds the regulator's overcurrent threshold causes the regulated output to shut down. Following shutdown, a module periodically attempts to recover by initiating a soft-start powerup. This is described as a *hiccup* mode of operation, whereby the module continues in a cycle of successive shutdown and power up until the load fault is removed. During this period, the average current flowing into the fault is significantly reduced. Once the fault is removed, the module automatically recovers and returns to normal operation.

## OVERTEMPERATURE PROTECTION (OTP)

Products with a high output current capability (>20 A), incorporate overtemperature protection. This feature is provided by an on-board temperature sensor that protects the module's internal circuitry against excessively high temperatures. A rise in the internal temperature may be the result of a drop in airflow, or a high ambient temperature. If the internal temperature exceeds the OTP threshold, the module's Inhibit control is automatically pulled low. This turns the output off. The output voltage drops as the external output capacitors are discharged by the load circuit. The recovery is automatic, and begins with a soft-start power up. It occurs when the sensed temperature decreases by about 10°C below the trip point.

*Note: The overtemperature protection is a last resort mechanism to prevent thermal stress to the regulator. Operation at or close to the thermal shutdown temperature is not recommended, and reduces the long-term reliability of the module. Always operate the regulator within the specified safe operating area (SOA) limits for the worst-case conditions of ambient temperature and airflow.*

## OUTPUT ON/OFF INHIBIT

For applications requiring output voltage on/off control, each series of the PTH family incorporates an output *Inhibit* control pin. The inhibit feature can be used wherever there is a requirement for the output voltage from the regulator to be turned off.

The power modules function normally when the Inhibit pin is left open-circuit, providing a regulated output whenever a valid source voltage is connected to $V_{in}$ with respect to *GND*.

Figure 13 shows the typical application of the inhibit function. Note the discrete transistor (Q1). The *Inhibit* control has its own internal pull-up to $V_I$ potential. The input is not compatible with TTL logic devices. An open-collector (or open-drain) discrete transistor is recommended for control.

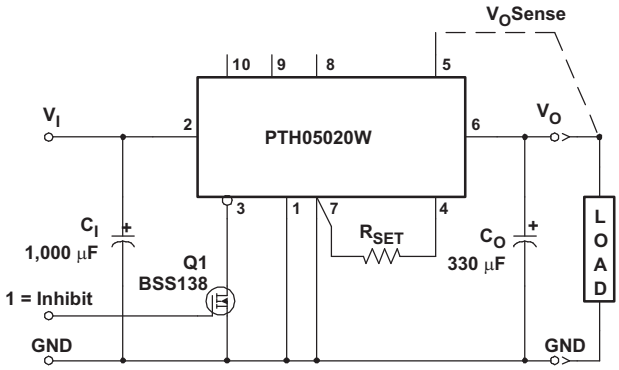



**Figure 13. Inhibit Control Circuit**

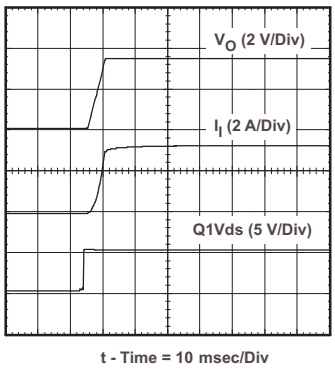



**Figure 14. Power-Up from Inhibit Control**

Turning Q1 on applies a low voltage to the *Inhibit* control and disables the output of the module. If Q1 is then turned off, the module executes a soft-start powerup. A regulated output voltage is produced within 20 ms. Figure 14 shows the typical rise in both the output voltage and input current, following the turn-off of Q1. The turn off of Q1 corresponds to the rise in the waveform, Q1 Vds. The waveforms were measured with a 5-A constant current load.

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## REMOTE SENSE

The remote sense feature allows the regulator to compensate for limited amounts of voltage drop, that may be incurred between the converter and load, due to resistance in the PCB traces. Connecting the *+Sense* and *–Sense* pins to the respective $V_O$ and *GND* output nodes improves the load regulation of the regulator output at those connection points. This is recommended even if the load circuit is located close to the module.

If either the *+Sense* and *–Sense* are left open-circuit, an internal low-value resistor (15-Ω or less), connected from the respective sense pin to either $V_O$ or *GND*, ensures the output voltage remains in regulation.

With the sense pins connected, the difference between the voltage measured across the $V_O$ and *GND* pins of the regulator, and that measured at *+Sense* with respect to *+Sense*, is the amount of IR drop being compensated by the regulator. This should be limited to a maximum of 0.3 V.

*Note: The remote sense feature is not designed to compensate for the forward drop of nonlinear or frequency dependent components that may be placed in series with the converter output. Examples include OR-ing diodes, filter inductors, ferrite beads, and fuses. When these components are enclosed by the remote sense connection they are effectively placed inside the regulation control loop, which can adversely affect the stability of the regulator.*

## Auto-Track™ FUNCTION

The Auto-Track function is unique to the PTH/PTV family, and is available with the all POLA-compatible products. Auto-Track was designed to simplify the amount of circuitry required to make the output voltage from each module power up and power down in sequence. The sequencing of two or more supply voltages during power up is a common requirement for complex mixed-signal applications, that use dual-voltage VLSI ICs such as the TMS320™ DSP family, micro-processors, and ASICs.

### *HOW Auto-Track WORKS*

Auto-Track works by forcing the module's output voltage to follow a voltage presented at the *Track* control pin. This control range is limited to between 0 V and the module's set-point voltage. Once the *Track* input is raised above the set-point voltage, the module's output remains at its set-point 1. As an example, if the *Track* pin of a 2.5-V regulator is at 1 V, the regulated output will be 1 V. But, if the voltage at the *Track* pin rises to 3 V, the regulated output does not go higher than 2.5 V.

When the *Track* input is used to connect a number of modules together, it forces the output voltage from each module to follow a common signal during power-up and power-down. The control signal can be an externally generated master ramp waveform, or the output voltage from another power supply circuit.(3) For convenience, each module's *Track* input incorporates an internal RC charge circuit. This operates off the module's input voltage to provide a suitable rising voltage ramp waveform.

### *TYPICAL Auto-Track APPLICATION*

Connecting the *Track* inputs of two or more modules forces their *Track* input to follow the same collective RC ramp waveform, and allows their power-up sequence to be coordinated from a common *Track* control signal. This can be an open-collector (or open drain) device, such as a power-up reset voltage supervisor IC.

To coordinate a power-up sequence the *Track* control must first pulled to ground potential. This should be done at or before input power is applied to the modules. The ground signal should be maintained for at least 10 ms after input power has been applied. This brief period gives the modules time to complete their internal soft-start initialization, enabling them to produce an output voltage. A low-cost supply voltage supervisor IC, that includes built-in time delay, is an ideal component for automatically controlling the *Track* inputs at power up.

Figure 17 shows how the TPS3808G50 supply voltage supervisor IC (U3) can be used to coordinate the sequenced power-up of two 5-V input Auto-Track modules. The output of the TPS3808 supervisor becomes active above an input voltage of 0.8 V, enabling it to assert a ground signal to the common *Track* control well before the input voltage has reached the module's undervoltage lockout threshold. The ground signal is maintained until approximately 27 ms after the input voltage has risen above U3's voltage threshold, which is 4.65 V. The 27-ms time period is controlled by the capacitor C3. The value of 4700 μF provides sufficient time delay for the modules to complete their internal soft-start initialization. The output voltage of each module remains at zero until the *Track* control voltage is allowed to rise. When U3 removes the ground signal, the *Track* control voltage automatically rises to the input voltage. This causes the output voltage of each module to rise simultaneously with the other modules, until each reaches its respective set-point voltage.


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Figure 15 shows the output voltage waveforms from the circuit of Figure 17 after input voltage is applied to the circuit. The waveforms, $V_O1$ and $V_O2$, represent the output voltages from the two power modules, U1 (3.3 V) and U2 (1.8 V), respectively. $V_{TRK}$, $V_O1$, and $V_O2$ are shown rising together to produce the desired simultaneous power-up characteristic.

The same circuit also provides a power-down sequence. When the input voltage falls below U3's voltage threshold, the ground signal is re-applied to the common *Track* control. This pulls the *Track* inputs to zero volts, forcing the output of each module to follow, as shown in Figure 16. In order for a simultaneous power-down to occur, the *Track* inputs must be pulled low before the input voltage has fallen below the modules' undervoltage lockout. This is an important constraint. Once the modules recognize that a valid input voltage is no longer present, their outputs can no longer follow the voltage applied at their *Track* input. During a power-down sequence, the fall in the output voltage from the modules is limited by the maximum output capacitance and the Auto-Track slew rate.

***NOTES ON USE OF Auto-Track***

1. The *Track* pin voltage must be allowed to rise above the module's set-point voltage before the module can regulate at its adjusted set-point voltage.
2. The Auto-Track function tracks almost any voltage ramp during power up, and is compatible with ramp speeds of up to 1 V/ms.
3. The absolute maximum voltage that may be applied to the *Track* pin is $V_I$.
4. The module does not follow a voltage at its *Track* input until it has completed its soft-start initialization. This takes at least 10 ms from the time that the module has sensed that a valid voltage is present. During this period, the *Track* input should be held at ground potential.
5. The module is capable of both sinking and sourcing current when following a voltage at its *Track* input. Therefore startup into an output prebias is not supported when the module is under Auto-Track control. Prebias hold off is not necessary when all supply voltages simultaneously under the control of Auto-Track.
6. The Auto-Track function can be disabled by connecting the *Track* pin to the input voltage ($V_I$). With Auto-Track disabled, the output voltage rises at a quicker and more linear rate after input power is applied.

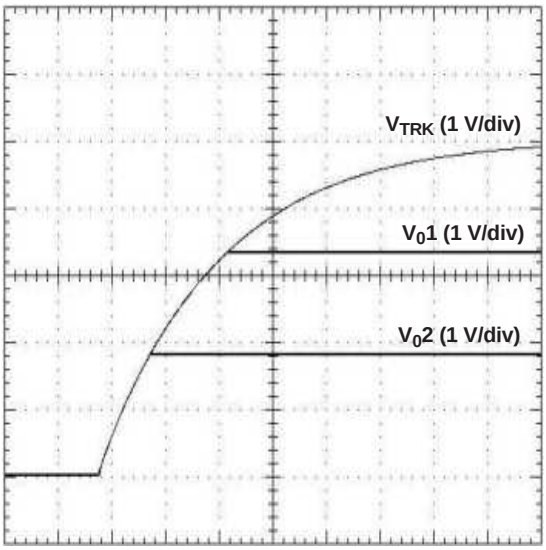



**Figure 15. Auto-Track Simultaneous Power Up Waveforms**

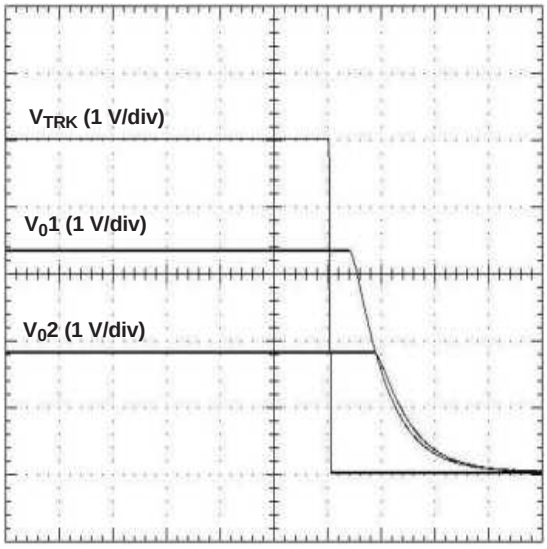



**Figure 16. Auto-Track Simultaneous Power Down Waveforms**

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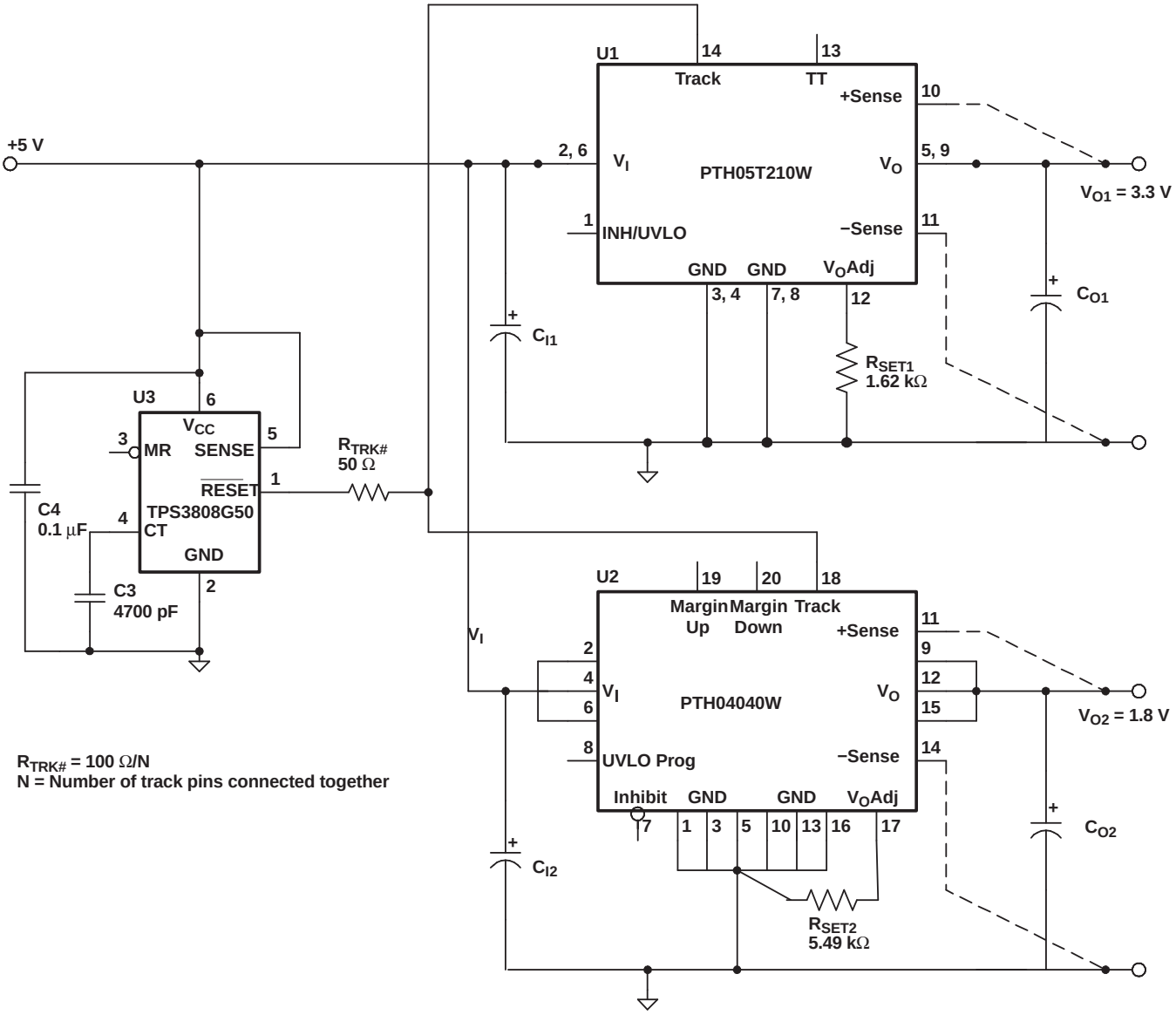



**Figure 17. Sequenced Power Up and Power Down using Auto-Track**


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## MARGIN UP/DOWN CONTROLS

The PTHxx060, PTHxx010, PTHxx020, and PTHxx030 products incorporate *Margin Up* and *Margin Down* control inputs. These controls allow the output voltage to be momentarily adjusted(1), either up or down, by a nominal 5%. This provides a convenient method for dynamically testing the operation of the load circuit over its supply margin or range. It can also be used to verify the function of supply voltage supervisors. The ±5% change is applied to the adjusted output voltage, as set by the external resistor, $R_{set}$ at the *$V_o$ Adjust* pin.

The 5% adjustment is made by pulling the appropriate margin control input directly to the GND terminal 2. A low-leakage open-drain device, such as an n-channel MOSFET or p-channel JFET is recommended for this purpose(3). Adjustments of less than 5% can also be accommodated by adding series resistors to the control inputs. The value of the resistor can be selected from Table 4, or calculated using the following formula.

### *UP/DOWN ADJUST RESISTANCE CALCULATION*

$$R_U \text{ or } R_D = \frac{499}{\Delta\,\%} - 99.8\ k\Omega \quad (4)$$

Where Δ% = The desired amount of margin adjusted in percent.

### *NOTES*

1. The *Margin Up* and *Margin Down* controls were not intended to be activated simultaneously. If they are activated simultaneously, the effects on the output voltage may not completely cancel, resulting in the possibility of a higher error in the output voltage set point.
2. The ground reference should be a direct connection to the module *GND* at pin 7 (pin 1 for the PTHxx050). This produces a more accurate adjustment at the load circuit terminals. The transistors Q1 and Q2 should be located close to the regulator.
3. The Margin Up and Margin Down control inputs are not compatible with devices that source voltage. This includes TTL logic. These are analog inputs and should only be controlled with a true open-drain device (preferably discrete MOSFET transistor). The device selected should have low off-state leakage current. Each input sources 8 µA when grounded, and has an open-circuit voltage of 0.8 V.

**Table 4. Margin Up/Down Resistor Values**

| % ADJUST | 5% | 4% | 3% | 2% | 1% |
|---|---|---|---|---|---|
| $R_U$ / $R_D$ | 0 kΩ | 24.9 kΩ | 66.5 kΩ | 150.0 kΩ | 397.0 kΩ |

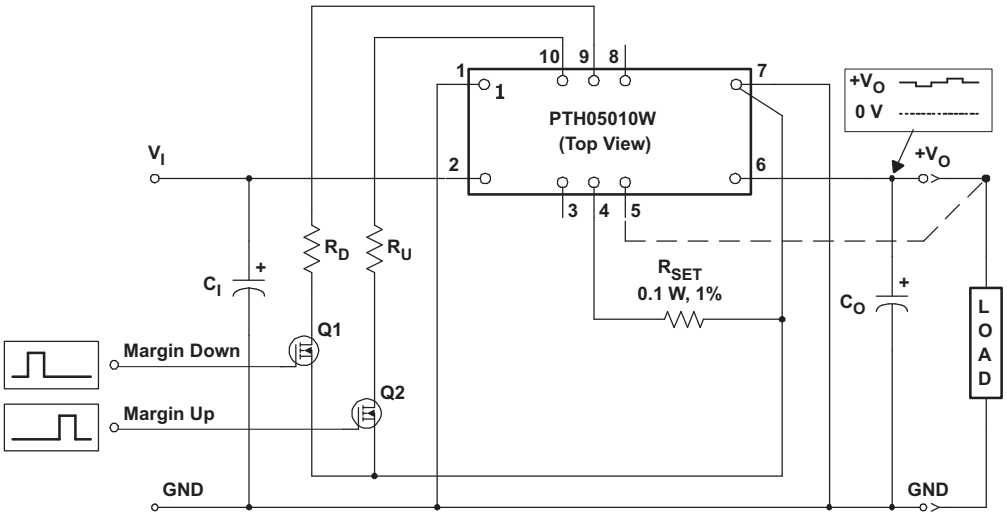



**Figure 18. Margin Up/Down Application Schematic**

## PREBIAS STARTUP CAPABILITY

A prebias startup condition occurs as a result of an external voltage being present at the output of a power module prior to its output becoming active. This often occurs in complex digital systems when current from another power source is backfed through a dual-supply logic component, such as an FPGA or ASIC. Another path might be via clamp diodes as part of a dual-supply power-up sequencing arrangement. A prebias can cause problems with power modules that incorporate synchronous rectifiers. This is because under most operating conditions, these types of modules can sink as well as source output current.

The PTH/PTV family of power modules incorporate synchronous rectifiers, but does not sink current during startup(1), or whenever the Inhibit pin is held low. However, to ensure satisfactory operation of this function, certain conditions must be maintained(2). Figure 19 shows an application demonstrating the prebias startup capability. The start-up waveforms are shown in Figure 20. Note that the output current from the PTH03010W ($I_o$) shows negligible current until its output voltage rises above that backfed through diodes D1 and D2.

*Note: The prebias start-up feature is not compatible with Auto-Track. When the module is under Auto-Track control, it sinks current if the output voltage is below that of a back-feeding source. To ensure a prebias hold-off, one of two approaches must be followed when input power is applied to the module. The Auto-Track function must be disabled(3), or the module's output held off (for at least 50 ms) using the Inhibit pin. Either approach ensures that the Track pin voltage is above the set-point voltage at start up.*

### *NOTES*

1. Startup includes the short delay (approximately 10 ms) prior to the output voltage rising, followed by the rise of the output voltage under the module's internal soft-start control. Startup is complete when the output voltage has risen to either the set-point voltage or the voltage at the *Track* pin, whichever is lowest.
2. To ensure that the regulator does not sink current when power is first applied (even with a ground signal applied to the *Inhibit* control pin), the input voltage *must* always be greater than the output voltage *throughout* the powerup and power-down sequence.
3. The Auto-Track function can be disabled at power up by immediately applying a voltage to the module's *Track* pin that is greater than its set-point voltage. This can be easily accomplished by connecting the *Track* pin to $V_{in}$.

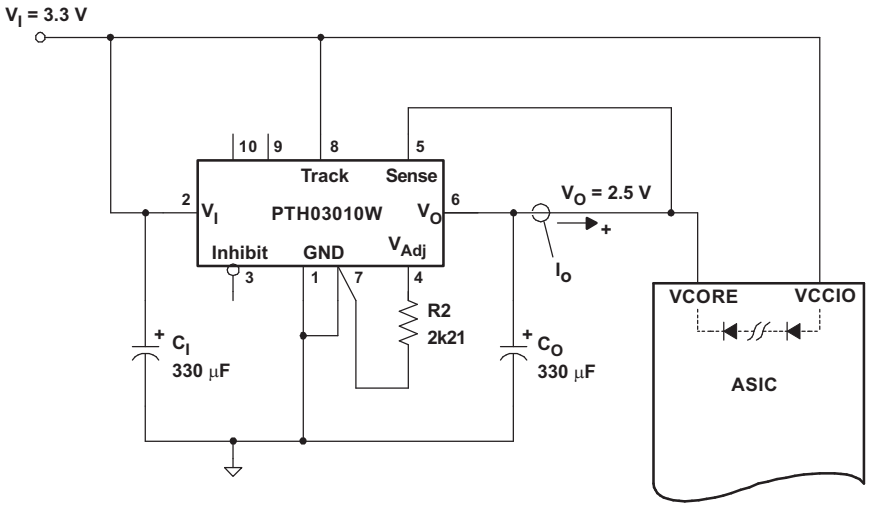



**Figure 19. Application Circuit Demonstrating Prebias Startup**


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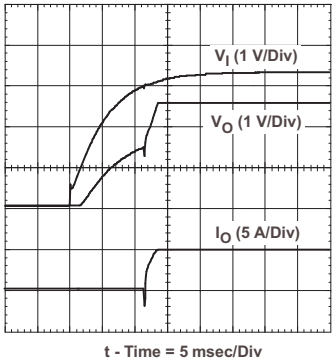



**Figure 20. Pre-Bias Startup Waveforms**

## REVISION HISTORY

| Changes from Revision B (JULY 2009) to Revision C | Page |
|---|---|
| • Changed from: "input" to: "output" | 2 |


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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| PTH04040WAD | Active | Production | Through-Hole Module (EVF) \| 20 | 12 \| TIW TRAY | Exempt | SN | N/A for Pkg Type | -40 to 85 | |
| PTH04040WAD.B | Active | Production | Through-Hole Module (EVF) \| 20 | 12 \| TIW TRAY | Exempt | SN | N/A for Pkg Type | -40 to 85 | |
| PTH04040WAH | Active | Production | Through-Hole Module (EVF) \| 20 | 12 \| TIW TRAY | Exempt | SN | Level-1-235C-UNLIM | -40 to 85 | |
| PTH04040WAH.B | Active | Production | Through-Hole Module (EVF) \| 20 | 12 \| TIW TRAY | Exempt | SN | Level-1-235C-UNLIM | -40 to 85 | |
| PTH04040WAS | Active | Production | Surface Mount Module (EVG) \| 20 | 12 \| TIW TRAY | No | SNPB | Level-1-235C-UNLIM/ Level-3-260C-168HRS | -40 to 85 | |
| PTH04040WAS.B | Active | Production | Surface Mount Module (EVG) \| 20 | 12 \| TIW TRAY | No | SNPB | Level-1-235C-UNLIM/ Level-3-260C-168HRS | -40 to 85 | |
| PTH04040WAZ | Active | Production | Surface Mount Module (EVG) \| 20 | 12 \| TIW TRAY | Exempt | SNAGCU | Level-3-260C-168 HR | -40 to 85 | |
| PTH04040WAZ.B | Active | Production | Surface Mount Module (EVG) \| 20 | 12 \| TIW TRAY | Exempt | SNAGCU | Level-3-260C-168 HR | -40 to 85 | |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

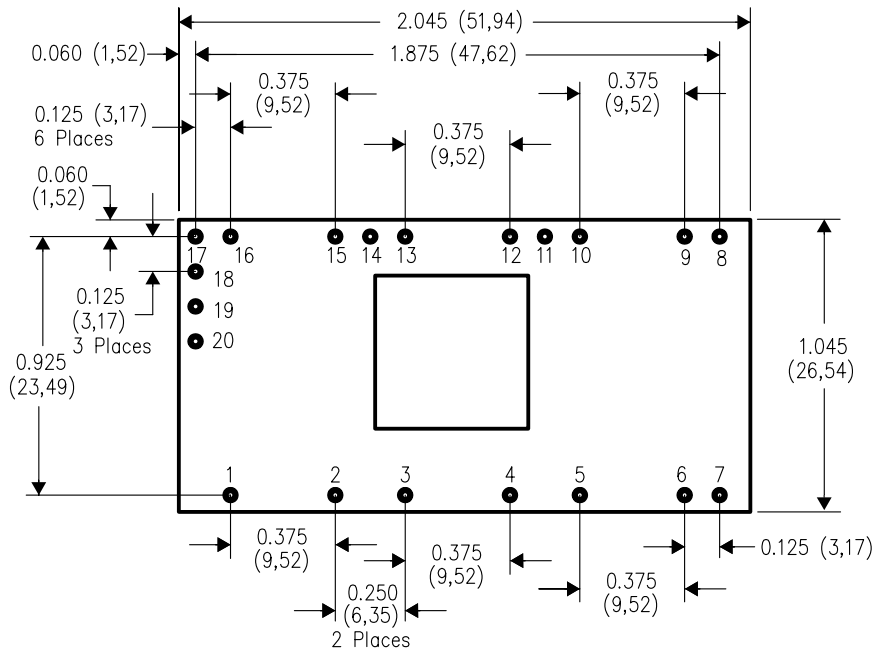
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

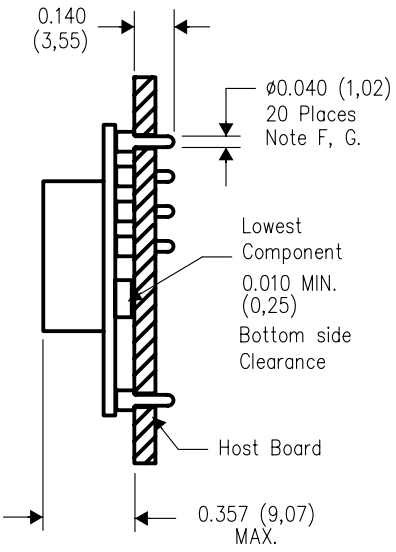
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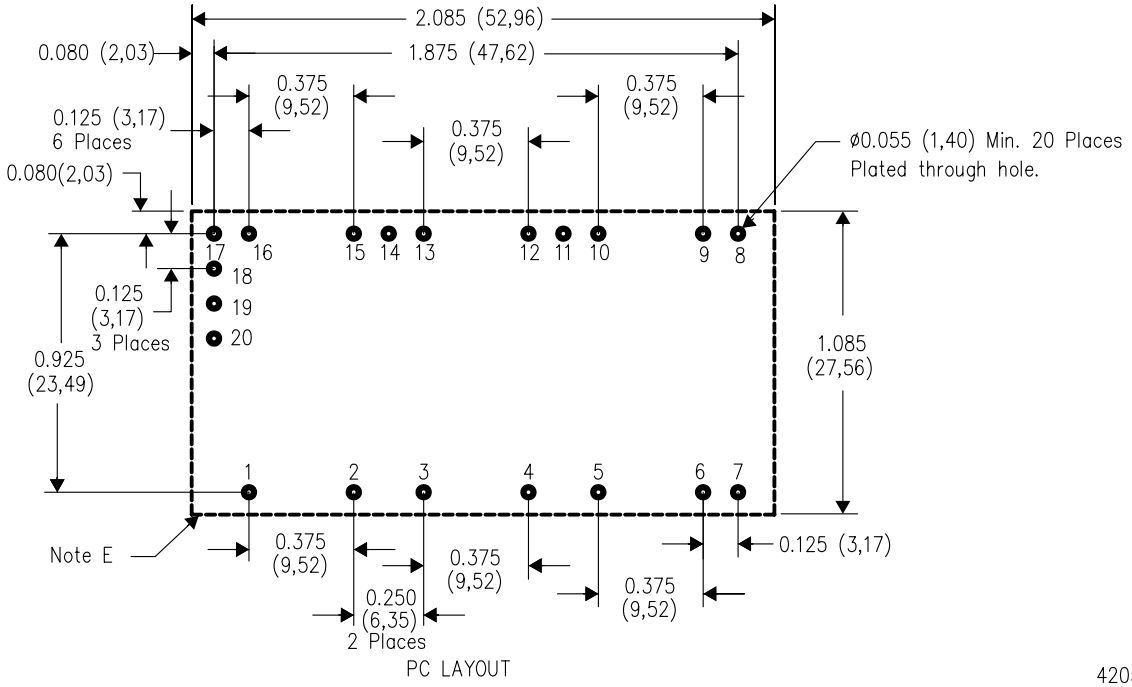
## EVF (R–PDSS–T20) DOUBLE SIDED MODULE




TOP VIEW




SIDE VIEW

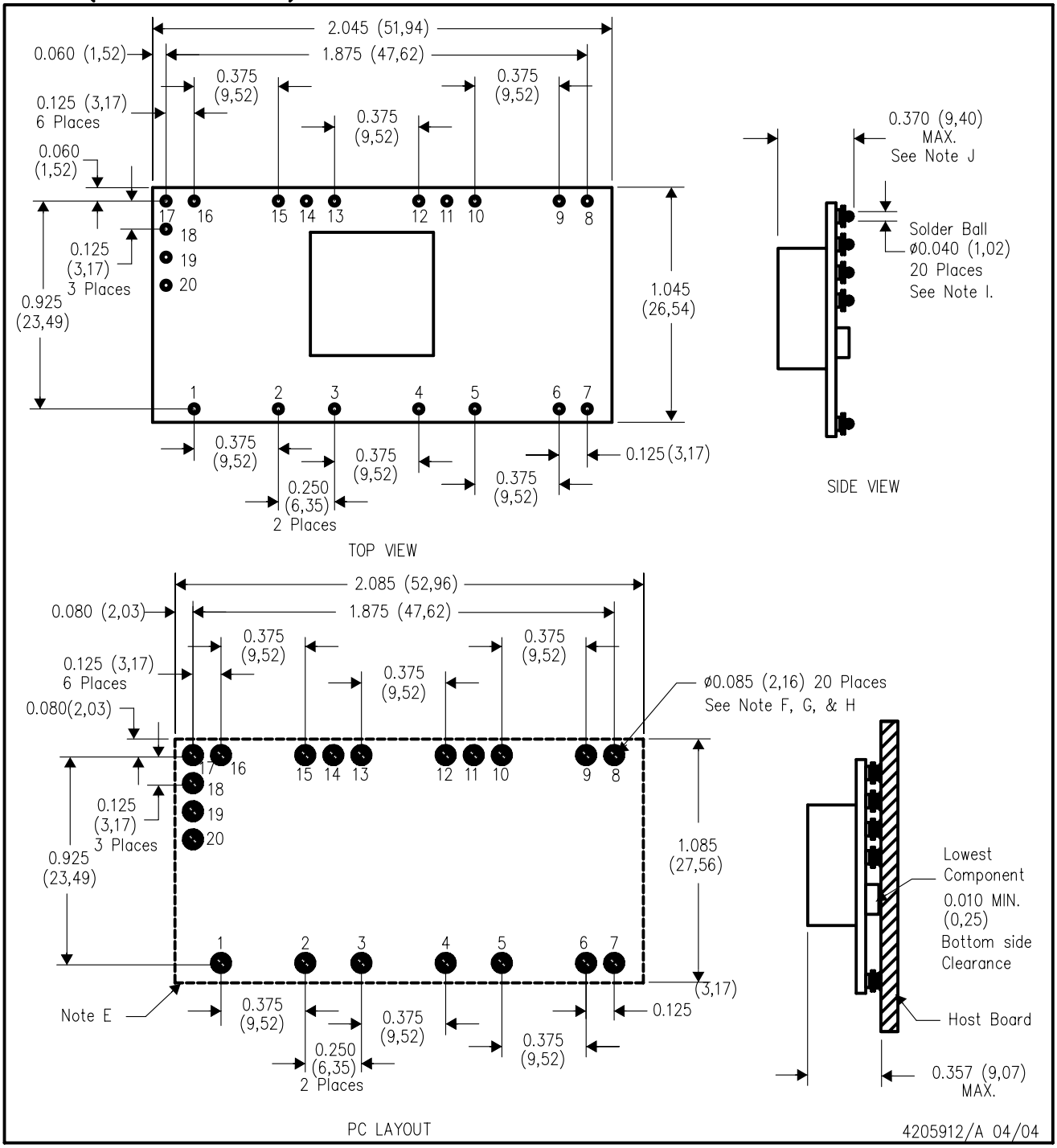



PC LAYOUT

4205911/A 04/04

NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Pins are 0.040" (1,02) diameter with 0.070" (1,78) diameter standoff shoulder.
G. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate

## EVG (R–PDSS–T20) DOUBLE SIDED MODULE




NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Power pin connection should utilize four or more vias to the interior power plane of 0.025 (0,63) I.D. per input, ground and output pin (or the electrical equivalent).
G. Paste screen opening: 0.080 (2,03) to 0.085 (2,16). Paste screen thickness: 0.006 (0,15).
H. Pad type: Solder mask defined.
I. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate
Solder Ball – See product data sheet.
J. Dimension prior to reflow solder.

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Last updated 10/2025