POLA Point-of-Load Alliance

30-A, 5-V Input Non-Isolated
Wide-Output Adjust Power Modules

SLTS210B – MAY 2003 – REVISED JANUARY 2004



**NOMINAL SIZE = 1.37 in x 1.12 in (34,8 mm x 28,5 mm)**

## Features

- Up to 30 A Output Current
- 5-V Input Voltage
- Wide-Output Voltage Adjust (0.8 V to 3.6 V)
- 180 W/in³ Power Density
- On/Off Inhibit
- Efficiencies up to 94 %
- Pre-Bias Startup
- Margin Up/Down Controls
- Under-Voltage Lockout
- Auto-Track™ Sequencing
- Output Over-Current Protection (Non-Latching, Auto-Reset)
- Over-Temperature Protection
- Operating Temp: –40 to +85 °C
- Safety Agency Approvals: UL 1950, CSA 22.2 950, EN60950 VDE (Pending)
- Point-of-Load Alliance (POLA) Compatible

## Description

The PTH05030 is a series of high-current non-isolated power modules from Texas Instruments. This product is characterized by high efficiencies, and up to 30 A of output current, while occupying a mere 1.64 in² of PCB area. In terms of cost, size, and performance, the series provides OEM's with a flexible module that meets the requirements of the most complex and demanding mixed-signal applications. These include the most densly populated, multi-processor systems that incorporate high-speed DSP's, microprocessors, and ASICs.

The series uses double-sided surface mount construction and provides high-performance step-down power conversion from a 5-V input bus voltage. The output voltage of the PTH05030W can be set to any value over the range 0.8 V to 3.6 V, using a single resistor.

This series includes Auto-Track™. Auto-Track simplifies power-up and power-down supply voltage sequencing in a system by enabling modules to track each other, or any other external voltage.

Each model also includes an on/off inhibit, output voltage adjust (trim), and margin up/down controls. An output voltage sense ensures tight load regulation, and an output over-current and thermal shutdown feature provide for protection against external load faults.

Package options inlude both through-hole and surface mount configurations.

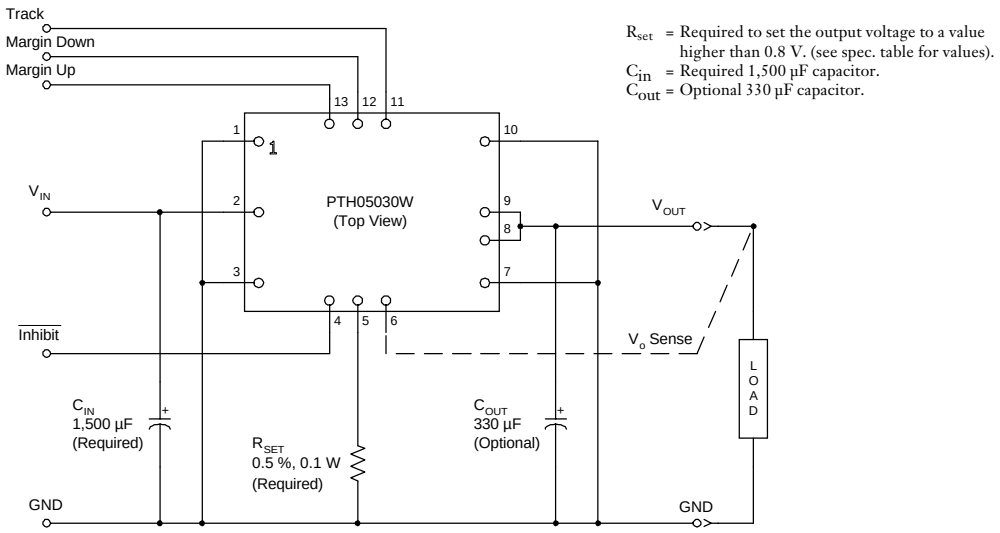
## Pin Configuration

| Pin | Function |
|---|---|
| 1 | GND |
| 2 | $V_{in}$ |
| 3 | GND |
| 4 | Inhibit * |
| 5 | $V_o$ Adjust |
| 6 | $V_o$ Sense |
| 7 | GND |
| 8 | $V_{out}$ |
| 9 | $V_{out}$ |
| 10 | GND |
| 11 | Track |
| 12 | Margin Down * |
| 13 | Margin Up * |

* *Denotes negative logic:*
*Open = Normal operation*
*Ground = Function active*

**Auto-Track™ Sequencing**

## Standard Application




$R_{set}$ = Required to set the output voltage to a value higher than 0.8 V. (see spec. table for values).
$C_{in}$ = Required 1,500 µF capacitor.
$C_{out}$ = Optional 330 µF capacitor.

## Ordering Information

**Output Voltage (PTH05030❒xx)**

| Code | Voltage |
|---|---|
| W | 0.8 V – 3.6 V (Adjust) |

**Package Options (PTH05030x❒❒)** (1)

| Code | Description | Pkg Ref. (2) |
|---|---|---|
| AH | Horiz. T/H | (EUM) |
| AS | SMD, Standard (3) | (EUN) |

**Notes:** *(1) Add "T" to end of part number for tape and reel on SMD packages only.*
*(2) Reference the applicable package reference drawing for the dimensions and PC board layout*
*(3) "Standard" option specifies 63/37, Sn/Pb pin solder material.*

## Pin Descriptions

**Vin:** The positive input voltage power node to the module, which is referenced to common *GND*.

**Vout:** The regulated positive power output with respect to the *GND* node.

**GND:** This is the common ground connection for the *Vin* and *Vout* power connections. It is also the 0 VDC reference for the control inputs.

**Inhibit:** The Inhibit pin is an open-collector/drain negative logic input that is referenced to *GND*. Applying a low-level ground signal to this input disables the module's output and turns off the output voltage. When the *Inhibit* control is active, the input current drawn by the regulator is significantly reduced. If the *Inhibit* pin is left open-circuit, the module will produce an output whenever a valid input source is applied.

**Vo Adjust:** A 0.1 W 1 % resistor must be directly connected between this pin and pin 7 (*GND*) to set the output voltage to a value higher than 0.8 V. The temperature stability of the resistor should be 100 ppm/°C (or better). The set point range for the output voltage is from 0.8 V to 3.6 V. The resistor value required for a given output voltage may be calculated from the following formula. If left open circuit, the output voltage will default to its lowest value. For further information on output voltage adjustment consult the related application note.

$$R_{set} = 10\text{ k} \cdot \frac{0.8\text{ V}}{V_{out} - 0.8\text{ V}} - 2.49\text{ k}$$

The specification table gives the preferred resistor values for a number of standard output voltages.

**Vo Sense:** The sense input allows the regulation circuit to compensate for voltage drop between the module and the load. For optimal voltage accuracy *Vo Sense* should be connected to *Vout*. It can also be left disconnected.

**Track:** This is an analog control input that enables the output voltage to follow an external voltage. This pin becomes active typically 20 ms after the input voltage has been applied, and allows direct control of the output voltage from 0 V up to the nominal set-point voltage. Within this range the output will follow the voltage at the *Track* pin on a volt-for-volt basis. When the control voltage is raised above this range, the module regulates at its set-point voltage. The feature allows the output voltage to rise simultaneously with other modules powered from the same input bus. If unused, this input should be connected to $V_{in}$. *Note: Due to the under-voltage lockout feature, the output of the module cannot follow its own input voltage during power up. For more information, consult the related application note.*

**Margin Down:** When this input is asserted to *GND*, the output voltage is decreased by 5% from the nominal. The input requires an open-collector (open-drain) interface. It is not TTL compatible. A lower percent change can be accomodated with a series resistor. For further information, consult the related application note.

**Margin Up:** When this input is asserted to *GND*, the output voltage is increased by 5%. The input requires an open-collector (open-drain) interface. It is not TTL compatible. The percent change can be reduced with a series resistor. For further information, consult the related application note.

## Environmental & Absolute Maximum Ratings (Voltages are with respect to GND)

| Characteristics | Symbols | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Track Input Voltage | $V_{track}$ | | –0.3 | — | $V_{in}$ + 0.3 | V |
| Operating Temperature Range | $T_a$ | Over $V_{in}$ Range | –40 | — | 85 | °C |
| Solder Reflow Temperature | $T_{reflow}$ | Surface temperature of module body or pins | | | 235 (i) | °C |
| Storage Temperature | $T_s$ | — | –40 | — | 125 | °C |
| Mechanical Shock | | Per Mil-STD-883D, Method 2002.3<br>1 msec, ½ Sine, mounted | — | 500 | — | G's |
| Mechanical Vibration | | Mil-STD-883D, Method 2007.2 Suffix S<br>20-2000 Hz Suffix H | —<br>— | 10<br>20 | —<br>— | G's |
| Weight | — | | — | 10 | — | grams |
| Flammability | — | Meets UL 94V-O | | | | |

**Notes:** *(i) During reflow of SMD package version do not elevate peak temperature of the module, pins or internal components above the stated maximum.*

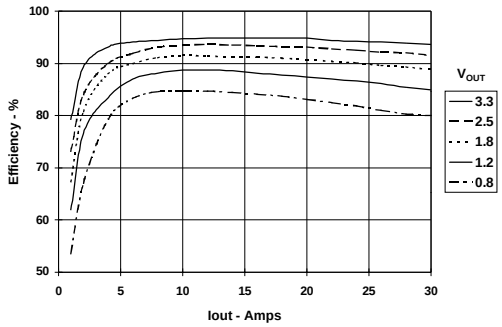
## Specifications (Unless otherwise stated, $T_a$ =25 °C, $V_{in}$ =5 V, $V_{out}$ =3.3 V, $C_{in}$ =1,500 µF, $C_{out}$ =0 µF, and $I_o$ =$I_o$ max)

| Characteristics | Symbols | Conditions | PTH05030W Min | PTH05030W Typ | PTH05030W Max | Units |
|---|---|---|---|---|---|---|
| Output Current | $I_o$ | 60 °C, 200 LFM airflow<br>25 °C, natural convection | 0<br>0 | —<br>— | 30 (1)<br>30 (1) | A |
| Input Voltage Range | $V_{in}$ | Over $I_o$ range | 4.5 | — | 5.5 | V |
| Set-Point Voltage Tolerance | $V_o$ tol | | — | — | ±2 (2) | %$V_o$ |
| Temperature Variation | $\Delta Reg_{temp}$ | –40 °C <$T_a$ < +85 °C | — | ±0.5 | — | %$V_o$ |
| Line Regulation | $\Delta Reg_{line}$ | Over $V_{in}$ range | — | ±10 | — | mV |
| Load Regulation | $\Delta Reg_{load}$ | Over $I_o$ range | — | ±12 | — | mV |
| Total Output Variation | $\Delta Reg_{tot}$ | Includes set-point, line, load,<br>–40 °C ≤ $T_a$ ≤ +85 °C | — | — | ±3 | %$V_o$ |
| Efficiency | η | $I_o$ =20 A $R_{SET}$ = 698 Ω $V_o$ = 3.3 V<br>$R_{SET}$ = 2.21 kΩ $V_o$ = 2.5 V<br>$R_{SET}$ = 5.49 kΩ $V_o$ = 1.8 V<br>$R_{SET}$ = 8.87 kΩ $V_o$ = 1.5 V<br>$R_{SET}$ = 17.4 kΩ $V_o$ = 1.2 V<br>$R_{SET}$ = 36.5 kΩ $V_o$ = 1.0 V | —<br>—<br>—<br>—<br>—<br>— | 94<br>93<br>90<br>89<br>87<br>86 | —<br>—<br>—<br>—<br>—<br>— | % |
| $V_o$ Ripple (pk-pk) | $V_r$ | 20 MHz bandwidth | — | 40 | — | mVpp |
| Over-Current Threshold | $I_o$ trip | Reset, followed by auto-recovery | — | 47 | — | A |
| Transient Response | $t_{tr}$<br>$\Delta V_{tr}$ | 1 A/µs load step, 50 to 100 % $I_o$max,<br>$C_{out}$ =330 µF<br>Recovery Time<br>$V_o$ over/undershoot | —<br>— | 70<br>100 | —<br>— | µSec<br>mV |
| Margin Up/Down Adjust | $V_o$ adj | | — | ± 5 | — | % |
| Margin Input Current (pins 12 /13) | $I_{IL}$ margin | Pin to GND | — | – 8 (3) | — | µA |
| Track Input Current (pin 11) | $I_{IL}$ track | Pin to GND | — | — | –130 (4) | µA |
| Track Slew Rate Capability | $dV_{track}/dt$ | $C_{out}$ ≤ $C_{out}$(max) | — | — | 1 | V/ms |
| Under-Voltage Lockout | UVLO | $V_{in}$ increasing<br>$V_{in}$ decreasing | —<br>3.4 | 4.3<br>3.7 | 4.45<br>— | V |
| Inhibit Control (pin4)<br>Input High Voltage<br>Input Low Voltage<br>Input Low Current | <br>$V_{IH}$<br>$V_{IL}$<br>$I_{IL}$ inhibit | Referenced to GND<br><br><br>Pin to GND | <br>$V_{in}$ –0.5<br>–0.2<br>— | <br>—<br>—<br>–130 | <br>Open (4)<br>0.8<br>— | V<br><br><br>µA |
| Input Standby Current | $I_{in}$ inh | Inhibit (pin 4) to GND, Track (pin 11) open | — | 10 | — | mA |
| Switching Frequency | $f_s$ | Over $V_{in}$ and $I_o$ ranges | 275 | 300 | 235 | kHz |
| External Input Capacitance | $C_{in}$ | | 1,500 (5) | — | — | µF |
| External Output Capacitance | $C_{out}$ | Capacitance value non-ceramic<br>ceramic<br>Equiv. series resistance (non-ceramic) | 0<br>0<br>4 (8) | 330 (6)<br>—<br>— | 16,500 (7)<br>300<br>— | µF<br><br>mΩ |
| Reliability | MTBF | Per Bellcore TR-332<br>50 % stress, $T_a$ =40 °C, ground benign | 2.8 | — | — | $10^6$ Hrs |

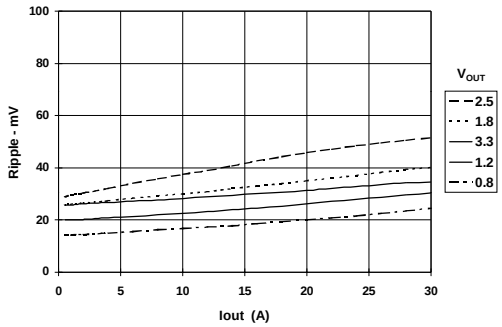
**Notes:** *(1) See SOA curves or consult factory for appropriate derating.*
*(2) The set-point voltage tolerlance is affected by the tolerance and stability of $R_{SET}$. The stated limit is unconditionally met if $R_{SET}$ has a tolerance of 1 % with 100 ppm/°C or better temperature stability.*
*(3) A small low-leakage (<100 nA) MOSFET is recommended to control this pin. The open-circuit voltage is less than 1 Vdc.*
*(4) This control pin has an internal pull-up to the input voltage Vin. If it is left open-circuit the module will operate when input power is applied. A small low-leakage (<100 nA) MOSFET is recommended for control. For further information, consult the related application note.*
*(5) A 1,500 µF electrolytic input capacitor is required for proper operation. The capacitor must be rated for a minimum of 900 mA rms of ripple current.*
*(6) An external output capacitor is not required for basic operation. Adding 330 µF of distributed capacitance at the load will improve the transient response.*
*(7) This is the calculated maximum. The minimum ESR limitation will often result in a lower value. Consult the application notes for further guidance.*
*(8) This is the typical ESR for all the electrolytic (non-ceramic) output capacitance. Use 7 mΩ as the minimum when using max-ESR values to calculate.*

## Characteristic Data; $V_{in}$ =5 V *(See Note A)*

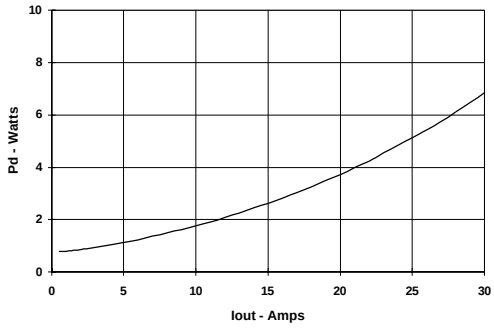
### Efficiency vs Load Current




### Output Ripple vs Load Current

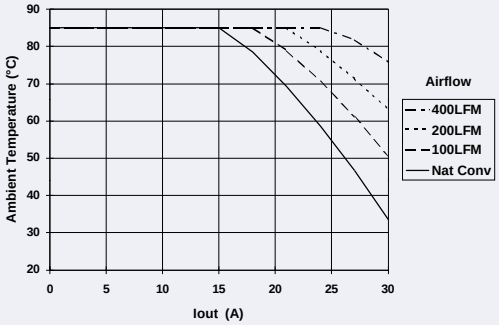



### Power Dissipation vs Load Current




## Safe Operating Area; $V_{in}$ =5 V *(See Note B)*

### All Output Voltages




**Note A:** *Characteristic data has been developed from actual products tested at 25°C. This data is considered typical data for the Converter.*
**Note B:** *SOA curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 4 in. × 4 in. double-sided PCB with 1 oz. copper.*

# Capacitor Recommendations for the PTH03030 & PTH05030 Series of Power Modules

### Input Capacitor

The recommended input capacitor(s) is determined by the 1,500 µF [(1)] minimum capacitance and 900 mArms minimum ripple current rating.

Ripple current and <100 mΩ equivalent series resistance (ESR) values are the major considerations, along with temperature, when designing with different types of capacitors. Unlike polymer tantalum, conventional tantalum capacitors have a recommended minimum voltage rating of 2 × (maximum DC voltage + AC ripple). This is standard practice to ensure reliability.

For improved ripple reduction on the input bus, ceramic capacitors may be used to complement electrolytic types and achieve the minimum required capacitance.

### Output Capacitors (Optional)

For applications with load transients (sudden changes in load current), regulator response will benefit from an external output capacitance. The recommended output capacitance of 330 µF will allow the module to meet its transient response specification (see product data sheet). For most applications, a high quality computer-grade aluminum electrolytic capacitor is most suitable. These capacitors provide adequate decoupling over the frequency range, 2 kHz to 150 kHz, and are suitable when ambient temperatures are above 0 °C. For operation below 0 °C, tantalum, ceramic or Os-Con type capacitors are recommended. When using one or more non-ceramic capacitors, the calculated equivalent ESR should be no lower than 4 mΩ (7 mΩ using the manufacturer's maximum ESR for a single capacitor). A list of preferred low-ESR type capacitors are identified in Table 1-1.

### Ceramic Capacitors

Above 150 kHz the performance of aluminum electrolytic capacitors becomes less effective. To further improve the reflected input ripple current or the output transient response, multilayer ceramic capacitors can also be added. Ceramic capacitors have very low ESR and their resonant frequency is higher than the bandwidth of the regulator. When used on the output their combined ESR is not critical as long as the total value of ceramic capacitance does not exceed 300 µF. Also, to prevent the formation of local resonances, do not place more than five identical ceramic capacitors in parallel with values of 10 µF or greater.

### Tantalum Capacitors

Tantalum type capacitors can be used at both the input and output, and are recommended for applications where the ambient operating temperature can be less than 0 °C. The AVX TPS, Sprague 593D/594/595 and Kemet T495/T510 capacitor series are suggested over many other tantalum types due to their higher rated surge, power dissipation, and ripple current capability. As a caution many general purpose tantalum capacitors have considerably higher ESR, reduced power dissipation and lower ripple current capability. These capacitors are also less reliable when determining their power dissipation and surge current capability. Tantalum capacitors that do not have a stated ESR or surge current rating are not recommended for power applications.

When specifying Os-Con and polymer tantalum capacitors for the output, the minimum ESR limit will be encountered well before the maximum capacitance value is reached.

### Capacitor Table

Table 1-1 identifies the characteristics of capacitors from a number of vendors with acceptable ESR and ripple current (rms) ratings. The recommended number of capacitors required at both the input and output buses is identified for each capacitor type.

*This is not an extensive capacitor list. Capacitors from other vendors are available with comparable specifications. Those listed are for guidance. The RMS ripple current rating and ESR (at 100kHz) are critical parameters necessary to insure both optimum regulator performance and long capacitor life.*

### Designing for Very Fast Load Transients

The transient response of the DC/DC converter has been characterized using a load transient with a di/dt of 1 A/µs. The typical voltage deviation for this load transient is given in the data sheet specification table using the optional value of output capacitance. As the di/dt of a transient is increased, the response of a converter's regulation circuit ultimately depends on its output capacitor decoupling network. This is an inherent limitation with any DC/DC converter once the speed of the transient exceeds its bandwidth capability. If the target application specifies a higher di/dt or lower voltage deviation, the requirement can only be met with additional output capacitor decoupling. In these cases special attention must be paid to the type, value and ESR of the capacitors selected.

If the transient performance requirements exceed that specified in the data sheet, or the total amount of load capacitance is above 3,000 µF, the selection of output capacitors becomes more important. For further guidance consult the separate application note, "*Selecting Capacitors for PTH Products in High-Performance Applications.*"

***Table 1-1: Input/Output Capacitors***

| Capacitor Vendor, Type: Series (Style) | Capacitor Characteristics | | | | | Quantity | | |
|---|---|---|---|---|---|---|---|---|
| | Working Voltage | Value (µF) | Max. ESR at 100 kHz | Max. Ripple Current @85 °C (I rms) | Physical Size (mm) | Input Bus | Output Bus | Vendor Part Number |
| Panasonic: | | | | | | | | |
| FC (Radial) | 10 V | 560 | 0.090 Ω | >900 mA | 10×12.5 | 3 | 1 | EEUFC1A561 |
| | 16 V | 1500 | 0.043 Ω | 1690 mA | 16×15 | 1 | 1 | EEUFC1C152S |
| FK (SMD) | 16 V | 1500 | 0.060 Ω | 1100 mA | 12.5×13.5 | 1 | 1 | EEVFK1C152Q |
| | 10 V | 2200 | 0.060 Ω | 1100 mA | 12.5×13.5 | 1 | 1 | EEVFK1A222Q |
| United Chemi-con | | | | | | | | |
| FX, Oscon (Radial) | 6.3 V | 1000 | 0.013 Ω | 4935 mA | 10×10.5 | 2 | ≤2 | 6FX1000M |
| PXA, (Poly-Aluminum (SMD.) | 6.3 V | 820 | 0.010 Ω | 5500 mA | 10×12.2 | 2 | ≤2 | PXA6.3VC820MJ12TP |
| LXZ, Aluminum (Radial) | 10 V | 680 | 0.090 Ω | >900 mA | 10×12.5 | 3 | 1 | LXZ10VB681M10X12LL |
| | 10 V | 1000 | 0.068 Ω | 1050 mA | 10×16 | 2 | 1 | LXZ10VB102M10X16LL |
| Nichicon, Aluminum: | | | | | | | | |
| HD (Radial) | 6.3 V | 1000 | 0.053 Ω | 1030 mA | 10×12.5 | 2 | 1 | UHD0J102MPR |
| PM (Radial) | 10 V | 1500 | 0.050 Ω | 1060 mA | 16×15 | 1 | 1 | UPM1A152MHH6 |
| Sanyo, Os-con: | | | | | | | | |
| SP (Radial) | 10 V | 470 | 0.015 Ω | >4500 mA | 10×10.5 | 3 [1] | ≤3 | 10SP470M |
| SVP (SMD) | 6.3 V | 820 | 0.012 Ω | >5440 mA | 10×12.7 | 2 | ≤2 | 6SVP820M |
| Panasonic, Poly-Aluminum: | | | | | | | | |
| WA (SMD) | 6.3 V | 560 | 0.020 Ω | 5100 mA | 10×10.2 | 3 | ≤4 | EEFWA0J561P |
| S/SE (SMD) | 6.3 V | 180 | 0.005 Ω | 4000 mA | 7.3×4.3×4.2 | N/R | ≤1 | EEFSE0J181R |
| AVX, Tantalum: | | | | | | | | |
| TPS (SMD) | 10 V | 470 | 0.045 Ω | 1723 mA | 7.3L | 3 [1] | ≤5 | TPSE477M010R0045 |
| | 10 V | 470 | 0.060 Ω | 1826 mA | ×5.7W×4.1H | 3 [1] | ≤5 | TPSV477M010R0060 |
| Kemet (SMD): | | | | | | | | |
| T520, Poly-Tant | 6.3 V | 470 | 0.018 Ω | >1200 mA | 4.3W | 3 [1] | ≤5 | T520X477M006SE018 |
| T530, Poly-Tant/Organic | 10 V | 330 | 0.015 Ω | >3800 mA | ×7.3L | 5 | ≤3 | T530X337M010AS |
| | 6.3 V | 470 | 0.012 Ω | 4200 mA | ×4.0H | 3 [1] | ≤2 | T530X477M006AS |
| Vishay-Sprague | | | | | 7.2L×6W | | | |
| 595D, Tantalum (SMD) | 10 V | 470 | 0.100 Ω | 1440 mA | ×4.1H | 3 [1] | ≤5 | 595D477X0010R2T |
| 94SA, Os-con (Radial) | 16 V | 2200 | 0.015 Ω | 9740 mA | 16×25 | 1 | ≤3 | 94SA108X0016HBP |
| Kemet, Ceramic X5R (SMD) | 16 V | 10 | 0.002 Ω | — | 1210 case | 1 [2] | ≤5 | C1210C106M4PAC |
| | 6.3 V | 47 | 0.002 Ω | | 3225 mm | 1 [2] | ≤5 | C1210C476K9PAC |
| Murata, Ceramic X5R (SMD) | 6.3 V | 100 | 0.002 Ω | — | 1210 case | 1 [2] | ≤3 | GRM32ER60J107M |
| | 6.3 V | 47 | | | 3225 mm | 1 [2] | ≤5 | GRM32ER60J476M |
| | 16 V | 22 | | | | 1 [2] | ≤5 | GRM32ER61C226K |
| | 16 V | 10 | | | | | ≤5 | GRM32DR61C106K |
| TDK, Ceramic X5R (SMD) | 6.3 V | 100 | 0.002 Ω | — | 1210 case | 1 [2] | ≤3 | C3225X5R0J107MT |
| | 6.3 V | 47 | | | 3225 mm | 1 [2] | ≤5 | C3225X5R0J476MT |
| | 16 V | 22 | | | | 1 [2] | ≤5 | C3225X5R1C226MT |
| | 16 V | 10 | | | | | ≤5 | C3225X5R1C106MT |

*[1] The total capacitance is slightly lower than 1,500 µF, but is acceptable based on the combined ripple current rating.*
*[2] A ceramic capacitor may be used to complement electrolytic types at the input to further reduce high-frequency ripple current*

## Adjusting the Output Voltage of the PTH03030W & PTH05030W Wide-Output Adjust Power Modules

The $V_o$ *Adjust* control (pin 4) sets the output voltage of the PTH03030W and PTH05030W products to a value higher than 0.8 V. The adjustment range of the PT03030W (3.3-V input) is from 0.8 V to 2.5 V [1], and the PTH05030W (5-V input) from 0.8 V to 3.6 V. For an output voltage other than 0.8 V a single external resistor, $R_{set}$, must be connected directly between the $V_o$ *Adjust* and *GND* pins [2]. Table 2-1 gives the preferred value of the external resistor for a number of standard voltages, along with the actual output voltage that this resistance value provides.

For other output voltages the value of the required resistor can either be calculated using the following formula, or simply selected from the range of values given in Table 2-2. Figure 2-1 shows the placement of the required resistor.

$$R_{set} = 10\,k\Omega \cdot \frac{0.8\ V}{V_{out} - 0.8\ V} - 2.49\,k\Omega$$

***Table 2-1; Preferred Values of $R_{set}$ for Standard Output Voltages***

| $V_{out}$ (Standard) | $R_{set}$ (Pref'd Value) | $V_{out}$ (Actual) |
|---|---|---|
| 3.3 V [1] | 698 Ω | 3.309V |
| 2.5 V | 2.21 kΩ | 2.502 V |
| 2 V | 4.12 kΩ | 2.010 V |
| 1.8 V | 5.49 kΩ | 1.803 V |
| 1.5 V | 8.87 kΩ | 1.504 V |
| 1.2 V | 17.4 kΩ | 1.202 V |
| 1 V | 36.5 kΩ | 1.005 V |
| 0.8 V | Open | 0.8 V |

***Figure 2-1; $V_o$ Adjust Resistor Placement***

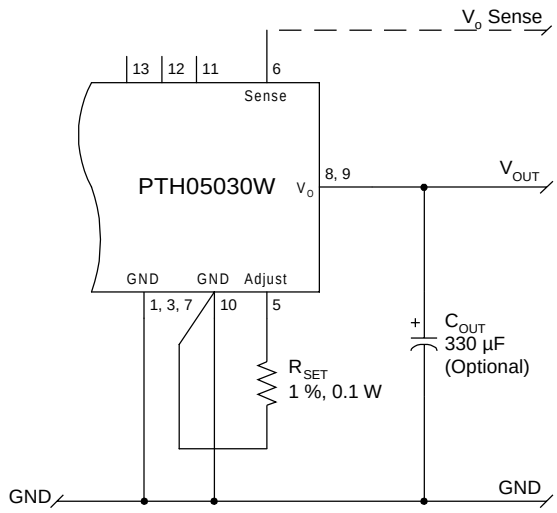



***Table 2-2; Output Voltage Set-Point Resistor Values***

| $V_a$ Req'd | $R_{set}$ | $V_a$ Req'd | $R_{set}$ |
|---|---|---|---|
| 0.800 | Open | 2.00 | 4.18 kΩ |
| 0.825 | 318 kΩ | 2.05 | 3.91 kΩ |
| 0.850 | 158 kΩ | 2.10 | 3.66 kΩ |
| 0.875 | 104 kΩ | 2.15 | 3.44 kΩ |
| 0.900 | 77.5 kΩ | 2.20 | 3.22 kΩ |
| 0.925 | 61.5 kΩ | 2.25 | 3.03 kΩ |
| 0.950 | 50.8 kΩ | 2.30 | 2.84 kΩ |
| 0.975 | 43.2 kΩ | 2.35 | 2.67 kΩ |
| 1.000 | 37.5 kΩ | 2.40 | 2.51 kΩ |
| 1.025 | 33.1 kΩ | 2.45 | 2.36 kΩ |
| 1.050 | 29.5 kΩ | 2.50 | 2.22 kΩ |
| 1.075 | 26.6 kΩ | 2.55 | 2.08 kΩ |
| 1.100 | 24.2 kΩ | 2.60 | 1.95 kΩ |
| 1.125 | 22.1 kΩ | 2.65 | 1.83 kΩ |
| 1.150 | 20.4 kΩ | 2.70 | 1.72 kΩ |
| 1.175 | 18.8 kΩ | 2.75 | 1.61 kΩ |
| 1.200 | 17.5 kΩ | 2.80 | 1.51 kΩ |
| 1.225 | 16.3 kΩ | 2.85 | 1.41 kΩ |
| 1.250 | 15.3 kΩ | 2.90 | 1.32 kΩ |
| 1.275 | 14.4 kΩ | 2.95 | 1.23 kΩ |
| 1.300 | 13.5 kΩ | 3.00 | 1.15 kΩ |
| 1.325 | 12.7 kΩ | 3.05 | 1.07 kΩ |
| 1.350 | 12.1 kΩ | 3.10 | 988 Ω |
| 1.375 | 11.4 kΩ | 3.15 | 914 Ω |
| 1.400 | 10.8 kΩ | 3.20 | 843 Ω |
| 1.425 | 10.3 kΩ | 3.25 | 775 Ω |
| 1.450 | 9.82 kΩ | 3.30 | 710 Ω |
| 1.475 | 9.36 kΩ | 3.35 | 647 Ω |
| 1.50 | 8.94 kΩ | 3.40 | 587 Ω |
| 1.55 | 8.18 kΩ | 3.45 | 529 Ω |
| 1.60 | 7.51 kΩ | 3.50 | 473 Ω |
| 1.65 | 6.92 kΩ | 3.55 | 419 Ω |
| 1.70 | 6.4 kΩ | 3.60 | 367 Ω |
| 1.75 | 5.93 kΩ | | |
| 1.80 | 5.51 kΩ | | |
| 1.85 | 5.13 kΩ | | |
| 1.90 | 4.78 kΩ | | |
| 1.95 | 4.47 kΩ | | |

Notes:

1. Modules that operate from a 3.3-V input bus should not be adjusted higher than 2.5 V.
2. Use a 0.1 W resistor. The tolerance should be 1 %, with temperature stability of 100 ppm/°C (or better). Place the resistor as close to the regulator as possible. Connect the resistor directly between pins 5 and 10 using dedicated PCB traces.
3. Never connect capacitors from $V_o$ *Adjust* to either *GND* or $V_{out}$. Any capacitance added to the $V_o$ *Adjust* pin will affect the stability of the regulator.

## Features of the PTH Family of Non-Isolated Wide Output Adjust Power Modules

### Point-of-Load Alliance

The PTH family of non-isolated, wide-output adjust power modules from Texas Instruments are optimized for applications that require a flexible, high performance module that is small in size. These products are part of the "Point-of-Load Alliance" (POLA), which ensures compatible footprint, interoperability and true second sourcing for customer design flexibility. The POLA is a collaboration between Texas Instruments, Artesyn Technologies, and Astec Power to offer customers advanced non-isolated modules that provide the same functionality and form factor. Product series covered by the alliance includes the PTHxx050W (6 A), PTHxx060W (10 A), PTHxx010W (15/12 A), PTHxx020W (22/18 A), and the PTHxx030W (30/26 A).

From the basic, "Just Plug it In" functionality of the 6-A modules, to the 30-A rated feature-rich PTHxx030W, these products were designed to be very flexible, yet simple to use. The features vary with each product. Table 3-1 provides a quick reference to the available features by product and input bus voltage.

***Table 3-1; Operating Features by Series and Input Bus Voltage***

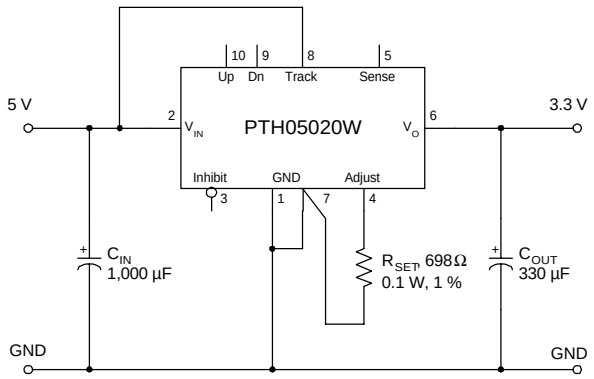
| Series | Input Bus | $I_{OUT}$ | Adjust (Trim) | On/Off Inhibit | Over-Current | Pre-Bias Startup | Auto-Track™ | Margin Up/Down | Output Sense | Thermal Shutdown |
|---|---|---|---|---|---|---|---|---|---|---|
| PTHxx050 | 3.3 V / 5 V | 6 A | • | • | • | • | • | | | |
| | 12 V | 6 A | • | • | • | | • | | | |
| PTHxx060 | 3.3 V / 5 V | 10 A | • | • | • | • | • | • | • | |
| | 12 V | 8 A | • | • | • | | • | • | • | |
| PTHxx010 | 3.3 V / 5 V | 15 A | • | • | • | • | • | • | • | |
| | 12 V | 12 A | • | • | • | | • | • | • | |
| PTHxx020 | 3.3 V / 5 V | 22 A | • | • | • | • | • | • | • | • |
| | 12 V | 18 A | • | • | • | | • | • | • | • |
| PTHxx030 | 3.3 V / 5 V | 30 A | • | • | • | • | • | • | • | • |
| | 12 V | 26 A | • | • | • | • | • | • | • | • |

For simple point-of-use applications, the PTHxx050W provides operating features such as an on/off inhibit, output voltage trim, pre-bias startup (3.3/5-V input only), and over-current protection. The PTHxx060W (10 A), and PTHxx010W (15/12 A) include an output voltage sense, and margin up/down controls. Then the higher output current, PTHxx020W and PTHxx030W products incorporate over-temperature shutdown protection. All of the products referenced in Table 3-1 include Auto-Track™. This is a feature unique to the PTH family, and was specifically designed to simplify the task of sequencing the supply voltage in a power system. These and other features are described in the following sections.

### Soft-Start Power Up

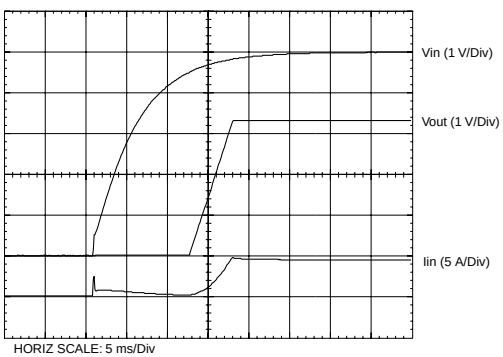
The Auto-Track feature allows the power-up of multiple PTH modules to be directly controlled from the *Track* pin. However in a stand-alone configuration, or when the Auto-Track feature is not being used, the *Track* pin should be directly connected to the input voltage, $V_{in}$ (see Figure 3-1).

***Figure 3–1***




When the *Track* pin is connected to the input voltage the Auto-Track function is permanently disengaged. This allows the module to power up entirely under the control of its internal soft-start circuitry. When power up is under soft-start control, the output voltage rises to the set-point at a quicker and more linear rate.

***Figure 3–2***



From the moment a valid input voltage is applied, the soft-start control introduces a short time delay (typically 5 ms-10 ms) before allowing the output voltage to rise. The output then progressively rises to the module's set-point voltage. Figure 3-2 shows the soft-start power-up characteristic of the 22-A output product (PTH05020W), operating from a 5-V input bus and configured for a 3.3-V output. The waveforms were measured with a 5-A resistive load, with Auto-Track disabled. The initial rise in input current when the input voltage first starts to rise is the charge current drawn by the input capacitors. Power-up is complete within 15 ms.

### Over-Current Protection

For protection against load faults, all modules incorporate output over-current protection. Applying a load that exceeds the regulator's over-current threshold will cause the regulated output to shut down. Following shutdown a module will periodically attempt to recover by initiating a soft-start power-up. This is described as a "hiccup" mode of operation, whereby the module continues in a cycle of successive shutdown and power up until the load fault is removed. During this period, the average current flowing into the fault is significantly reduced. Once the fault is removed, the module automatically recovers and returns to normal operation.

### Over-Temperature Protection

The PTHxx020 and PTHxx030 series of products have over-temperature protection. These products have an on-board temperature sensor that protects the module's internal circuitry against excessively high temperatures. A rise in the internal temperature may be the result of a drop in airflow, or a high ambient temperature. If the internal temperature exceeds the OTP threshold, the module's *Inhibit* control is automatically pulled low. This turns the output off. The output voltage will drop as the external output capacitors are discharged by the load circuit. The recovery is automatic, and begins with a soft-start power up. It occurs when the the sensed temperature decreases by about 10 °C below the trip point.

*Note: The over-temperature protection is a last resort mechanism to prevent thermal stress to the regulator. Operation at or close to the thermal shutdown temperature is not recommended and will reduce the long-term reliability of the module. Always operate the regulator within the specified Safe Operating Area (SOA) limits for the worst-case conditions of ambient temperature and airflow.*

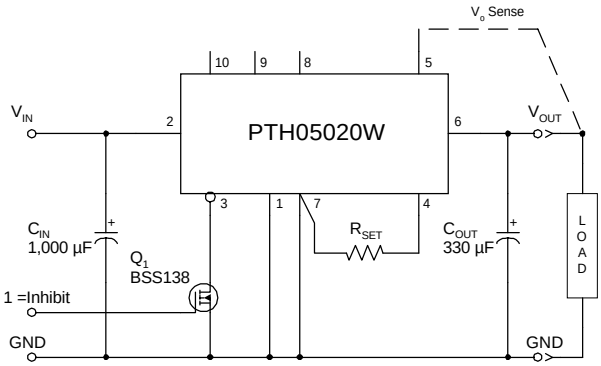
### Output On/Off Inhibit

For applications requiring output voltage on/off control, each series of the PTH family incorporates an output *Inhibit* control pin. The inhibit feature can be used wherever there is a requirement for the output voltage from the regulator to be turned off.

The power modules function normally when the *Inhibit* pin is left open-circuit, providing a regulated output whenever a valid source voltage is connected to $V_{in}$ with respect to *GND*.

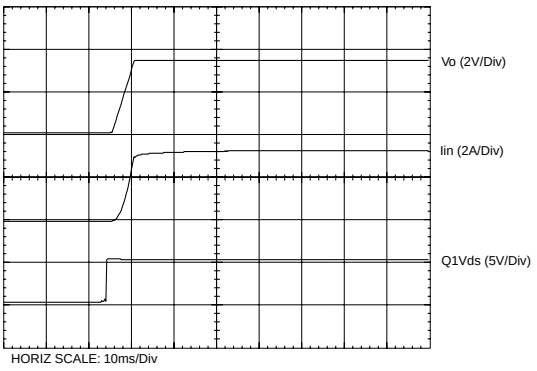
Figure 3-3 shows the typical application of the inhibit function. Note the discrete transistor ($Q_1$). The *Inhibit* control has its own internal pull-up to $V_{in}$ potential. The input is not compatible with TTL logic devices. An open-collector (or open-drain) discrete transistor is recommended for control.

***Figure 3–3***




Turning $Q_1$ on applies a low voltage to the *Inhibit* control and disables the output of the module. If $Q_1$ is then turned off, the module will execute a soft-start power-up. A regulated output voltage is produced within 20 msec. Figure 3-4 shows the typical rise in both the output voltage and input current, following the turn-off of $Q_1$. The turn off of $Q_1$ corresponds to the rise in the waveform, $Q_1$ $V_{ds}$. The waveforms were measured with a 5-A load.

***Figure 3–4***



## Auto-Track™ Function

The Auto-Track function is unique to the PTH family, and is available with the all "Point-of-Load Alliance" (POLA) products. Auto-Track was designed to simplify the amount of circuitry required to make the output voltage from each module power up and power down in sequence. The sequencing of two or more supply voltages during power up is a common requirement for complex mixed-signal applications, that use dual-voltage VLSI ICs such as DSPs, micro-processors, and ASICs.

### How Auto-Track Works

Auto-Track works by forcing the module's output voltage to follow a voltage presented at the *Track* control pin. This control range is limited to between 0 V and the module's set-point voltage. Once the track-pin voltage is raised above the set-point voltage, the module's output remains at its set-point [1]. As an example, if the Track pin of a 2.5-V regulator is at 1 V, the regulated output will be 1 V. But if the voltage at the Track pin rises to 3 V, the regulated output will not go higher than 2.5 V.

When under track control, the regulated output from the module follows the voltage at its Track pin on a volt-for-volt basis. By connecting the Track pin of a number of these modules together, the output voltages will follow a common signal during power-up and power-down. The control signal can be an externally generated master ramp waveform, or the output voltage from another power supply circuit [3]. For convenience the Track control incorporates an internal RC charge circuit. This operates off the module's input voltage to provide a suitable rising voltage ramp waveform.

### Typical Application

The basic implementation of Auto-Track allows for simultaneous voltage sequencing of a number of Auto-Track compliant modules. Connecting the Track control pins of two or more modules forces the Track control of all modules to follow the same collective RC ramp waveform, and allows them to be controlled through a single transistor or switch; $Q_1$ in Figure 3-5.

To initiate a power-up sequence the Track control must first pulled to ground potential. This should be done at or before input power is applied to the modules, and then held for at least 10 ms thereafter. This brief period gives the modules time to complete their internal soft-start initialization, which enables them to produce an output voltage.

Applying a logic-level high signal to the circuit's On/Off Control turns $Q_1$ on and applies a ground signal to the Track control. After completing their internal soft-start intialization, the output of all modules will remain at zero volts while $Q_1$ is on. 10 ms after a valid input voltage has been applied to all modules, $Q_1$ can be turned off. This allows the track control voltage to automatically rise toward to the modules' input voltage. During this period the output voltage of each module will rise in unison with other modules, to its respective set-point voltage.

Figure 3-6 shows the output voltage waveforms from the circuit of Figure 3-5 after the On/Off Control is set from a high to a low-level voltage. The waveforms, $Vo_1$ and $Vo_2$ represent the output voltages from the two power modules, $U_1$ (3.3 V) and $U_2$ (1.8 V) respectively. $Vo_1$ and $Vo_2$ are shown rising together to produce the desired simultaneous power-up characteristic.

The same circuit also provides a power-down sequence. Power down is the reverse of power up, and is accomplished by lowering the track control voltage back to zero volts. The important constraint is that a valid input voltage must be maintained until the power down is complete. It also requires that $Q_1$ be turned off relatively slowly. This is so that the Track control voltage does not fall faster than Auto-Track's slew rate capability, which is 1 V/ms. The components $R_1$ and $C_1$ in Figure 3-5 limit the rate at which $Q_1$ can pull down the Track control voltage. The values of 100 k-ohm and 0.1 µF correlate to a decay rate of about 0.17 V/ms.

The power-down sequence is initiated with a low-to-high transition at the On/Off Control input to the circuit. Figure 3-7 shows the power-down waveforms. As the Track control voltage falls below the nominal set-point voltage of each power module, then its output voltage decays with all the other modules under Auto-Track control.

### Notes on Use of Auto-Track™

1. The Track pin voltage must be allowed to rise above the module's set-point voltage before the module can regulate at its adjusted set-point voltage.
2. The Auto-Track function will track almost any voltage ramp during power up, and is compatible with ramp speeds of up to 1 V/ms.
3. The absolute maximum voltage that may be applied to the Track pin is $V_{in}$.
4. The module will not follow a voltage at its Track control input until it has completed its soft-start initialization. This takes about 10 ms from the time that the module has sensed that a valid voltage has been applied its input. During this period, it is recommended that the Track pin be held at ground potential.
5. The module is capable of both sinking and sourcing current when following a voltage at its Track pin. Therefore startup into an output prebias is not supported during Auto-Track control. *Note: A pre-bias holdoff is not necessary when all supply voltages rise simultaneously under the control of Auto-Track.*
6. The Auto-Track function can be disabled by connecting the *Track* pin to the input voltage ($V_{in}$). With Auto-Track disabled, the output voltage will rise at a quicker and more linear rate after input power is applied.

***Figure 3–5; Sequenced Power Up & Power Down Using Auto-Track***

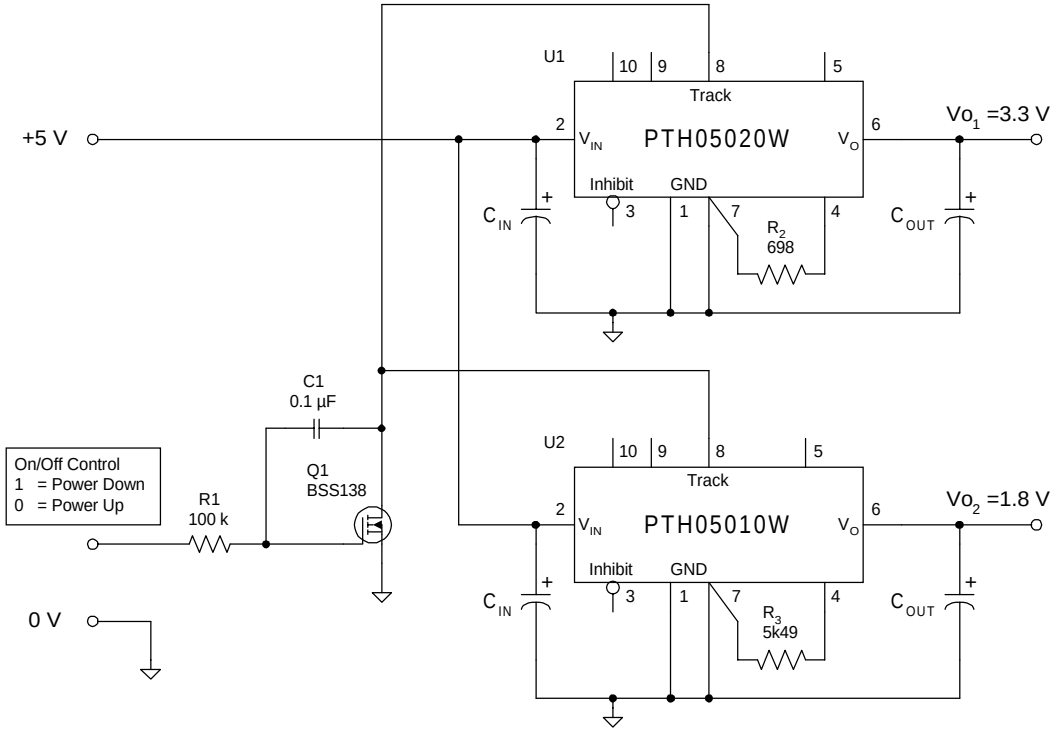



***Figure 3–6; Simultaneous Power Up with Auto-Track Control***

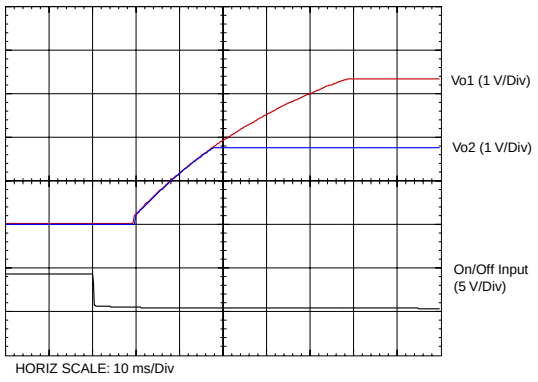
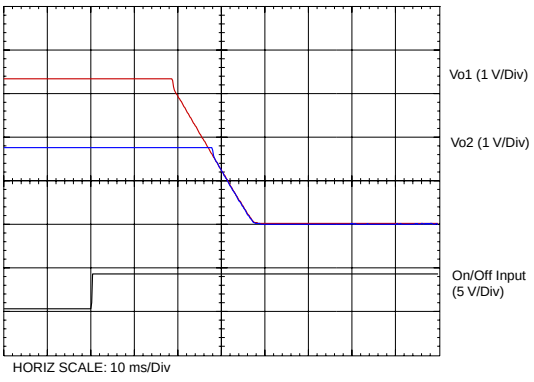



***Figure 3–7; Simultaneous Power Down with Auto-Track Control***



## Margin Up/Down Controls

The PTHxx060W, PTHxx010W, PTHxx020W, and PTHxx030W products incorporate *Margin Up* and *Margin Down* control inputs. These controls allow the output voltage to be momentarily adjusted [1], either up or down, by a nominal 5 %. This provides a convenient method for dynamically testing the operation of the load circuit over its supply margin or range. It can also be used to verify the function of supply voltage supervisors. The ±5 % change is applied to the adjusted output voltage, as set by the external resistor, $R_{set}$ at the *$V_o$ Adjust* pin.

The 5 % adjustment is made by pulling the appropriate margin control input directly to the *GND* terminal [2]. A low-leakage open-drain device, such as an n-channel MOSFET or p-channel JFET is recommended for this purpose [3]. Adjustments of less than 5 % can also be accommodated by adding series resistors to the control inputs. The value of the resistor can be selected from Table 3-2, or calculated using the following formula.

### Up/Down Adjust Resistance Calculation

To reduce the margin adjustment to something less than 5 %, series resistors are required (See $R_D$ and $R_U$ in Figure 3-8). For the same amount of adjustment, the resistor value calculated for $R_U$ and $R_D$ will be the same. The formulas is as follows.

$$R_U \text{ or } R_D = \frac{499}{\Delta\%} - 99.8 \quad k\Omega$$

Where $\Delta\%$ = The desired amount of margin adjust in percent.

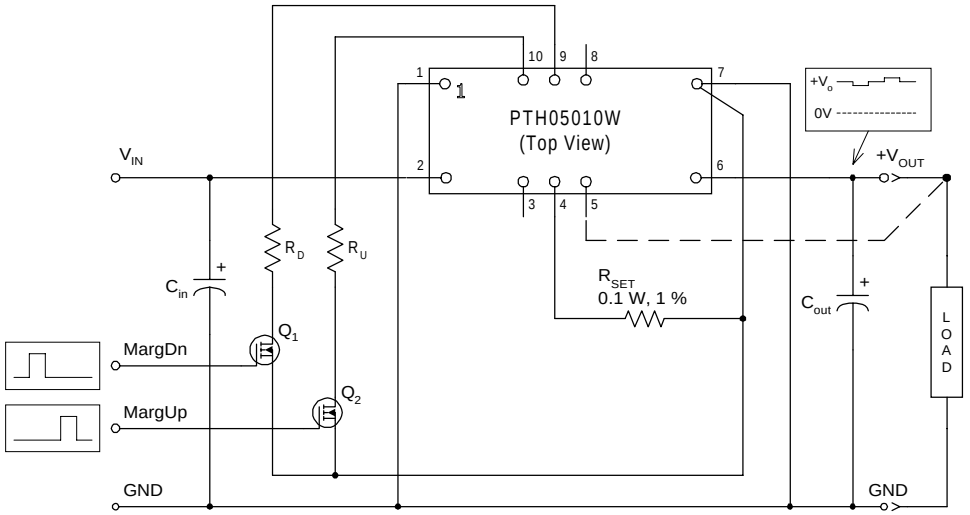
Notes:

1. The *Margin Up** and *Margin Dn** controls were not intended to be activated simultaneously. If they are their affects on the output voltage may not completely cancel, resulting in the possibility of a slightly higher error in the output voltage set point.
2. The ground reference should be a direct connection to the module *GND* at pin 7 (pin 1 for the PTHxx050). This will produce a more accurate adjustment at the load circuit terminals. The transistors $Q_1$ and $Q_2$ should be located close to the regulator.
3. The Margin Up and Margin Dn control inputs are not compatible with devices that source voltage. This includes TTL logic. These are analog inputs and should only be controlled with a true open-drain device (preferably a discrete MOSFET transistor). The device selected should have low off-state leakage current. Each input sources 8 µA when grounded, and has an open-circuit voltage of 0.8 V.

***Table 3-2; Margin Up/Down Resistor Values***

| % Adjust | $R_U$ / $R_D$ |
|---|---|
| 5 | 0.0 kΩ |
| 4 | 24.9 kΩ |
| 3 | 66.5 kΩ |
| 2 | 150.0 kΩ |
| 1 | 397.0 kΩ |

***Figure 3–8; Margin Up/Down Application Schematic***



## Pre-Bias Startup Capability

Only selected products in the PTH family incorporate this capability. Consult Table 3-1 to identify which products are compliant.

A pre-bias startup condition occurs as a result of an external voltage being present at the output of a power module prior to its output becoming active. This often occurs in complex digital systems when current from another power source is backfed through a dual-supply logic component, such as an FPGA or ASIC. Another path might be via clamp diodes as part of a dual-supply power-up sequencing arrangement. A prebias can cause problems with power modules that incorporate synchronous rectifiers. This is because under most operating conditions, these types of modules can sink as well as source output current.

The PTH family of power modules incorporate synchronous rectifiers, but will not sink current during startup [1], or whenever the *Inhibit* pin is held low. However, to ensure satisfactory operation of this function, certain conditions must be maintained. [2] Figure 3-9 shows an application demonstrating the pre-bias startup capability. The start-up waveforms are shown in Figure 3-10. Note that the output current from the PTH03010W ($I_o$) shows negligible current until its output voltage rises above that backfed through diodes $D_1$ and $D_2$.

*Note: The pre-bias start-up feature is not compatible with Auto-Track. When the module is under Auto-Track control, it will sink current if the output voltage is below that of a back-feeding source. To ensure a pre-bias hold-off one of two approaches must be followed when input power is applied to the module. The Auto-Track function must either be disabled [3], or the module's output held off (for at least 50 ms) using the Inhibit pin. Either approach ensures that the Track pin voltage is above the set-point voltage at start up.*

Notes

1. Startup includes the short delay (approx. 10 ms) prior to the output voltage rising, followed by the rise of the output voltage under the module's internal soft-start control. Startup is complete when the output voltage has risen to either the set-point voltage or the voltage at the *Track* pin, whichever is lowest.
2. To ensure that the regulator does not sink current when power is first applied (even with a ground signal applied to the *Inhibit* control pin), the input voltage must always be greater than the output voltage throughout the power-up and power-down sequence.
3. The Auto-Track function can be disabled at power up by immediately applying a voltage to the module's *Track* pin that is greater than its set-point voltage. This can be easily accomplished by connecting the *Track* pin to $V_{in}$.

***Figure 3–10; Pre-Bias Startup Waveforms***

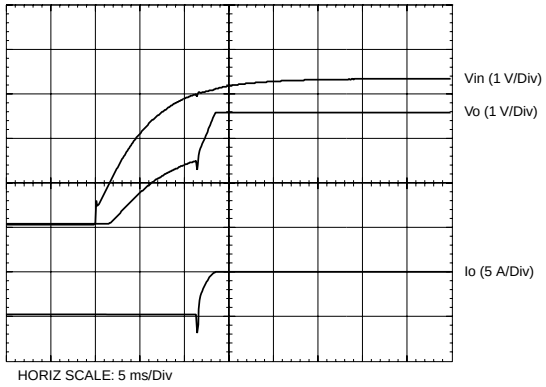
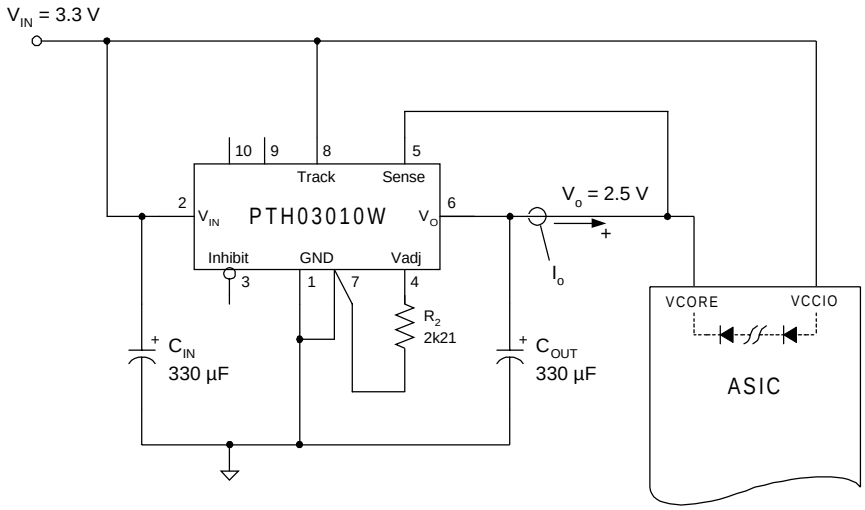



***Figure 3–9; Application Circuit Demonstrating Pre-Bias Startup***



### Remote Sense

The PTHxx060W, PTHxx010W, PTHxx020W, and PTHxx030W products incorporate an output voltage sense pin, *$V_o$ Sense*. The *$V_o$ Sense* pin should be connected to $V_{out}$ at the load circuit (see data sheet standard application). A remote sense improves the load regulation performance of the module by allowing it to compensate for any 'IR' voltage drop between itself and the load. An IR drop is caused by the high output current flowing through the small amount of pin and trace resistance. Use of the remote sense is optional. If not used, the *$V_o$ Sense* pin can be left open-circuit. An internal low-value resistor (15-Ω or less) is connected between the *$V_o$ Sense* and $V_{out}$. This ensures the output voltage remains in regulation.

With the sense pin connected, the difference between the voltage measured directly between the $V_{out}$ and *GND* pins, and that measured from *$V_o$ Sense* to *GND*, is the amount of IR drop being compensated by the regulator. This should be limited to a maximum of 0.3 V.

*Note: The remote sense feature is not designed to compensate for the forward drop of non-linear or frequency dependent components that may be placed in series with the converter output. Examples include OR-ing diodes, filter inductors, ferrite beads, and fuses. When these components are enclosed by the remote sense connection they are effectively placed inside the regulation control loop, which can adversely affect the stability of the regulator.*

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| PTH05030WAD | Last Time Buy | Production | Through-Hole Module (EUM) \| 13 | 16 \| TIW TRAY | Exempt | SN | N/A for Pkg Type | -40 to 85 | |
| PTH05030WAD.B | NRND | Production | Through-Hole Module (EUM) \| 13 | 16 \| TIW TRAY | Exempt | SN | N/A for Pkg Type | -40 to 85 | |
| PTH05030WAH | Last Time Buy | Production | Through-Hole Module (EUM) \| 13 | 16 \| TIW TRAY | Exempt | SN | N/A for Pkg Type | -40 to 85 | |
| PTH05030WAH.B | NRND | Production | Through-Hole Module (EUM) \| 13 | 16 \| TIW TRAY | Exempt | SN | N/A for Pkg Type | -40 to 85 | |
| PTH05030WAST | Last Time Buy | Production | Surface Mount Module (EUN) \| 13 | 200 \| SMALL T&R | No | SNPB | Level-1-235C-UNLIM/ Level-3-260C-168HRS | -40 to 85 | |
| PTH05030WAST.B | NRND | Production | Surface Mount Module (EUN) \| 13 | 200 \| SMALL T&R | No | SNPB | Level-1-235C-UNLIM/ Level-3-260C-168HRS | -40 to 85 | |
| PTH05030WAZ | Last Time Buy | Production | Surface Mount Module (EUN) \| 13 | 16 \| TIW TRAY | Exempt | SNAGCU | Level-3-260C-168 HR | -40 to 85 | |
| PTH05030WAZ.B | NRND | Production | Surface Mount Module (EUN) \| 13 | 16 \| TIW TRAY | Exempt | SNAGCU | Level-3-260C-168 HR | -40 to 85 | |
| PTH05030WAZT | Last Time Buy | Production | Surface Mount Module (EUN) \| 13 | 200 \| SMALL T&R | Exempt | SNAGCU | Level-3-260C-168 HR | -40 to 85 | |
| PTH05030WAZT.B | NRND | Production | Surface Mount Module (EUN) \| 13 | 200 \| SMALL T&R | Exempt | SNAGCU | Level-3-260C-168 HR | -40 to 85 | |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

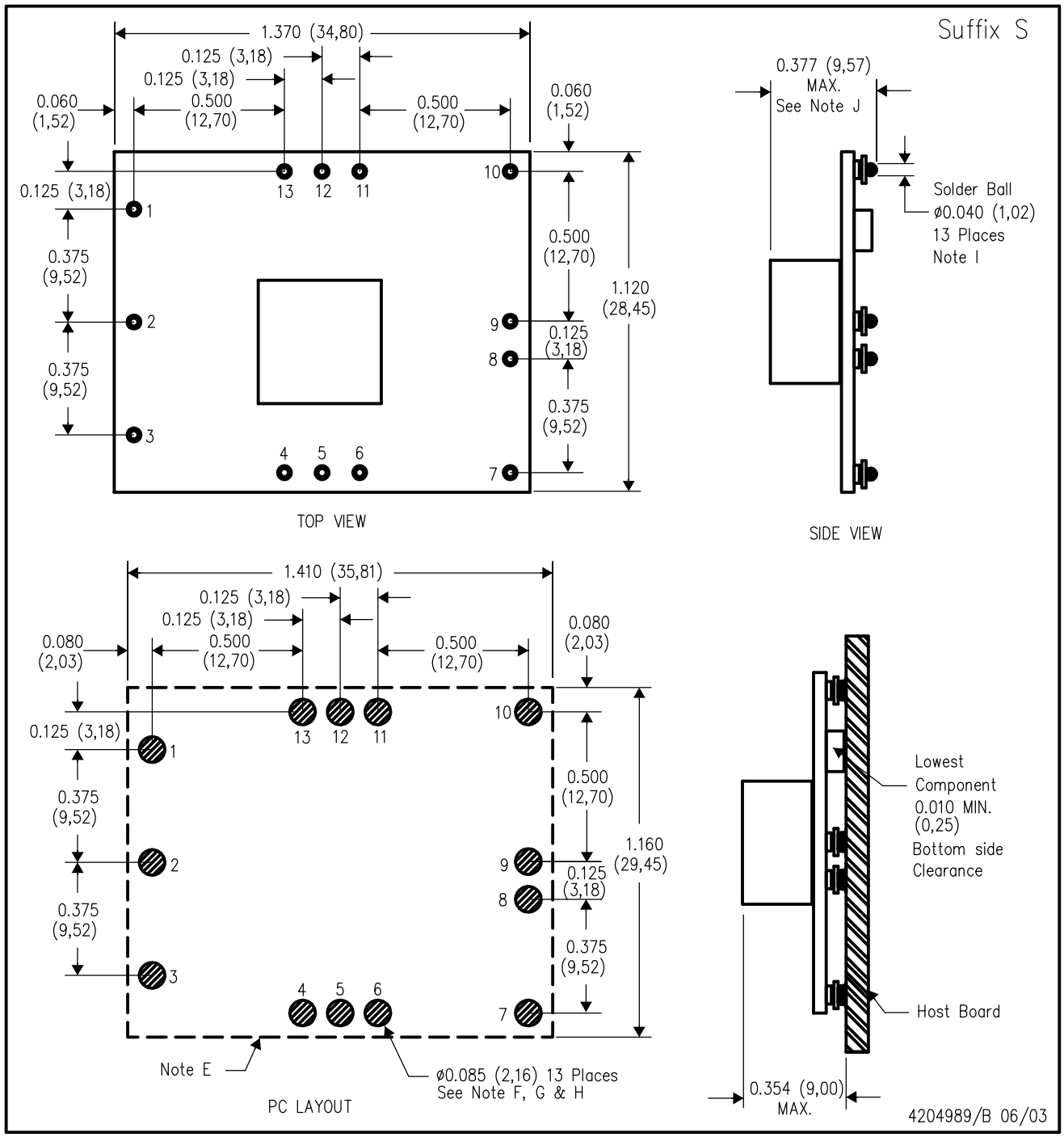
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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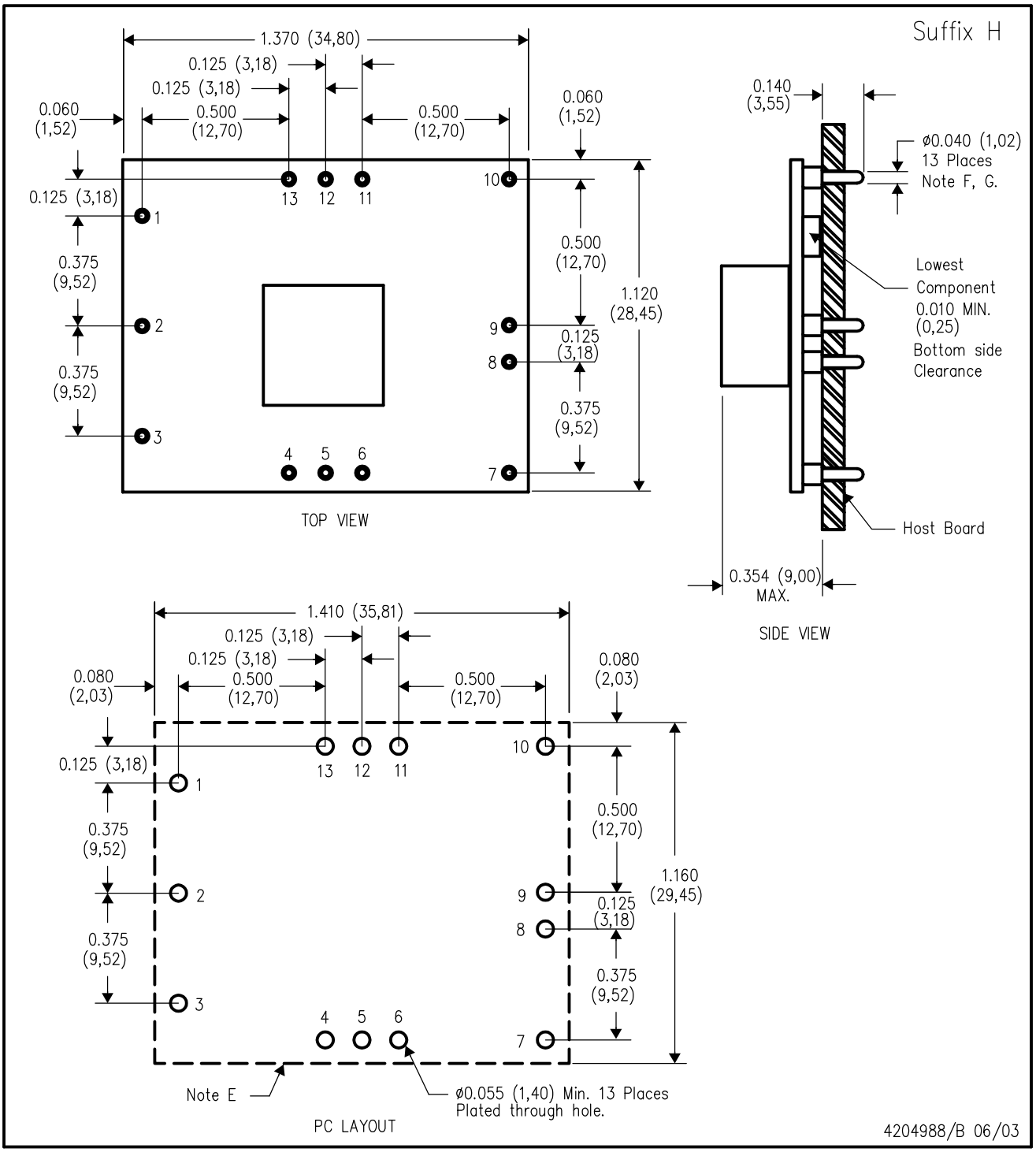
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## EUN (R–PDSS–B13) DOUBLE SIDED MODULE




NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Power pin connection should utilize two or more vias to the interior power plane of 0.025 (0,63) I.D. per input, ground and output pin (or the electrical equivalent).
G. Paste screen opening: 0.080 (2,03) to 0.085 (2,16). Paste screen thickness: 0.006 (0,15).
H. Pad type: Solder mask defined.
I. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate
Solder Ball – See product data sheet.
J. Dimension prior to reflow solder.

## EUM (R–PDSS–T13) DOUBLE SIDED MODULE




NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Pins are 0.040" (1,02) diameter with 0.070" (1,78) diameter standoff shoulder.
G. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate

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