Precision Micropower, Low Dropout Voltage Reference

Enhanced Product

REF191-EP

FEATURES

- Temperature coefficient: 5 ppm/°C maximum
- High output current: 30 mA
- Low supply current: 50 µA maximum
- Initial accuracy: 2.050 V maximum
- Sleep mode: 15 µA maximum
- Low dropout voltage
- Load regulation: 4 ppm/mA typical at T_A = 25°C
- Line regulation: 2 ppm/V typical at T_A = 25°C
- Short-circuit protection

ENHANCED PRODUCT FEATURES

- Supports defense and aerospace applications (AQEC standard)
- Military temperature range: −55°C to +125°C
- Controlled manufacturing baseline
- 1 assembly/test site
- 1 fabrication site
- Product change notification
- Qualification data available on request

APPLICATIONS

- Portable instruments
- ADCs and DACs
- Smart sensors
- Solar powered applications
- Loop current powered instruments

PIN CONFIGURATION DIAGRAM

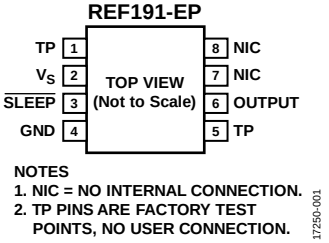


Figure 1.

GENERAL DESCRIPTION

The REF191-EP precision band gap voltage reference uses a proprietary temperature drift curvature correction circuit and laser trimming of highly stable, thin film resistors to achieve a very low temperature coefficient and high initial accuracy.

The REF191-EP is a micropower, low dropout voltage device, providing stable output voltage from supplies with low headroom and consuming less than 50 µA of supply current. In sleep mode, which is enabled by applying a low transistor to transistor logic (TTL) or complementary metal-oxide semiconductor (CMOS) level to the $\overline{\text{SLEEP}}$ pin, the output is turned off and supply current is further reduced to less than 15 µA.

The REF191-EP reference is specified over the full military temperature range (−55°C to +125°C).

The REF191-EP is available in an 8-lead SOIC package.

Pin 1 and Pin 5 (TP) are reserved for in package Zener zaps. To achieve the highest level of accuracy at the output, the Zener zapping technique is used to trim the output voltage. Because each unit may require a different amount of adjustment, the resistance value at the test pins varies widely from pin to pin and from device to device. Leave Pin 1 and Pin 5 unconnected.

Additional application and technical information can be found in the REF19x Series data sheet.

Rev. 0 Document Feedback

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REVISION HISTORY

2/2020—Revision 0: Initial Version

SPECIFICATIONS

At V_S = 3.3 V, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INITIAL ACCURACY[1]	V_O	Output current (I_{OUT}) = 0 mA	2.046	2.048	2.050	V
REGULATION[2]						
Line	$\Delta V_O/\Delta V_{IN}$	3.0 V ≤ V_S ≤ 15 V, I_{OUT} = 0 mA		2	4	ppm/V
Load	$\Delta V_O/\Delta V_{LOAD}$	V_S = 5.0 V, 0 mA ≤ I_{OUT} ≤ 30 mA		4	11	ppm/mA
DROPOUT VOLTAGE	$V_S - V_O$	V_S = 3.0 V, load current (I_{LOAD}) = 2 mA			0.95	V
		V_S = 3.3 V, I_{LOAD} = 10 mA			1.25	V
		V_S = 3.6 V, I_{LOAD} = 30 mA			1.55	V
LONG-TERM STABILITY[3]	DV_O	1000 hours at 125°C		1.2		mV
NOISE VOLTAGE	e_N	0.1 Hz to 10 Hz		20		μV p-p

[1] Initial accuracy does not include shift due to solder heat effect.
[2] Line and load regulation specifications include the effect of self heating.
[3] Long-term stability specification is noncumulative. The drift in subsequent 1000-hour periods is significantly lower than in the first 1000-hour period.

At V_S = 3.3 V, −40°C ≤ T_A ≤ +125°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
TEMPERATURE COEFFICIENT[1, 2]	TCV_O	I_{OUT} = 0 mA		2	5	ppm/°C
REGULATION[3]						
Line	$\Delta V_O/\Delta V_{IN}$	3.0 V ≤ V_S ≤ 15 V, I_{OUT} = 0 mA		5	10	ppm/V
Load	$\Delta V_O/\Delta V_{LOAD}$	V_S = 5.0 V, 0 mA ≤ I_{OUT} ≤ 20 mA		5	15	ppm/mA
DROPOUT VOLTAGE	$V_S - V_O$	V_S = 3.0 V, I_{LOAD} = 2 mA			0.95	V
		V_S = 3.3 V, I_{LOAD} = 10 mA			1.25	V
		V_S = 3.6 V, I_{LOAD} = 20 mA			1.55	V
$\overline{\text{SLEEP}}$ PIN						
Logic High Input Voltage	V_H		2.4			V
Logic High Input Current	I_H				−8	μA
Logic Low Input Voltage	V_L				0.8	V
Logic Low Input Current	I_L				−8	μA
SUPPLY CURRENT		No load			50	μA
Sleep Mode		No load			15	μA

[1] For proper operation, a 1 μF capacitor is required between the output pin and the GND pin of the device.
[2] TCV_O is defined as the ratio of the output voltage change (between the maximum output voltage (V_{MAX}) and the minimum output voltage (V_{MIN})) with temperature variation to the specified temperature range, expressed in ppm/°C.

$$TCV_O = (V_{MAX} - V_{MIN})/V_O(T_{MAX} - T_{MIN})$$

[3] Line and load regulation specifications include the effect of self heating.

At V_S = 3.3 V, −55°C ≤ T_A ≤ +125°C, unless otherwise noted.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
TEMPERATURE COEFFICIENT[1, 2]	TCV_O	I_{OUT} = 0 mA		2		ppm/°C
REGULATION[3]						
Line	$\Delta V_O/\Delta V_{IN}$	3.0 V ≤ V_S ≤ 15 V, I_{OUT} = 0 mA		10		ppm/V
Load	$\Delta V_O/\Delta V_{LOAD}$	V_S = 5.0 V, 0 mA ≤ I_{OUT} ≤ 25 mA, T_A = −55°C		10	15	ppm/mA
		V_S = 5.0 V, 0 mA ≤ I_{OUT} ≤ 20 mA, T_A = 125°C		10	15	ppm/mA
DROPOUT VOLTAGE	$V_S - V_O$	V_S = 3.3 V, I_{LOAD} = 10 mA			1.25	V
		V_S = 3.6 V, I_{LOAD} = 20 mA			1.55	V

[1] For proper operation, a 1 μF capacitor is required between the output pin and the GND pin of the device.
[2] TCV_O is defined as the ratio of the output voltage change (between the maximum output voltage (V_{MAX}) and the minimum output voltage (V_{MIN})) with temperature variation to the specified temperature range, expressed in ppm/°C.

$$TCV_O = (V_{MAX} - V_{MIN})/V_O(T_{MAX} - T_{MIN})$$

[3] Line and load regulation specifications include the effect of self heating.

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	−0.3 V to +18 V
Output to GND	−0.3 V to V_S + 0.3 V
Output to GND Short-Circuit Duration	Indefinite
Temperature Ranges	
Storage	−65°C to +150°C
Operating	−55°C to +125°C
Junction	−65°C to +150°C
Lead Temperature (Soldering 60 sec)	260°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Table 5. Thermal Resistance

Package Type[1]	θ_{JA}	θ_{JC}	Unit
R-8	158	43	°C/W

[1] Thermal impedance simulated values are based on JEDEC specifications. Use these values in compliance with JESD51-12.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

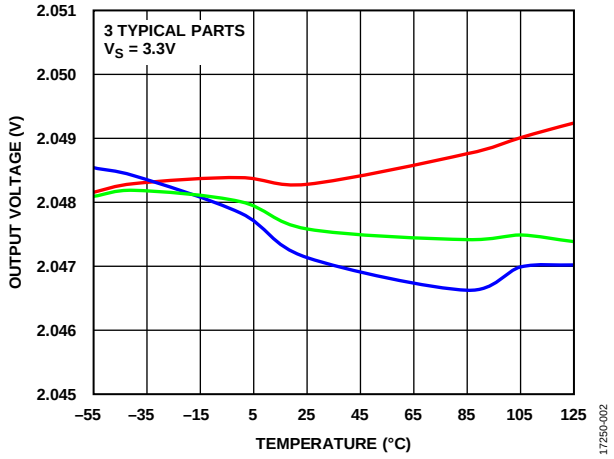


Figure 2. Output Voltage vs. Temperature

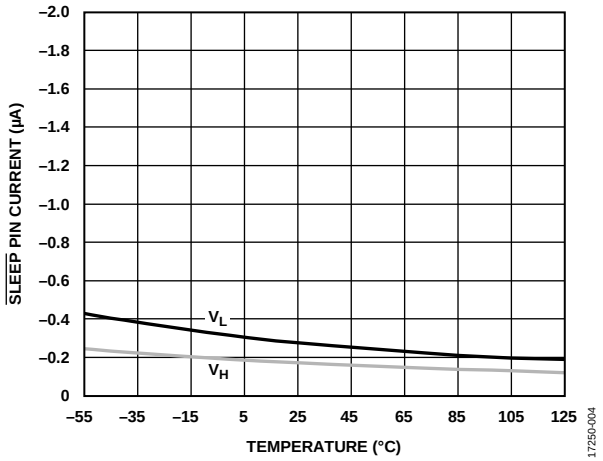


Figure 4. $\overline{SLEEP}$ Pin Current vs. Temperature

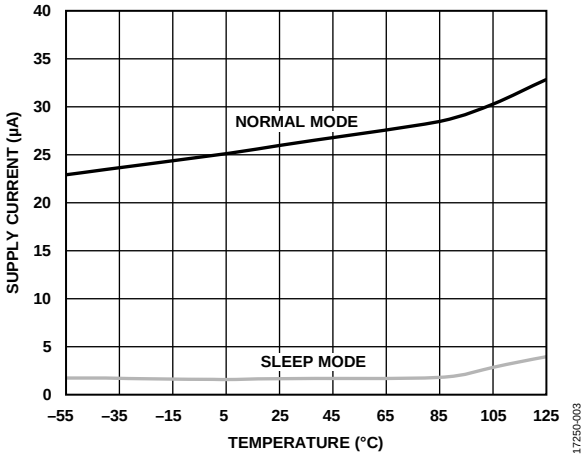
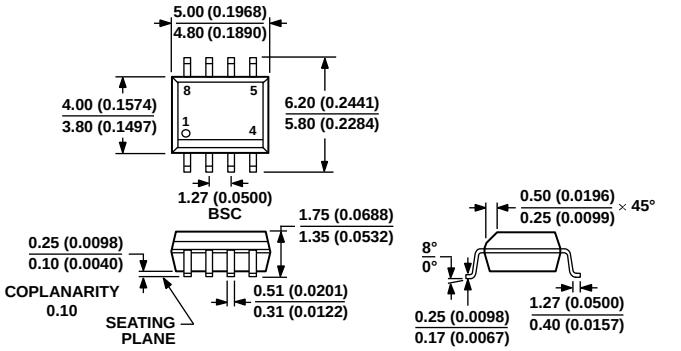


Figure 3. Supply Current vs. Temperature

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012407-A

Figure 5. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
S-Suffix (R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
REF191TRZ-EP	−55°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
REF191TRZ-EP-RL	−55°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8

[1] Z = RoHS Compliant Part.

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