S2-LPTX

Datasheet

Sub-1 GHz proprietary radio transmitter



Maturity status link
S2-LPTX

Features

- Frequency bands:
  - 413-479 MHz
  - 826-958 MHz
- Modulation schemes:
  - 2(G)FSK, 4(G)FSK
  - OOK, ASK
- Air data rate from 0.1 to 500 kbps
- Ultra-low power consumption:
  - 10 mA TX @ +10 dBm
- Programmable RF output power up to +16 dBm
- Programmable channel spacing
- Fast start-up and frequency synthesizer settling time
- Battery indicator and low battery detector
- TX 128 bytes FIFO buffers
- 4-wire SPI interface
- ST companion integrated filter chips are available
- Fully integrated ultra-low power RC oscillator
- Wake-up driven by internal timer or external event
- Flexible packet length with dynamic payload length
- IEEE 802.15.4g hardware packet support with whitening, FEC, CRC
- Wireless M-BUS supported
- Enables operations in the SIGFOX™ network
- Suitable to build systems targeting:
  - Europe: ETSI EN 300 220, ETSI EN 303 131
  - US: FCC part 15 and part 90
  - Japan: ARIB STD T67, T108
  - China: SRRC
- Operating temperature range: -40 °C to +105 °C

Applications

- Sensors to Cloud
- Smart metering
- Home energy management systems
- Wireless alarm systems
- Smart home
- Building automation
- Industrial monitoring and control
- Smart lighting systems

Description

The S2-LPTX is a high performance ultra-low power RF transmitter, intended for RF wireless applications in the sub-1 GHz band. It is designed to operate in both the license-free ISM and SRD frequency bands at 433, 868 and 920 MHz, but can also be programmed to operate at other additional frequencies in the 413-479 MHz, 826-958 MHz.

The S2-LPTX supports different modulation schemes: 2(G)FSK, 4(G)FSK, OOK and ASK. The air data rate is programmable from 0.1 to 500 kbps.

The S2-LPTX meets the regulatory requirements applicable in territories worldwide, including Europe, Japan, China and the USA.

1 Detailed functional description

The S2-LPTX integrates a configurable baseband modulator with proprietary fully programmable packet format allowing also:

- IEEE 802.15.4g applications
  - The hardware packet supports whitening, CRC, FEC
- Wireless M-Bus applications

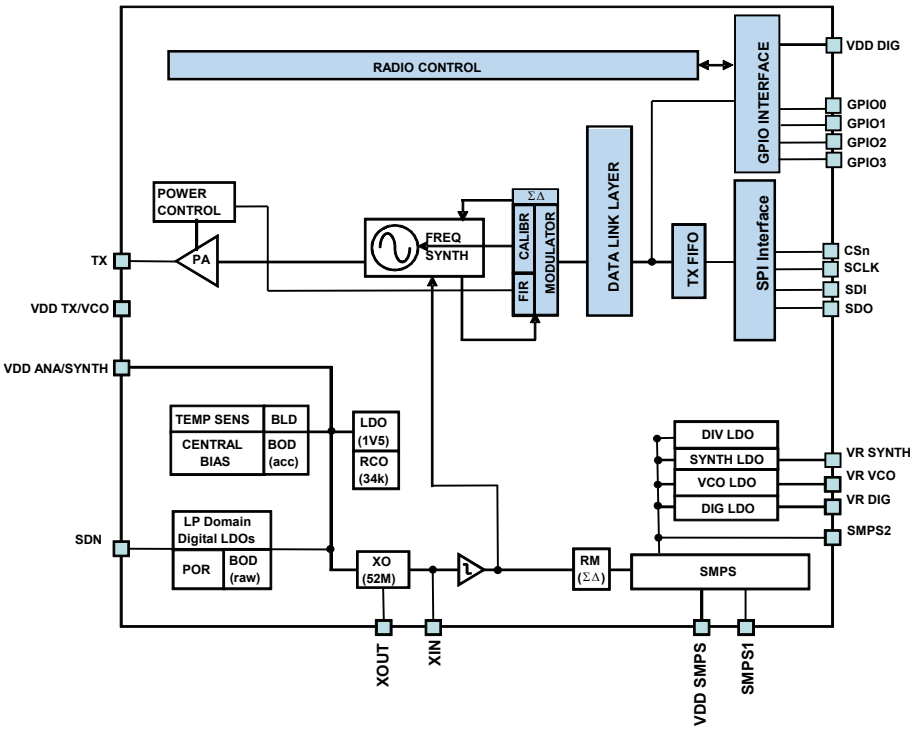
Transmitted data bytes are buffered in a 128 bytes FIFO accessible via SPI interface for host processing.

In addition, the reduced number of external components enables a cost effective solution permitting a compact PCB footprint.

The S2-LPTX targets volume applications like:

- Sensors to Cloud
- Smart metering
- Home energy management systems
- Wireless alarm systems
- Smart home
- Building automation
- Industrial monitoring and control

Figure 1. Simplified S2-LPTX block diagram



The transmitter of the S2-LPTX is based on direct synthesis of the RF frequency. The power amplifier (PA) input is the LO generated by the RF synthesizer, while the output level can be configured between -30 dBm and +14 dBm (+16 dBm in boost mode), at antenna level with 0.5 dB steps.

The data to be transmitted can be provided by an external MCU either through the 128-byte TX FIFO writable via SPI, or directly using a programmable GPIO pin. The S2-LPTX supports frequency hopping.

The S2-LPTX has a very efficient power management (PM) system. An integrated switched mode power supply (SMPS) regulator allows operation from a battery voltage ranging from +1.8 V to +3.6 V, and with power conversion efficiency of 90%.

A crystal must be connected between XIN and XOUT. It is digitally configurable to operate with different crystals. As an alternative, an external clock signal can be used to feed XIN for proper operation. The S2-LPTX also has an integrated low-power RC oscillator, generating the 34.7 kHz signal used as a clock for the slowest timeouts.

A standard 4-pin SPI bus is used to communicate with the external MCU. Four configurable general purpose I/Os are available.

2 Typical application diagram and pin description

This section describes three different application diagrams for the S2-LPTX. Two main configurations are available:

- HPM (high performance mode) configuration
- LPM (low power mode) configuration

In the LPM operating mode the LDOs are bypassed and the SMPS provides the regulator voltage at 1.2 V. Note that in LPM the PA is supplied from SMPS at 1.2 V (instead of 1.5 V as in HPM), so the max. output power is lower than HPM. The figure below shows the suggested configuration with discrete matching network and SMPS-ON.

Figure 2. Suggested application diagram (embedded SMPS used)

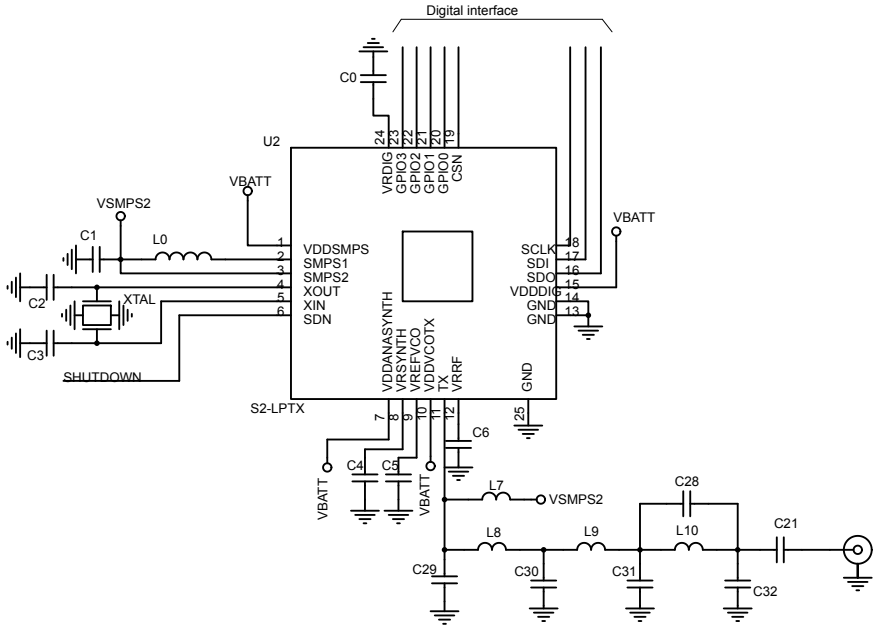


Figure 3. Suggested application diagram (embedded SMPS not used) shows the suggested configuration with discrete matching network and SMPS-OFF mode.

Figure 3. Suggested application diagram (embedded SMPS not used)

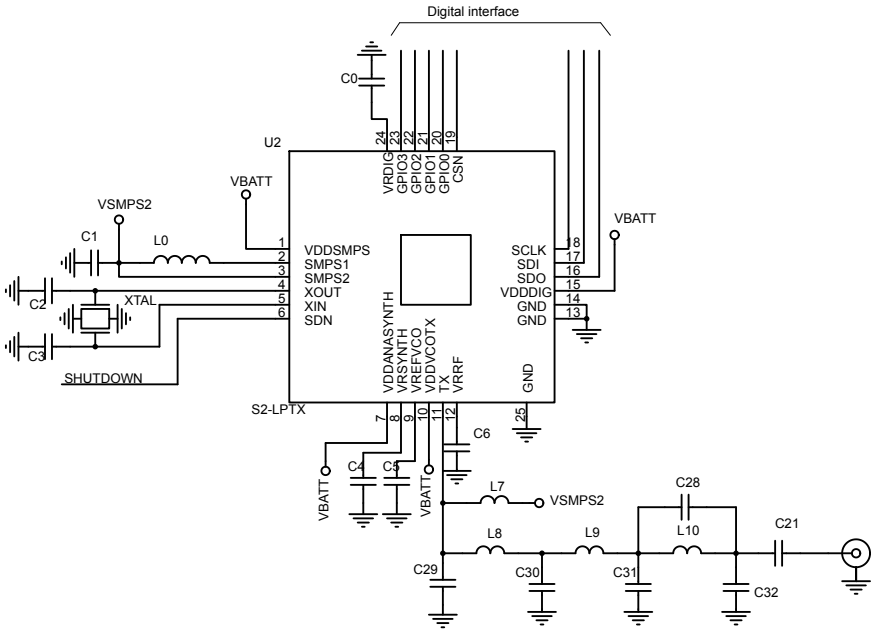


Figure 4. Suggested application diagram HPM/LPM (integrated balun, embedded SMPS used)

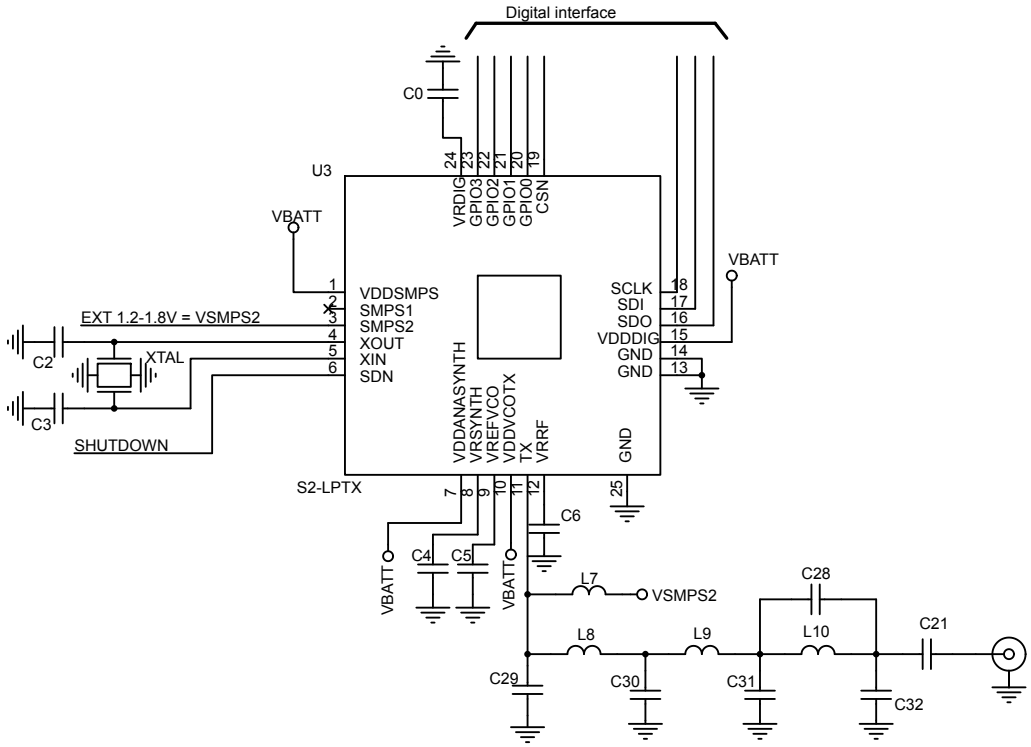
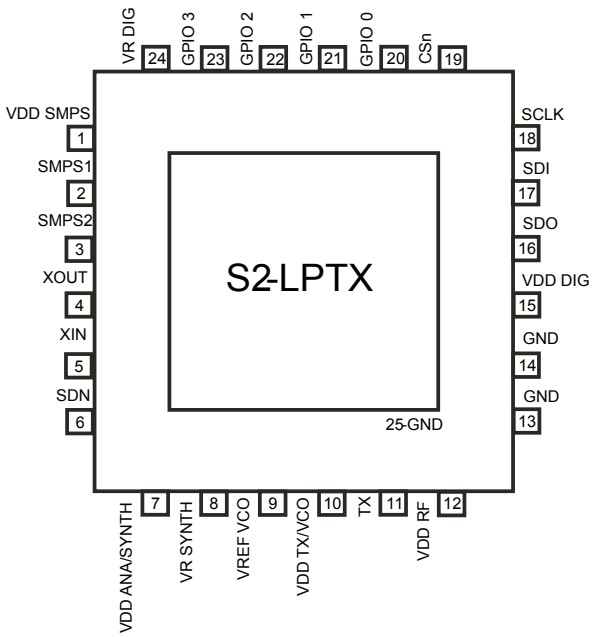


Table 1. Description of the external components of the typical application diagrams

Components	HPM/LPM discrete balun		HPM/LPM integrated balun	Description
	SMPS ON	SMPS OFF		
C0	X	X	X	Decoupling capacitor for on-chip voltage regulator to digital part
C1	X		X	SMPS LC filter capacitors
C2, C3	X	X	X	Crystal loading capacitors
C4	X	X	X	Load capacitor for on-chip voltage regulator to synthesizer (LF part)
C5	X	X	X	Load capacitor for on-chip voltage regulator to VCO
C6	X	X	X	Load capacitor for on-chip voltage regulator
C10			X	Matching capacitors
C16			X	Decoupling capacitor
C21	X	X	X	Decoupling capacitor
C28	X	X		Notch filter capacitor
C29, C30, C31, C32	X	X		Matching capacitors
L0	X		X	SMPS LC filter inductor
L7	X	X	X	RF choke inductor or resonating inductor (upon RF network topology)
L8, L9, L10	X	X		LC filter/matching inductors
XTAL	X	X	X	Crystal

2.1 Pin diagram

Figure 5. Pin diagram, QFN24 (4x4 mm) package



2.2 Pin description

Table 2. Pinout

Number	Pin name	Pin type	Description
1	VDD SMPS	Power	1.8 V to 3.6 V analog power supply for SMPS only.
2	SMPS1	Analog out	1.1 V to 1.8 V SMPS regulator output to be externally filtered
3	SMPS2	Analog in	1.1 V to 1.8 V SMPS voltage input after LC filtering applied to SMPS1 output
4	XOUT	Analog out	Crystal oscillator output. Connect to an external crystal or leave floating if driving the XIN pin with an external clock source
5	XIN	Analog in	Crystal oscillator input. Connect to an external crystal or to an external clock source. If using an external clock source, DC coupling with a minimum 0.2 VDC level is recommended and minimum AC amplitude of 400 mVpp (however, the instantaneous level at input cannot exceed the 0 – 1.4 V range)
6	SDN	Digital in	Shutdown input pin. SDN should be = ‘0’ in all modes, except shutdown mode
7	VDD ANA/ SYNTH	Power	1.8 V to 3.6 V power
8	VR SYNTH	Analog in/out	1.2 V SYNTH-LDO output for decoupling
9	VREF VCO	Analog out	1.2 V VCO-LDO band-gap reference voltage decoupling
10	VDD VCO/TX	Power	1.8 V to 3.6 V power supply
11	TX	RF output	RF output signal
12	VR RF	Analog in/out	1.2 V LDO output for decoupling
13	GND	Ground	Ground of the application board
14	GND	Ground	
15	VDDDIG	Power	1.8 V to 3.6 V power supply
16	SDO	Digital out	SPI slave data output
17	SDI	Digital in	SPI slave data input
18	SCLK	Digital in	SPI slave clock input
19	CSn	Digital in	SPI chip select
20	GPIO0	Digital I/O	General purpose I/O that may be configured through the SPI registers to perform various functions
21	GPIO1	Digital I/O	
22	GPIO2	Digital I/O	
23	GPIO3	Digital I/O	
24	VR DIG	Analog in/out	1.2 V digital power supply output for decoupling
25	GND	Ground	Exposed pad connected to the ground of the application board

3 Specifications

3.1 Absolute maximum ratings

Absolute maximum ratings are those values above which damage to the device may occur. Functional operation under these conditions is not implied. All voltages refer to GND.

Table 3. Absolute maximum ratings

Parameter	Min.	Typ.	Max.	Unit
Supply and SMPS pins	-0.3		+3.9	V
DC voltage on VREG pins	-0.3		+3.9	
DC voltage on digital input pins	-0.3		+3.9	
DC voltage on digital output pins	-0.3		+3.9	
DC voltage on ground pins	-0.3		+3.9	
DC voltage on analog pins	-0.3		+1.8	
DC voltage on TX pin	-0.3		+3.9	
Storage temperature range	-40		+125	°C
VESD-HBM	-500		+500	V

3.2 Operating range

Table 4. Operating range

Parameter	Min.	Typ.	Max.	Unit
Operating battery supply voltage (V_{BAT})	1.8(1)	3.0	3.6	V
Operating ambient temperature range	-40	25	+105	°C

1. *2 V when the device works in boost mode with SMPS ON.*

3.3 Thermal properties

Table 5. Thermal data

Parameter	QFN24	Unit
Thermal resistance junction-ambient	66	°C/W

3.4 Power consumption

Characteristics measured over recommended operating conditions unless otherwise specified. Typical values are referred to 25 °C temperature, V_{BAT} = 3.3 V.

Table 6. Low-power state power consumption

Parameter	Test conditions	Min.	Typ.	Max.	Unit
Supply current	Shutdown	-	2.5	-	nA
	Standby		500		
	Sleep		700		
	Sleep (FIFOs retained)		0.95		µA
	Ready		350		

Table 7. Power consumption fc= 915 MHz

Parameter	Test conditions	Min.	Typ.	Max.	Unit
Supply current	TX CW @ 14 dBm	-	22	-	mA
	TX CW @ 10 dBm(1)		12.5		
	TX CW @ 16 dBm in Boost (2)		32		

1. *SMPS output voltage 1.2 V, LDOs disable.*
2. *SMPS output voltage 1.8 V.*

Table 8. Power consumption fc= 840-868 MHz

Parameter	Test conditions	Min.	Typ.	Max.	Unit
Supply current	TX CW @ 14 dBm	-	20	-	mA
	TX CW @ 10 dBm(1)		11.5		
	TX CW @ 16 dBm in Boost (2)		29		

1. *SMPS output voltage 1.2 V, LDOs disable.*
2. *SMPS output voltage 1.8 V.*

Table 9. Power consumption fc= 434 MHz

Parameter	Test conditions	Min.	Typ.	Max.	Unit
Supply current	TX CW @ 14 dBm(1)	-	21	-	mA
	TX CW @ 10 dBm(2)		11.5		

1. *SMPS output voltage 1.6 V.*
2. *SMPS output voltage 1.2 V, LDOs disable.*

3.5 General characterization

Table 10. General characteristics

Parameter		Typ.	Unit
Frequency range		413 - 479	MHz
		826 - 958	
Data rate DR	2-(G)FSK	0.1 - 250	kbps
	4-(G)FSK	0.2 - 500	
	OOK/ASK	0.1 -125	
Data rate accuracy		±100	ppm
Frequency deviation FDEV		0.15 - 500	kHz

If "Manchester" or "3-out-of-6" or FEC coding options are enabled the actual bit rate is affected as follows:

Table 11. Data rate with different coding options

Coding option	4(G)FSK data rate [kbps]
NRZ	500
FEC	250
Manchester	250
3-out-of-6	333.3

3.6 Frequency synthesizer

Table 12. Frequency synthesizer parameters

Parameter	Test conditions	50 MHz	Unit
Frequency step size	Out-loop divider ratio = 4	23.8	Hz
RF carrier phase noise 433 MHz	10 kHz	-109	dBc/Hz
	100 kHz	-110	
	1 MHz	-124	
	10 MHz	-141	
RF carrier phase noise 868 MHz	10 kHz	-102	
	100 kHz	-103	
	1 MHz	-117	
	10 MHz	-138	
RF carrier phase noise 915 MHz	10 kHz	-102	
	100 kHz	-102	
	1 MHz	-117	
	10 MHz	-138	

3.7 Crystal oscillator

Characteristics measured over recommended operating conditions unless otherwise specified. All typical values are referred to 25 °C temperature, V_{BAT} = 3.0 V.

The device supports crystals in the range [24-26] MHz and [48-52] MHz.

If the crystal is in the [24–26] MHz range, both the analog and the digital parts must work at this frequency. Otherwise, if a crystal in the [48-52] MHz range is used, the analog part must work at this frequency and the digital part at this frequency divided by 2. From now on in this document the XTAL oscillator will be indicated with f_{XO} and the digital clock with f_{dig}

The divider for the digital part can be set by the PD_CLKDIV bit of the XO_RCO_CONFIG1 in the following way:

- if a [48 – 52] MHz crystal is used, this bit must be 0 (digital divider enabled):

$$f_{dig} = \frac{f_{xo}}{2} \quad (1)$$

- if a [24 – 26] MHz crystal is used, this bit must be 1 (digital divider disabled):

$$f_{dig} = f_{xo} \quad (2)$$

The safest procedure to disable the divider without any risk of glitches in the digital clock is to switch into STANDBY mode, hence, disable the divider through register setting, and then come back to the READY state.

In order to avoid potential RF performance degradations, the crystal frequency should be chosen to satisfy the following equation:

$$nF_{CH} - \mathrm{ROUND}\left(n\frac{F_{CH}}{f_{XO}}\right)f_{XO} \geq 1\mathrm{MHz} \quad (3)$$

where n is an integer in the set [1-7, B] (B is the synthesizer's divider ratio).

Table 13. Crystal oscillator characteristics

Parameter	Test conditions	Min.	Typ.	Max.	Unit
Crystal frequency		24		26	MHz
		48		52	
Frequency tolerance (1)			± 40		ppm
Minimum requirement on external reference phase noise mask $f_{XO} = 26$ MHz, to avoid degradation on synthesizer phase/noise	10 kHz			-135	dBc/Hz
	100 kHz			-140	
	1 MHz			-140	
	10 MHz			-140	
Programmable trans-conductance of the oscillator at start-up		13		43	mS
Start-up time (2)	VBAT=1.8 V, $f_{XO} = 26$ MHz		100		µs

1. *Including initial tolerance, crystal loading, aging, and temperature dependence. The acceptable crystal tolerance depends on RF frequency and channel spacing/bandwidth.*
2. *Start-up times are crystal dependent. The crystal oscillator trans-conductance can be tuned to compensate the variation of crystal oscillator series resistance.*

Table 14. Ultra-low power RC oscillator

Parameter	Test conditions	Typ.	Unit
Calibrated frequency	Calibrated RC oscillator frequency is derived from crystal oscillator frequency.	33.3 (1)	kHz
Frequency accuracy after calibration		±1	%

1. *Depending on the crystal frequency, the reported value is referring to 50 MHz*

3.8 RF transmitter

Characteristics measured over recommended operating conditions unless otherwise specified. All typical values are referred to 25 °C temperature, V_{BAT} = 3.3 V.

Table 15. RF transmitter characteristics

Parameter	Test conditions	HPM typ.	LPM typ.	Unit
Maximum output power	CW @ antenna level	14	10	dBm
Maximum output power in boost mode	CW @ antenna level	16	12	
Minimum output power	CW @ antenna level	-30	-30	
Output power step	-10<=output power<=+10 dBm	0.5	0.5	dB
Output power step (1)	Output power>+10 dBm	1(1)		

1. *In this case the register 0x64 is set to 0x4A.*

Table 16. PA impedance

Parameter	Test conditions	Typ.	Unit
Optimum load impedance	433 MHz	56+25j	Ω
	868 MHz	30+24j	
	920 MHz	29+23j	
Max. permitted VSWR @ antenna level	433 MHz	2	
	868 MHz	5	
	920 MHz	5	

Table 17. Regulatory standards

Frequency band	Suitable for compliance with:
413 - 479 MHz	ETSI EN300 220 category 1.5
	FCC part 15, FCC part 90
	ARIB STD-T67
	Chinese SRRC
826 - 958 MHz	ETSI EN300 220-2 category 1.5
	FCC part 15
	ARIB STD-T108

3.8.1 Harmonic emission at 433 MHz

Table 18. Harmonic emission at 433 MHz

Parameter	Test conditions	SMPS on	Unit
H1	CW	14	dBm
H2	CW	-51	
H3	CW	-56	
H4	CW	-39	
H5	CW	-34	
H6	CW	-46	
H7	CW	-44	

3.8.2 Harmonic emission at 840-868 MHz

Table 19. Harmonic emission at 840-868 MHz

Parameter	Test conditions	HPM/LPM/SMPS on	Unit
H1	CW	14	dBm
H2	CW	-38	
H3	CW	-54	
H4	CW	-52	
H5	CW	-52	
H6	CW	-43	
H7	CW	-51	

3.8.3 Harmonic emission at 915 MHz

Table 20. Harmonic emission at 915 MHz

Parameter	Test conditions	HPM/LPM/SMPS on	Unit
H1	CW	14	dBm
H2	CW	-46	
H3	CW	-55	
H4	CW	-46	
H5	CW	-49	
H6	CW	-48	
H7	CW	-51	

3.9 Digital interface specification

Table 21. Digital SPI input, output and GPIO specification

Parameter	Test conditions	Min.	Typ.	Max.	Unit
SPI clock frequency			8	10	MHz
Port I/O capacitance			1.4		pF

Parameter	Test conditions	Min.	Typ.	Max.	Unit
Rise time	From 0.1*VDD to 0.9*VDD, CL=20 pF (low output current programming)		6.0		ns
	From 0.1*VDD to 0.9*VDD, CL=20 pF (high output current programming)		2.5		
Fall time	From 0.1*VDD to 0.9*VDD, CL=20 pF (low output current programming)		7.0		ns
	From 0.1*VDD to 0.9*VDD, CL=20 pF (high output current programming)		2.5		
Logic high level input voltage		VDD/2 +0.3			V
Logic low level input voltage				VDD/8 +0.3	V
High level output voltage	IOH = -2.4 mA (-4.2 mA into high output current mode).	(5/8)* VDD+ 0.1			V
Low level output voltage	IOL = +2.0 mA (+4.0 mA into high output current mode).			0.5	V
CSn low to positive edge on SCLK in low power mode state			40		µs
CSn low to positive edge on SCLK in ready state		30			ns

3.10 Battery indicator

Characteristics measured over recommended operating conditions unless otherwise specified. All typical values are referred to 25 °C temperature, V_{BAT} = 3.0 V.

Table 22. Battery indicator and low battery detector

Parameter	Test conditions	Min.	Typ.	Max.	Unit
Battery level thresholds #1			2.1		V
Battery level thresholds #2			2.3		
Battery level thresholds #3			2.5		
Battery level thresholds #4			2.7		
Brownout threshold	Measured in slow battery variation (static) conditions (inaccurate mode)		1.5		
	Measured in slow battery variation (static) conditions (accurate mode)		1.7		
Brownout threshold hysteresis			70		mV

Note: For battery-powered equipment, the TX does not transmit at a wrong frequency under low battery voltage conditions. It remains on either channel or stops transmitting. The latter can of course be realized by using a lock detect and/or by switching off the PA under control of the battery monitor. For testing reasons this control is enabled/disabled by SPI.

4 Block description

4.1 Power management

The S2-LPTX integrates a high efficiency step-down converter cascaded with LDOs meant to supply both analog and digital parts. However, an LDO directly fed by the external battery provides a controlled voltage to the data interface block.

The S2-LPTX power management (PM) strategy, besides the basic functionality of providing different blocks with proper supplies, faces two main constraints: the first one is to implement such a power distribution with maximum efficiency, and the second one is to guarantee the isolation among critical blocks.

The efficiency target is obtained by using a switch mode power supply (SMPS) which converts the battery voltage (1.8 V - 3.6 V) to a lower voltage (settable from 1.2 V to 1.8 V) with efficiency higher than 90%.

The SMPS output voltage can be controlled by the SET_SMPS_LVL field in the PM_CONF0 register. The relation between the SET_SMPS_LVL and the V_{OUT} of the SMPS is given by the following table:

Table 23. SMPS output voltage

SET_SMPS_LVL	SMPS output voltage
001b	1.2 V
010b	1.3 V
011b	1.4 V
100b	1.5 V
101b	1.6 V
110b	1.7 V
111b	1.8 V

The SMPS switching frequency is settable by the 2 registers PM_CONF3 and PM_CONF2.

If the KRM_EN is 0, then the digital divider by 4 enabled. In this case SMPS' switching frequency is:

$$F_{sw} = \frac{f_{dig}}{4} \quad (4)$$

If the KRM_EN is 1, the SMPS' switching frequency can be set by the KRM word according to the formula:

$$F_{sw} = K_{rm}\frac{f_{dig}}{2^{15}} \quad (5)$$

As f_{dig} is the digital domain frequency (f_{XO} if it is 24, 25 or 26 MHz) and ($\frac{f_{XO}}{2}$ if f_{XO} is 48, 50 or 52 MHz).

The isolation target is reached by using, for each critical block, a dedicated linear low-dropout regulator (LDO), which provides typically 1.2 V output voltage, either from battery level or from SMPS level, depending from the operating mode.

The S2-LPTX PM can be configured by SPI (BYPASS_LDO field in PM_CONFIG [1] register) in two main modes:

1. High performance mode (HPM)
2. Low power mode (LPM)

In HPM all available LDOs supplied from SMPS are used, to get the best possible isolation and minimum low-frequency noise level and SMPS ripple. SMPS must be set to 1.4 V at least.

In LPM the LDOs connected to the SMPS are by-passed and SMPS must be configured to provide 1.2 V output level to increase the regulation efficiency but with reduced isolation and higher low-frequency noise and SMPS ripple.

The load inductor of the SMPS has to have the following characteristics:

- A typical 10 µH nominal value +/-10%

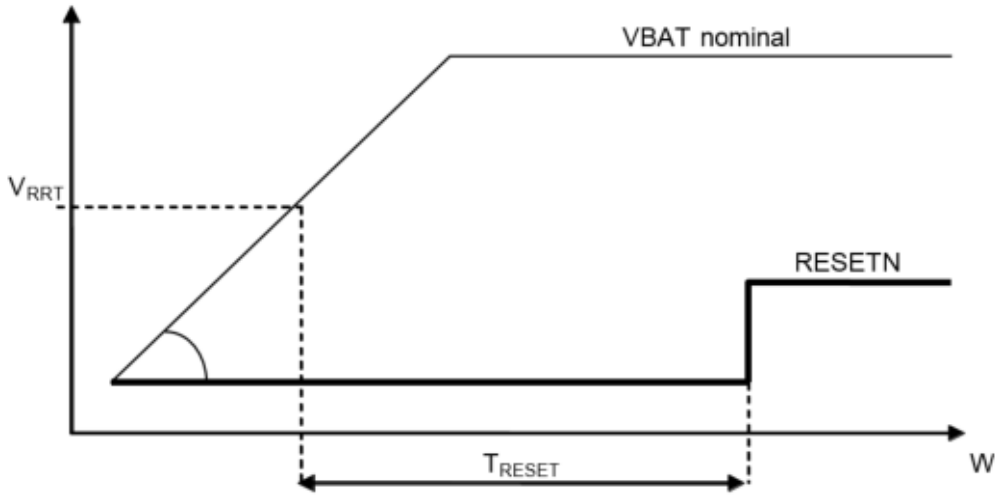
- A rated current of 100 mA minimum
- A DC resistance as low as possible (to guarantee maximum efficiency of the SMPS block), around 1 Ω is a typically good value, but the lower the better

4.2 Power-On-Reset

The Power-On-Reset (POR) circuit generates a reset pulse upon power-up which is used to initialize the entire digital logic. Power-on-reset senses V_{BAT} voltage.

The S2-LPTX provides an automatic POR circuit, which generates an internal RESETN (active low) level for a time T_{RESET}, after the V_{BAT} reaches the reset release voltage threshold V_{RRT}, as shown in Figure 6. Power-On-Reset timing and limits. The same reset pulse is generated after a step-down on the input pin SDN (VDD>V_{RRT}). This signal is available on the GPIO0 pin.

Figure 6. Power-On-Reset timing and limits



The parameters VRRT and TRESET are fixed by design in order to guarantee a reliable reset procedure of the state machine. In addition, all the registers are initialized to their default values.

A software command SRES is also available, it generates an internal but partial resetting of the S2-LPTX.

Table 24. POR parameters

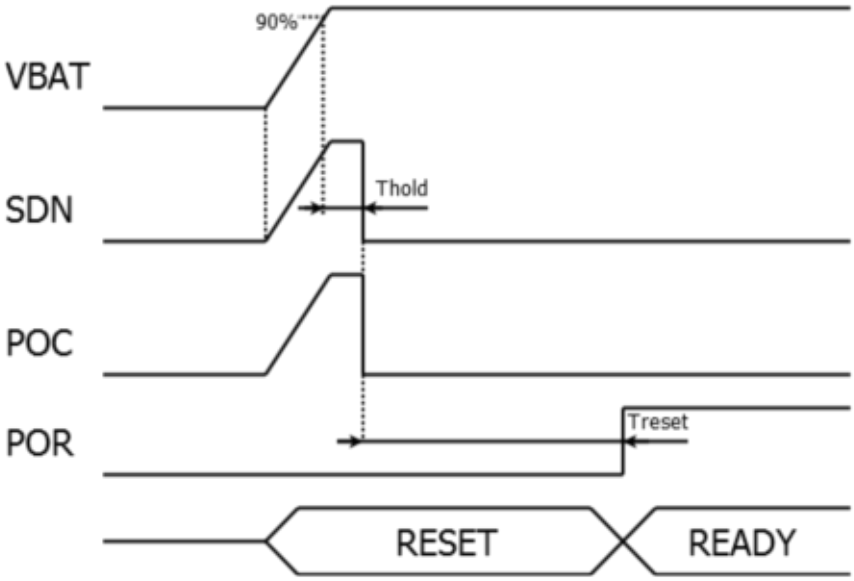
Parameter	Comment	Min.	Typ.	Max.	Unit
Reset start-up threshold voltage			0.5		V
Hold pulse width (T_{hold}, figure below)	For SDN to be effective	1			µs
Reset pulse width (T_{reset}, figure below)			0.7	2	ms
Power-on VDD slope			2.0		V/ms

The following picture shows how the S2-LPTX must be controlled, i.e. the SDN signal must be tied to VBAT pin in order to avoid two potential issues during the start-up phase:

1. A cross conduction can appear on the GPIO until an available command is present on it.
2. The ESD protection diode from the SDN pad can sink current from the external driver connected to the SDN.

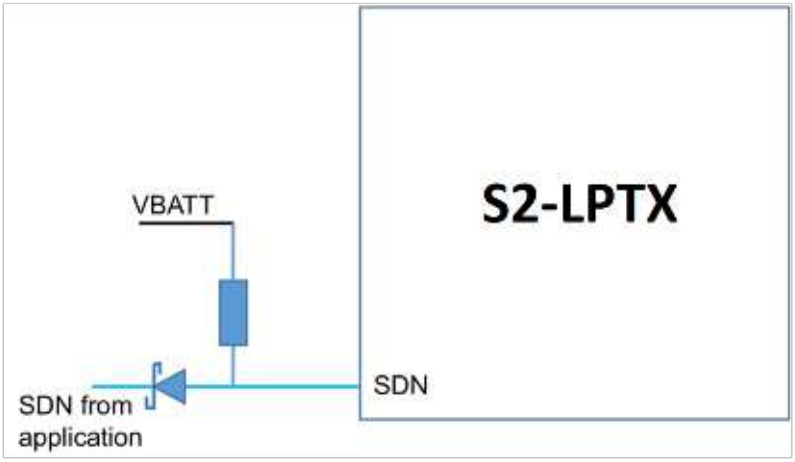
Also the SDN signal generates an internal signal (POC), which disables the digital I/Os when set to 1.

Figure 7. **Start-up phase**



Examples of possible connections

Figure 8. **Examples of possible connections for SDN pin**



4.3 RF synthesizer

A crystal connected to XIN and XOUT provides a clock signal to the frequency synthesizer. The allowed clock signal frequency is either 24, 25, 26, 48, 50, or 52 MHz.

As an alternative, an external clock signal feeds XIN for proper operation. In this option, XOUT can be left either floating or tied to ground.

Since the digital macro cannot be clocked at that double frequency (48, 50 or 52 MHz), a divided clock is used in this case (see Crystal oscillator).

The integrated phase locked loop (PLL) is capable to synthesize a band of frequencies from 413 to 479 MHz, 826 to 958 MHz, providing the input signal for the PA in the TX chain.

Depending on the RF frequency and channel used, a very high accurate crystal or TCXO can be required.

The RF synthesizer implements fractional sigma delta architecture to allow fast settling and narrow channel spacing. It is fully integrated, and it uses a multi-band VCO to cover the whole frequency range. All internal calibrations are automatic.

According to the frequency synthesized the user must set the charge pump current according to the LO frequency variations, in order to have a constant loop bandwidth. The charge pump current is controlled by the PLL_CP_ISEL field (SYNT3 register) and the PLL_PFD_SPLIT_EN (SYNTH_CONFIG2). These fields should be set in the following way:

Table 25. Charge pump words

VCO Freq (MHz)	fxo (MHz)	PLL_CP_ISEL	PLL_PFD_SPLIT_EN	ICP (µA)
3760	50	010	0	120
3760	25	001	1	200
3460	50	011	0	140
3460	25	010	1	240

The S2-LPTX provides an automatic and very fast calibration procedure for the frequency synthesizer. If not disabled, it performs the calibration each time the synthesizer is required to lock to the programmed RF channel frequency (transaction from READY to LOCK/TX/). After completion, the S2-LPTX uses the calibration word and is stored in registers.

In order to get the synthesizer locked with the calibration procedure disabled, the correct calibration words must be previously stored in registers by user. The advantage is reduce the LOCK setting time.

The transition time enables the S2-LPTX for frequency hopping operation due to its reduced response time and very quick programming synthesizer.

4.3.1 RF channel frequency settings

The channel center frequency can be programmed as follows:

Center frequency setting

$$f_C = f_{base} + \left(\frac{f_{XO}}{2^{15}} \cdot CHSPACE\right) \cdot CHNUM \quad (6)$$

The f_{base} sets the main channel frequency; the value depends on the value of f_{xo} (the frequency of the XTAL oscillator, typically 24-26 MHz or 48-52 MHz.

Base frequency setting

$$f_{base} = \frac{f_{XO}}{\frac{B}{2} \cdot D} \cdot \frac{SYNT}{2^{20}} \quad (7)$$

where:

SYNT is a programmable 28-bits integer (SYNT[3:0] registers).

B is the out-of-loop SYNTH divider (BS field of the SYNT3 register):

PLL divider

$$B = \begin{cases} 4\ for\ the\ high\ band & (826\ MHz\ to\ 958\ MHz,\ BS = 0) \\ 8\ for\ the\ middle\ band & (413\ MHz\ to\ 479\ MHz,\ BS = 1) \end{cases} \quad (8)$$

D is the reference divider (REFDIV bit of XO_RCO_CONFIG0 register)

Reference divider

$$D = \begin{cases} 1\ if\ REFDIV = 0\ (internal\ reference\ divider\ is\ disabled) \\ 2\ if\ REFDIV = 1\ (internal\ reference\ divider\ is\ enabled) \end{cases} \quad (9)$$

The resolution in the programmed value of the base frequency depends on the actual band selected.

Table 26. **Resolution frequency**

fxo [MHz]	High band resolution [Hz]	Low band resolution [Hz]
24	11.4	5.7
25	11.9	6.0
26	12.4	6.2
48	22.9	11.4
50	23.8	11.9
52	24.8	12.4

The f_c is the frequency related to the channel specified. RF channels can be defined using the CHSPACE and CHNUM registers. In this way, it is possible to change faster the channel by changing just an 8-bits register, allowing the setting of 256 channels and frequency-hopping sequences. The actual channel spacing is from 793 Hz to 202342 Hz in 793 Hz steps for the 26 MHz configuration and from 1587 to 404685 Hz in 1587 Hz steps for the 52 MHz configuration.

Table 27. **Channel spacing resolution**

fxo [MHz]	Channel spacing resolution [Hz]
24	732.42
25	762.94
26	793.45
48	1464.84
50	1525.88
52	1586.91

4.4 Digital modulator

The S2-LPTX supports frequency modulation: 2-FSK, 4-FSK, 2-GFSK, 4-GFSK as well amplitude modulation OOK and ASK. Using register, the user can also program an unmodulated carrier for lab test and measurement. A special mode, direct polar modulation, allows building specific modulation scheme controlling directly the amplitude and the frequency of the carrier synthesized. The register MOD_TYPE is used to select one of the following modulation scheme.

Table 28. **Modulation scheme**

MOD_TYPE	Modulation scheme
0000b	2-FSK
0001b	4-FSK
0010b	2-GFSK
0011b	4-GFSK
0101b	ASK/OOK
0110b	Direct polar (TX only)
0111b	CW

4.4.1 Frequency modulation

For frequency modulation 2-(G)FSK and 4-(G)FSK the frequency deviation can be tuned in wide range that depends on f_{xo} (XTAL frequency) according the following formula:

Frequency deviation

$$f_{dev} = \begin{cases} \frac{f_{XO}}{2^{19}} \cdot \frac{round\left(D \cdot FDEV_M \cdot {}^{B}/_{8}\right)}{D \cdot B} & if\ FDEV_E = 0 \\ \frac{f_{XO}}{2^{19}} \cdot \frac{round\left(D \cdot \left(256 + FDEV_M\right) \cdot 2^{(FDEV_E\ -\ 1)} \cdot {}^{B}/_{8}\right)}{D \cdot B} & if\ FDEV_E\ > 0 \end{cases} \quad (10)$$

Where f_{xo} is the XTAL oscillation frequency, D is the reference divider and B is the band selector.

The frequency deviation programmed corresponds to the deviation of the outer constellation symbols. The deviation of the inner symbols is 1/3 of such programmed values, as reported in the table below, where 4 options are available.

Furthermore, since the payload is normally arranged in bytes, the arrangement can change the mapping for both 2-(G)FSK and 4-(G)FSK modulations, by using the CONST_MAP (register MOD1), in the following way:

Table 29. Constellation mapping 2-(G)FSK

Format	Symbol	CONST_MAP coding			
		0	1	2	3
2-(G)FSK	0	-FDEV	NA	+FDEV	NA
	1	+FDEV	NA	-FDEV	NA

Table 30. Constellation mapping 4-(G)FSK

Format	Symbol	CONST_MAP coding			
		0	1	2	3
4-(G)FSK	00	-FDEV/3	-FDEV	+FDEV/3	+FDEV
	01	-FDEV	-FDEV/3	+FDEV	+FDEV/3
	10	+FDEV/3	+FDEV	-FDEV/3	-FDEV
	11	+FDEV	+FDEV/3	-FDEV	-FDEV/3

Furthermore, in the 4-(G)FSK it is also possible to swap the symbols using the 4FSK_SYM_SWAP field (register PCKTCTRL3) as follows:

$$\text{When 4FSK_SYM_SWAP} = 0: \begin{cases} S0 = < b7b6 > \\ S1 = < b5b4 > \\ S2 = < b3b2 > \\ S3 = < b1b0 > \end{cases} \quad (11)$$

$$\text{When 4FSK_SYM_SWAP} = 1 \begin{cases} S0 = < b6b7 > \\ S1 = < b4b5 > \\ S2 = < b2b3 > \\ S3 = < b0b1 > \end{cases}$$

4.4.1.1 *Gaussian shaping*

In 2-GFSK or 4-GFSK mode, the Gaussian filter BT product can be set by using the register BT_SEL to 1 or 0.5.

The Gaussian filtering is implemented by poly-phase filtering with eight taps per symbol time. In order to further smooth the filter shape and improve spectral shaping, the output of the filter can be linearly interpolated by setting the register MOD_INTERP_EN.

A mathematical interpolation factor is applied at each sample of the Gaussian filter output. This factor is 64 for data rates corresponding to DATA_RATE_E < 5, it is automatically scaled as $\frac{64}{2^{DATA_RATE_E-5}}$ for 5 ≤ DATA_RATE_E < 11 and it is automatically disabled for DATA_RATE_E = 11.

Note: The actual interpolation factor achieved may be limited by the minimal frequency resolution of the frequency synthesizer.

4.4.2 Amplitude modulation

Amplitude modulation OOK and ASK are both supported by the S2-LPTX. The ASK selection depends on power ramping enable.

When OOK is selected, a bit '1' is transmitted with a programmed power, set by register PA_POWER[PA_LEVEL_MAX_INDEX], and a bit '0' is transmitted without output power (PA off) and specified by the register PA_POWER[0].

In case PA_POWER[0] = 0 then the modulation will be OOK, otherwise when PA_POWER[0] is not set to zero the modulation will be ASK. The 0/1 mapping can be reversed by setting the CONST_MAP register to any value other than zero.

When ASK is selected, a bit '1' is transmitted with a power ramp increasing from the minimum value specified by register PA_POWER[0] to specified PA maximum level in register PA_POWER[PA_LEVEL_MAX_INDEX], vice versa for a bit '0'. The duration of each power step is a multiple of 1/8 of the symbol time, configurable with the register PA_RAMP_STEP_WIDTH. If more '1's are transmitted consecutively, the PA power maintains the output power at the programmed value. If more '0's are transmitted consecutively, the PA power remains at minimum power for all '0's following the first one.

In order to improve the spectral emission mask in ASK a digital interpolation optional features have been implemented. When this feature is enabled, thought the register PA_INTERP_EN, the modulator linearly interpolates the power values specified in the PA_POWER registers before being applied to the PA.

The interpolation factor of each ramp step is 64 time the data rate corresponding to DATA_RATE_E < 5 it is automatically scaled as $64/2^{(DATA_RATE_E-5)}$ for 5 ≤ DATA_RATE_E < 11 and it is automatically disabled for DATA_RATE_E=11.

Note that the number of clock cycles between successive PA ticks, for DATA_RATE_E≥5, is always between 8 and 4 (8 for DATA_RATE_M=0; 4 for DATA_RATE_M=65535).

4.4.2.1 *OOK smoothing*

The OOK can be smoothed using a FIR filter added in the data path. This feature is activated by setting the FIR_EN bit at 1 inside register PA_CONFIG1.

The FIR filter is not fully customizable but it can be set in 3 different configurations that change the spectrum shape (and thus the bandwidth):

- **filter**: it is the proper FIR filtering function of the stream of bits 8 times oversampled;
- **ramp**: the FIR filter is optimized to perform a ramping between PA_POWER_MAX and PA_POWER_0 (for OOK should be set to 0).
- **switch**: logic 1s and 0s are associated with a single value of power and no transition between the 2 is envisaged.

When the FIR_EN bit is 1, the DIG_SMOOTH_EN (PA_POWER_0 register) must be set to 1.

Finally, a 2nd order Bessel analog filter can be used to smooth the output signal. The bandwidth of this filter should be set according to the data rate used by setting the PA_FC field of the register PA_CONFIG0 according to the following table:

Table 31. PA Bessel filter words

PA_FC bits	Cut-off frequency (kHz)	Max. data rate (kbit/s)
00	12.5	16
01	25	32
10	50	62.5
11	100	125

Note: The FIR ramping modes are used in a mutually exclusive way with the digital ramping. When the digital ramping is used, the FIR ramping should be disabled. Vice versa, if the FIR ramping is used, the digital one is not used.

4.4.3 Direct polar mode

The S2-LPTX allows the user to drive the SYNTH and the PA at a very low level. The byte couples written in the TX_FIFO are sampled with a rate related to the DATARATE chip setting (sampling rate = 8*DATARATE).

The first byte of the couple drives the frequency synthesizer to obtain an instantaneous output frequency deviation given by the formula below:

Frequency deviation in polar mode

$$fdev = fdev_programmed * \frac{fdev_fifo_sample}{128} \quad (12)$$

Where $fdev_programmed$ is the frequency deviation programmed in the chip by the registers MOD[1:0] (see Section 4.4.1 Frequency modulation), $fdev_fifo_sample$ is the first byte of the bytes couple sampled from the TX_FIFO.

The $fdev_fifo_sample$ is interpreted as a 2-complement 8-bit number, thus it can be either a positive or a negative value.

The instantaneous frequency is given by the formula:

Instantaneous frequency in polar mode

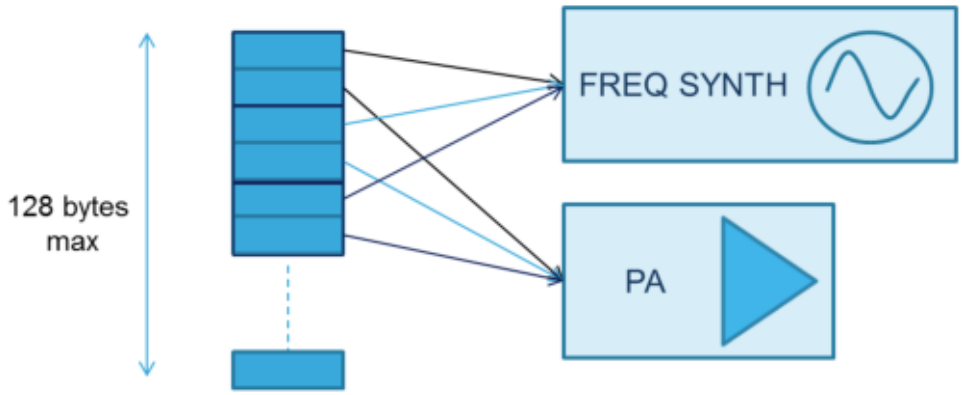
$$f = fc_programmed + fdev \quad (13)$$

The second byte of the TX_FIFO couple drives the PA giving an instantaneous output power.

The output power will be generated according to this value following the same code as the PA_POWER registers (see Section 4.4.6.1 PA configuration).

Figure 9. Direct polar mode shows how the byte couples are sampled from the TX FIFO and sent to the SYNTH and PA blocks.

Figure 9. Direct polar mode



As for the normal TX operations, the TX_FIFO samples are consumed and a management of the TX_FIFO_THRESHOLD is needed to perform transmissions longer than 128 samples.

The transmission is never automatically stopped and a specific command SABORT should be given to terminate it.

This function is suitable to implement differential binary phase shift keying modulation (DBPSK) such as the data modulation used by the SigFox protocol.

4.4.4 Test modes

4.4.4.1 Continuous wave

The device can be programmed to generate a continuous wave carrier without any modulation. In this way, the carrier will be continuously transmitted until a SABORT command is sent to the device.

To set the continuous wave the MOD_TYPE field (of the MOD2 register) must be set to 0x7.

4.4.4.2 *PN9*

It is possible to set a pseudo random binary sequence 9 (PN9) as data source for the modulator. In this way, these data are continuously modulated until a SABORT command is sent to the device.

The TXSOURCE field (of the PCKTCTRL1 register) must be set to 0x03.

4.4.5 Data rate

The data rate programmable is from 0.1 kbps to 500 kbps (see Table 1. Description of the external components of the typical application diagrams for further details).

The data rate formula that relates the value of the DATARATE_M and DATARATE_E registers to the data rate in symbol per second is the following:

Data rate formula

$$DataRate = \begin{cases} f_{dig} \cdot \dfrac{DATARATE_M}{2^{32}} & if\ DATARATE_E = 0 \\ f_{dig} \cdot \dfrac{\left(2^{16} + DATARATE_M\right) \cdot 2^{DATARATE_E}}{2^{33}} & if\ DATARATE_E > 0 \\ \dfrac{f_{dig}}{8 \cdot DATARATE_M} & if\ DATARATE_E = 15 \end{cases} \quad (14)$$

where f_{dig} is the digital clock frequency.

In the cases where DATARATE_E<15, the actual modulator timing is generated by a fractional clock divider hence is affected by a certain amount of jitter. In order to have a jitter free data rate generation a specific mode the last equation must be used, DATARATE_E = 15.

4.4.6 Transmitter

The S2-LPTX contains an integrated PA capable of transmitting at output levels programmable between -30 dBm to +14 dBm (+16 dBm in boost mode), at step of 0.5 dB.

The PA is single-ended and has a dedicated pin (TXOUT). The PA output is ramped up and down to prevent unwanted spectral splatter. In TX mode the PA drives the signal generated by the frequency synthesizer out to the antenna terminal. Delivered power, as well as harmonic content, depends on the external impedance seen by the PA. It is possible to program TX to send an unmodulated carrier.

The output stage is supplied from the SMPS through an external choke and is loaded with a LC-type network which has the function of transforming the impedance of the antenna and filter out the harmonics.

4.4.6.1 *PA configuration*

The PA output power level is programmable in 0.5 dB steps. The user can store up to eight output levels to provide flexible PA power ramp-up and ramp-down at the start and end of a frequency modulation transmission as well as ASK modulation shaping.

With the digital power-ramping enabled (PA_RAMP_EN = 1 in the PA_POWER0 register) the ramp starts from the minimum output power programmed and stops at the programmed maximum value, thus a maximum of 8 steps can be set up as shown in Figure 10. Output power ramping configuration. The interpolation factor ranges from 64 down to 1 depending on the actual data rate. The assumption is that output power monotonically decrease. Each step is held for a programmable time interval expressed in terms of bit period units ($T_b/8$), maximum value is 3 (which means $4 \times T_b/8 = T_b/2$). Therefore, the PA ramp may last up to 4 T_b (about 3.3 ms if the bit rate is 1.2 kbit/s).

$$T_{ramp} = \frac{(PA_RAMP_STEP_LEN + 1) \times (PA_LEVEL_MAX_IDX + 1)}{8 \times DataRate} \quad (15)$$

where *DataRate* is the transmission data rate expressed in symbols/s.

The set of eight levels is used to shape the ASK signal. In this case, the modulator works as a counter that counts when transmitting a one and down when transmitting a zero. The counter counts at a rate equal to 8 times the symbol rate (in this case, the step width is fixed by symbol rate).

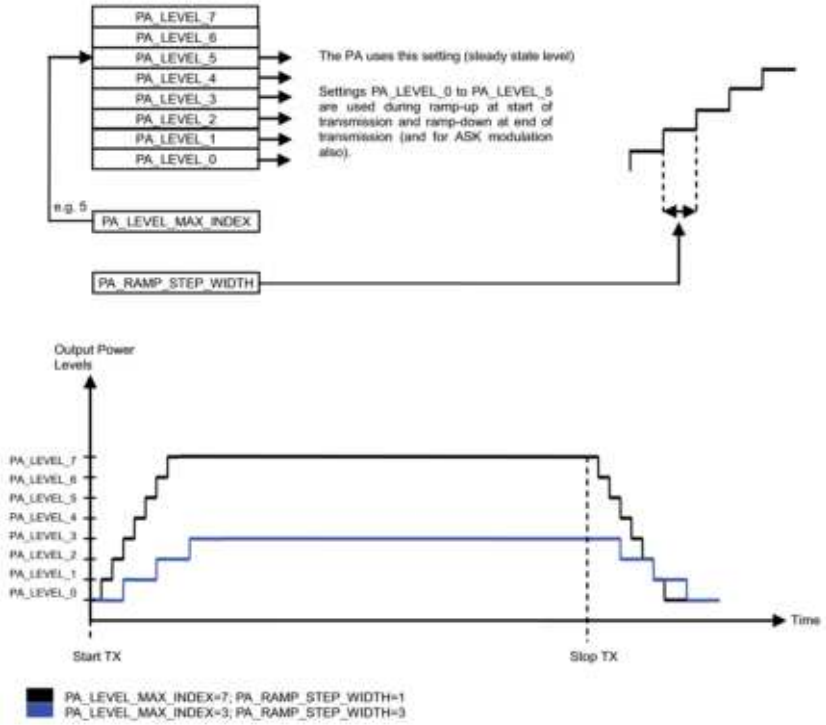
For OOK modulation, the signal is abruptly switched between two levels only: no power and maximum. This mode is obtained setting the PA_RAMP_EN=0.

With the digital power-ramping, the digital PA interpolation can be enabled through the PA_INTERP_EN field of the MOD1 register.

When this feature is enabled, the power values specified in the PA_POWER registers are linearly interpolated by the modulator before being applied to the PA.

The mathematical interpolation factor applied at each output sample is 64 for data rates corresponding to DATA_RATE_E < 5, it is then automatically scaled as $\frac{64}{2^{DATA_RATE_E-5}}$ and it is automatically disabled for DATA_RATE_E = 11.

Figure 10. Output power ramping configuration



4.4.6.2 *Transmitter data modes*

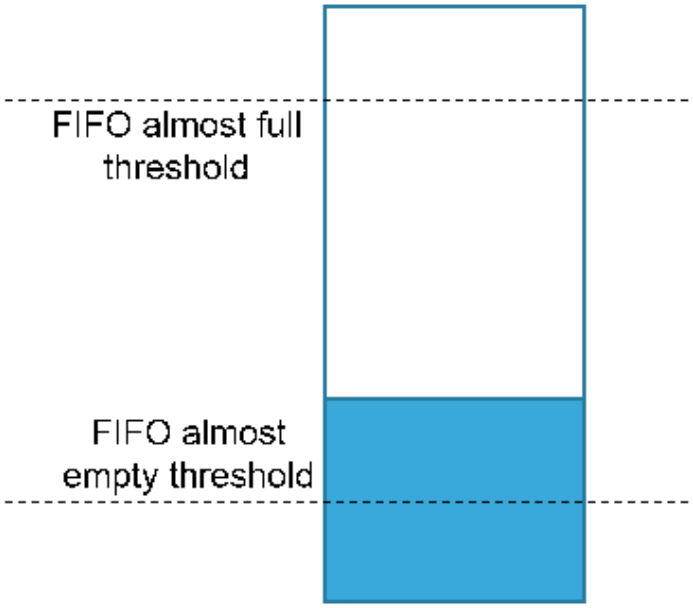
Direct modes are primarily intended to completely bypass the automatic packet handler, in order to give the user maximum flexibility in the choice of frame formats. In specific:

- **Direct through FIFO mode**: the packet is written in TX FIFO. The user build the packet according to his need including preamble, payload and soon on. The data are transmitted without any processing.
- **Direct through GPIO mode**: the packet bits are continuously read from one of the GPIO pins, properly configured, and transmitted without any processing. To allow the synchronization of an external data source, a data clock signal is also provided on one of the GPIO pins. Data are sampled by the device on the rising edge of such clock signal; it is the responsibility of the external data source to provide a stable input at this edge.
- **PN9 mode**: a pseudo-random binary sequence is generated internally. This mode is provided for test purposes only.

4.4.6.3 *Data FIFO*

In the S2-LPTX there is a TX FIFO for data to be transmitted of 128 bytes. The SPI interface is used to write to the TX FIFO starting from the address 0xFF.

Figure 11. **Threshold in FIFO**



The TX FIFO has two programmable thresholds (see figure above). An interrupt event occurs when the data in the TX FIFO reaches any of these thresholds. The first threshold is the “FIFO Almost Full” threshold, TX_AF_THR registers. The value in this field corresponds to the desired threshold value in number of bytes + 2. When empty locations (free) amount inside the TX FIFO reaches this threshold limit, an interrupt to the MCU is generated so it can send a TX command to transmit the contents of the TX FIFO. The second threshold for TX is the “FIFO Almost Empty” threshold, TX_AE_THR register. When the data being shifted out of the TX FIFO reaches the Almost Empty threshold, an interrupt will be generated also. The MCU could to switch out of TX mode or fill new data into the TX FIFO.

To enable the TX_FIFO thresholds interrupts the FIFO_GPIO_OUT_MUX_SEL must be set to 0.

The FIFO controller detects overflow or underflow in the TX FIFO. It is the responsibility of the MCU to avoid TX FIFO overflow since the MCU only can decide to writing on the TX FIFO. A TX FIFO overflow results in an error in the TX FIFO content, while an underflow results in the continuous transmission of the last byte stored in the TX FIFO.

When an overflow or an underflow is detected, the MCU has to issue a SABORT and a FLUSHTXFIFO command before resuming the normal transmitter activity. Regarding to FIFO, when one of these errors is detected an interrupt is generated to the MCU.

The TX FIFO may be flushed by issuing a FLUSHTXFIFO command (see Table 1. Description of the external components of the typical application diagrams).

The full status of FIFO is readable on the bit MC_STATE[10] = TX_FIFO_FULL of the MC_STATE registers, and at the same time, the related IRQs is generated.

In the SLEEP state, the FIFO content is retained only if the SLEEP_B mode is selected (bit SLEEP_MODE_SEL=1 in the register 0x79).

4.4.7 Integrated RCO

The S2-LPTX contains an ultra-low power RC oscillator with accuracy better than 1%. The RC oscillator frequency is calibrated using as a reference the XO frequency. It depends on two values: raw (4 bits) and fine (5 bits). The raw value is obtained by a linear search algorithm in which for each value a counting of half clock reference inside the period of RCO is done. When the correction is near to the final value, a dichotomy search algorithm starts.

The RCO calibration starts as soon as the RCO_CALIBRATION bit is set to 1. When it finishes, the RC_CAL_OK bit is set and the ERROR_LOCK bit is reset.

Moreover, after a sleep or standby state, if the RCO_CALIBRATION bit is kept to 1, when the device returns to the ready state, an RCO calibration automatically runs to compensate some drift.

It is possible to perform an offline calibration of the RCO using the following procedure:

1. Enable the RCO CALIB setting the bit to 1
2. Wait until the RC_CAL_OK becomes 1
3. Copy the RWT_OUT and RFB_OUT (registers 0x94 and 0x95) out values in the RWT_IN and RFB_IN fields (registers 0x6E and 0x6F)
4. Disable the RCO CALIB setting the bit to 0

In this way, the RCO works with these values. It is advisable to repeat the RCO calibration to reject effects related to the variation of temperature. It is recommended to use this procedure if the following SLEEP time (i.e. when using LDC mode) is shorter or comparable to the calibration time.

By default, the calibration is disabled at reset to avoid using an out-of-range reference frequency, after the internal clock divider is correctly configured, the user can enable the RCO calibration by register.

Once calibrated, the RCO generates a clock frequency that depends on the XO frequency used:

Table 32. RCO Frequency

Ref. frequency [MHz]	RCO frequency [kHz]
24 or 48	32
25 or 50	33.33
26 or 52	34.66

4.4.8 Low battery indicator

The battery indicator can provide the user with an indication of the battery voltage level.

There are two blocks to detect battery level:

- Brownout with a fixed threshold
- Battery level detector with a programmable threshold

The MCU enables optionally these blocks to provide an early warning of impending power failure. It does not reset the system, but gives the MCU time to prepare for an orderly power-down and provides hardware protection of data stored in the program memory.

The low battery indicator function is available in any of the S2-LPTX operation modes. As this function requires the internal bias circuit operation, the overall current consumption in STANDBY, SLEEP, and READY modes increase by 400 µA.

4.4.9 Voltage reference

This block provides the precise reference voltage needed by the internal circuit.

4.5 Operating modes

The S2-LPTX is provided with a built-in main controller which controls the switching to the transmitter (TX) state, driven by SPI commands.

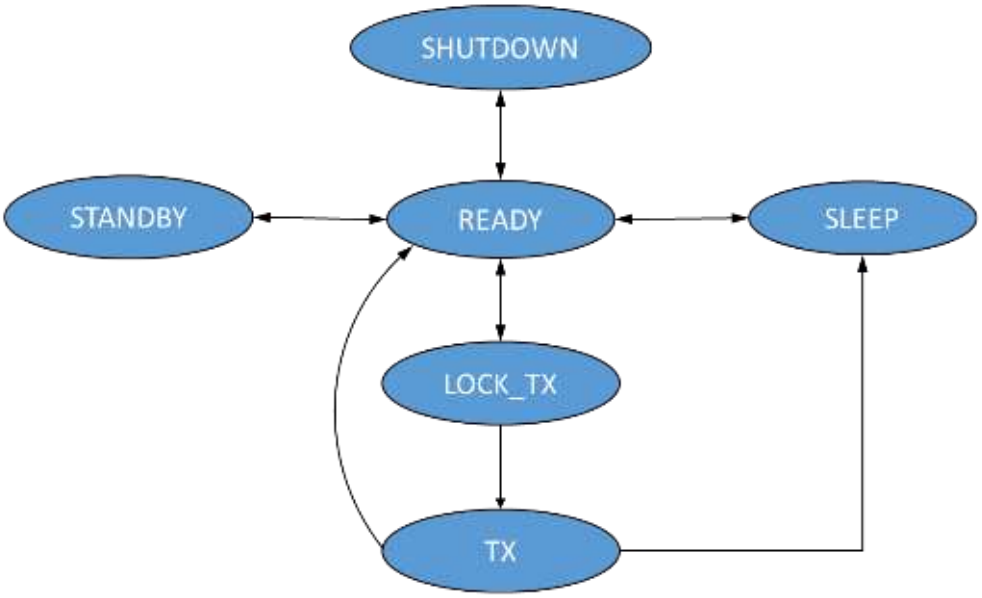
In shutdown condition (the S2-LPTX can be switched on/off with the external pin SDN), no internal supply is generated, and all stored data and configurations are lost.

From shutdown, the S2-LPTX can be switched on going to READY state, where the reference clock signal is available.

From READY state, the S2-LPTX can be moved to LOCK state to generate the high precision LO signal and then in TX mode. At the end of the operations, the S2-LPTX can return to READY state or can go to SLEEP state, having a very low power consumption.

SLEEP state can be configured to retain the FIFO content or not enabling very low power mode. If also no wake-up timer is required, the S2-LPTX can be moved from READY to STANDBY state, which has the lowest possible current consumption.

Figure 12. **State diagram**



Three states: READY, STANDBY and LOCK may be defined as stable state.

All other states are transient, which means that, in a typical configuration, the controller remains in those states, at most for any timeout timer duration. Also the READY and LOCK states behave as transients when they are not directly accessed with the specific commands (for example, when LOCK is temporarily used before reaching the TX state).

Table 33. **States**

State code[1]	State name	Digital LDO	SPI	XTAL	RF synth.	Wake-up timer
NA	SHUTDOWN	OFF	Off	Off	Off	Off
0x02	STANDBY	ON	On	Off	Off	Off
0x01	SLEEP_A		On	Off	Off	On
0x03	SLEEP_B		On	Off	Off	On
0x00	READY		On	On	Off	Do not care
0x0C	LOCK		On	On	On	Do not care
0x5C	TX		On	On	On	Do not care
0x50	SYNTH_SETUP		On	On	On	Do not care

1. *Other codes are invalid and are an indication of an error condition due to bad register configuration and/or hardware issue in the application board hosting.*

Commands are used in the S2-LPTX to change the operating mode and to use its functionality. A command is sent on the SPI interface and may be followed by any other SPI access without pulling CSn high. A command code is the second byte to be sent on the MOSI pin (the first byte must be 0x80). The commands are immediately valid after SPI transfer completion (no need for any CSn positive edge).

4.5.1 Command list

Table 34. **Commands**

Command code	Command name	State for execution	Description
0x60	TX	READY	Send the S2-LPTX to TX state for transmission
0x62	READY	STANDBY, SLEEP, LOCK	Go to READY state
0x63	STANDBY	READY	Go to STANDBY state
0x64	SLEEP	READY	Go to SLEEP state
0x66	LOCKTX	READY	Go to LOCK state by using the TX configuration of the synthesizer
0x67	SABORT	TX	Exit from TX state and go to READY state
0x68	LDC_RELOAD	ANY	Reload the LDC timer with a pre-programmed value stored in registers
0x70	SRES	ANY	Reset the S2-LPTX state machine and registers values
0x72	FLUSHTXFIFO	All	Clean the TX FIFO
0x73	SEQUENCE_UPDA TE	ANY	Reload the packet sequence counter with the value stored in register

4.5.2 State transaction response time

Table 35. **Response time**

Initial state	Final state	Response time [µs]
SHUTDOWN	READY	500
READY	STANDBY/ SLEEP	3
READY	LOCK with no VCO calibration	70
READY	LOCK with VCO calibration	85
TX	READY	1
STANDBY/SLEEP	READY	100
LOCK	TX	26

Note: The transition time enables the S2-LPTX for frequency hopping operation due to its reduced response time and very quick programming synthesizer. The response time depends on frequency of the clock in digital domain, from 24 MHz to 26 MHz.

Note: The first bit of preramble is sent after TX state is reached, if PA ramping is not enabled. If PA ramping is enabled, the first bit is sent after tramp (see Section 4.4.6.1 PA configuration).

4.5.3 Sleep states

S2-LPTX provides 2 SLEEP states:

- SLEEP without FIFO retention (SLEEP_A): in this low power state, the device keeps all the register values but not the TX FIFO. This is the device default SLEEP state.
- SLEEP with FIFO retention (SLEEP_B): in this low power state, the device keeps the content of the registers and the FIFO.

The responsibility of the SLEEP type to be used is demanded to the user. To select the SLEEP mode, the bit SLEEP_MODE_SEL (register 0x79) can be used. If this bit is set to 0, SLEEP_A is used each time the device enters SLEEP (by SPI command, LDC flow). If it is 1, SLEEP_B is used instead.

The usage of SLEEP_B mode is mandatory in the configuration like LDC in Tx.

5 Packet handler engine

The S2-LPTX offers a highly flexible and fully programmable packet handler (framer) that build the packet according to the user configuration settings. The packet types are available: BASIC format 802.15.4g packet format and UART over the air packet format.

WMBUS format is supported but it can be obtained using the proper features combination.

The device supports 3 different packet formats. The current packet format is set by the PCK_FRMT field of the PCKTCTRL3 register.

In particular:

- 0: Basic packet format
- 1: 802.15.4g packet format
- 2: UART over the air packet format

5.1 BASIC packet format

The packet format BASIC is selected by writing 0b in the register PCK_FRMT. The packet frame is as follows.

Table 36. BASIC packet format

Preamble	Sync	Length	Address	Payload	CRC	Postamble
0:2046 bits	0:32 bits	0:2 bytes	0:1 bytes	0:65535 bytes	0:4 bytes	0:510 bits

- **Preamble**: each preamble is a pair of ‘01’ or ‘10’ from 0 pair to 2046 pairs, programmed by the register PREAMBLE_LENGTH. The binary sequences transmitted in the various modulation modes are summarized in the following table (leftmost bit is transmitted first).

Table 37. Preamble field selection

PREAMBLE_SEL	2(G)FSK or OOK/ASK	4(G)FSK
0	0101	0111
1	1010	0010
2	1100	1101
3	0011	1000

- **Sync**: the pattern that identify the start of the frame can be configured in value with a programmable length from 0 to 32 bits, in steps of 1-bit length. The setting is done by the register SYNC_LENGTH. The S2LP supports dual synchronization with a either a primary or a secondary synchronization word. The binary content of the primary SYNC word is programmable through registers SYNCx (x= 1, 2, 3, 4). The binary content of the secondary SYNC word is programmable through registers SEC_SYNCx (x= 1, 2, 3, 4). Both the primary and the secondary word is transmitted according to the value of the SECONDARY_SYNC_SEL register, in particular if SECONDARY_SYNC_SEL = 0 then the primary synchronization word is transmitted; if SECONDARY_SYNC_SEL = 1 then the secondary synchronization word is transmitted. The binary pattern programmed in SYNCx (or SEC_SYNCx) is transmitted on air starting with the most significant bit of x = 1, to the least significant bit of x = 4 according to the programmed synchronization word length.
- **Length**: The device supports packet length transmission from 0 to 65535 bytes, On the transmitting device, the packet length is always set by using the two registers PCKTLENx (x= 1, 2) as: PCKTLEN1 × 256 + PCKTLEN0. Furthermore, when packet length is enabled (FIX_VAR_LEN=1b):
  - FIX_VAR_LEN = 0 means no LENGTH bit field inside the transmitted frame
  - FIX_VAR_LEN=1 means LENGTH in the frame according to PACKTLENx and LEN_WID info

- **Destination address**: can be enabled or no by the register ADDRESS_LEN. If enabled, ADDRESS_LEN=1b, its size is 1 byte.
- **Payload**: the main data from transmitter with a max length up to 65535 supported by the embedded automatic packet handler.
- **CRC**: can optionally be calculated on the transmitted data (Length field, Address field and Payload) and appended at the end of the payload (see Section 5.7 CRC).
- **Postamble**: The packet postamble allows inserting a certain number of '01' bit pairs at the end of the data packet. The number of postamble bit pairs can be set through the MBUS_PSTMBL register.

5.2 802.15.4g packet

Table 38. 802.15.4g packet

Preamble	Sync	PHR	MHR + MAC payload	CRC
0:2046 bits	0:32 bits	2 bytes	2:2047 bytes	0:4 bytes

- **Preamble**: each preamble is a pair of '01' or '10' from 0 pair to 2046 pairs, programmed by the register PREAMBLE_LENGTH. The binary sequences transmitted in the various modulation modes are summarized in Table 2 (leftmost bit is transmitted first).
- **Sync**: the pattern that identify the start of the frame can be configured in value with a programmable length from 0 to 32 bits, in steps of 1-bit length. The setting is done by the register SYNC_LENGTH. The S2LPTX supports dual synchronization with a either a primary or a secondary synchronization word. The binary content of the primary SYNC word is programmable through registers SYNCx (x= 1, 2, 3, 4). The binary content of the secondary SYNC word is programmable through registers SEC_SYNCx (x= 1, 2, 3, 4). Both the primary or the secondary word is transmitted according to the value of the SECONDARY_SYNC_SEL register, in particular if SECONDARY_SYNC_SEL = 0, the primary synchronization word is transmitted; if SECONDARY_SYNC_SEL = 1 then the secondary synchronization word is transmitted. The binary pattern programmed in SYNCx (or SEC_SYNCx) is transmitted on air starting with the most significant bit of x = 1, to the least significant bit of x = 4 according to the programmed synchronization word length. For the 802.15.4g packet format, the secondary synchronization word is automatically selected when FEC is enabled (FEC_EN = 1) and the setting of SECONDARY_SYNC_SEL is ignored.
- **PHR**: The PHR (physical header) field is specific for the 802.15.4g packet format and is automatically built by the packet handler block based on current register configuration.

Table 39. PHR frame

Bit string index	0	1-2	3	4	5-15
Bit mapping	MS	R_1-R_0	FCS	DW	L_{10}-L_0
Field name	Mode switch	Reserved	FSC type	Data whitening	Frame length

In particular:

- MS is always set to 0b (mode switch not supported).
- R_1-R_0 are always set to 00b.
- FCS is set to:
  - 0b if CRC mode 3 is selected.
  - 1b if CRC mode 5 is selected.
- DW is set to:
  - 0b if whitening is disabled, register WHIT_EN = 0.
  - 1b if whitening is enabled, register WHIT_EN = 1.

- L_{10}-L_0 are set equal to the 11 bits LSB of the packet length registers set by using the two registers PCKTLENx (x= 1, 2) as: PCKTLEN1 × 256 + PCKTLEN0. The packet length is from 0 to 65535 bytes (MHR + MAC Payload + CRC), then LEN_WID = 1b (2 byte length field transmitted).
- **Payload**: the main data from transmitter with a max length up to 65535 supported by the embedded automatic packet handler.
- **CRC**: can optionally be calculated on the transmitted data (PHR, MHR + MAC Payload) and appended at the end of the payload (see Section 5.7 CRC)
- In the 802.5.4g the CRC, named FCS in the standard, is considered part of the PSDU (PHY payload) hence the packet length, must include the 2 or 4 CRC bytes:
  - If the packet length programmed in PCKTLEN1 and PCKTLEN0 is L and CRC mode is 3, then L-2 bytes are read from the TX FIFO and interpreted as MHR + MAC Payload, 2 bytes CRC are automatically calculated and inserted at the end of the packet in transmission.
  - If the packet length programmed in PCKTLEN1 and PCKTLEN0 is L and CRC mode is 5, then L-4 bytes are read/written from/to the TX FIFO and interpreted as MHR + MAC Payload, 4 byte CRC are automatically calculated and inserted at the end of the packet in transmission.
  - If CRC mode is 0, then L bytes are read/written from/to the TX FIFO and interpreted as MHR + MAC Payload + MCS. In this case no CRC calculation, insertion/stripping is done, and it is the responsibility of the MAC layer to process it.

For CRC mode 3, according to the standard specifications, the CRC output is complemented to 1 before transmission.

For CRC mode 5, if the payload length is less than 4 bytes then the payload is zero-padded to reach a minimum length of 4 bytes. The padding bits are only used to compute the CRC and are not transmitted on-air.

5.3 UART over the air packet format

Table 40. UART over the air packet format

Preamble	Sync	Payload
0:2046 bits	0:32 bits	0:65535 bytes

When this format is selected, a start bit and a stop bit can be programmed to be added to each byte of the TX FIFO. Start and stop bits are not added to the SYNC word.

Also, the BYTE_SWAP bit can be set in order to send the FIFO bytes in LSbit first (default is indeed MSbit first).

The current binary value of the start and stop bit can be set through the START_BIT and the STOP_BIT fields of the PCKTCTRL2 register.

5.4 Wireless MBUS packet (W-MBUS, EN13757-4)

The W-MBUS packet structure referred to EN13757 can be obtained through registers setting programming the basic packet to fit the specific sub-mode used.

Preamble	Sync	1st block	2nd block	Opt. blocks	Postamble

Preamble: the preamble is fully programmable to fit the W-MBUS protocol. The generic setting is a pair of ‘01’ or ‘10’ from 1 pair to 1024 pairs (max. 256 bytes).

Sync: the pattern that identify the start of the frame is fully programmable to fit the W-MBUS protocol. The generic setting is in value with a programmable length from 1 bit to 64 bytes, in steps of 1-bit length.

Data blocks: the data coding can be fully programmed in NRZ, Manchester or 3-out-of-6.

Postamble: The packet postamble allows inserting a certain number of ‘01’ bit pairs at the end of the data packet. The number of postamble bit pairs can be set through the MBUS_PSTMBL register depending on the chosen sub-mode according to the W-MBUS protocol.

5.5 Payload transmission order

The bit order of the data from TX FIFO is controlled by the BYTE_SWAP register. In particular, the transmission is MSB first if BYTE_SWAP = 0 and LSB first if BYTE_SWAP = 1.

5.6 Data coding and integrity check

5.6.1 FEC

The device provides hardware support for error correction.

Error correction can be either enabled or disabled according to link reliability and power consumption needs.

Convolution coding (rate 1/2) and interleaving (FEC) can optionally be applied to the data. FEC can be enabled by setting the FEC_EN register. When FEC is enabled the number of transmitted bits is roughly doubled hence the on-air packet duration in time is roughly double as well. The data rate specified in section always applies to the on-air transmitted data.

FEC is applied to all the fields of BASIC packet format, except Preamble, Sync and Postamble. While is applied to all the fields except Preamble and Sync for the 802.15.4g packet format.

For the 802.15.4g packet format, two different coding schemes can be selected depending on the setting of the FEC_TYPE_4G register. In particular if FEC_TYPE_4G = 0 then the NRNSC encoder is selected, otherwise the RSC one is selected.

When FEC is enabled then the transmitter automatically selects the secondary SYNC word.

Use of FEC coding is exclusive with Manchester and Three-out-of-six coding.

5.6.1.1 Interleaving

In order to improve the effectiveness of convolutional encoding, matrix interleaving is applied to the encoded data at the output of the convolutional encoder.

The symbols from the output of the encoder are written raw-wise into a 4x4 matrix buffer starting from the upper-left cell and read column-wise starting from the lower-right cell.

Each pair of encoded symbols corresponding to one single encoded bit is packet into a single matrix cell. For each encoded symbols pair $s_0(n)$ is transmitted first on air, $s_1(n)$ is transmitted second.

Note that interleaving is always enabled together with FEC for the Basic packet format while it can be optionally enabled in the case of the 802.15.4g packet format by setting to ‘1’ the INT_EN_4G register.

5.6.2 Manchester coding

Manchester coding can be enabled for the Basic packet format only by setting to ‘1’ the MANCHESTER_EN register.

Use of Manchester coding is exclusive with FEC and Three-out-of-six coding.

When Manchester coding is enabled each bit ‘1’ is actually transmitted on air as a ‘10’ sequence while a bit ‘0’ is transmitted as a ‘01’ sequence. If enabled, Manchester encoding is applied to all bits following the SYNC word.

5.6.3 3-out-of-6 coding

The 3-out-of-6 coding is a form of block coding that can be enabled for the Basic packet format for compatibility with the MBUS standard setting to ‘1’ the MBUS_3OF6_EN bit of PCKTCTRL2. This coding is not expected to be used in other packet formats and is exclusive with FEC and Manchester coding.

Coding is done according to the table below.

Table 41. 3-out-of-6 coding scheme

NRZ code	NRZ-decimal	6-bit code	6-bit decimal	N. of transitions
0000	0	010110	22	4
0001	1	001101	13	3

NRZ code	NRZ-decimal	6-bit code	6-bit decimal	N. of transitions
0010	2	001110	14	2
0011	3	001011	11	3
0100	4	011100	28	2
0101	5	011001	25	3
0110	6	011010	26	4
1000	8	101100	44	3
1001	9	100101	37	4
1010	10	100110	38	3
1011	11	100011	35	2
1100	12	110100	52	3
1101	13	110001	49	2
1110	14	110010	50	3
1111	15	101001	41	4

5.7 CRC

Error detection is implemented by means of cyclic redundancy check codes. The CRC is calculated over all fields excluding preamble and SYNC word. The length of the checksum is programmable to 8, 16, 24 or 32 bits. The following standard CRC polynomials can be selected:

- mode 1: 8 bits: the poly is (0x07) X^8+X^2+X+1
- mode 2: 16 bits: the poly is (0x8005) $X^{16}+X^{15}+X^2+1$
- mode 3: 16 bits: the poly is (0x1021) $X^{16}+X^{12}+X^5+1$
- mode 4: 24 bits: the poly is (0x864CFB) $X^{24}+X^{23}+X^{18}+X^{17}+X^{14}+X^{11}+X^{10}+X^7+X^6+X^5+X^4+X^3+X+1$
- mode 5: 32 bits the poly is (0x04C011BB7) $x^{32}+x^{26}+ x^{23}+ x^{22}+ x^{16}+ x^{12}+ x^{11}+ x^{10}+ x^8+ x^7+ x^5+ x^4+ x^2+x+1$. 802.15.4g compatible

The initial state of the CRC polynomial is state to all 1b in all cases.

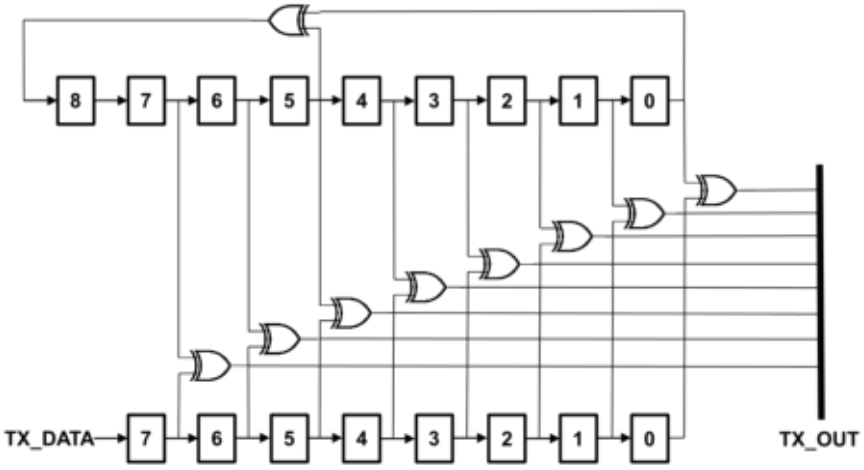
5.8 Data whitening

To prevent short repeating sequences (e.g., runs of 0's or 1's) that create spectral lines, which may interfere with other transmissions, the device implements a data whitening feature. Data whitening is implemented with a maximum length LFSR generating a pseudo-random binary sequence used to XOR data before entering the encoding chain. The length of the LSFR is set to 9 bits. The pseudo-random sequence is initialized to all 1's. When enabled through WHIT_EN register, the data are scrambled before being transmitted in such a way that long sequences of zeros or ones become very unlikely and physical layer algorithms perform better.

Data whitening is always recommended.

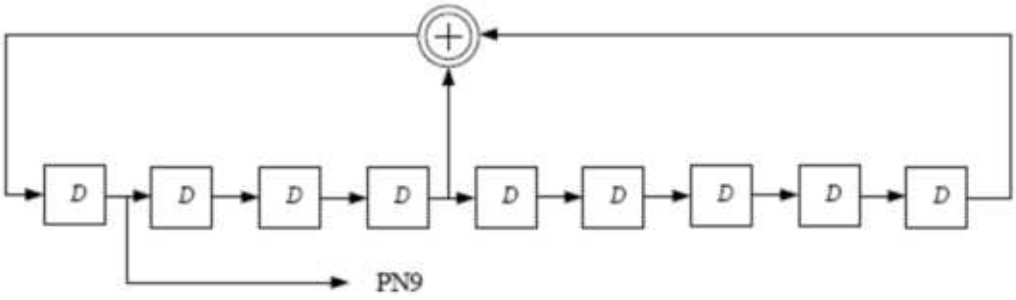
Data whitening is applied on all fields excluding the preamble, the SYNC words and the postamble for BASIC packet format according to the following scheme:

Figure 13. **Data whitening scheme**



In the case of 802.15.4g packet format, the use of whitening is signaled by the value, if enabled, is applied to all fields following the PHR field, and is performed according to the following block diagram:

Figure 14. **Data whitening scheme 802.15.4g**



6 Link layer protocol

6.1 Timeout protocol engine

The S2-LPTX provides programmable timers to reach the lowest low power consumption while at the same time keeping an efficient communication link.

Table 42. Timer description and duration (the values are related to f_{dig} of 26 MHz)

Timer name	Description	f_{source}	Time step [µs]	Max. time	Formula
LDC timer (1)	Set the wake-up period during LDC operations	$frco, \frac{Frco}{2}, \frac{Frco}{4}, \frac{Frco}{8}$	~29 ~58 ~116 ~232	~2s ~4s ~8s ~16s	$\frac{1}{f\text{source}}*(PRESCALER+1)*\left(COUNTER+1\right)$ PRESCALER : register 0x48, 0x4A COUNTER: register 0x49, 0x4B

1. *The LDC timer can be scaled by 1, 2, 4 or 8.*

6.1.1 Low duty cycle mode

The S2-LPTX provides an embedded low duty cycle mode (LDC), that allows reducing the average power consumption to build a synchronized start network where transmitter can go in low power mode periodically to reduce average power consumption.

The LDC mode is controlled essentially by the LDC timer, which periodically wakes up the S2-LPTX to perform a transmission.

The timer used to wait for the wakeup (T_{WU}) is clocked by the signal generated by the RCO circuit (or by an external clock from a GPIO pin), and is programmable with the registers LDC_PRESCALER and LDC_COUNTER. The internal RC oscillator used by the LDC timer must be calibrated just before the LDC mode is used.

After the wake-up signaling from its internal timer, the S2-LPTX switches to TX state and an interrupt request is issued (if enabled and not masked).

The details about LDC operation for the TX device are the following:

1. The starting state is READY: as soon as user sets the LDC_MODE bit, LDC counter starts in free running mode.
2. The first TX operation is triggered by the TX command.
3. First TX is executed always (even if TX FIFO is empty); the next happens only if TX FIFO is not empty.
4. At first TX, the LDC counter automatically is reloaded.
5. If TX FIFO is empty, the current slot is skipped and the device remains in SLEEP state.
6. The TX FIFO can be written during the SLEEP state also.
7. When the LDC_MODE bit is reset, the LDC counter continues decrementing and
   a. If the LDC_MODE bit is cleared during SLEEP mode, then the LDC timer does not wakes up the device any longer. A READY command is needed from MCU.
   b. If the LDC_MODE bit is cleared during the TX operation (so when still in active mode), then the device enters SLEEP mode at the end of the TX.

   However, it is also true that:
   a. In case the TX FIFO is empty, the device still remains in SLEEP state until the FIFO is written or a READY command is provided.
   b. In case the TX FIFO is not empty, a last TX operation is performed before the LDC stops.

For the TX, the bit SLEEP_MODE_SEL should be set to 1, selecting the SLEEP_B mode. In this way, FIFO can be written in SLEEP.

7 MCU interface

Communication with the MCU goes through a standard 4-wire SPI interface and 4 GPIOs (plus SHUTDOWN pin).

MCU can performs the following operations:

- Program the S2-LPTX in different operating modes by sending commands
- Write data into the TX FIFO
- Configure the S2-LPTX through the registers
- Retrieve information from the S2-LPTX
- Get interrupt requests and signals from the GPIO pins
- Apply external signals to the GPIO pins
- Put the S2-LPTX in SHUTDOWN state or exit from SHUTDOWN state.

7.1 Serial peripheral interface

The four-wire SPI interface consist of:

- **SCLK**: the SPI clock from MCU to the S2-LPTX
- **MOSI**: data from MCU to the S2-LPTX
- **MISO**: data from the S2-LPTX to MCU
- **CSn**: chip select signal, active low.

As the MCU is the master, it always drives the CSn and SCLK. According to the active SCLK polarity and phase, the S2-LPTX SPI can be classified as mode 1 (CPOL=0, CPHA=0), which means that the base value of SCLK is zero, data are read on the clock rising edge and data are changed on the clock falling edge. The MISO is in tri-state mode when CSn is high. All transfers are MSB first.

The interface allows the following operations:

- Write data (to registers or TX FIFO)
- Read data (from registers)
- Send commands.

The SPI communication is supported in all the active states, and also during the low power state: STANDBY and SLEEP.

When accessing the SPI interface, the two status bytes of the MC_STATE (MC_STATE[1], MC_STATE[0]) registers are sent to the MISO pin.

Figure 15. SPI write sequence

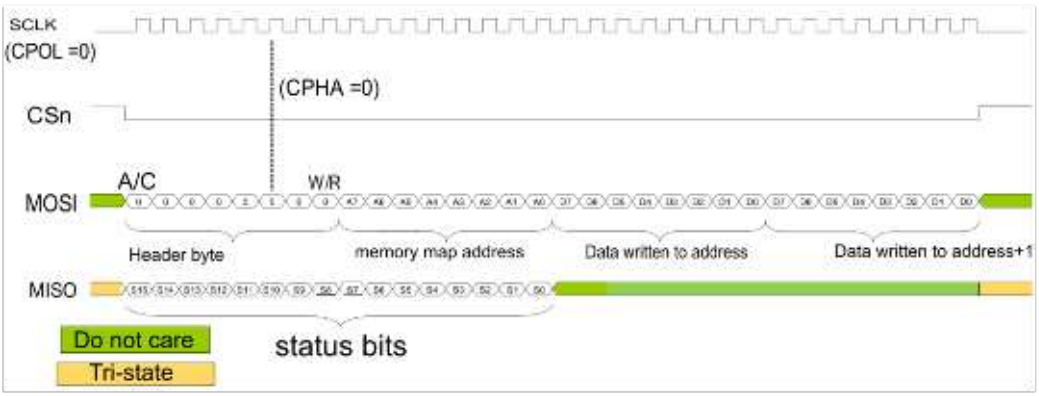


Figure 16. **SPI read sequence**

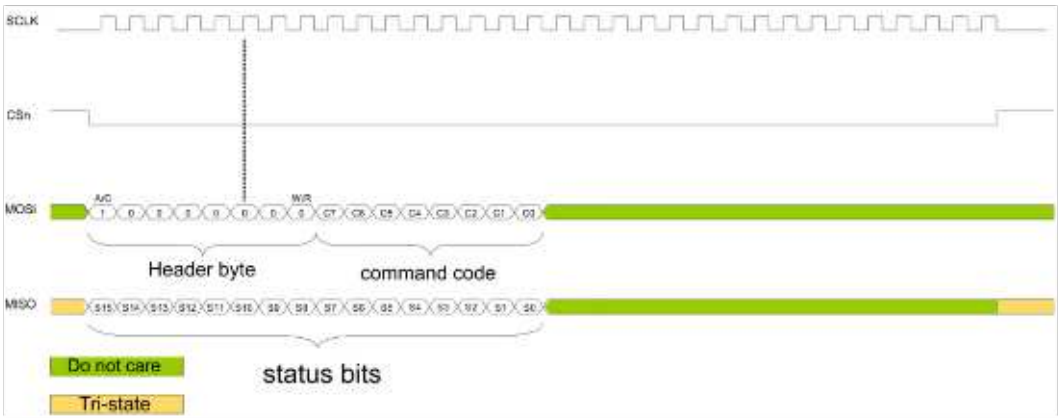


Figure 17. **SPI command sequence**



Concerning the first byte, the MSB is an A/C bit (address/commands: 0 indicates that the following byte is an address, 1 indicates that the following byte is a command code), while the LSB is a W/R bit (write/read: 1 indicates a read operation). All other bits must be zero.

Read and write operations are persistently executed while CSn is kept active (low), the address is automatically incremented (burst mode).

Accessing the FIFO is done as usual with the read and write commands, by putting, as address, the code 0xFF. Burst mode is available to access the sequence of bytes in the FIFO. Clearly, TX-FIFO is accessed with a write operation.

7.2 Interrupts

In order to notify the MCU of a certain number of events an interrupt signal is generated on a selectable GPIO. The following events trigger an interrupt to the MCU:

Table 43. Interrupts list

Bit	Events group	Interrupt event
2	Packet oriented	TX data sent
5		TX FIFO underflow/overflow error
7		TX FIFO almost full
8		TX FIFO almost empty
15	Device status related	Wake-up timeout in LDCR mode (1)
16		READY (2)
17		STANDBY state switching in progress
18		Low battery level
19		Power-on reset

1. *The interrupt flag n.15 is set (and consequently the interrupt request) only when the XO clock is available for the state machine. This time may be delayed compared to the actual timer expiration. However, the real time event can be sensed putting the end-of-counting signal on a GPIO output.*
2. *The interrupt flag n.16 is set each time the S2-LPTX goes to READY state and the XO has completed its setting transient (XO ready condition detected).*

All interrupts are reported on a set of interrupt status registers and are individually maskable. The interrupt status register must be cleared upon a read event from the MCU.

The status of all the interrupts are reported in the IRQ_STATUS register: bits are high for the events that have generated any interrupts. The interrupts are individually maskable using the IRQ_MASK registers: if the mask bit related to a particular event is programmed at 0, that event does not generate any interrupt request.

7.3 GPIOs

The four GPIOs can be configured as follows:

Table 44. GPIO digital output functions

I/O selection	Output signal
0	nIRQ (interrupt request, active low)
1	POR inverted (active low)
2	Wake-up timer expiration: ‘1’ when WUT has expired
3	Low battery detection: ‘1’ when battery is below threshold setting
4	TX data internal clock output (TX data are sampled on the rising edge of it)
5	TX state outputs a command information coming from the RADIO_TX block
6	TX FIFO almost empty flag
7	TX FIFO almost full flag
11	Device in a state other than SLEEP or STANDBY: ‘0’ when in SLEEP/STANDBY
12	Device in STANDBY state
17	Reserved
18	TX mode indicator (to enable an external range extender)

I/O selection	Output signal
19	VDD (to emulate an additional GPIO of the MCU, programmable by SPI)
20	GND (to emulate an additional GPIO of the MCU, programmable by SPI)
21	External SMPS enable signal (active high)
22	Device in SLEEP state
23	Device in READY state
24	Device in LOCK state
25	Device waiting for a high level of the lock-detector output signal
26	TX_DATA_OOK signal (internal control signal generated in the OOK analog smooth mode)
27	Device waiting for a high level of the READY2 signal from XO
28	Device waiting for timer expiration to allow PM block settling
29	Device waiting for end of VCO calibration
30	Device enables the full circuitry of the SYNTH block
31	Reserved

Table 45. GPIO digital input functions

I/O selection	Input signal
0	1 >> TX command
1	
2	TX data input for direct modulation
3	Wake-up from external input (sensor output)
4	External clock @ 34.7 kHz (used for LDC modes timing)
From 5 to 31	Not used

8 Register contents

Table 46. **Register contents**

Name	Addr	Default	Bit	Field name	Description
GPIO0_CONF	00	0A	7:3	GPIO_SELECT	Specify the GPIO0 I/O signal, default setting POR (see Table 44. GPIO digital output functions).
			2	RESERVED	-
			1:0	GPIO_MODE	GPIO0 Mode: • 01b: Digital input • 10b: Digital output low power • 11b: Digital output high power
GPIO1_CONF	01	A2	7:3	GPIO_SELECT	Specify the GPIO1 I/O signal, default setting digital GND (see Table 44. GPIO digital output functions).
			2	RESERVED	-
			1:0	GPIO_MODE	GPIO1 mode: • 01b: Digital input1 • 0b: Digital output low power • 11b: Digital output high power
GPIO2_CONF	02	A2	7:3	GPIO_SELECT	Specify the GPIO2 I/O signal, default setting digital GND (see Table 44. GPIO digital output functions).
			2	RESERVED	-
			1:0	GPIO_MODE	GPIO2 mode: • 01b: Digital input • 10b: Digital output low power • 11b: Digital output high power
GPIO3_CONF	03	A2	7:3	GPIO_SELECT	Specify the GPIO3 I/O signal, default setting digital GND (see Table 44. GPIO digital output functions).
			2	RESERVED	-
			1:0	GPIO_MODE	GPIO3 mode: • 00b: Analog • 01b: Digital input • 10b: Digital output low power • 11b: Digital output high power

Name	Addr	Default	Bit	Field name	Description
SYNT3	05	42	7:5	PLL_CP_ISEL	Set the charge pump current according to the XTAL frequency (see Table 34. Commands).
			4	BS	Synthesizer band select. This parameter selects the out-of loop divide factor of the synthesizer: • 0: 4, band select factor for high band • 1: 8, band select factor for middle band (see Section 4.3.1 RF channel frequency settings).
			3:0	SYNT[27:24]	MSB bits of the PLL programmable divider.
SYNT2	06	16	7:0	SYNT[23:16]	Intermediate bits of the PLL programmable divider (see Section 4.3.1 RF channel frequency settings).
SYNT1	07	27	7:0	SYNT[15:8]	Intermediate bits of the PLL programmable divider (see Section 4.3.1 RF channel frequency settings).
SYNT0	08	62	7:0	SYNT[7:0]	LSB bits of the PLL programmable divider (see Section 4.3.1 RF channel frequency settings).
CHSPACE	0C	3F	7:0	CH_SPACE	Channel spacing setting.
CHNUM	0D	00	7:0	CH_NUM	Channel number. This value is multiplied by the channel spacing and added to the synthesizer base frequency to generate the actual RF carrier frequency.
MOD4	0E	83	7:0	DATARATE_M[15:8]	The MSB of the mantissa value of the data rate equation.
MOD3	0F	2B	7:0	DATARATE_M[7:0]	The LSB of the mantissa value of the data rate equation.
MOD2	10	77	7:4	MOD_TYPE	Modulation type: • 0: 2-FSK • 1: 4-FSK • 2: 2-GFSK BT=1 • 3: 4-GFSK BT=1 • 5: ASK/OOK • 6: polar mode • 7: unmodulated • 10: 2-GFSK BT=0.5 • 11: 4-GFSK BT=0.5
			3:0	DATARATE_E	The exponent value of the data rate equation.

Name	Addr	Default	Bit	Field name	Description
MOD1	11	03	7	PA_INTERP_EN	1: enable the PA power interpolator (see Section 4.4.6.1 PA configuration).
			6	MOD_INTERP_EN	1: enable frequency interpolator for the GFSK shaping (see Section 4.4.1.1 Gaussian shaping).
			5:4	CONST_MAP	Select the constellation map for 4-(G)FSK or 2-(G)FSK modulations (see Table 38. 802.15.4g packet and Table 39. PHR frame).
			3:0	FDEV_E	The exponent value of the frequency deviation equation.
MOD0	12	93	7:0	FDEV_M	The mantissa value of the frequency deviation equation.
PCKTCTRL6	2B	80	7:2	SYNC_LEN	The number of bits used for the SYNC field in the packet.
			1:0	PREAMBLE_LEN[9:8]	The MSB of the number of '01 or '10' of the preamble of the packet.
PCKTCTRL5	2C	10	7:0	PREAMBLE_LEN[7:0]	The LSB of the number of '01 or '10' of the preamble of the packet.
PCKTCTRL4	2D	00	7	LEN_WID	The number of bytes used for the length field: • 0: 1 byte • 1: 2 bytes.
			6:4	RESERVED	-
			3	ADDRESS_LEN	1: include the ADDRESS field in the packet.
			2:0	RESERVED	-
PCKTCTRL3	2E	20	7:6	PCKT_FRMT	Format of packet: • 0: Basic • 1: 802.15.4g • 2: UART (see Section 5 Packet handler engine)
			5:4	RESERVED	-
			3	FSK4_SYM_SWAP	Select the symbol mapping for 4(G)FSK.
			2	BYTE_SWAP	Select the transmission order between MSB and LSB.
			1:0	PREAMBLE_SEL	Select the preamble pattern.

Name	Addr	Default	Bit	Field name	Description
PCKTCTRL2	2F	00	7:6	RESERVED	-
			5	FCS_TYPE_4G	This is the FCS type in header field of 802.15.4g packet.
			4	FEC_TYPE_4G/STOP_BIT	• If the 802.15.4 mode is enabled, this is the FCS type in header field of 802.15.4g packet. Select the FEC type of 802.15.4g packet: – 0: NRNSC – 1: RSC. • If the UART packet is enabled, this is the value of the STOP_BIT.
			3	INT_EN_4G/START_BIT	• If the 802.15.4 mode is enabled, 1: enable the interleaving of 802.15.4g packet. • If the UART packet is enabled, this is the value of the START_BIT.
			2	MBUS_3OF6_EN	1: enable the 3-out-of-6 encoding/decoding.
			1	MANCHESTER_EN	1: enable the Manchester encoding/decoding.
			0	FIX_VAR_LEN	Packet length mode: • 0: No LENGTH field inserted in the basic packet • 1: LENGTH field inserted in the basic data packet according to LEN_WID and PCKTLEN3 register value

Name	Addr	Default	Bit	Field name	Description
PCKTCTRL1	30	2C	7:5	CRC_MODE	CRC field: • 0: no CRC field • 1: CRC using poly 0x07 • 2: CRC using poly 0x8005 • 3: CRC using poly 0x1021 • 4: CRC using poly 0x864CBF • 5: CRC using poly 0x04C011BB7
			4	WHIT_EN	1: enable the whitening mode.
			3:2	TXSOURCE	Tx source data: • 0: normal mode • 1: direct through FIFO • 2: direct through GPIO • 3: PN9
			1	SECOND_SYNC_SEL	• 0 select the primary SYNC word • 1 select the secondary SYNC word.
			0	FEC_EN	1: enable the FEC encoding in TX
PCKTLEN1	31	00	7:0	PCKTLEN1	MSB of length of packet in bytes.
PCKTLEN0	32	14	7:0	PCKTLEN0	LSB of length of packet in bytes.
SYNC3	33	88	7:0	SYNC3	SYNC word byte 3.
SYNC2	34	88	7:0	SYNC2	SYNC word byte 2.
SYNC1	35	88	7:0	SYNC1	SYNC word byte 1.
SYNC0	36	88	7:0	SYNC0	SYNC word byte 0.
QI	37	01	7:5	Reserved	-
			4:1	Reserved	-
			0	Reserved	-
PCKT_PSTMBL	38	00	7:0	PCKT_PSTMBL	Set the packet postamble length.

Name	Addr	Default	Bit	Field name	Description
PROTOCOL2	39	40	7	Reserved	-
			6	Reserved	-
			5	Reserved	-
			4:3	TX_SEQ_NUM_RELOAD	TX sequence number to be used when counting reset is required using the related command.
			2	FIFO_GPIO_OUT_MUX_SEL	1: select the almost empty/full control for TX FIFO. 0: almost empty/full control for TX FIFO disabled.
			1:0	LDC_TIMER_MULT	Set the LDC timer multiplier factor: • 00b: x1 • 01b: x2 • 10b: x4 • 11b: x8.
PROTOCOL1	3A	00	7	LDC_MODE	1: enable the low duty cycle mode.
			6	Reserved	-
			5	Reserved	-
			4		-
			3	Reserved	
			2	Reserved	
			1	Reserved	
			0	Reserved	
FIFO_CONFIG1	3E	30	7	RESERVED	-
			6:0	TX_AFTHR	Set the TX FIFO almost full threshold.
FIFO_CONFIG0	3F	30	7	RESERVED	-
			6:0	TX_AETHR	Set the TX FIFO almost empty threshold.
PCKT_FLT_GOALS3	42	00	7:0	DUAL_SYNC3	If dual sync mode enabled: dual SYNC word byte 3.
PCKT_FLT_GOALS2	43	00	7:0	DUAL_SYNC2	If dual sync mode enabled: dual SYNC word byte 2.
PCKT_FLT_GOALS1	44	00	7:0	DUAL_SYNC1	If dual sync mode enabled: dual SYNC word byte 1.
PCKT_FLT_GOALS0	45	00	7:0	DUAL_SYNC0	If dual sync mode enabled: dual SYNC word byte 0, RX packet destination field.
TIMERS3	48	01	7:0	LDC_TIMER_PRESC	Prescaler for wake up timer.
TIMERS2	49	00	7:0	LDC_TIMER_CNTR	Counter for wake up timer.
TIMERS1	4A	01	7:0	LDC_RELOAD_PRSC	Prescaler value for reload operation of wake up timer.
TIMERS0	4B	00	7:0	LDC_RELOAD_CNTR	Counter value for reload operation of wake up timer.

Name	Addr	Default	Bit	Field name	Description
IRQ_MASK3	50	00	7:0	INT_MASK[31:24]	Enable the routing of the interrupt flag on the configured IRQ GPIO.
IRQ_MASK2	51	00	7:0	INT_MASK[23:16]	Enable the routing of the interrupt flag on the configured IRQ GPIO.
IRQ_MASK1	52	00	7:0	INT_MASK[15:8]	Enable the routing of the interrupt flag on the configured IRQ GPIO.
IRQ_MASK0	53	00	7:0	INT_MASK[7:0]	Enable the routing of the interrupt flag on the configured IRQ GPIO.
PA_POWER8	5A	01	7	RESERVED	-
			6:0	PA_LEVEL8	Output power level for 8th slot.
PA_POWER7	5B	0C	7	RESERVED	-
			6:0	PA_LEVEL_7	Output power level for 7th slot.
PA_POWER6	5C	18	7	RESERVED	-
			6:0	PA_LEVEL_6	Output power level for 6th slot.
PA_POWER5	5D	24	7	RESERVED	-
			6:0	PA_LEVEL_5	Output power level for 5th slot.
PA_POWER4	5E	30	7	RESERVED	-
			6:0	PA_LEVEL_4	Output power level for 4th slot.
PA_POWER3	5F	48	7	RESERVED	-
			6:0	PA_LEVEL_3	Output power level for 3rd slot.
PA_POWER2	60	60	7	RESERVED	-
			6:0	PA_LEVEL_2	Output power level for 2nd slot.
PA_POWER1	61	00	7	RESERVED	-
			6:0	PA_LEVEL_1	Output power level for 1st slot.
PA_POWER0	62	47	7	DIG_SMOOTH_EN	1: enable the generation of the internal signal TX_DATA which is the input of the FIR. Needed when FIR_EN=1.
			6	PA_MAXDBM	1: configure the PA to send maximum output power. Power ramping is disable with this bit set to 1.
			5	PA_RAMP_EN	1: enable the power ramping.
			4:3	PA_RAMP_STEP_LEN	Set the step width (unit: 1/8 of bit period).
			2:0	PA_LEVEL_MAX_IDX	Final level for power ramping or selected output power index.

Name	Addr	Default	Bit	Field name	Description
PA_CONFIG1	63	03	7:4	RESERVED	-
			3:2	FIR_CFG	FIR configuration: • 00b: filtering • 01b: ramping • 10b: switching (see Section 4.4.2.1 OOK smoothing)
			1	FIR_EN	1: enable FIR (see Section 4.4.2.1 OOK smoothing
			0	RESERVED	-
PA_CONFIG0	64	8A	7:4	PA_DEGEN_TRIM	11xx ® code threshold: 485 10xx ® code threshold: 465 01xx ® code threshold: 439 00xx ® code threshold: 418 xx11 ® clamp voltage: 0.55 V xx10 ® clamp voltage: 0.50 V xx01 ® clamp voltage: 0.45 V xx00 ® clamp voltage: 0.40 V.
			3	PA_DEGEN_ON	Enables the 'degeneration' mode that introduces a pre-distortion to linearize the power control curve.
			2	SAFE_ASK_CAL	During a TX operation, enables and starts the digital ASK calibrator.
			1:0	PA_FC	PA Bessel filter bandwidth: • 00b: 12.5 kHz (data rate 16.2 kbps) • 01b: 25 kHz (data rate 32 kbps) • 10b: 50 kHz (data rate 62.5 kbps) • 11b: 100 kHz (data rate 125 kbps), (see Section 4.4.2.1 OOK smoothing).
SYNTH_CONFIG2	65	D0	7:3	RESERVED	-
			2	PLL_PFD_SPLIT_EN	Enables increased DN current pulses to improve linearization of CP/PFD (see Table 34. Commands).
			1:0	RESERVED	-
VCO_CONFIG	68	03	7:6	RESERVED	-
			5	VCO_CALAMP_EXT_SEL	1 → VCO amplitude calibration will be skipped (external amplitude word forced on VCO).
			4	VCO_CALFREQ_EXT_SEL	1 → VCO frequency calibration will be skipped (external amplitude word forced on VCO).
			3:0	RESERVED	-

Name	Addr	Default	Bit	Field name	Description
VCO_CALIBR_IN2	69	88	7:0	RESERVED	-
VCO_CALIBR_IN1	6A	40	7:0	RESERVED	-
VCO_CALIBR_IN0	6B	40	7:0	RESERVED	-
XO_RCO_CONF1	6C	45	7:5	RESERVED	-
			4	PD_CLKDIV	1: disable divider of digital clock (and reference clock for the SMPS).
			3:0	RESERVED	-
XO_RCO_CONF0	6D	30	7	EXT_REF	• 0: reference signal from XO circuit • 1: reference signal from XIN pin.
			5:4	GM_CONF	Set the driver gm of the XO at start up.
			3	REFDIV	1: enable the the reference clock divider.
			2	RESERVED	-
			1	EXT_RCO_OSC	1: the 34.7 kHz signal must be supplied from any GPIO.
			0	RCO_CALIBRATION	1: enable the automatic RCO calibration.
RCO_CALIBR_CONF3	6E	70	7:4	RWT_IN	RWT word value for the RCO.
			3:0	RFB_IN[4:1]	MSB part of RFB word value for RCO.
RCO_CALIBR_CONF2	6F	4D	7	RFB_IN[0]	LSB part of RFB word value for RCO.
			6:0	RESERVED	-
PM_CONF4	75	17	7:6	RESERVED	-
			5	EXT_SMPS	1: disable the internal SMPS.
			4:0	RESERVED	-
PM_CONF3	76	20	7	KRM_EN	• 0: divider by 4 enabled (SMPS' switching frequency is FSW=Fdig/4) • 1: rate multiplier enabled (SMPS' switching frequency is FSW=KRM*Fdig/(2^15).
			6:0	KRM[14:8]	Sets the divider ratio (MSB) of the rate multiplier (default: Fsw=Fdig/4)
PM_CONF2	77	00	7:0	KRM[7:0]	Sets the divider ratio (LSB) of the rate multiplier (default: Fsw=Fdig/4)

Name	Addr	Default	Bit	Field name	Description
PM_CONF1	78	39	7	RESERVED	-
			6	BATTERY_LVL_EN	1: enable battery level detector circuit.
			5:4	SET_BLD_TH	Set the BLD threshold: • 00b: 2.7 V • 01b: 2.5 V • 10b: 2.3 V • 11b: 2.1 V.
			3	Reserved	-
			2	BYPASS_LDO	Set to 0 (default value)
			1:0	RESERVED	-
PM_CONF0	79	42	7	RESERVED	-
			6:4	SET_SMPS_LVL	SMPS output voltage: • 000b: not used • 001b: 1.2 V • 010b: 1.3 V • 011b: 1.4 V • 100b: 1.5 V • 101b: 1.6 V • 110b: 1.7 V • 111b: 1.8 V
			3:1	RESERVED	-
			0	SLEEP_MODE_SEL	• 0: SLEEP without FIFO retention (SLEEP A) • 1: SLEEP with FIFO retention (SLEEP B).
MC_STATE1	8D	52	7:5	RESERVED	-
			4	RCO_CAL_OK	RCO calibration successfully terminated.
			3	ANT_SEL	Currently selected antenna.
			2	TX_FIFO_FULL	1: TX FIFO is full.
			1	Reserved	
			0	ERROR_LOCK	1: RCO calibrator error.
MC_STATE0	8E	07	7:1	STATE	Current state.
			0	XO_ON	1: XO is operating.
TX_FIFO_STATUS	8F	00	7:0	NELEM_TXFIFO	Number of elements in TX FIFO.
RCO_CALIBR_OUT4	94	70	7:4	RWT_OUT	RWT word from internal RCO calibrator.
			3:0	RFB_OUT[4:1]	RFB word (MSB) from internal RCO calibrator.
RCO_CALIBR_OUT3	95	00	7	RFB_OUT[0]	RF word (LSB) from internal RCO calibrator.
			6:0	RESERVED	-

Name	Addr	Default	Bit	Field name	Description
VCO_CALIBR_OUT1	99	00	7:4	RESERVED	-
			3:0	VCO_CAL_AMP_OUT	VCO magnitude calibration output word (binary coding internally converted from thermometric coding).
VCO_CALIBROUT0	9A	00	7	RESERVED	-
			6:0	VCO_CAL_FREQ_OUT	VCO Cbank frequency calibration output word (binary coding internally converted from thermometric coding).
TX_PCKT_INFO	9C	00	7:6	RESERVED	-
			5:4	TX_SEQ_NUM	Current TX packet sequence number.
			3:0	RESERVED	-
DEVICE_INFO1	F0	03	7:0	PARTNUM	S2-LPTX part number
DEVICE_INFO0	F1	C1	7:0	VERSION	S2-LPTX version number
IRQ_STATUS3	FA	00	7:0	INT_LEVEL[31:24]	Interrupt status register 3
IRQ_STATUS2	FB	09	7:0	INT_LEVEL[23:16]	Interrupt status register 2
IRQ_STATUS1	FC	05	7:0	INT_LEVEL[15:8]	Interrupt status register 1
IRQ_STATUS0	FD	00	7:0	INT_LEVEL[7:0]	Interrupt status register 0

9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

9.1 QFN24L (4x4 mm) package information

Figure 18. **QFN24L (4x4 mm) package outline**

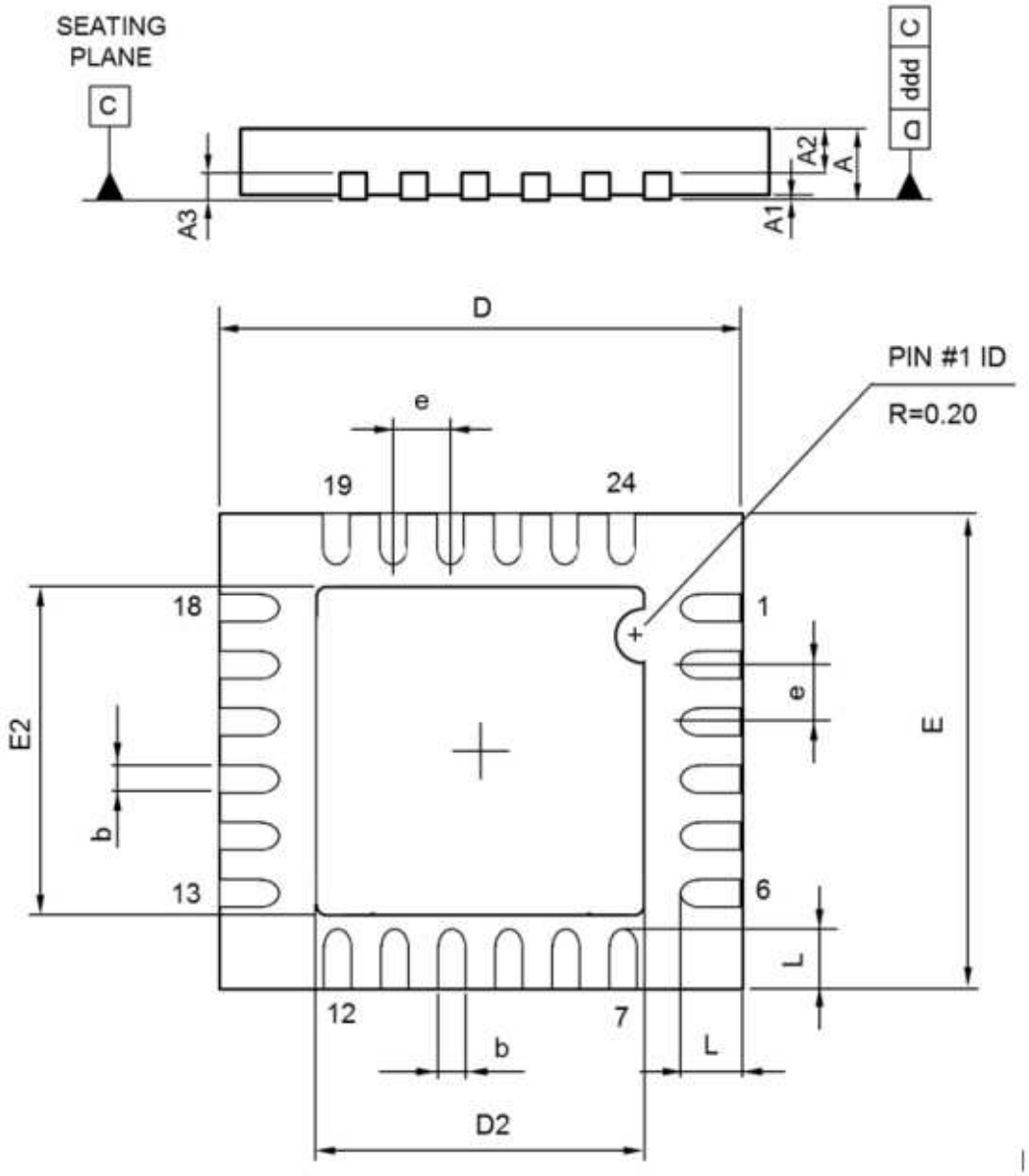


Table 47. **QFN24L (4x4 mm) package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1		0.02	0.05
A2		0.65	1.00
A3		0.20	
b	0.18	0.25	0.30
D	3.85	4.00	4.15
D2	2.60	2.70	2.80
E	3.85	4.00	4.15
E2	2.60	2.70	2.80
e		0.50	
L	0.35	0.40	0.45
ddd			0.08

9.2 PCB pad pattern

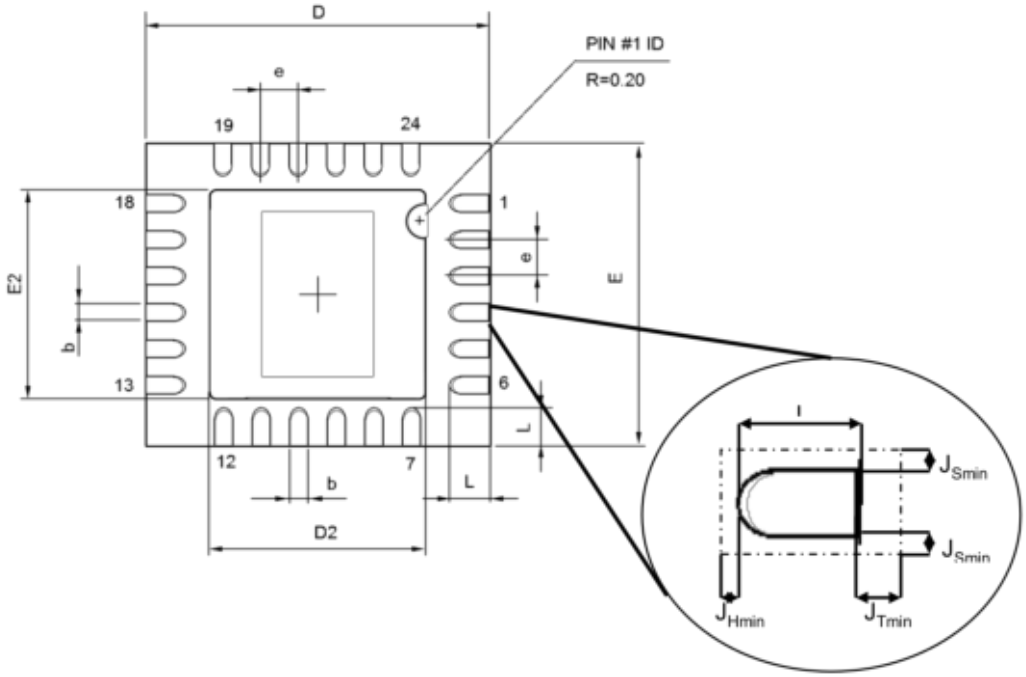
In order to design a proper pad pattern, tolerance analysis is required on package and motherboard dimensions. The tolerance analysis requires consideration of component tolerances, PCB tolerances and the accuracy of the equipment used to place the component.

For the pad dimensioning three different minimum values have been considered:

- Minimum toe fillet = JTmin = 0.1 mm
- Minimum heel fillet = JHmin = 0.05 mm
- Minimum side fillet = JSmin = 0 mm

The PCB thermal pad should at least match the exposed die paddle size. The solder mask opening should be 120 to 150 microns larger than the pad size resulting in 60 to 75 microns clearance between the copper pas and solder mask.

Figure 19. **QFN24 4x4x1pitch 0.5 mm PCB pad pattern**



9.3 QFN recommended profile parameters

The temperature profile is the most important control in the re-flow soldering and it must be fine tuned to establish a robust process. QFN recommended soldering profile for lead-free mounting is shown in the following table and picture.

Figure 20. **QFN recommended soldering profiles**

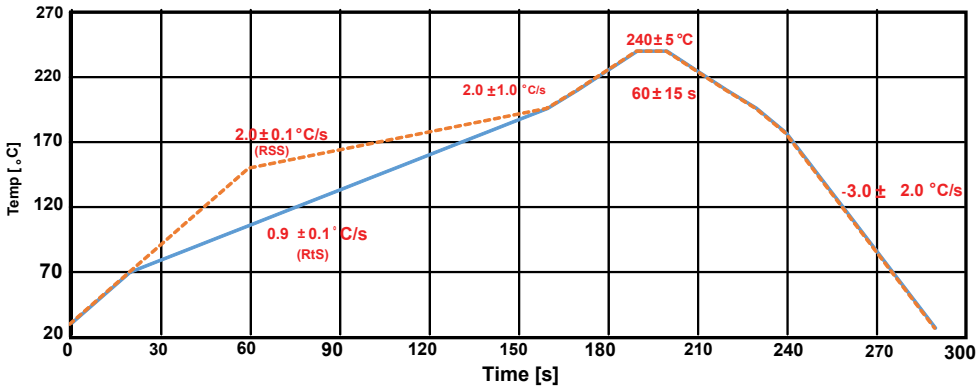


Table 48. Temperature profiles

Profile	Ramp-to-spike	Ramp-soak-spike
Temperature gradient in preheat	T from 70 °C to 150 °C 0.8 °C/s to 1.0 °C/s	T from 70 °C to 150 °C 1 °C/s to 3 °C/s
Soak/dwell (refer to solder paste supplier recommendation)	N/A or temp.: 150 °C to 200 °C, 40 to 80 s	Soak 150 °C to 200 °C, 40 to 100 s
Temperature gradient in preheat	Temp.: 200 °C to 225 °C, 1 °C/s to 3 °C/s	Temp.: 200 °C to 225 °C, 1 °C/s to 3 °C/s
Peak temperature	235 °C to 245 °C	
Duration above 220 °C	45 to 75 s	
Temperature gradient in cooling	-1 °C to -5 °C	
Time from 50 to 220 °C	150 to 230 s	

10 Ordering information

Table 49. **Ordering information**

Order code	Package	Packing
S2-LPTXQTR	QFN24 4x4x1	Tape and reel

Revision history

Table 50. **Document revision history**

Date	Version	Changes
19-Sep-2019	1	Initial release.

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