SCAN90CP02 1.5 Gbps 2x2 LVDS Crosspoint Switch with Pre-Emphasis and IEEE 1149.6

Check for Samples: SCAN90CP02

FEATURES

- **1.5 Gbps per Channel**
- **Low Power: 70 mA in Dual Repeater Mode @1.5 Gbps**
- **Low Output Jitter**
- **Configurable 0/25/50/100% Pre-Emphasis Drives Lossy Backplanes and Cables**
- **Non-Blocking Architecture Allows 1:2 Splitter, 2:1 Mux, Crossover, and Dual Buffer Configurations**
- **Flow-Through Pinout**
- **LVDS/BLVDS/CML/LVPECL Inputs, LVDS Outputs**
- **IEEE 1149.1 and 1149.6 Compliant**
- **Single 3.3V Supply**
- **Separate Control of Inputs and Outputs Allows for Power Savings**
- **Industrial -40 to +85°C Temperature Range**
- **28-Lead UQFN Package, or 32-Lead LQFP Package**

DESCRIPTION

The SCAN90CP02 is a 1.5 Gbps 2 x 2 LVDS crosspoint switch. High speed data paths and flow-through pinout minimize internal device jitter, while configurable 0/25/50/100% pre-emphasis overcomes external ISI jitter effects of lossy backplanes and cables. The differential inputs interface to LVDS and Bus LVDS signals such as those on TI's 10-, 16-, and 18- bit Bus LVDS SerDes, as well as CML and LVPECL. The SCAN90CP02 can also be used with ASICs and FPGAs. The non-blocking crosspoint architecture is pin-configurable as a 1:2 clock or data splitter, 2:1 redundancy mux, crossover function, or dual buffer for signal booster and stub hider applications.

Integrated IEEE 1149.1 (JTAG) and 1149.6 circuitry supports testability of both single-ended LVTTL/CMOS and differential LVDS PCB interconnect. The 3.3V supply, CMOS process, and LVDS I/O ensure high performance at low power over the entire industrial -40 to +85°C temperature range.

Block Diagram

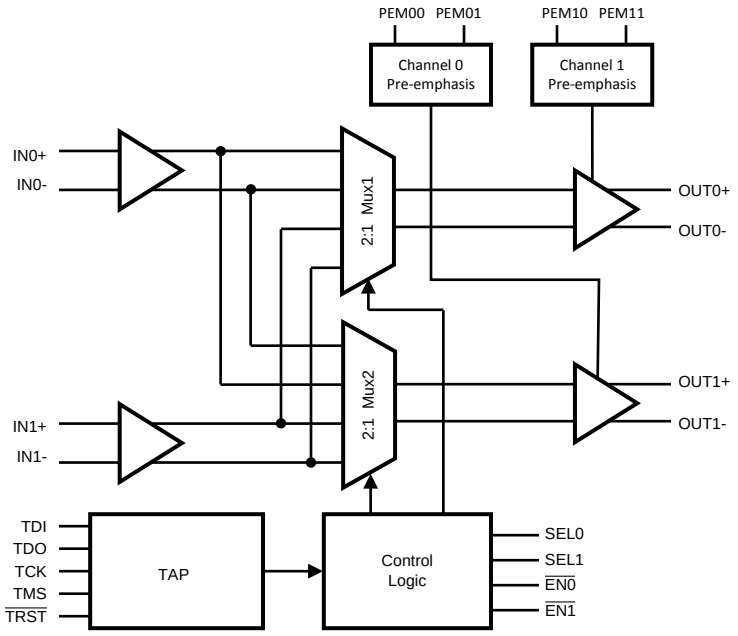


Figure 1. SCAN90CP02 Block Diagram

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PIN DESCRIPTIONS

Pin Name	UQFN Pin Number	LQFP Pin Number	I/O, Type	Description
DIFFERENTIAL INPUTS COMMON TO ALL MUXES				
IN0+ IN0−	9 10	9 10	I, LVDS	Inverting and non-inverting differential inputs. LVDS, Bus LVDS, CML, or LVPECL compatible.
IN1+ IN1−	12 13	13 14	I, LVDS	Inverting and non-inverting differential inputs. LVDS, Bus LVDS, CML, or LVPECL compatible.
SWITCHED DIFFERENTIAL OUTPUTS				
OUT0+ OUT0−	27 26	32 31	O, LVDS	Inverting and non-inverting differential outputs. OUT0± can be connected to any one pair IN0±, or IN1±. LVDS compatible (1).
OUT1+ OUT1−	24 23	28 27	O, LVDS	Inverting and non-inverting differential outputs. OUT1± can be connected to any one pair IN0±, or IN1±. LVDS compatible (1).
DIGITAL CONTROL INTERFACE				
SEL0, SEL1	6 5	7 6	I, LVTTL	Select Control Inputs
$\overline{EN0}$, $\overline{EN1}$	7 15	8 17	I, LVTTL	Output Enable Inputs
PEM00, PEM01	4 3	4 3	I, LVTTL	Channel 0 Output Pre-emphasis Control Inputs
PEM10, PEM11	2 1	2 1	I, LVTTL	Channel 1 Output Pre-emphasis Control Inputs
TDI	19	22	I, LVTTL	Test Data Input to support IEEE 1149.1 features
TDO	20	23	O, LVTTL	Test Data Output to support IEEE 1149.1 features
TMS	18	21	I, LVTTL	Test Mode Select to support IEEE 1149.1 features
TCK	17	19	I, LVTTL	Test Clock to support IEEE 1149.1 features
$\overline{TRST}$	21	24	I, LVTTL	Test Reset to support IEEE 1149.1 features
N/C	8, 28			Not Connected
POWER				
V_{DD}	11, 14, 16, 22, 25	12, 16, 18, 25, 29	I, Power	V_{DD} = 3.3V ±0.3V. At least 4 low ESR 0.01 µF bypass capacitors should be connected from V_{DD} to GND plane.
GND	See (2)	5, 11, 15, 20, 26, 30		Ground reference to LVDS and CMOS circuitry. For the UQFN package, the DAP is used as the primary GND connection to the device. The DAP is the exposed metal contact at the bottom of the UQFN-28 package. It should be connected to the ground plane with at least 4 vias for optimal AC and thermal performance.

(1) The LVDS outputs do not support a multidrop (BLVDS) environment. The LVDS output characteristics of the SCAN90CP02 device have been optimized for point-to-point backplane and cable applications.
(2) Note that for the UQFN package GND is not an actual pin on the package, the GND is connected thru the DAP on the back side of the UQFN package.

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Connection Diagrams

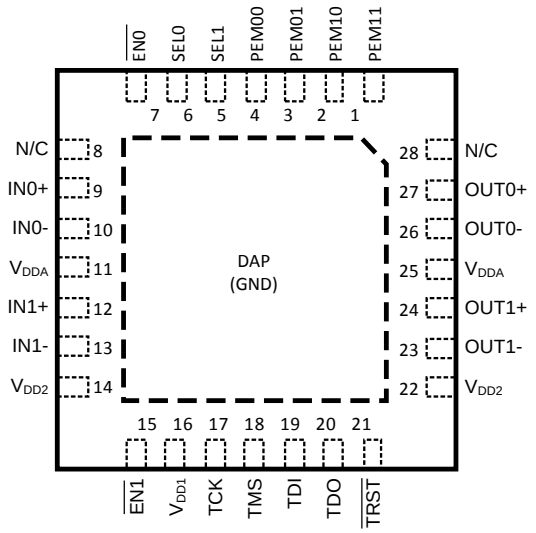


Figure 2. UQFN Top View
DAP = GND

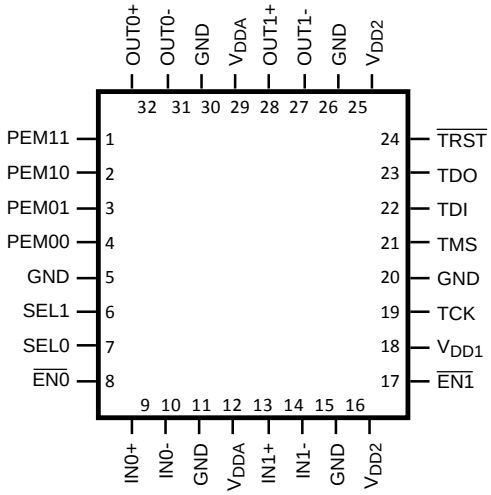


Figure 3. LQFP Top View

CONFIGURATION SELECT TRUTH TABLE(1)

SEL0	SEL1	$\overline{EN0}$	$\overline{EN1}$	OUT0	OUT1	Mode
0	0	0	0	IN0	IN0	1:2 Splitter (IN1 powered down)
0	1	0	0	IN0	IN1	Dual Channel Repeater
1	0	0	0	IN1	IN0	Dual Channel Switch
1	1	0	0	IN1	IN1	1:2 Splitter (IN0 powered down)
0	1	0	1	IN0	PD	Single Channel Repeater (Channel 1 powered down)
1	1	0	1	IN1	PD	Single Channel Switch (IN0 and OUT1 powered down)
0	0	1	0	PD	IN0	Single Channel Switch (IN1 and OUT0 powered down)
0	1	1	0	PD	IN1	Single Channel Repeater (Channel 0 powered down)
X	X	1	1	PD	PD	Both Channels in Power Down Mode
0	0	0	1			Invalid State(2)
1	0	0	1			Invalid State(2)
1	0	1	0			Invalid State(2)
1	1	1	0			Invalid State(2)

(1) PD = Power Down mode to minimize power consumption
X = Don't Care
(2) Entering these states is not forbidden, however device operation is not defined in these states.

PRE-EMPHASIS

The pre-emphasis is used to compensate for long or lossy transmission media. Separate pins are provided for each output to minimize power consumption. Pre-emphasis is programmable to be off or to preset values per Table 1.

Output Characteristics

The output characteristics of the SCAN90CP02 device have been optimized for point-to-point backplane and cable applications.

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Table 1. Pre-emphasis Control Selection Table

Channel 0		Channel 1		Pre-emphasis
PEM01	PEM00	PEM11	PEM10	
0	0	0	0	0%
0	1	0	1	25%
1	0	1	0	50%
1	1	1	1	100%

Applications Information

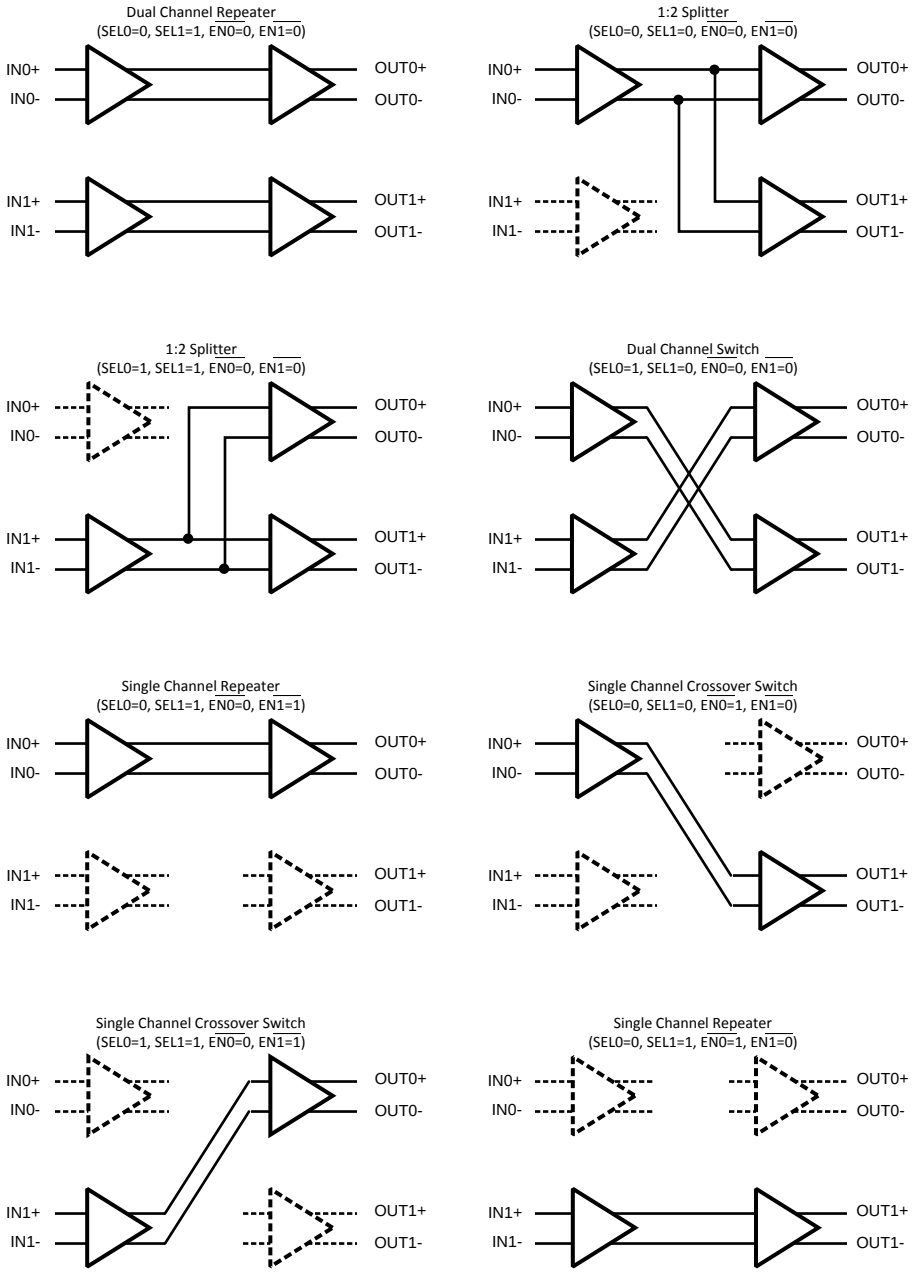


Figure 4. SCAN90CP02 Configuration Select Decode

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)

Supply Voltage (V_{DD})		−0.3V to +4.0V
CMOS Input Voltage		−0.3V to (V_{DD} +0.3V)
LVDS Receiver Input Voltage		−0.3V to +3.6V
LVDS Driver Output Voltage		−0.3V to +3.6V
LVDS Output Short Circuit Current		40mA
Junction Temperature		+150°C
Storage Temperature		−65°C to +150°C
Lead Temperature (Soldering, 4sec.)		+260°C
Maximum Package Power Dissipation at 25°C	UQFN-28	4.31 W
	LQFP-32	1.47 W
Derating above 25°C	UQFN-28	34.5 mW/°C
	LQFP-32	11.8 mW/°C
Thermal Resistance, θ_{JA}	UQFN-28	29°C/W
	LQFP-32	85°C/W
ESD Rating	HBM, 1.5 kΩ, 100 pF	6.5 kV
	EIAJ, 0Ω, 200 pF	>250V

(1) "Absolute Maximum Ratings" are the ratings beyond which the safety of the device cannot be specified. They are not meant to imply that the device should be operated at these limits.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.

RECOMMENDED OPERATING CONDITIONS

	Min	Typ	Max	Unit
Supply Voltage (V_{DD}– GND)	3.0	3.3	3.6	V
Receiver Input Voltage	0		3.6	V
Operating Free Air Temperature	−40	25	85	°C
Junction Temperature			150	°C

ELECTRICAL CHARACTERISTICS

Over recommended operating supply and temperature ranges unless other specified.

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Units
LVTTL DC SPECIFICATIONS (SEL0, SEL1, $\overline{EN1}$, $\overline{EN2}$, PEM00, PEM01, PEM10, PEM11, TDI, TCK, TMS, $\overline{TRST}$)						
V_{IH}	High Level Input Voltage		2.0		V_{DD}	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
I_{IH}	High Level Input Current	$V_{IN} = V_{DD} = V_{DDMAX}$	−10		+10	µA
I_{IL}	Low Level Input Current	$V_{IN} = V_{SS}$, $V_{DD} = V_{DDMAX}$	−10		+10	µA
I_{ILR}	Low Level Input Current	TDI, TMS, $\overline{TRST}$	-40		-200	µA
C_{IN1}	Input Capacitance	Any Digital Input Pin to V_{SS}		3.5		pF
C_{OUT1}	Output Capacitance	Any Digital Output Pin to V_{SS}		5.5		pF
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA	−1.5	−0.8		V
V_{OH}	High Level Output Voltage (TDO)	I_{OH} = −12 mA, V_{DD} = 3.0 V	2.4			V
		I_{OH} = −100 µA, V_{DD} = 3.0 V	V_{DD}-0.2			V
V_{OL}	Low Level Output Voltage (TDO)	I_{OL} = 12 mA, V_{DD} = 3.0 V			0.5	V
		I_{OL} = 100 µA, V_{DD} = 3.0 V			0.2	V
I_{OS}	Output Short Circuit Current	TDO	-15		-125	mA

(1) Typical parameters are measured at V_{DD} = 3.3V, T_A = 25°C. They are for reference purposes, and are not production-tested.

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ELECTRICAL CHARACTERISTICS (continued)

Over recommended operating supply and temperature ranges unless other specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Units
LVDS INPUT DC SPECIFICATIONS (IN0±, IN1±)						
V_{TH}	Differential Input High Threshold[2]	V_{CM} = 0.8V or 1.2V or 3.55V, V_{DD} = 3.6V		0	100	mV
V_{TL}	Differential Input Low Threshold	V_{CM} = 0.8V or 1.2V or 3.55V, V_{DD} = 3.6V	−100	0		mV
V_{ID}	Differential Input Voltage	V_{CM} = 0.8V to 3.55V, V_{DD} = 3.6V	100			mV
V_{CMR}	Common Mode Voltage Range	V_{ID} = 150 mV, V_{DD} = 3.6V	0.05		3.55	V
C_{IN2}	Input Capacitance	IN+ or IN− to V_{SS}		3.5		pF
I_{IN}	Input Current	V_{IN} = 3.6V, V_{DD} = V_{DDMAX} or 0V	−10		+10	µA
		V_{IN} = 0V, V_{DD} = V_{DDMAX} or 0V	−10		+10	µA
LVDS OUTPUT DC SPECIFICATIONS (OUT0±, OUT1±)						
V_{OD}	Differential Output Voltage, 0% Pre-emphasis[2]	R_L = 100Ω between OUT+ and OUT−	250	400	575	mV
ΔV_{OD}	Change in V_{OD} between Complementary States		−35		35	mV
V_{OS}	Offset Voltage[3]		1.09	1.25	1.475	V
ΔV_{OS}	Change in V_{OS} between Complementary States		−35		35	mV
I_{OS}	Output Short Circuit Current, One Complementary Output	OUT+ or OUT− Short to GND		−60	-90	mA
C_{OUT2}	Output Capacitance	OUT+ or OUT− to GND when TRI-STATE		5.5		pF
SUPPLY CURRENT (Static)						
I_{CC0}	Supply Current	All inputs and outputs enabled and active, terminated with differential load of 100Ω between OUT+ and OUT-.		42	60	mA
I_{CC1}	Supply Current - one channel powered down	Single channel crossover switch or single channel repeater modes (1 channel active, one channel in power down mode)		22	30	mA
I_{CC2}	Supply Current - one input powered down	Splitter mode (One input powered down, both outputs active)		30	40	mA
I_{CCZ}	TRI-STATE Supply Current	Both input/output Channels in Power Down Mode		1.4	2.5	mA
SWITCHING CHARACTERISTICS—LVDS OUTPUTS (Figure 5, Figure 6)						
t_{LHT}	Differential Low to High Transition Time	Use an alternating 1 and 0 pattern at 200 Mb/s, measure between 20% and 80% of V_{OD}.	70	150	215	ps
t_{HLT}	Differential High to Low Transition Time		50	135	180	ps
t_{PLHD}	Differential Low to High Propagation Delay	Use an alternating 1 and 0 pattern at 200 Mb/s, measure at 50% V_{OD} between input to output.	0.5	2.4	3.5	ns
t_{PHLD}	Differential High to Low Propagation Delay		0.5	2.4	3.5	ns
t_{SKD1}	Pulse Skew	$\lvert t_{PLHD} - t_{PHLD} \rvert$		55	120	ps
t_{SKCC}	Output Channel to Channel Skew	Difference in propagation delay (t_{PLHD} or t_{PHLD}) among all output channels in Splitter mode (any one input to all outputs).	0	130	315	ps

(2) Differential output voltage V_{OD} is defined as ABS(OUT+–OUT−). Differential input voltage V_{ID} is defined as ABS(IN+–IN−).
(3) Output offset voltage V_{OS} is defined as the average of the LVDS single-ended output voltages at logic high and logic low states.

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ELECTRICAL CHARACTERISTICS (continued)

Over recommended operating supply and temperature ranges unless other specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Units
t_{JIT}	Jitter (0% Pre-emphasis)[4]	RJ - Alternating 1/0 @ 750 MHz[5]			1.4	2.5	psrms
		DJ - K28.5 Pattern	LQFP		110	140	psp-p
		1.5 Gbps[6]	UQFN		42	75	psp-p
		TJ - PRBS 2^{23}-1 Pattern	LQFP		113	148	psp-p
		1.5 Gbps[7]	UQFN		93	126	psp-p
t_{ON}	LVDS Output Enable Time	Time from $\overline{ENx}$ to OUT± change from TRI-STATE to active.		50	110	150	ns
t_{OFF}	LVDS Output Disable Time	Time from $\overline{ENx}$ to OUT± change from active to TRI-STATE.			5	12	ns
t_{SW}	LVDS Switching Time SELx to OUT±	Time from configuration select (SELx) to new switch configuration effective for OUT±.			110	150	ns

(4) Jitter is not production tested, but specified through characterization on a sample basis.
(5) Random Jitter, or RJ, is measured RMS with a histogram including 1500 histogram window hits. The input voltage = V_{ID} = 500mV, 50% duty cycle at 750MHz, $t_r = t_f$ = 50ps (20% to 80%).
(6) Deterministic Jitter, or DJ, is measured to a histogram mean with a sample size of 350 hits. The input voltage = V_{ID} = 500mV, K28.5 pattern at 1.5 Gbps, $t_r = t_f$ = 50ps (20% to 80%). The K28.5 pattern is repeating bit streams of (0011111010 1100000101).
(7) Total Jitter, or TJ, is measured peak to peak with a histogram including 3500 window hits. Stimulus and fixture jitter has been subtracted. The input voltage = V_{ID} = 500mV, 2^{23}-1 PRBS pattern at 1.5 Gbps, $t_r = t_f$ = 50ps (20% to 80%).

SCAN CIRCUITRY TIMING REQUIREMENTS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{MAX}	Maximum TCK Clock Frequency	R_L = 500Ω, C_L = 35 pF	25.0			MHz
t_S	TDI to TCK, H or L		1.0			ns
t_H	TDI to TCK, H or L		2.0			ns
t_S	TMS to TCK, H or L		2.0			ns
t_H	TMS to TCK, H or L		1.5			ns
t_W	TCK Pulse Width, H or L		10.0			ns
t_W	$\overline{TRST}$ Pulse Width, L		2.5			ns
t_{REC}	Recovery Time, $\overline{TRST}$ to TCK		2.0			ns

TIMING DIAGRAMS

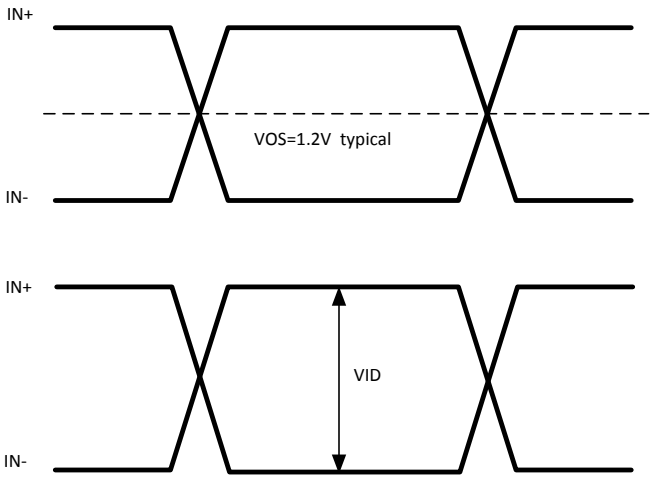


Figure 5. LVDS Signals

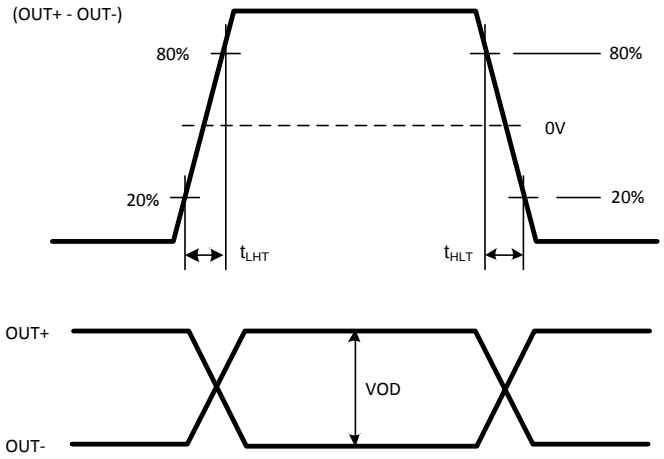


Figure 6. LVDS Output Transition Time

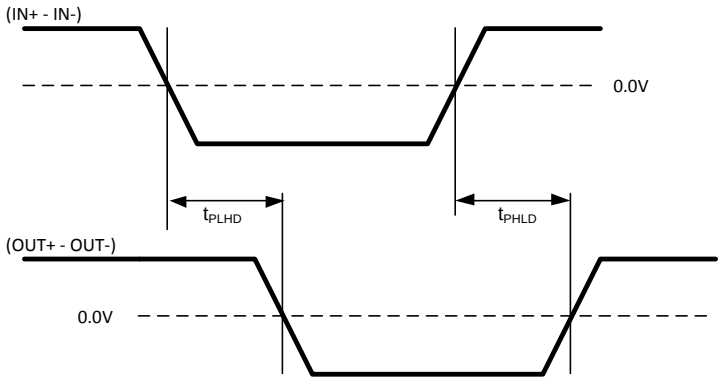


Figure 7. LVDS Output Propagation Delay

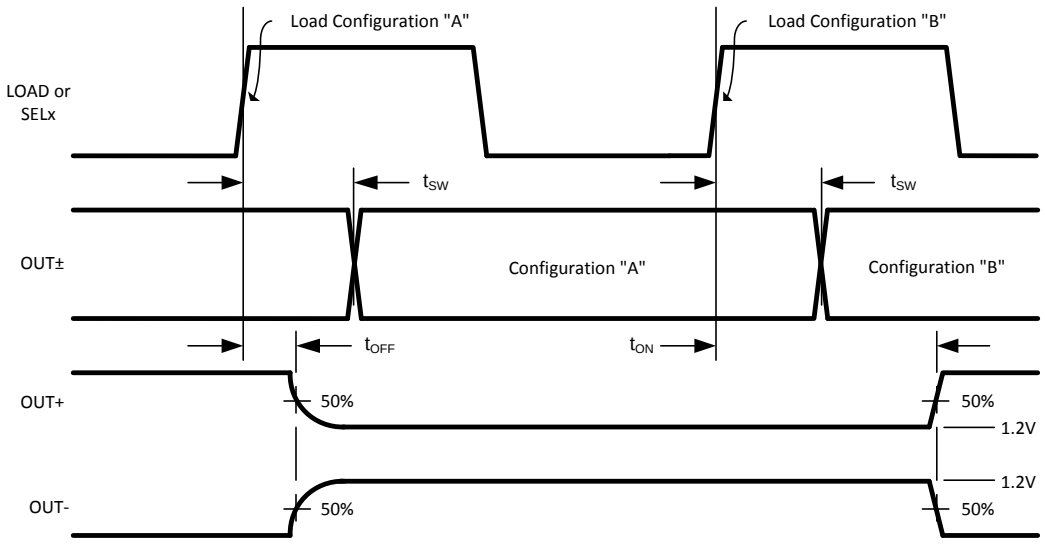


Figure 8. Configuration and Output Enable/Disable Timing

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Input Interfacing

The SCAN90CP02 accepts differential signals and allow simple AC or DC coupling. With a wide common mode range, the SCAN90CP02 can be DC-coupled with all common differential drivers (i.e. LVPECL, LVDS, CML). The following three figures illustrate typical DC-coupled interface to common differential drivers.

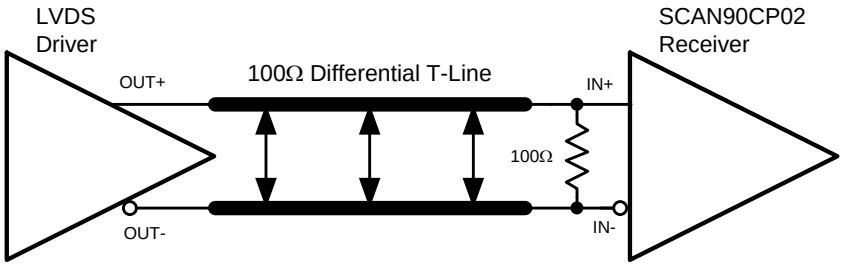


Figure 9. Typical LVDS Driver DC-Coupled Interface to SCAN90CP02 Input

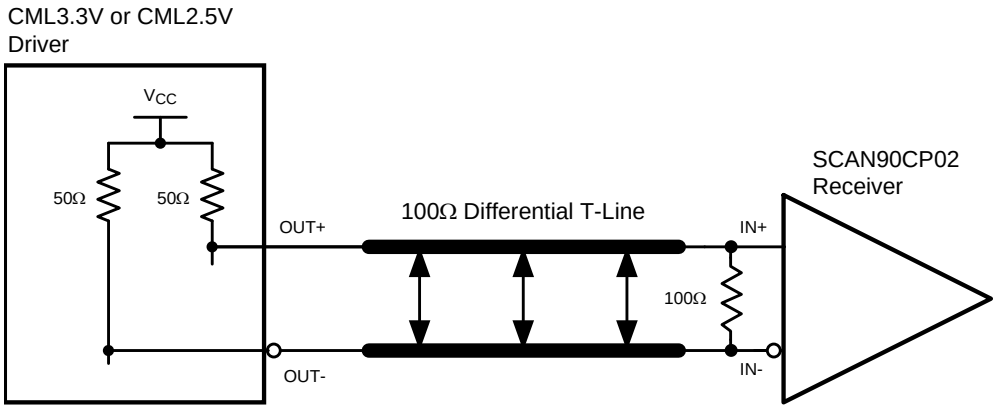


Figure 10. Typical CML Driver DC-Coupled Interface to SCAN90CP02 Input

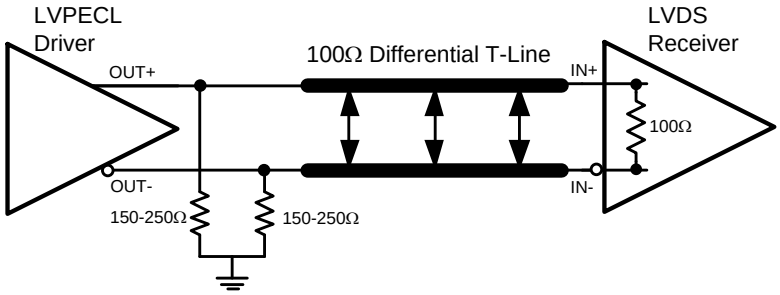


Figure 11. Typical LVPECL Driver DC-Coupled Interface to SCAN90CP02 Input

Output Interfacing

The SCAN90CP02 outputs signals that are compliant to the LVDS standard. Their outputs can be DC-coupled to most common differential receivers. Figure 12 illustrates typical DC-coupled interface to common differential receivers and assumes that the receivers have high impedance inputs. While most differential receivers have a common mode input range that can accommodate LVDS compliant signals, it is recommended to check respective receiver's data sheet prior to implementing the suggested interface implementation.

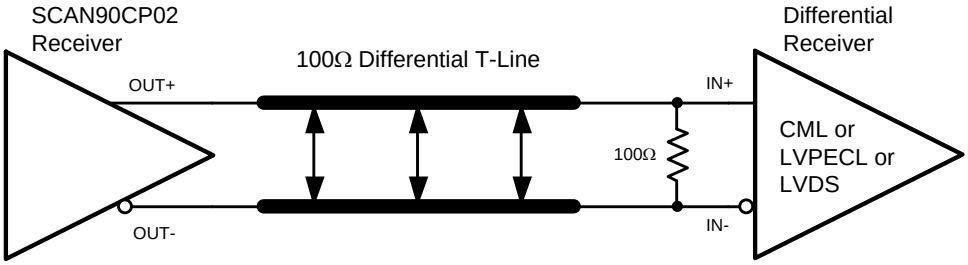
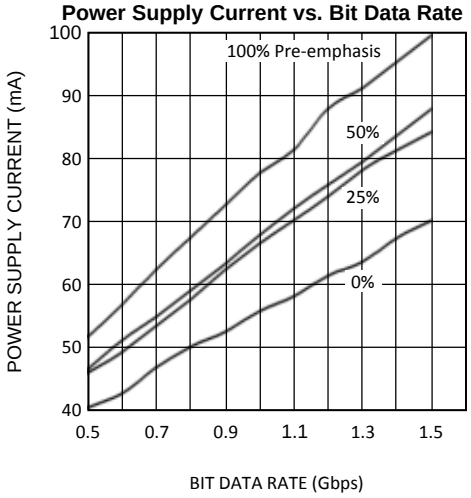


Figure 12. Typical SCAN90CP02 Output DC-Coupled Interface to an LVDS, CML or LVPECL Receiver

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TYPICAL PERFORMANCE CHARACTERISTICS FOR UQFN PACKAGE

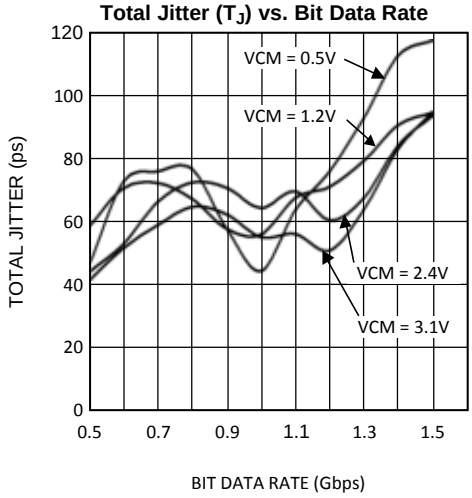
Power Supply Current vs. Bit Data Rate



Dynamic power supply current was measured while running a PRBS 2^{23}-1 pattern in dual channel repeater mode. V_{CC} = 3.3V, T_A = +25°C, V_{ID} = 0.5V, V_{CM} = 1.2V

Figure 13.

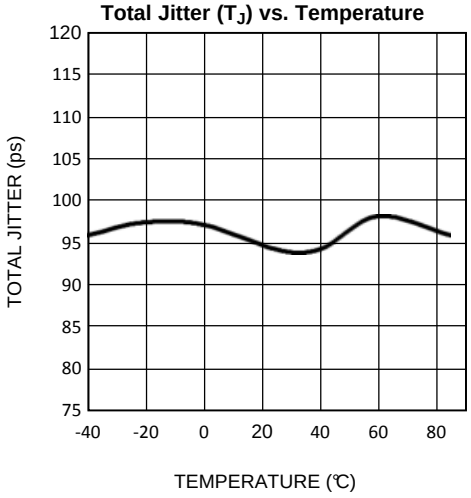
Total Jitter (T_J) vs. Bit Data Rate



Total Jitter measured at 0V differential while running a PRBS 2^{23}-1 pattern in single channel repeater mode. V_{CC} = 3.3V, T_A = +25°C, V_{ID} = 0.5V, 0% Pre-emphasis

Figure 14.

Total Jitter (T_J) vs. Temperature



Total Jitter measured at 0V differential while running a PRBS 2^{23}-1 pattern in dual channel repeater mode. V_{CC} = 3.3V, V_{ID} = 0.5V, V_{CM} = 1.2V, 1.5 Gbps data rate, 0% Pre-emphasis

Figure 15.

Positive Edge Transition vs. Pre-emphasis Level

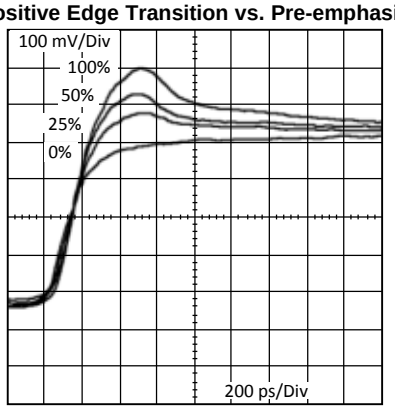


Figure 16.

DESIGN-FOR-TEST (DFT) FEATURES

IEEE 1149.1 SUPPORT

The SCAN90CP02 supports a fully compliant IEEE 1149.1 interface. The Test Access Port (TAP) provides access to boundary scan cells at each LVTTL I/O on the device for interconnect testing. Differential pins are included in the same boundary scan chain but instead contain IEEE1149.6 cells. IEEE1149.6 is the improved IEEE standard for testing high-speed differential signals.

Refer to the BSDL file located on TI's website for the details of the SCAN90CP02 IEEE 1149.1 implementation.

IEEE 1149.6 SUPPORT

AC-coupled differential interconnections on very high speed (1+ Gbps) data paths are not testable using traditional IEEE 1149.1 techniques. The IEEE 1149.1 structures and methods are intended to test static (DC-coupled), single ended networks. IEEE1149.6 is specifically designed for testing high-speed differential, including AC coupled networks.

The SCAN90CP02 is intended for high-speed signaling up to 1.5 Gbps and includes IEEE1149.6 on all differential inputs and outputs.

FAULT INSERTION

Fault Insertion is a technique used to assist in the verification and debug of diagnostic software. During system testing faults are "injected" to simulate hardware failure and thus help verify the monitoring software can detect and diagnose these faults. In the SCAN90004 an IEEE1149.1 "stuck-at" instruction can create a stuck-at condition, either high or low, on any pin or combination of pins.

A more detailed description of the stuck-at feature can be found in Texas Instruments Applications note AN-1313(SNLA060).

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REVISION HISTORY

Changes from Revision L (April 2013) to Revision M	Page
• Changed layout of National Data Sheet to TI format	12

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SCAN90CP02SP/NOPB	Active	Production	UQFN (NJD) | 28	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	SCP02SP
SCAN90CP02SP/NOPB.A	Active	Production	UQFN (NJD) | 28	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	SCP02SP
SCAN90CP02VY/NOPB	Active	Production	LQFP (NEY) | 32	250 | JEDEC TRAY (10+1)	Yes	SN	Level-3-260C-168 HR	-40 to 85	SCAN90 CP02VY
SCAN90CP02VY/NOPB.A	Active	Production	LQFP (NEY) | 32	250 | JEDEC TRAY (10+1)	Yes	SN	Level-3-260C-168 HR	-40 to 85	SCAN90 CP02VY

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

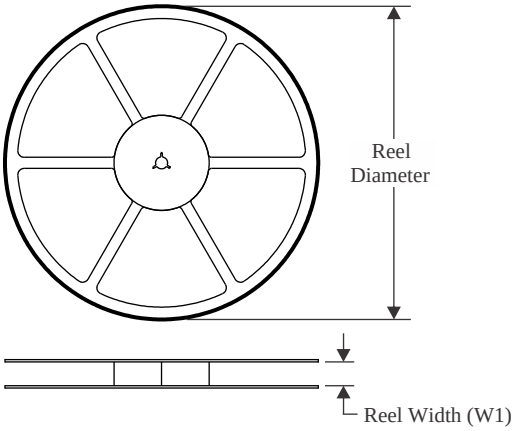
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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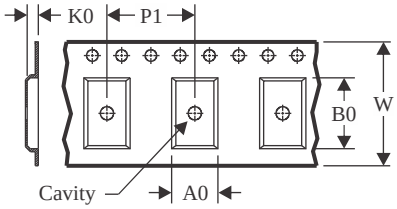
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

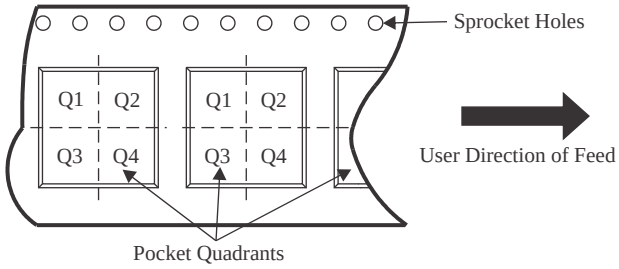


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

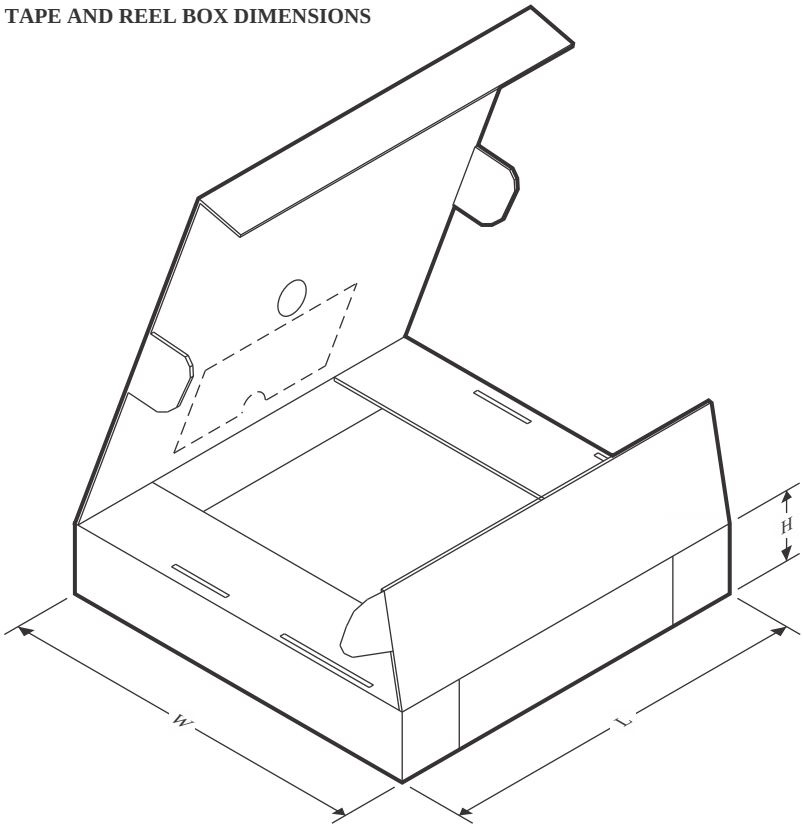
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SCAN90CP02SP/NOPB	UQFN	NJD	28	1000	177.8	12.4	5.3	5.3	1.3	8.0	12.0	Q1

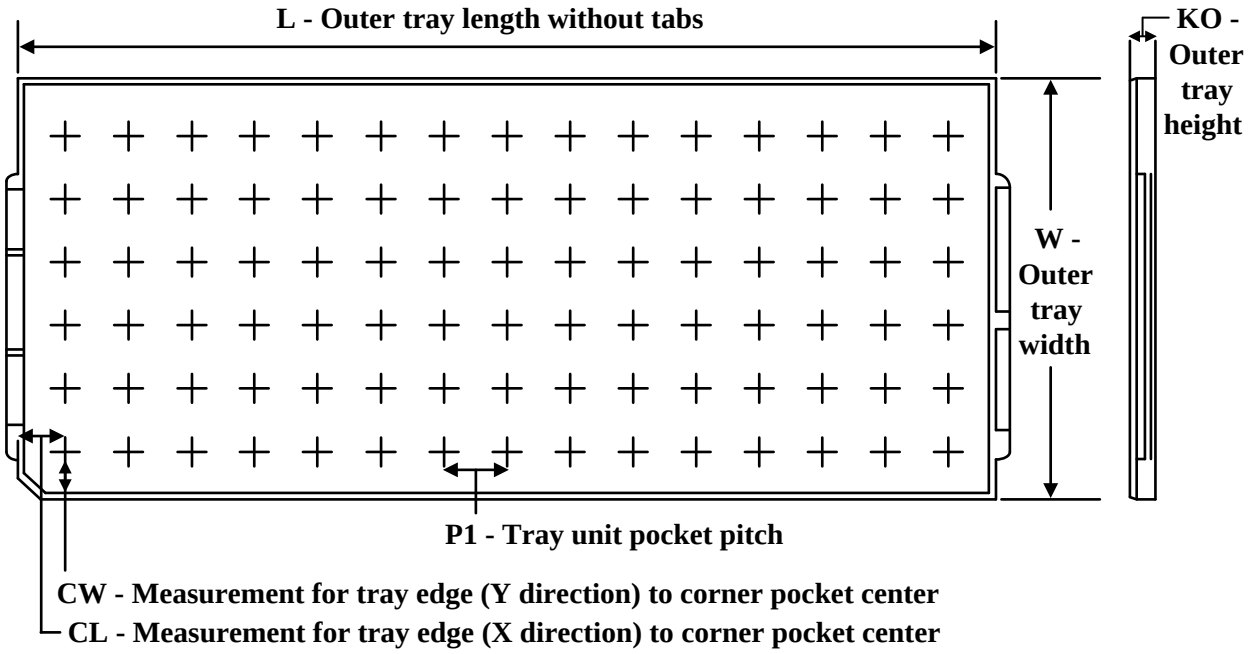
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SCAN90CP02SP/NOPB	UQFN	NJD	28	1000	208.0	191.0	35.0

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
SCAN90CP02VY/NOPB	NEY	LQFP	32	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
SCAN90CP02VY/ NOPB.A	NEY	LQFP	32	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25

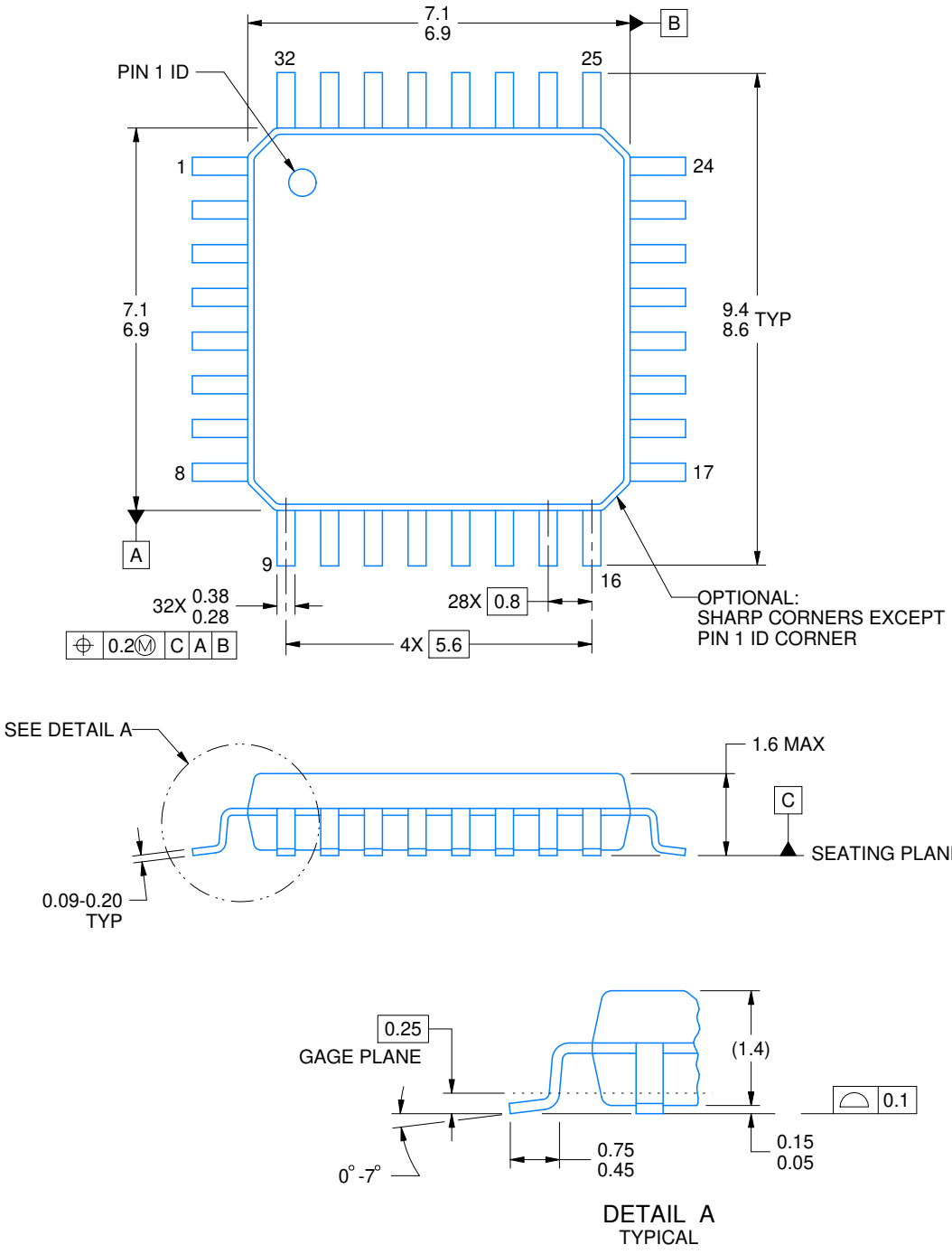


PACKAGE OUTLINE

NEY0032A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



NOTES:

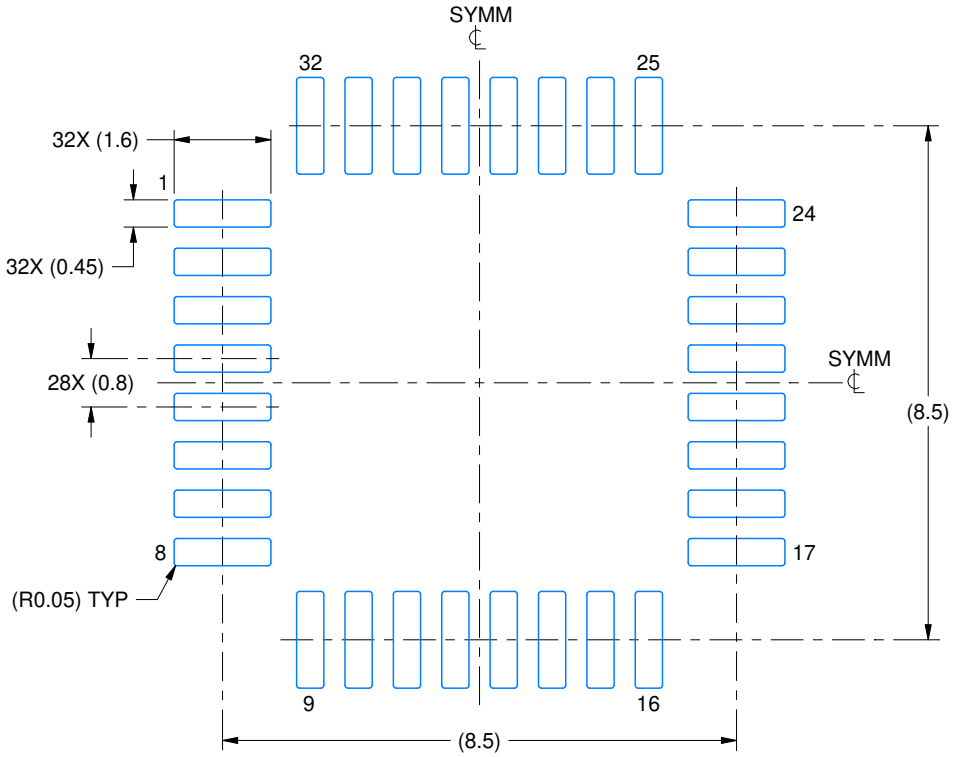
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.

EXAMPLE BOARD LAYOUT

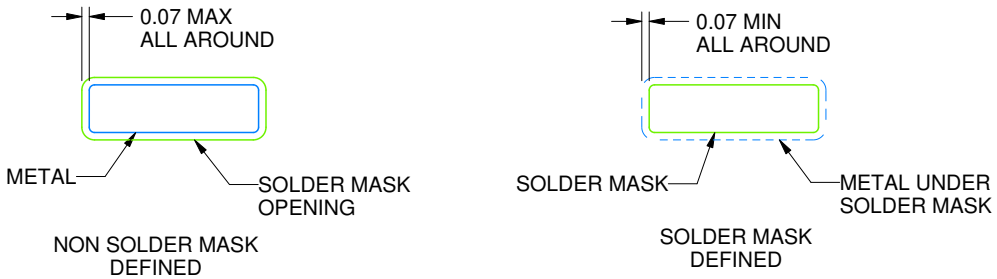
NEY0032A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4219901/B 05/2026

NOTES: (continued)

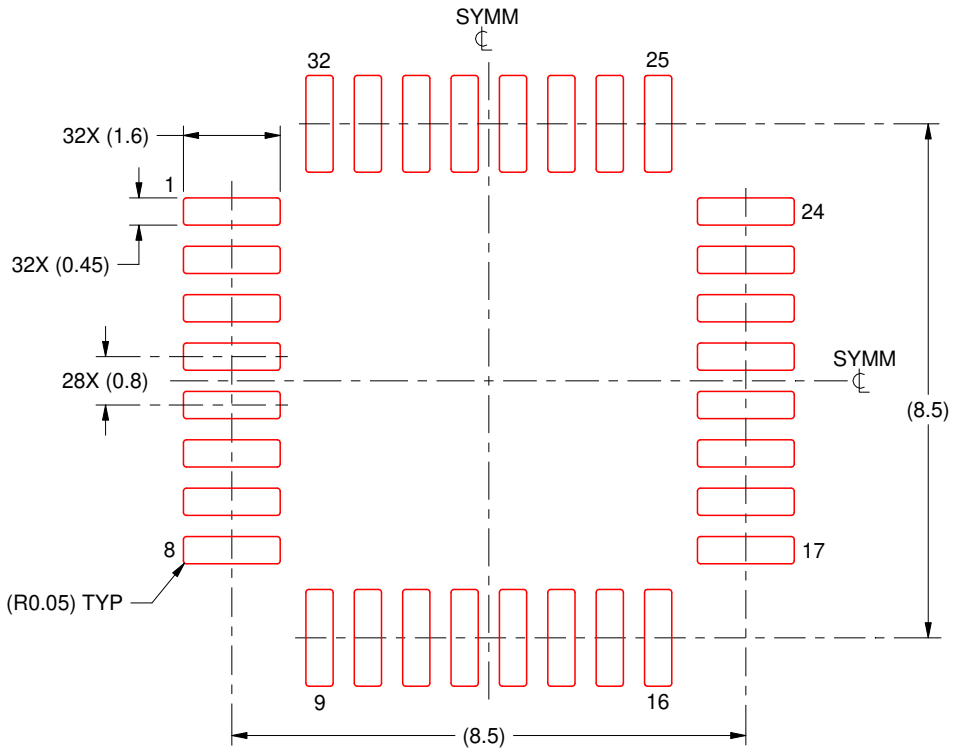
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

NEY0032A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



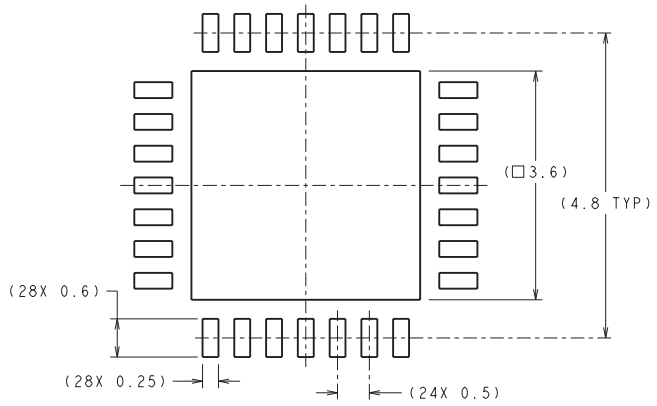
SOLDER PASTE EXAMPLE
SCALE 8X

4219901/B 05/2026

NOTES: (continued)

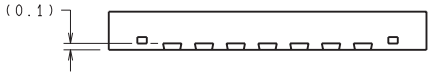
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

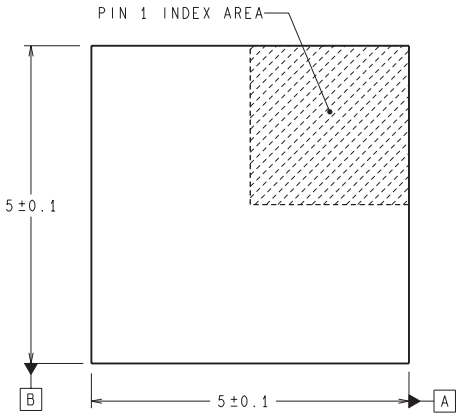
NJD0028A

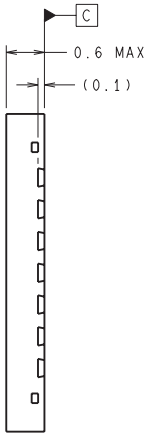


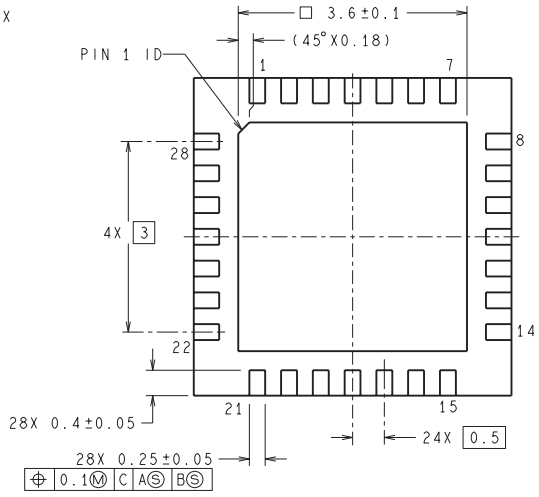
RECOMMENDED LAND PATTERN

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY









SPA28A (Rev A)

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