SN54LVC573A, SN74LVC573A
SCAS300S – JANUARY 1993 – REVISED MAY 2014

# SNx4LVC573A Octal Transparent D-Type Latches With 3-State Outputs

## 1 Features

- Operate From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max $t_{pd}$ of 6.9 ns at 3.3 V
- Typical $V_{OLP}$ (Output Ground Bounce) < 0.8 V at $V_{CC}$ = 3.3 V, $T_A$ = 25°C
- Typical $V_{OHV}$ (Output $V_{OH}$ Undershoot) > 2 V at $V_{CC}$ = 3.3 V, $T_A$ = 25°C
- Support Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V $V_{CC}$)
- $I_{off}$ Supports Live Insertion, Partial Power Down Mode, and Back Drive Protection
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

## 2 Applications

- Servers
- PC, Notebook
- Network Switch
- Health & Fitness/Wearables
- Telecom Infrastructure
- Electronic Point of Sales

## 3 Description

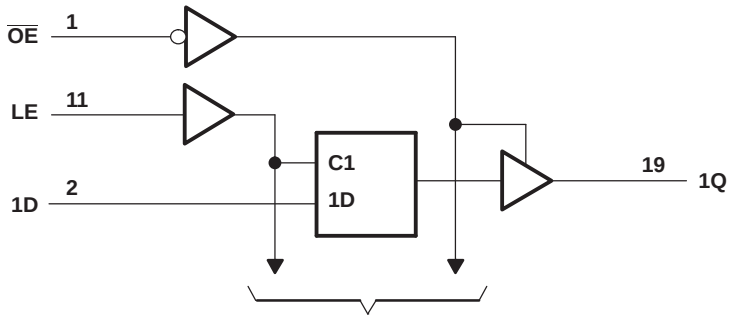
The SN54LVC573A octal transparent D-type latch is designed for 2.7-V to 3.6-V $V_{CC}$ operation, and the SN74LVC573A octal transparent D-type latch is designed for 1.65-V to 3.6-V $V_{CC}$ operation. These devices feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, input/output (I/O) ports, bidirectional bus drivers, and working registers.

**Device Information**(1)

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| SN74LVC573A | PDIP (20) | 25.40 x 6.35 mm |
| | VQGN (20) | 4.50 x 3.50 mm |
| | SOIC (20) | 12.80 x 7.50 mm |
| | SSOP (20) | 7.20 x 5.30 mm |
| | TVSOP (20) | 5.00 x 4.40 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

## 4 Simplified Schematic




Pin numbers shown are for the DB, DGV, DW, FK, J, N, NS, PW, RGY, and W packages.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production

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## 5 Revision History

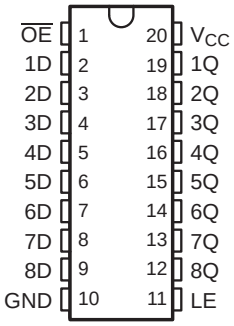
**Changes from Revision R (September 2005) to Revision S** — **Page**

- Removed Ordering Information table. ... 1
- Updated device temperature ratings. ... 4
- Added Handling Ratings. ... 4
- Added Typical Characteristics. ... 7
- Added Detailed Description section. ... 9
- Added Applications and Implemetation section. ... 10
- Added Power Supply Recommendations section. ... 11
- Added Layout section. ... 11

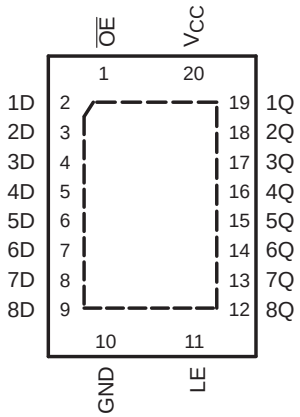

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# 6 Pin Configuration and Functions

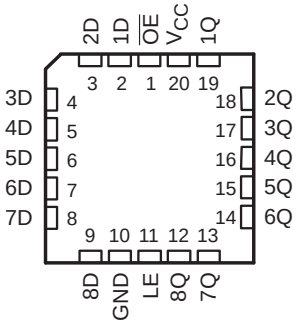
**SN54LVC573A . . . J OR W PACKAGE**
**SN74LVC573A . . . DB, DGV, DW, N, NS, OR PW PACKAGE**
**(TOP VIEW)**



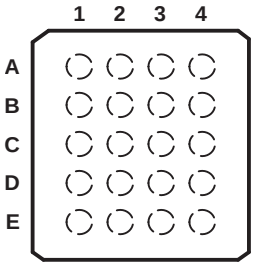

**SN74LVC573A . . . RGY PACKAGE**
**(TOP VIEW)**




**SN54LVC573A . . . FK PACKAGE**
**(TOP VIEW)**




**GQN OR ZQN PACKAGE**
**(TOP VIEW)**




## Pin Functions

| PIN | | | | DESCRIPTION |
|---|---|---|---|---|
| NAME | SN54LVC573A | SN74LVC573A | GQN AND ZQN | |
| | J, W, AND FK | DB, DGV, DW, N, NS, PW, AND RGY | | |
| $\overline{OE}$ | 1 | 1 | A2 | Enable Pin |
| 1D | 2 | 2 | A1 | Input 1 |
| 2D | 3 | 3 | B3 | Input 2 |
| 3D | 4 | 4 | B1 | Input 3 |
| 4D | 5 | 5 | C2 | Input 4 |
| 5D | 6 | 6 | C1 | Input 5 |
| 6D | 7 | 7 | D3 | Input 6 |
| 7D | 8 | 8 | D1 | Input 7 |
| 8D | 9 | 9 | E2 | Input 8 |
| GND | 10 | 10 | E1 | Ground Pin |
| LE | 11 | 11 | E3 | Latch Enable |
| 8Q | 12 | 12 | E4 | Output 8 |
| 7Q | 13 | 13 | D2 | Output 7 |
| 6Q | 14 | 14 | D4 | Output 6 |
| 5Q | 15 | 15 | C3 | Output 5 |
| 4Q | 16 | 16 | C4 | Output 4 |
| 3Q | 17 | 17 | B2 | Output 3 |
| 2Q | 18 | 18 | B4 | Output 2 |
| 1Q | 19 | 19 | A4 | Output 1 |
| $V_{CC}$ | 20 | 20 | A3 | Power Pin |

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# 7 Specifications

## 7.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | –0.5 | 6.5 | V |
| $V_I$ | Input voltage range(2) | | –0.5 | 6.5 | V |
| $V_O$ | Voltage range applied to any output in the high-impedance or power-off state(2) | | –0.5 | 6.5 | V |
| $V_O$ | Voltage range applied to any output in the high or low state(2)(3) | | –0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | $V_I$ < 0 | | –50 | mA |
| $I_{OK}$ | Output clamp current | $V_O$ < 0 | | –50 | mA |
| $I_O$ | Continuous output current | | | ±50 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±100 | mA |
| $\theta_{JA}$ | Package thermal impedance | DB package(4) | | 70 | °C/W |
| | | DGV package(4) | | 92 | |
| | | DW package(4) | | 58 | |
| | | GQN or ZQN package(4) | | 78 | |
| | | N package(4) | | 69 | |
| | | NS package(4) | | 60 | |
| | | PW package(4) | | 83 | |
| | | RGY package(5) | | 37 | |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of $V_{CC}$ is provided in the recommended operating conditions table.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.
(5) The package thermal impedance is calculated in accordance with JESD 51-5.

## 7.2 Handling Ratings

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | 0 | 2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | 0 | 1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as 500 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as 250 V may actually have higher performance.


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## 7.3 Recommended Operating Conditions(1)

| | | | SN54LVC573A | | SN74LVC573A | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | Operating | 2 | 3.6 | 1.65 | 3.6 | V |
| | | Data retention only | 1.5 | | 1.5 | | |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | | | 0.65 × $V_{CC}$ | | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | | 1.7 | | |
| | | $V_{CC}$ = 2.7 V to 3.6 V | 2 | | 2 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | | | | 0.35 × $V_{CC}$ | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | | | 0.7 | |
| | | $V_{CC}$ = 2.7 V to 3.6 V | | 0.8 | | 0.8 | |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | High or low state | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| | | 3-state | 0 | 5.5 | 0 | 5.5 | |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 1.65 V | | | | –4 | mA |
| | | $V_{CC}$ = 2.3 V | | | | –8 | |
| | | $V_{CC}$ = 2.7 V | | –12 | | –12 | |
| | | $V_{CC}$ = 3 V | | –24 | | –24 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 1.65 V | | | | 4 | mA |
| | | $V_{CC}$ = 2.3 V | | | | 8 | |
| | | $V_{CC}$ = 2.7 V | | 12 | | 12 | |
| | | $V_{CC}$ = 3 V | | 24 | | 24 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | | 6 | | 6 | ns/V |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## 7.4 Thermal Information

| THERMAL METRIC(1) | | SN74LVC573A | UNIT |
|---|---|---|---|
| | | PW | |
| | | 20 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 102.5 | °C/W |
| $R_{\theta JCtop}$ | Junction-to-case (top) thermal resistance | 35.9 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 53.5 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 2.2 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 52.9 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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## 7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | $V_{CC}$ | SN54LVC573A | | | SN74LVC573A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP(1) | MAX | MIN | TYP(1) | MAX | |
| $V_{OH}$ | $I_{OH}$ = –100 µA | | 1.65 V to 3.6 V | | | | $V_{CC}$ – 0.2 | | | V |
| | | | 2.7 V to 3.6 V | $V_{CC}$ – 0.2 | | | | | | |
| | $I_{OH}$ = –4 mA | | 1.65 V | | | | 1.2 | | | |
| | $I_{OH}$ = –8 mA | | 2.3 V | | | | 1.7 | | | |
| | $I_{OH}$ = –12 mA | | 2.7 V | 2.2 | | | 2.2 | | | |
| | | | 3 V | 2.4 | | | 2.4 | | | |
| | $I_{OH}$ = –24 mA | | 3 V | 2.2 | | | 2.2 | | | |
| $V_{OL}$ | $I_{OL}$ = 100 µA | | 1.65 V to 3.6 V | | | | | | 0.2 | V |
| | | | 2.7 V to 3.6 V | | | 0.2 | | | | |
| | $I_{OL}$ = 4 mA | | 1.65 V | | | | | | 0.45 | |
| | $I_{OL}$ = 8 mA | | 2.3 V | | | | | | 0.7 | |
| | $I_{OL}$ = 12 mA | | 2.7 V | | | 0.4 | | | 0.4 | |
| | $I_{OL}$ = 24 mA | | 3 V | | | 0.55 | | | 0.55 | |
| $I_I$ | $V_I$ = 0 to 5.5 V | | 3.6 V | | | ±5 | | | ±5 | µA |
| $I_{off}$ | $V_I$ or $V_O$ = 5.5 V | | 0 | | | | | | ±10 | µA |
| $I_{OZ}$ | $V_O$ = 0 to 5.5 V | | 3.6 V | | | ±15 | | | ±10 | µA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND | $I_O$ = 0 | 3.6 V | | | 10 | | | 10 | µA |
| | 3.6 V ≤ $V_I$ ≤ 5.5 V(2) | | | | | 10 | | | 10 | |
| $\Delta I_{CC}$ | One input at $V_{CC}$ – 0.6 V, Other inputs at $V_{CC}$ or GND | | 2.7 V to 3.6 V | | | 500 | | | 500 | µA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | | 3.3 V | | 4 | | | 4 | | pF |
| $C_o$ | $V_O$ = $V_{CC}$ or GND | | 3.3 V | | 5.5 | | | 5.5 | | pF |

(1) All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.
(2) This applies in the disabled state only.

## 7.6 Timing Requirements, SN54LVC573A

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

| | | SN54LVC573A | | | | UNIT |
|---|---|---|---|---|---|---|
| | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | |
| | | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration, LE high | 3.3 | | 3.3 | | ns |
| $t_{su}$ | Setup time, data before LE↓ | 2 | | 2 | | ns |
| $t_h$ | Hold time, data after LE↓ | 2.5 | | 2.5 | | ns |

## 7.7 Timing Requirements, SN74LVC573A

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

| | | SN74LVC573A | | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | $V_{CC}$ = 1.8 V ± 0.15 V | | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | |
| | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration, LE high | 9 | | 4 | | 3.3 | | 3.3 | | ns |
| $t_{su}$ | Setup time, data before LE↓ | 6 | | 4 | | 2 | | 2 | | ns |
| $t_h$ | Hold time, data after LE↓ | 4 | | 2 | | 1.5 | | 1.5 | | ns |


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## 7.8 Switching Characteristics, SN54LVC573A

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LVC573A | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | |
| | | | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | D | Q | | 7.7 | 1 | 6.9 | ns |
| | LE | | | 8.4 | 1 | 7.7 | |
| $t_{en}$ | $\overline{OE}$ | Q | | 8.5 | 1 | 7.5 | ns |
| $t_{dis}$ | $\overline{OE}$ | Q | | 7 | 0.5 | 6.7 | ns |

## 7.9 Switching Characteristics, SN74LVC573A

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN74LVC573A | | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 1.8 V ± 0.15 V | | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | D | Q | 1 | 19.1 | 1 | 9.6 | 1 | 7.7 | 1.5 | 6.9 | ns |
| | LE | | 1 | 22.8 | 1 | 10.5 | 1 | 8.4 | 2 | 7.7 | |
| $t_{en}$ | $\overline{OE}$ | Q | 1 | 20 | 1 | 10.5 | 1 | 8.5 | 1.5 | 7.5 | ns |
| $t_{dis}$ | $\overline{OE}$ | Q | 1 | 19.3 | 1 | 7.8 | 1 | 7 | 1.6 | 6.5 | ns |
| $t_{sk(o)}$ | | | | | | | | | | 1 | ns |

## 7.10 Operating Characteristics

$T_A$ = 25°C

| PARAMETER | | | TEST CONDITIONS | $V_{CC}$ = 1.8 V | $V_{CC}$ = 2.5 V | $V_{CC}$ = 3.3 V | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | TYP | TYP | TYP | |
| $C_{pd}$ | Power dissipation capacitance per latch | Outputs enabled | f = 10 MHz | 61 | 56 | 37 | pF |
| | | Outputs disabled | | 3 | 3 | 4 | |

## 7.11 Typical Characteristics

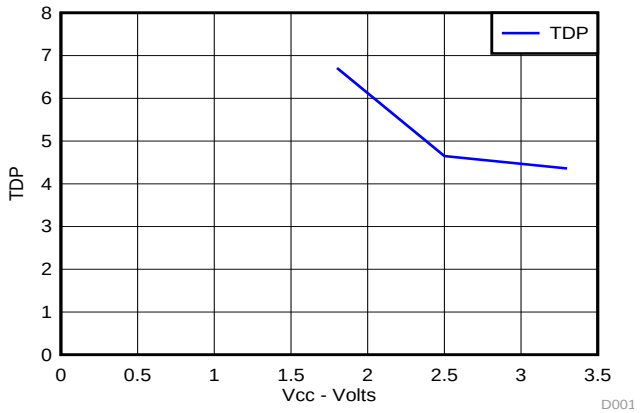



**Figure 1. SN74LVC573A LE to Q TDP Vcc vs TPD at 25°C**

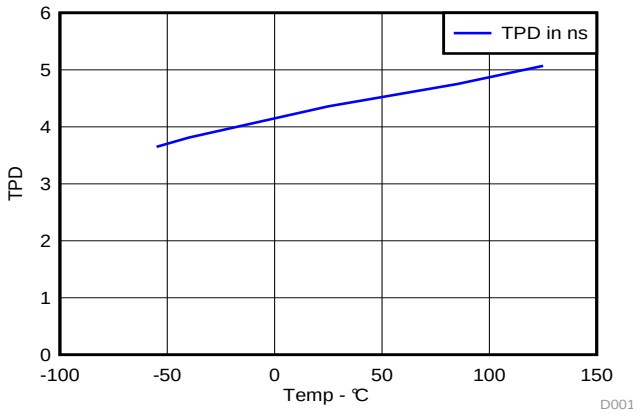
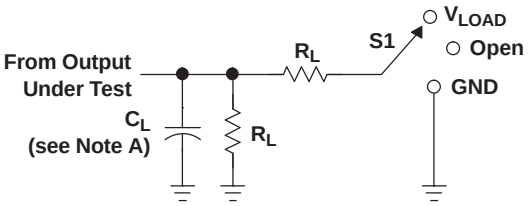



**Figure 2. SN74LVC573A LE to Q Across Temp 3.3V Vcc**

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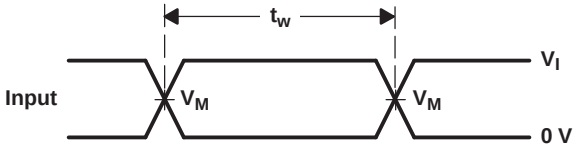
# 8 Parameter Measurement Information



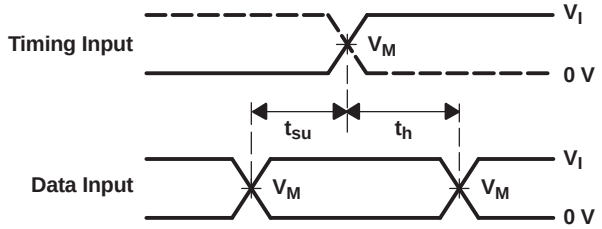

LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

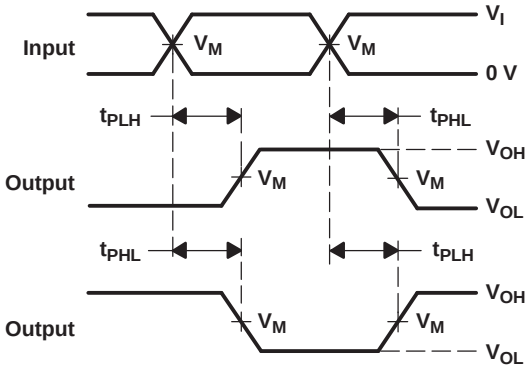
| $V_{CC}$ | INPUTS | | $V_M$ | $V_{LOAD}$ | $C_L$ | $R_L$ | $V_\Delta$ |
|---|---|---|---|---|---|---|---|
| | $V_I$ | $t_r/t_f$ | | | | | |
| 1.8 V ± 0.15 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 kΩ | 0.15 V |
| 2.5 V ± 0.2 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 Ω | 0.15 V |
| 2.7 V | 2.7 V | ≤2.5 ns | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
| 3.3 V ± 0.3 V | 2.7 V | ≤2.5 ns | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |



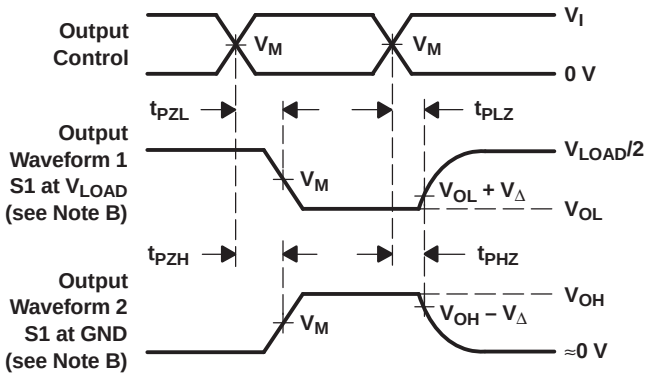

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.
H. All parameters and waveforms are not applicable to all devices.

**Figure 3. Load Circuit and Voltage Waveforms**

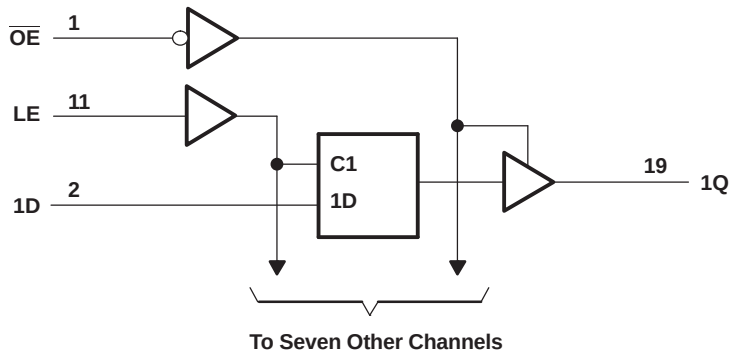

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# 9 Detailed Description

## 9.1 Overview

The SN54LVC573A octal transparent D-type latch is designed for 2.7-V to 3.6-V $V_{CC}$ operation, and the SN74LVC573A octal transparent D-type latch is designed for 1.65-V to 3.6-V $V_{CC}$ operation. These devices feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, input/output (I/O) ports, bidirectional bus drivers, and working registers. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels at the D inputs. A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components. $\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state. These devices are fully specified for partial-power-down applications using $I_{off}$. The $I_{off}$ circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

## 9.2 Functional Block Diagram




Pin numbers shown are for the DB, DGV, DW, FK, J, N, NS, PW, RGY, and W packages.

## 9.3 Feature Description

- Wide operating voltage range
  - Operates from 1.65 V to 3.6 V
- Allows down voltage translation
  - Inputs accept voltages to 5.5 V
- $I_{off}$ Feature
  - Allows voltages on the inputs and outputs when $V_{CC}$ is 0 V

## 9.4 Device Functional Modes

**Function Table (Each Latch)**

| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OE}$ | LE | D | Q |
| L | H | H | H |
| L | H | L | L |
| L | L | X | $Q_0$ |
| H | X | X | Z |

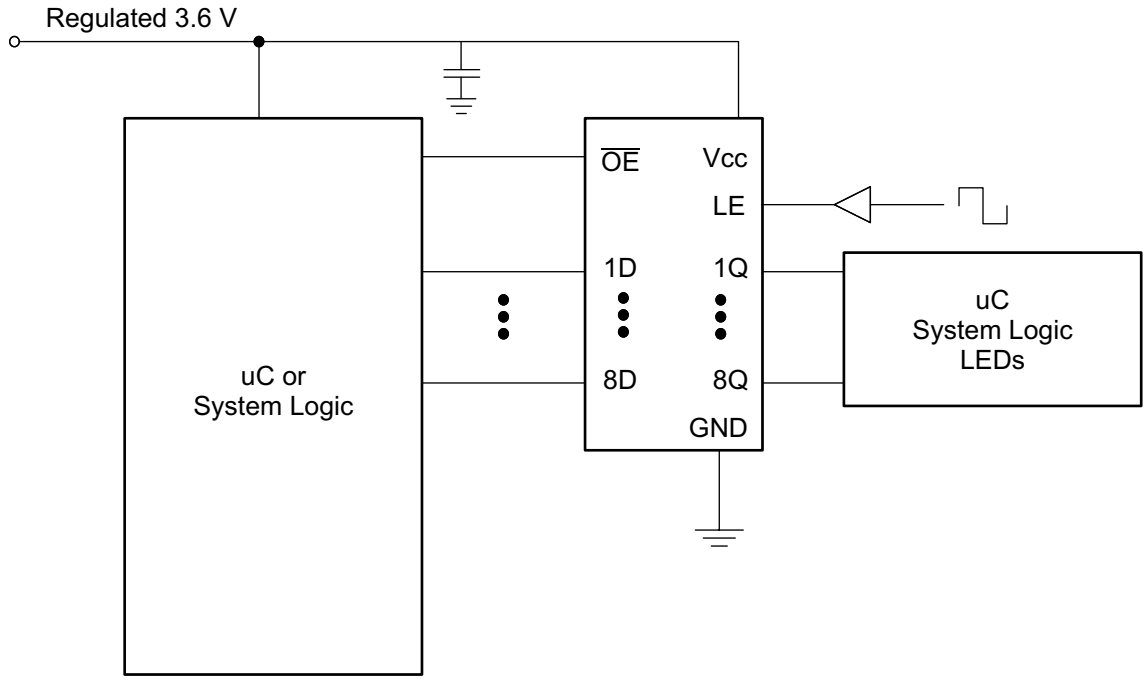
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# 10 Applications and Implementation

## 10.1 Application Information

The SN74LVC573A is a high drive CMOS device that can be used for a multitude of bus interface type applications where the data needs to be retained or latched . It can produce 24 mA of drive current at 3.3 V making it Ideal for driving multiple outputs and good for high speed applications up to 100 MHz. The inputs are 5.5 V tolerant allowing it to translate down to $V_{CC}$.

## 10.2 Typical Application




### 10.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

### 10.2.2 Detailed Design Procedure

1. Recommended Input conditions
   - Rise time and fall time specifications. See (Δt/ΔV) in Recommended Operating Conditions table.
   - Specified high and low levels. See ($V_{IH}$ and $V_{IL}$) in Recommended Operating Conditions table.
   - Inputs are overvoltage tolerant allowing them to go as high as 5.5V at any valid $V_{CC}$.
2. Recommend output conditions
   - Load currents should not exceed 25 mA per output and 50 mA total for the part.
   - Outputs should not be pulled above $V_{CC}$.


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## Typical Application (continued)

### 10.2.3 Application Curves

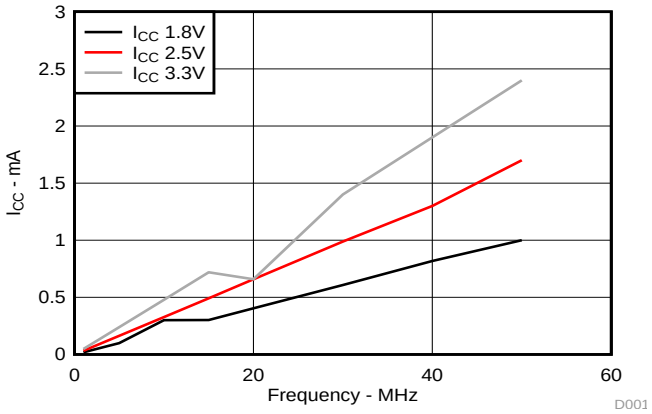



**Figure 4. SN74LVC573A $I_{CC}$ vs Frequency**

## 11 Power Supply Recommendations

The power supply can be any voltage between the Min and Max supply voltage rating located in the Recommended Operating Conditions table.

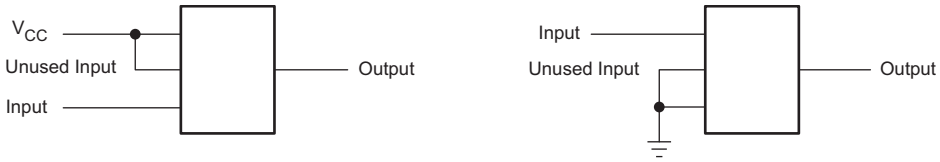
Each $V_{CC}$ pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-µF capacitor is recommended. If there are multiple VCC pins, then a 0.01-µF or 0.022-µF capacitor is recommended for each power pin. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

## 12 Layout

### 12.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or $V_{CC}$ whichever make more sense or is more convenient. It is generally OK to float outputs unless the part is a transceiver. If the transceiver has an output enable pin it will disable the outputs section of the part when asserted. This will not disable the input section of the IOs so they also cannot float when disabled.

### 12.2 Layout Example



# 13 Device and Documentation Support

## 13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 1. Related Links**

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| SN54LVC573A | Click here | Click here | Click here | Click here | Click here |
| SN74LVC573A | Click here | Click here | Click here | Click here | Click here |

## 13.2 Trademarks

All trademarks are the property of their respective owners.

## 13.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 13.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

# 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| 5962-9757501Q2A | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9757501Q2A SNJ54LVC573AFK |
| 5962-9757501QRA | Active | Production | CDIP (J) \| 20 | 20 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9757501QRA SNJ54LVC573AJ |
| 5962-9757501QSA | Active | Production | CFP (W) \| 20 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9757501QSA SNJ54LVC573AW |
| SN74LVC573ADBR | Active | Production | SSOP (DB) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC573A |
| SN74LVC573ADBR.B | Active | Production | SSOP (DB) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC573A |
| SN74LVC573ADGVR | Active | Production | TVSOP (DGV) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC573A |
| SN74LVC573ADGVR.B | Active | Production | TVSOP (DGV) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC573A |
| SN74LVC573ADW | Active | Production | SOIC (DW) \| 20 | 25 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC573A |
| SN74LVC573ADW.B | Active | Production | SOIC (DW) \| 20 | 25 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC573A |
| SN74LVC573ADWR | Active | Production | SOIC (DW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC573A |
| SN74LVC573ADWR.A | Active | Production | SOIC (DW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC573A |
| SN74LVC573ADWR.B | Active | Production | SOIC (DW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC573A |
| SN74LVC573ADWRG4 | Active | Production | SOIC (DW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC573A |
| SN74LVC573AN | Active | Production | PDIP (N) \| 20 | 20 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 125 | SN74LVC573AN |
| SN74LVC573AN.B | Active | Production | PDIP (N) \| 20 | 20 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 125 | SN74LVC573AN |
| SN74LVC573ANS.B | Active | Production | SOP (NS) \| 20 | 40 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVC573A |
| SN74LVC573ANSR | Active | Production | SOP (NS) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC573A |
| SN74LVC573ANSR.B | Active | Production | SOP (NS) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC573A |
| SN74LVC573ANSRE4 | Active | Production | SOP (NS) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC573A |
| SN74LVC573APW | Active | Production | TSSOP (PW) \| 20 | 70 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC573A |
| SN74LVC573APW.B | Active | Production | TSSOP (PW) \| 20 | 70 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC573A |
| SN74LVC573APWG4 | Active | Production | TSSOP (PW) \| 20 | 70 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC573A |
| SN74LVC573APWR | Active | Production | TSSOP (PW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | LC573A |
| SN74LVC573APWR.A | Active | Production | TSSOP (PW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC573A |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| SN74LVC573APWR.B | Active | Production | TSSOP (PW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC573A |
| SN74LVC573APWRE4 | Active | Production | TSSOP (PW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC573A |
| SN74LVC573APWRG4 | Active | Production | TSSOP (PW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC573A |
| SN74LVC573APWRG4.B | Active | Production | TSSOP (PW) \| 20 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC573A |
| SN74LVC573APWT | Active | Production | TSSOP (PW) \| 20 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC573A |
| SN74LVC573APWT.B | Active | Production | TSSOP (PW) \| 20 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC573A |
| SN74LVC573ARGYR | Active | Production | VQFN (RGY) \| 20 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | LC573A |
| SN74LVC573ARGYR.A | Active | Production | VQFN (RGY) \| 20 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | LC573A |
| SN74LVC573ARGYR.B | Active | Production | VQFN (RGY) \| 20 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | LC573A |
| SN74LVC573ARGYRG4 | Active | Production | VQFN (RGY) \| 20 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | LC573A |
| SN74LVC573ARGYRG4.A | Active | Production | VQFN (RGY) \| 20 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | LC573A |
| SN74LVC573ARGYRG4.B | Active | Production | VQFN (RGY) \| 20 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | LC573A |
| SNJ54LVC573AFK | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9757501Q2A SNJ54LVC 573AFK |
| SNJ54LVC573AJ | Active | Production | CDIP (J) \| 20 | 20 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9757501QR A SNJ54LVC573AJ |
| SNJ54LVC573AW | Active | Production | CFP (W) \| 20 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9757501QS A SNJ54LVC573AW |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**(5) MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54LVC573A, SN74LVC573A :**

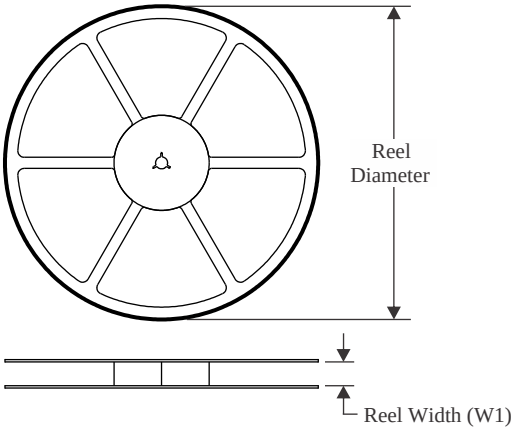
- Catalog : SN74LVC573A
- Automotive : SN74LVC573A-Q1, SN74LVC573A-Q1
- Enhanced Product : SN74LVC573A-EP, SN74LVC573A-EP
- Military : SN54LVC573A

NOTE: Qualified Version Definitions:

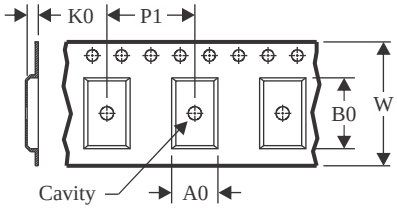
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

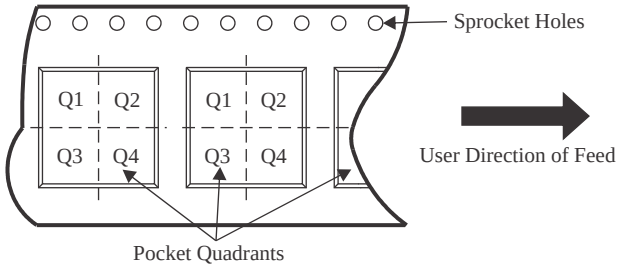



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

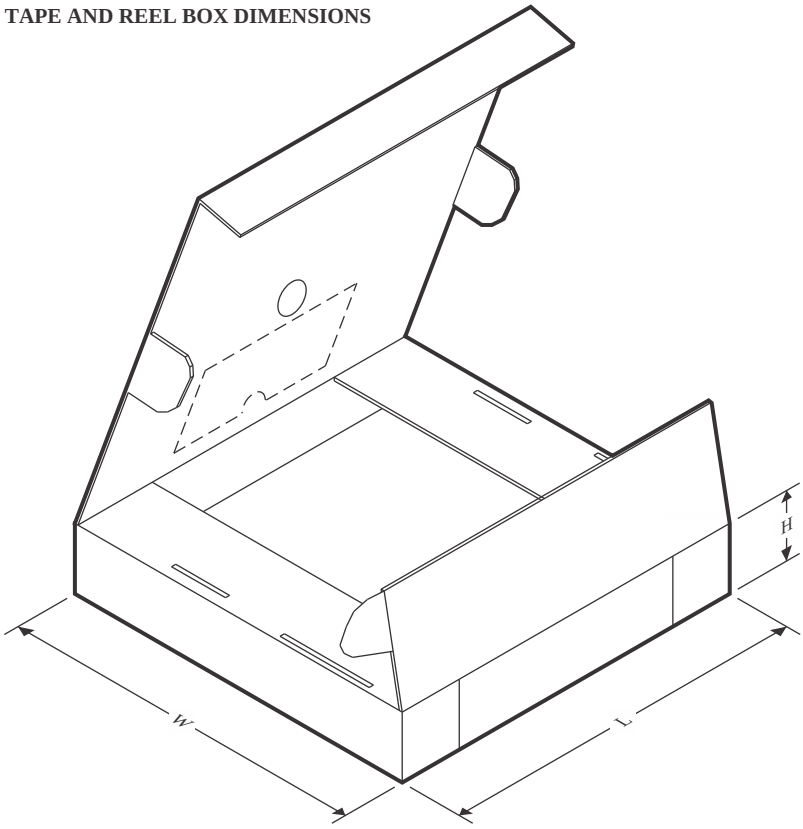
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LVC573ADBR | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LVC573ADGVR | TVSOP | DGV | 20 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LVC573ADWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.9 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74LVC573ANSR | SOP | NS | 20 | 2000 | 330.0 | 24.4 | 8.4 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |
| SN74LVC573APWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |
| SN74LVC573APWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| SN74LVC573APWRG4 | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |
| SN74LVC573APWT | TSSOP | PW | 20 | 250 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |
| SN74LVC573ARGYR | VQFN | RGY | 20 | 3000 | 330.0 | 12.4 | 3.71 | 4.71 | 1.1 | 8.0 | 12.0 | Q1 |
| SN74LVC573ARGYRG4 | VQFN | RGY | 20 | 3000 | 330.0 | 12.4 | 3.71 | 4.71 | 1.1 | 8.0 | 12.0 | Q1 |

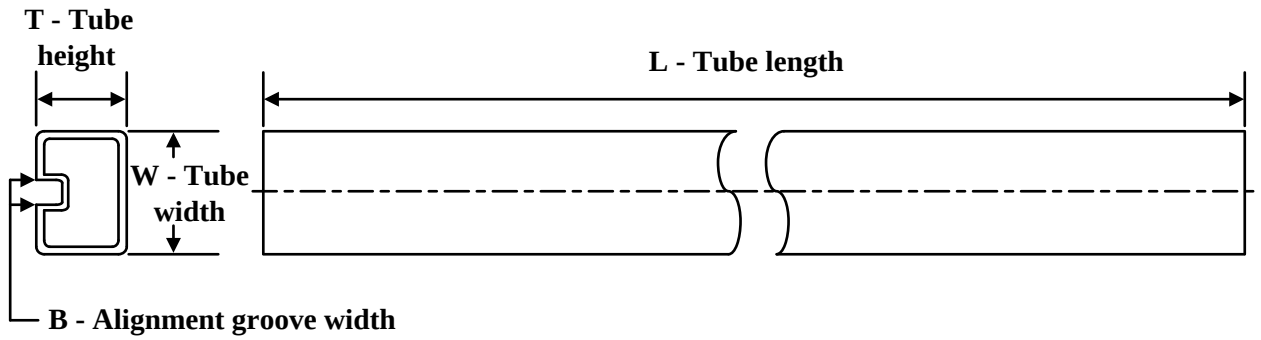
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74LVC573ADBR | SSOP | DB | 20 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74LVC573ADGVR | TVSOP | DGV | 20 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74LVC573ADWR | SOIC | DW | 20 | 2000 | 356.0 | 356.0 | 45.0 |
| SN74LVC573ANSR | SOP | NS | 20 | 2000 | 356.0 | 356.0 | 45.0 |
| SN74LVC573APWR | TSSOP | PW | 20 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74LVC573APWR | TSSOP | PW | 20 | 2000 | 364.0 | 364.0 | 27.0 |
| SN74LVC573APWRG4 | TSSOP | PW | 20 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74LVC573APWT | TSSOP | PW | 20 | 250 | 353.0 | 353.0 | 32.0 |
| SN74LVC573ARGYR | VQFN | RGY | 20 | 3000 | 353.0 | 353.0 | 32.0 |
| SN74LVC573ARGYRG4 | VQFN | RGY | 20 | 3000 | 353.0 | 353.0 | 32.0 |

## TUBE




*All dimensions are nominal

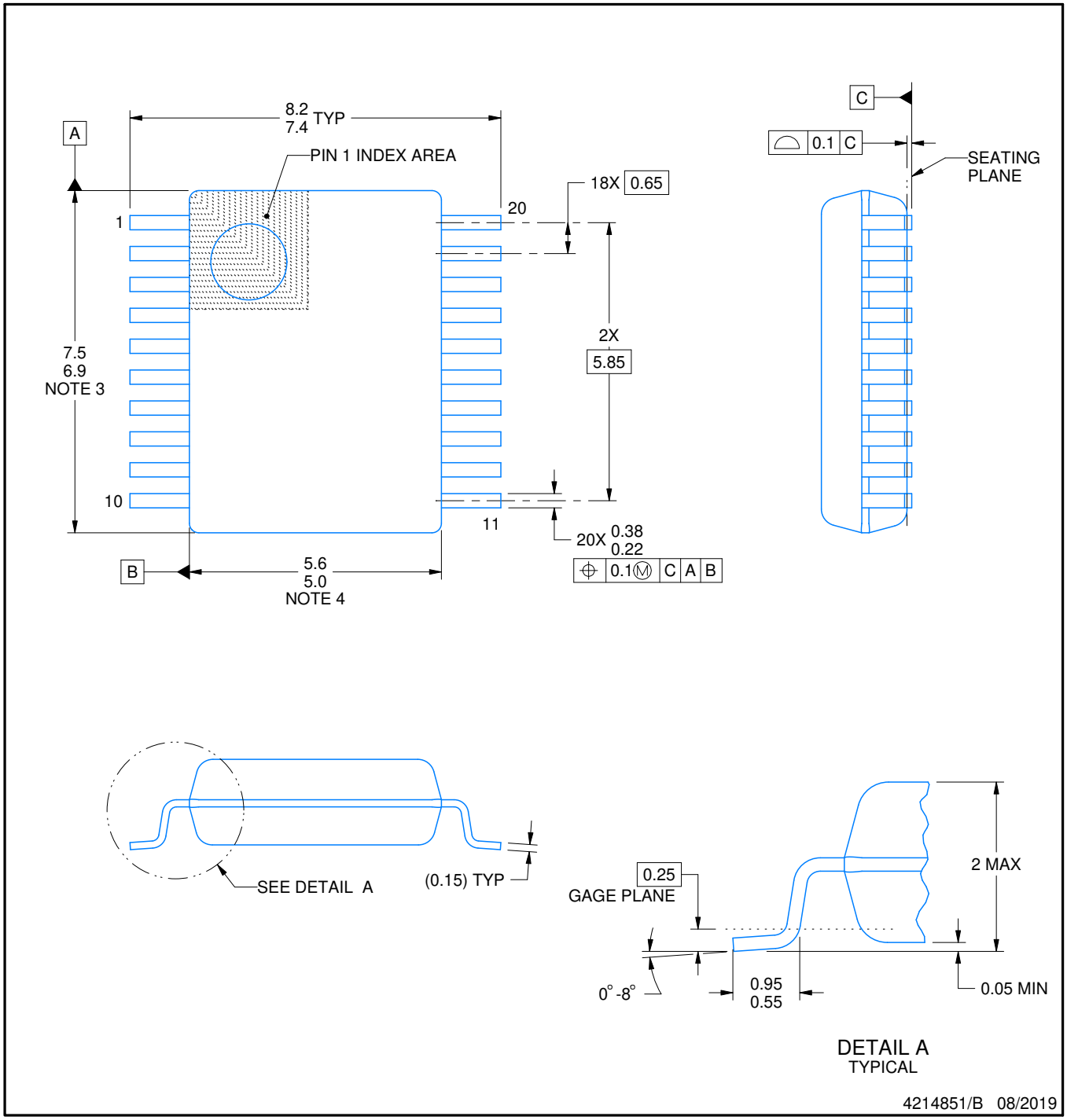
| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| 5962-9757501Q2A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| 5962-9757501QSA | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |
| SN74LVC573ADW | DW | SOIC | 20 | 25 | 507 | 12.83 | 5080 | 6.6 |
| SN74LVC573ADW.B | DW | SOIC | 20 | 25 | 507 | 12.83 | 5080 | 6.6 |
| SN74LVC573AN | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| SN74LVC573AN.B | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| SN74LVC573ANS.B | NS | SOP | 20 | 40 | 530 | 10.5 | 4000 | 4.1 |
| SN74LVC573APW | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| SN74LVC573APW.B | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| SN74LVC573APWG4 | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| SNJ54LVC573AFK | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SNJ54LVC573AW | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |

# PACKAGE OUTLINE

## DB0020A

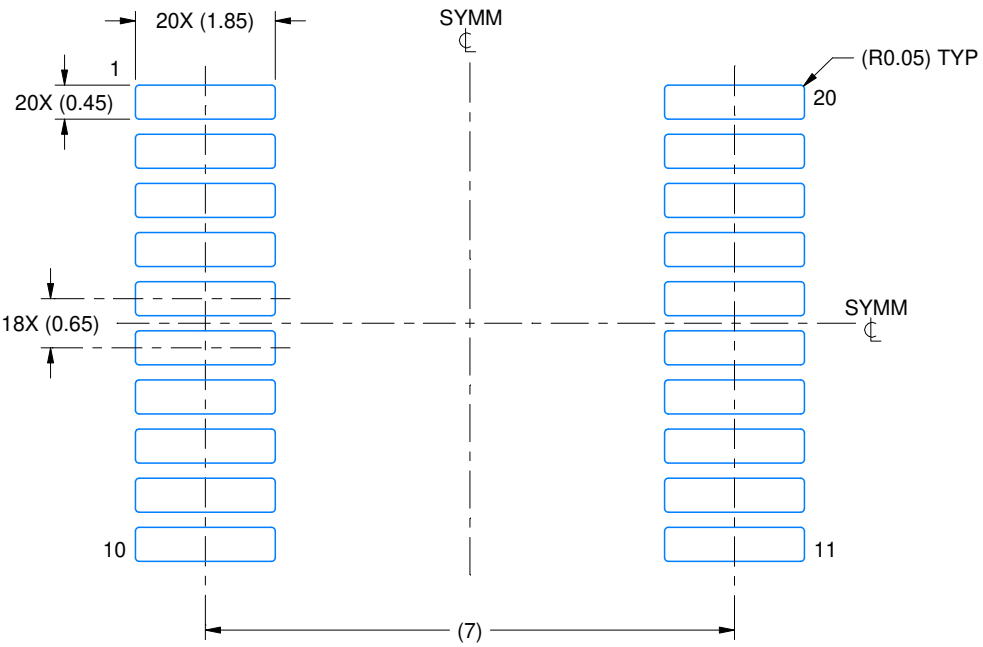
## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

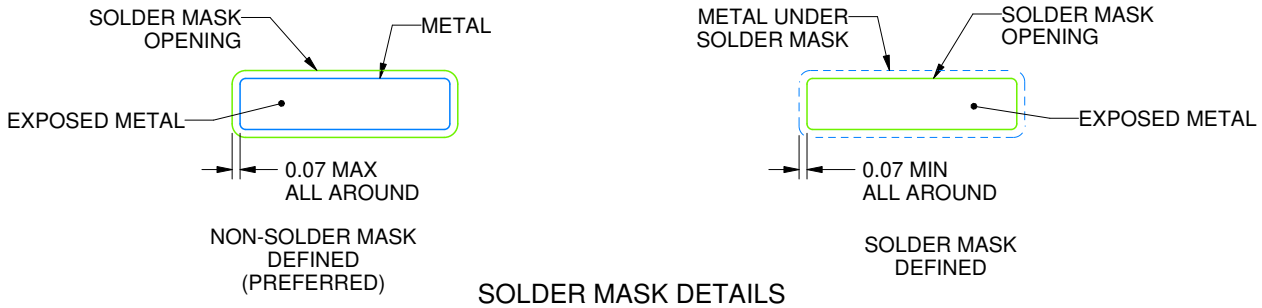



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

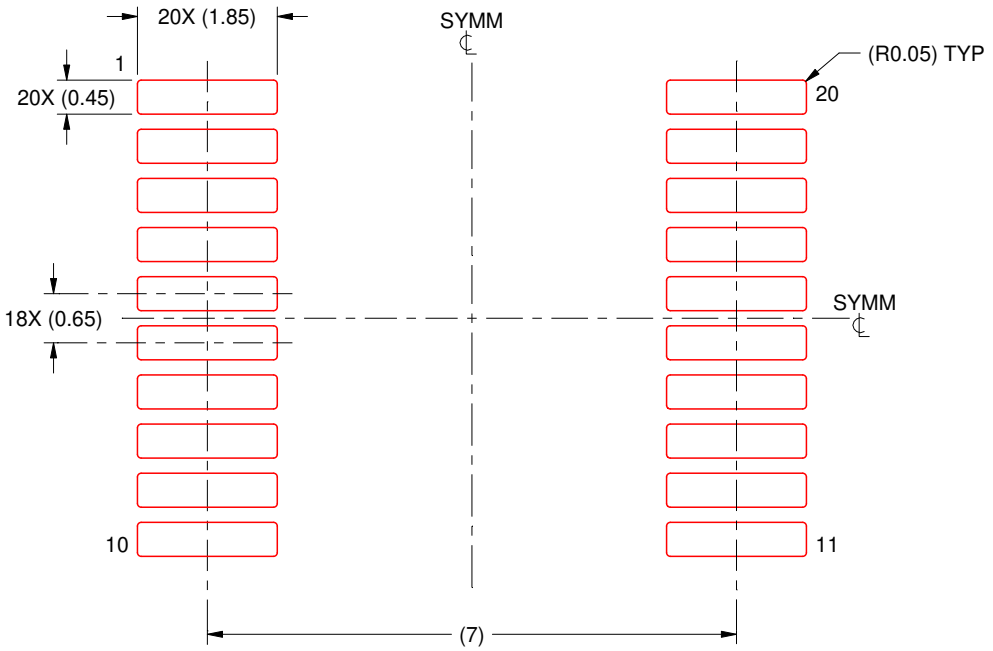



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

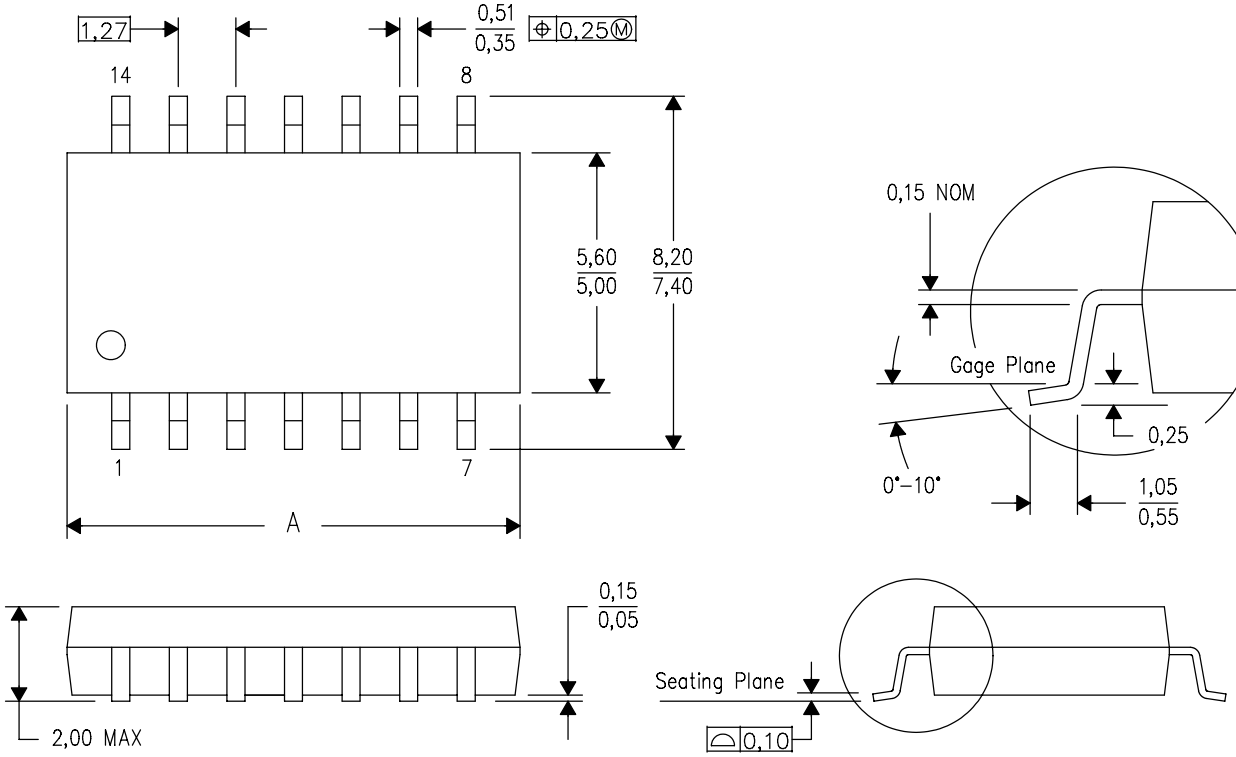
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

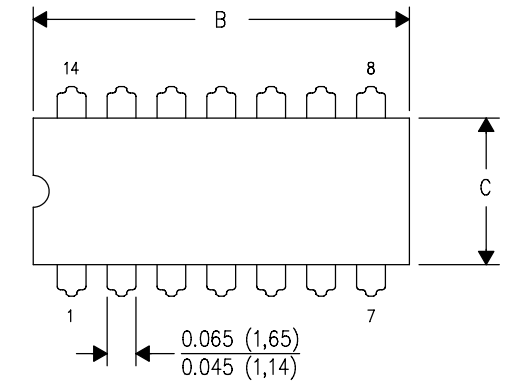
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

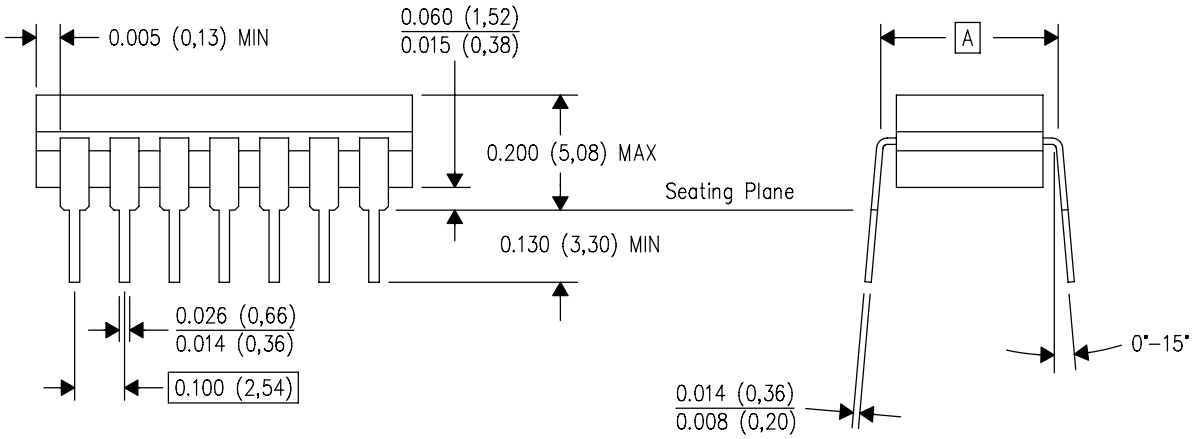
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |

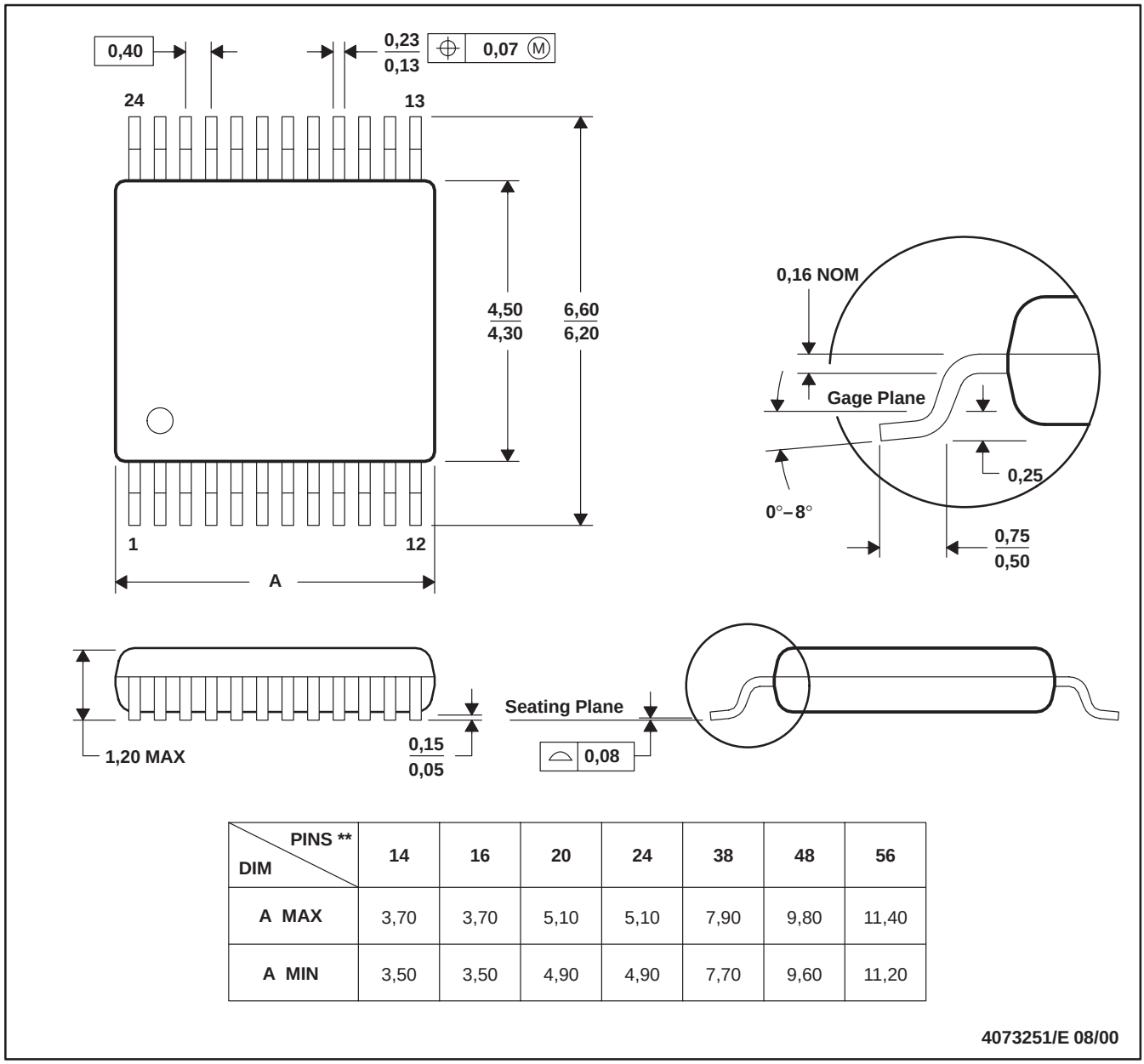



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

**DGV (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

**24 PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 | 38 | 48 | 56 |
|---|---|---|---|---|---|---|---|
| A MAX | 3,70 | 3,70 | 5,10 | 5,10 | 7,90 | 9,80 | 11,40 |
| A MIN | 3,50 | 3,50 | 4,90 | 4,90 | 7,70 | 9,60 | 11,20 |

**4073251/E 08/00**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

# GENERIC PACKAGE VIEW

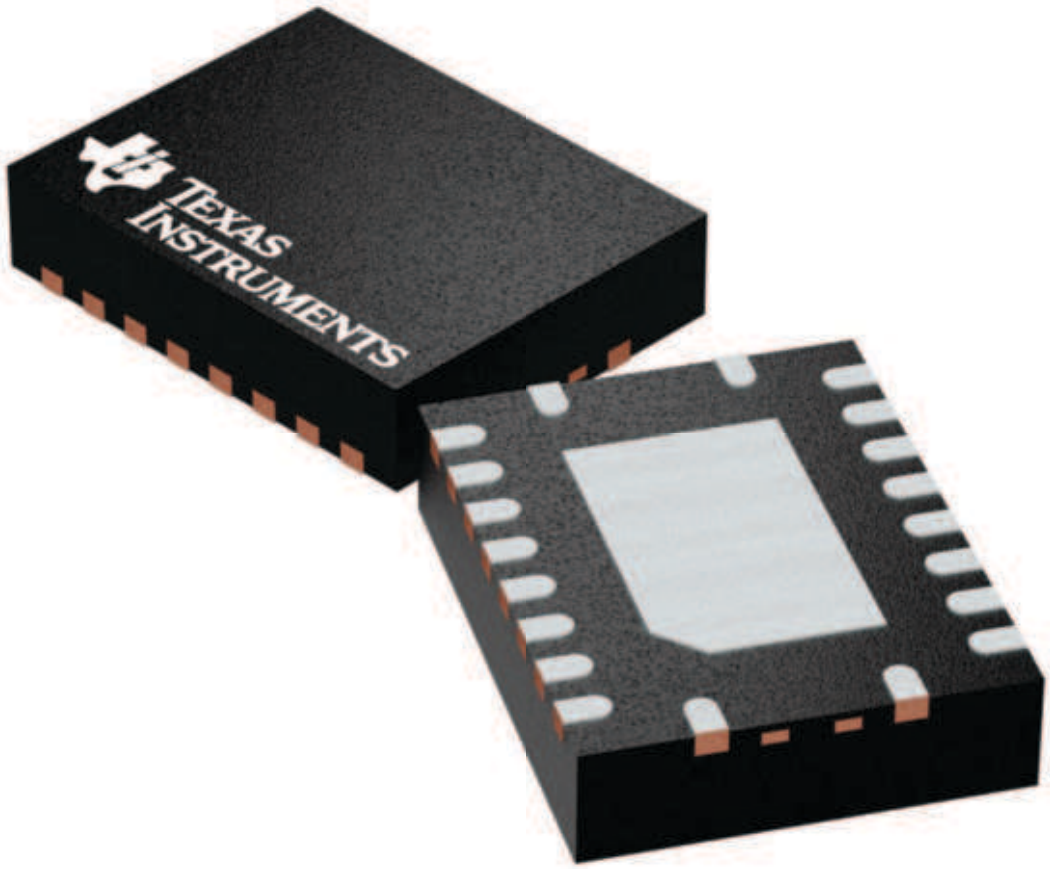
## RGY 20

## VQFN - 1 mm max height

**3.5 x 4.5, 0.5 mm pitch**

PLASTIC QUAD FGLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.




4225264/A

# GENERIC PACKAGE VIEW

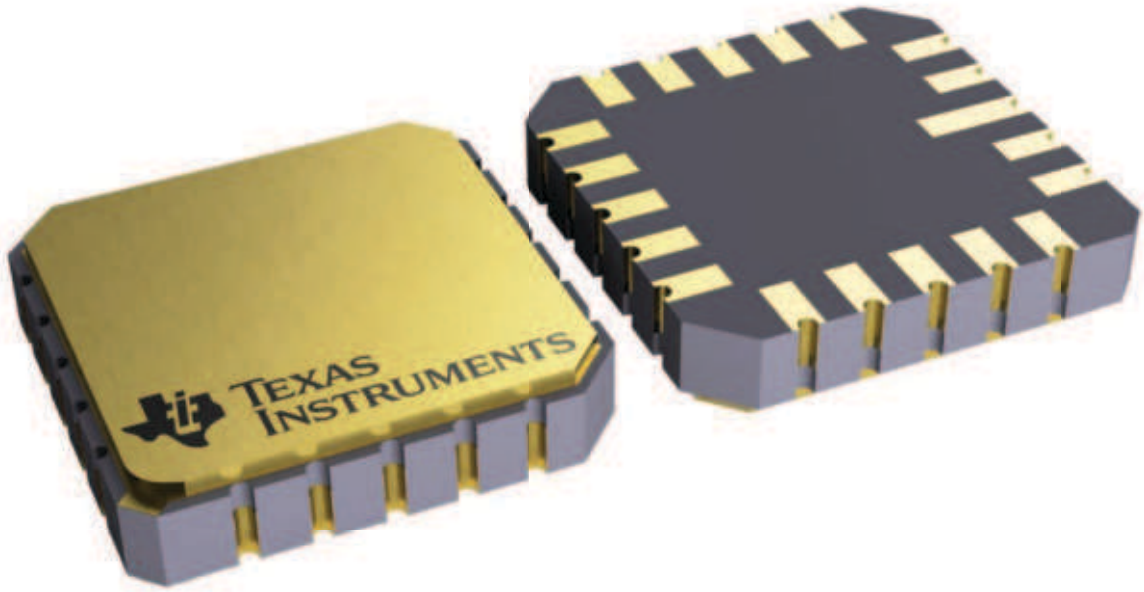
## FK 20

## LCCC - 2.03 mm max height

**8.89 x 8.89, 1.27 mm pitch**

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

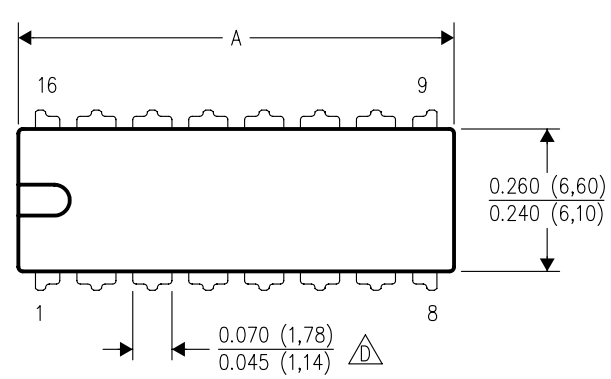



4229370\VA\

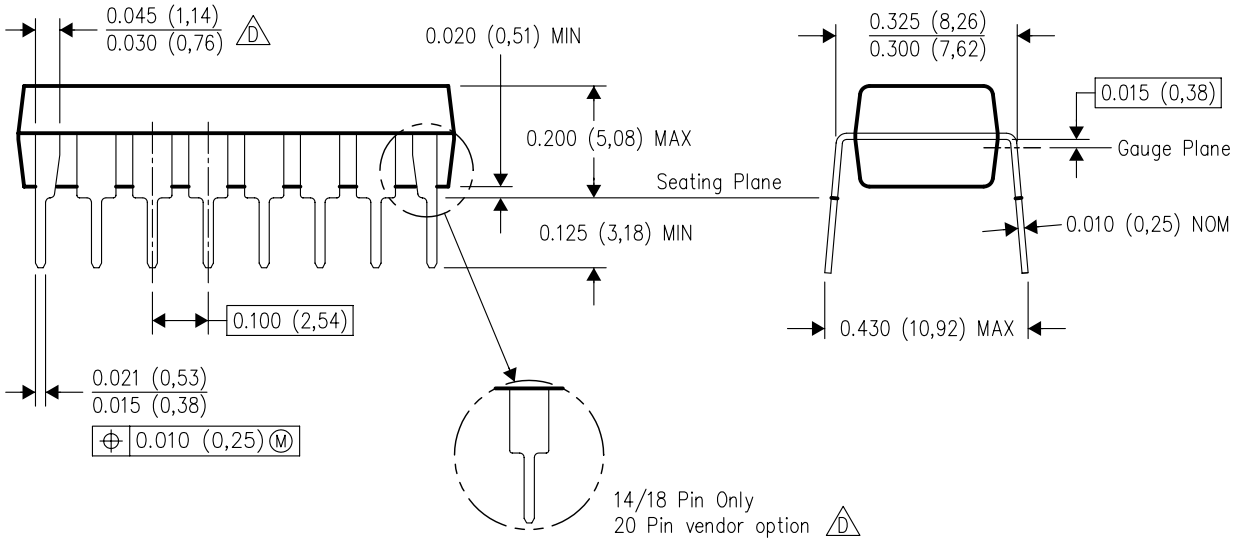
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

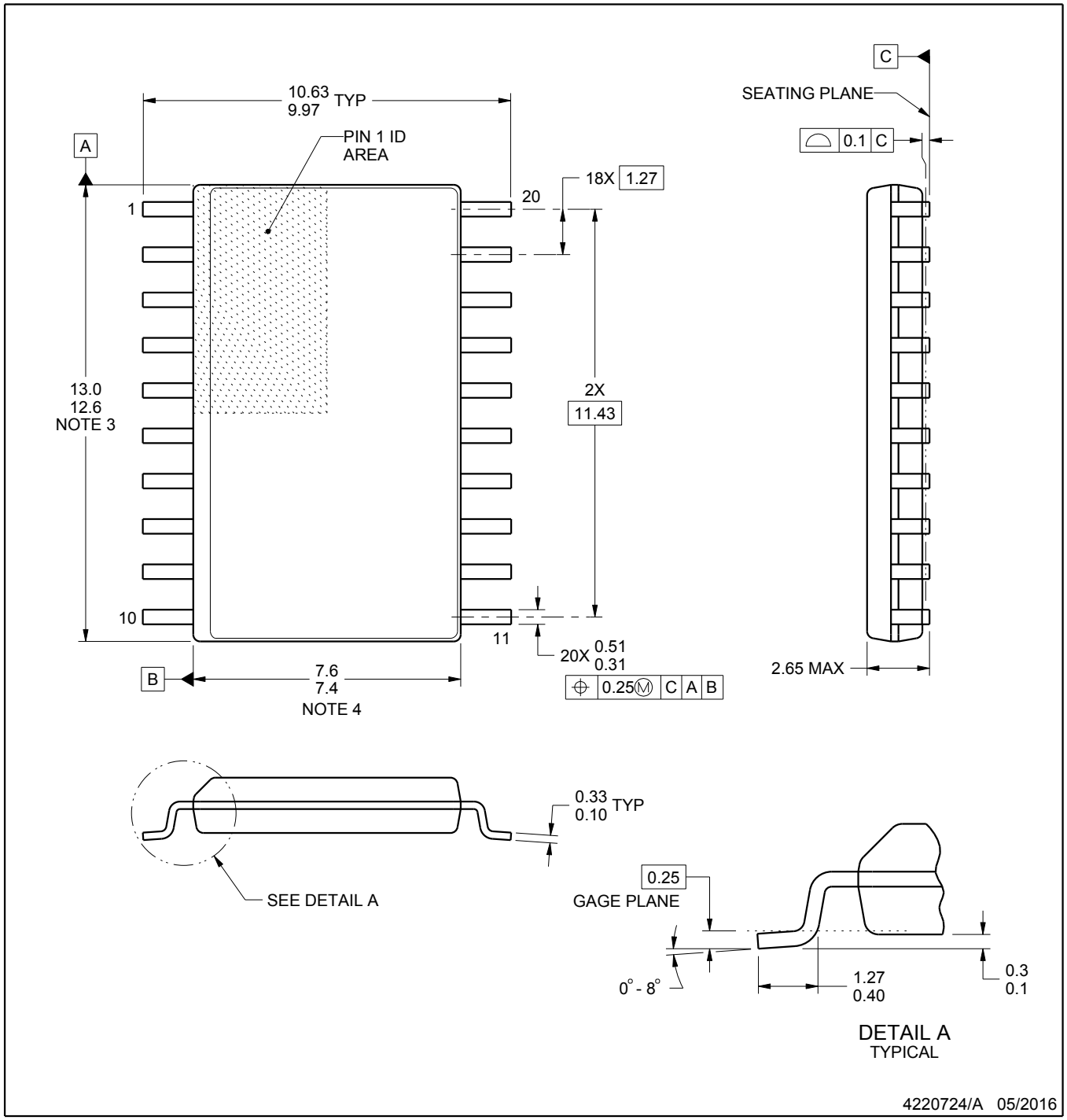


# PACKAGE OUTLINE

## DW0020A

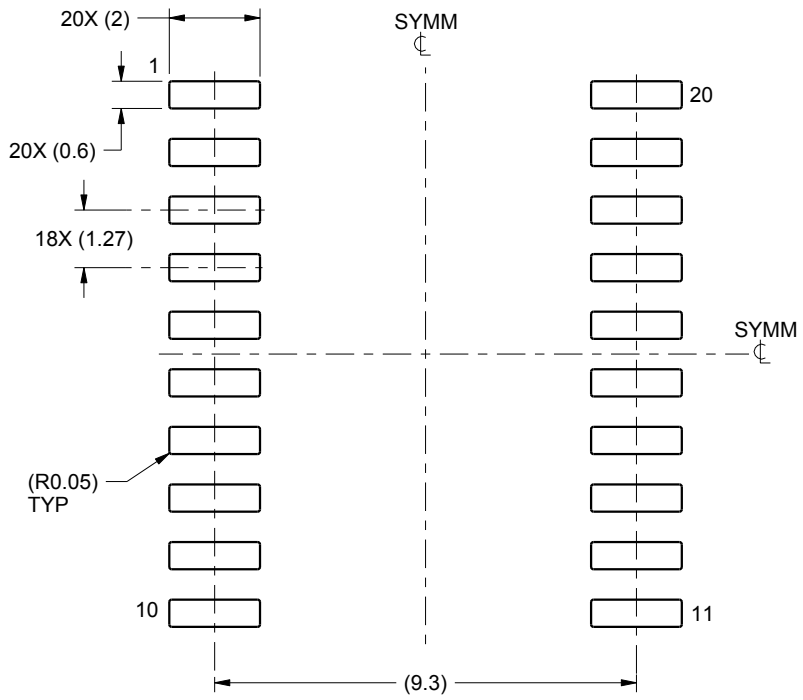
## SOIC - 2.65 mm max height

SOIC

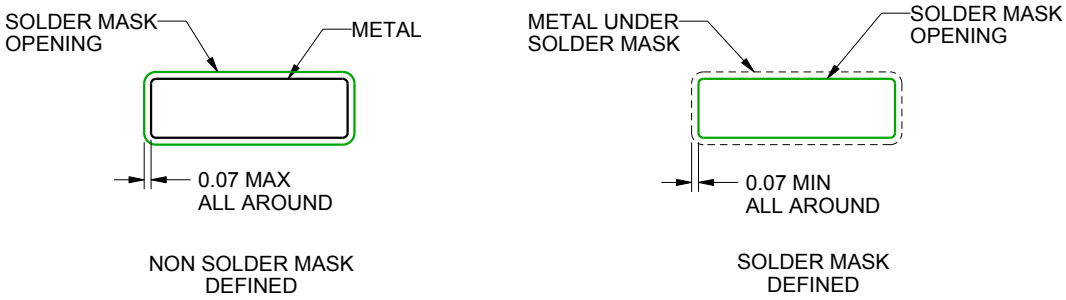



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.




LAND PATTERN EXAMPLE
SCALE:6X

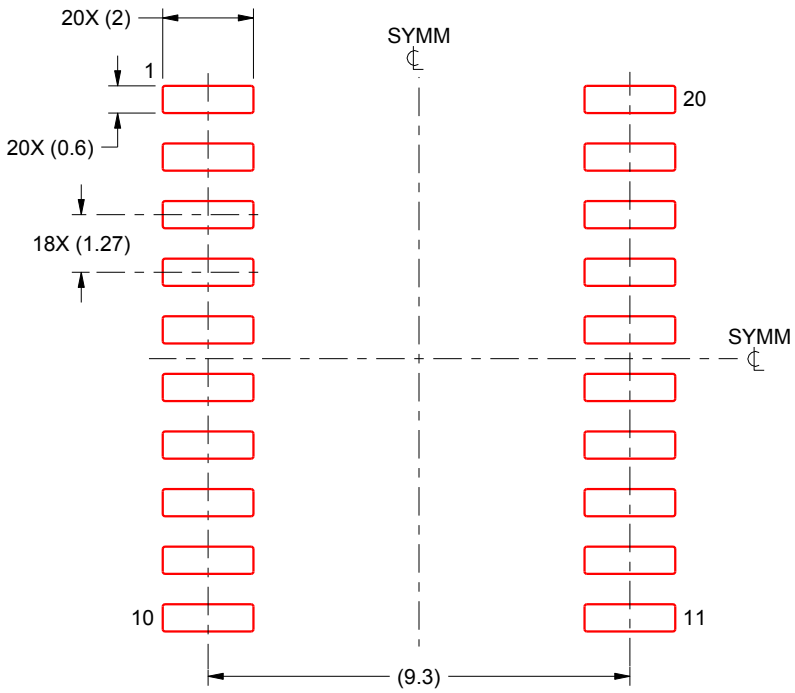



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



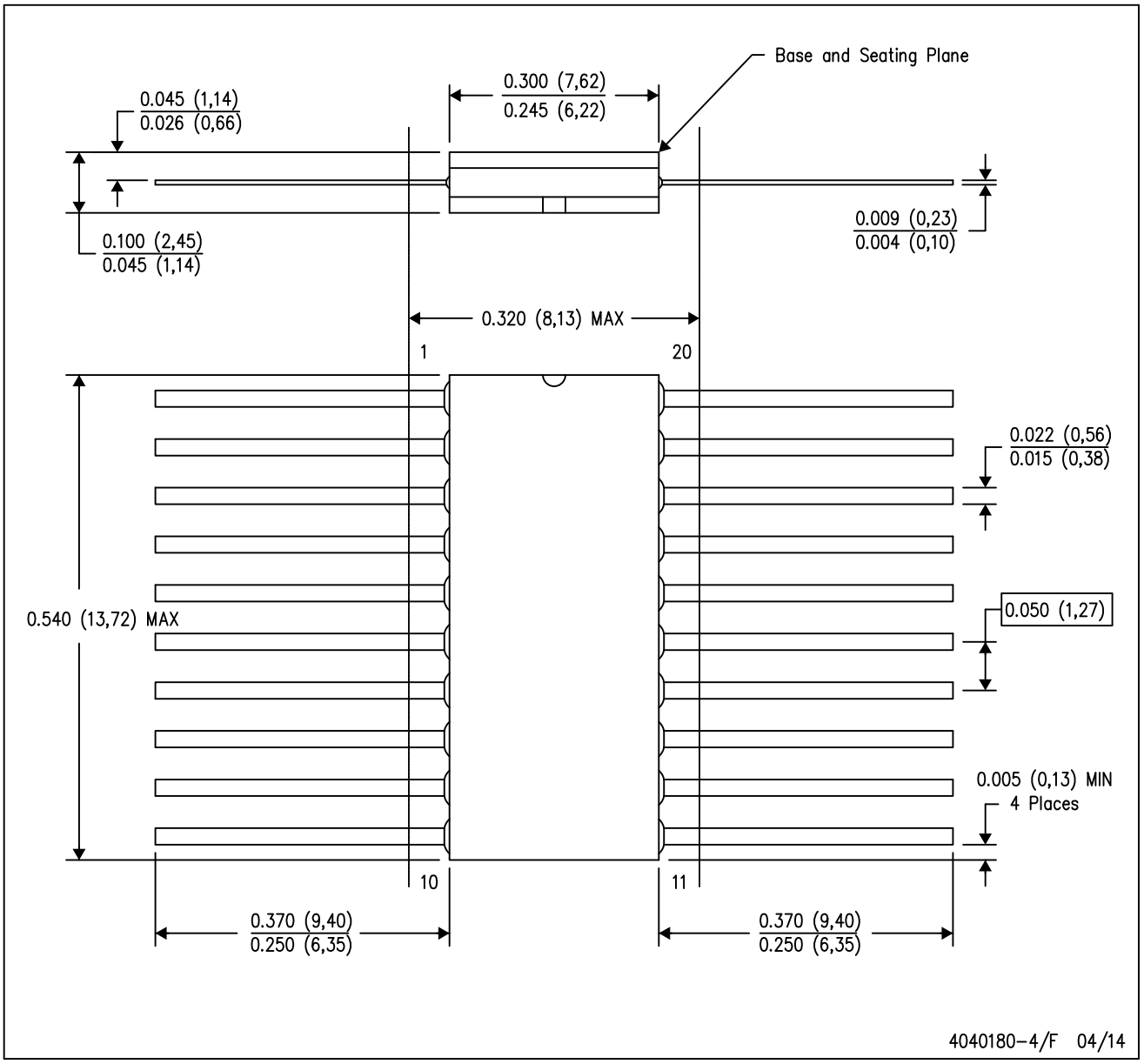

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

W (R–GDFP–F20) CERAMIC DUAL FLATPACK



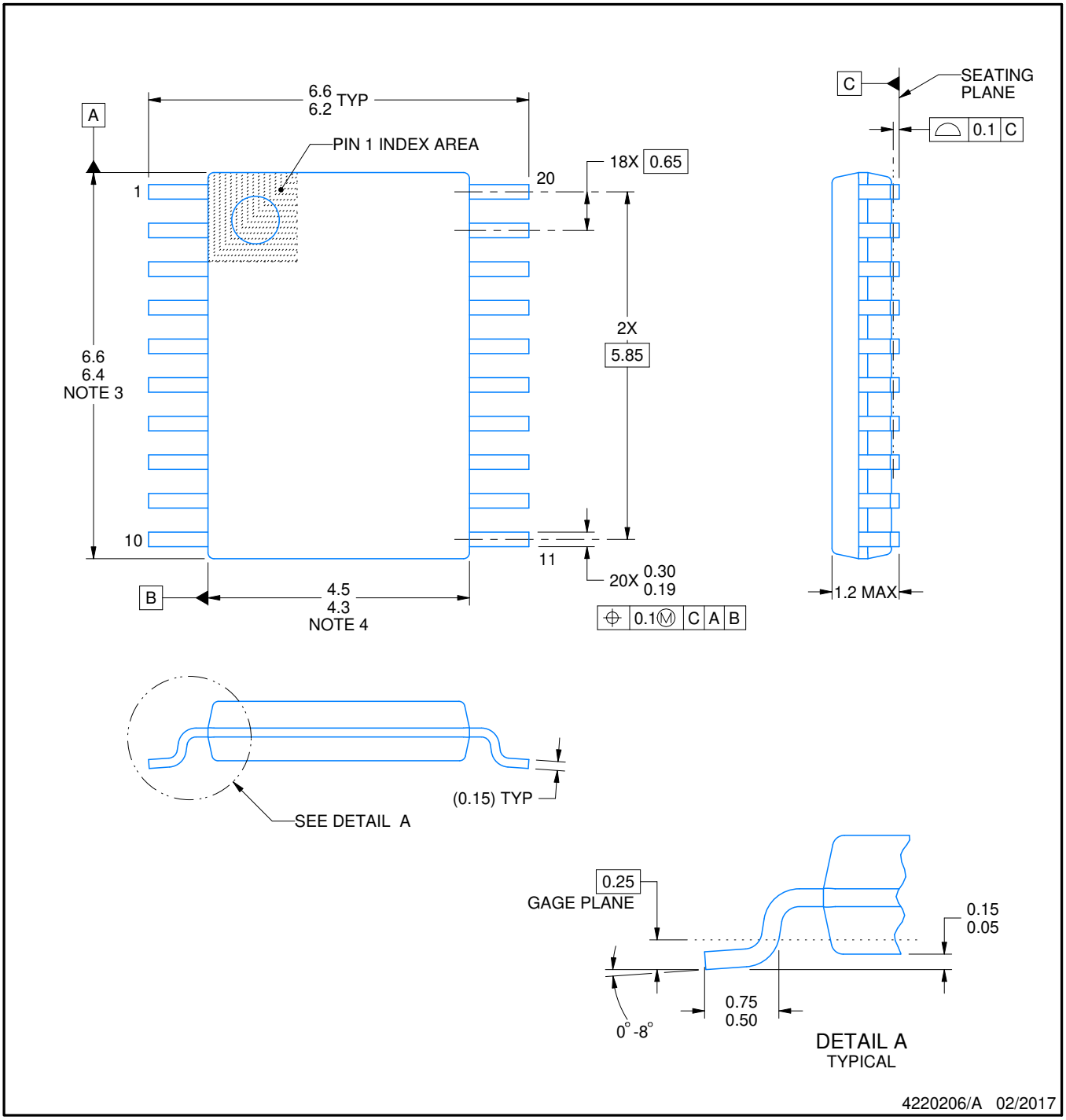

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within Mil–Std 1835 GDFP2–F20

# PACKAGE OUTLINE

## PW0020A

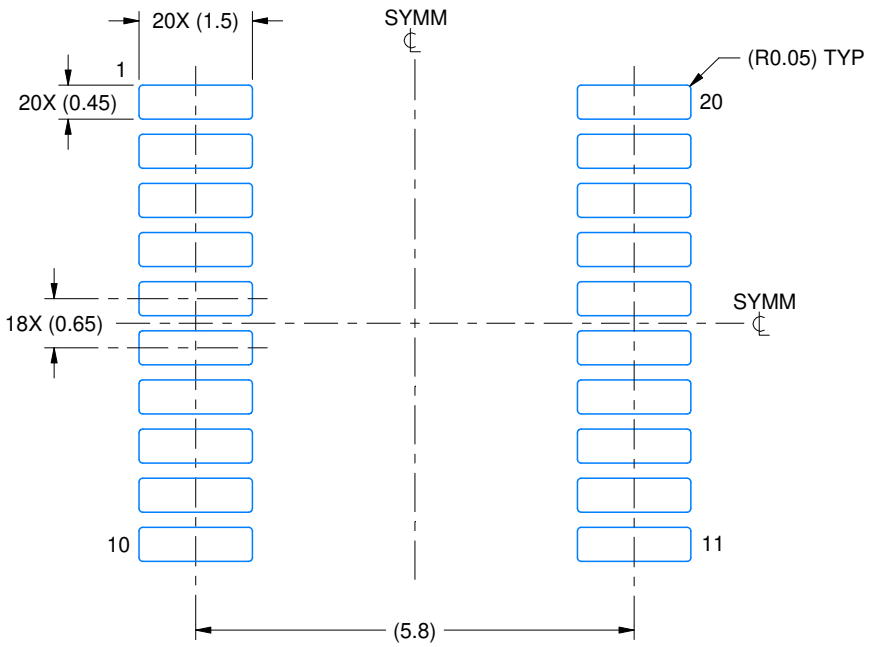
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE




NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

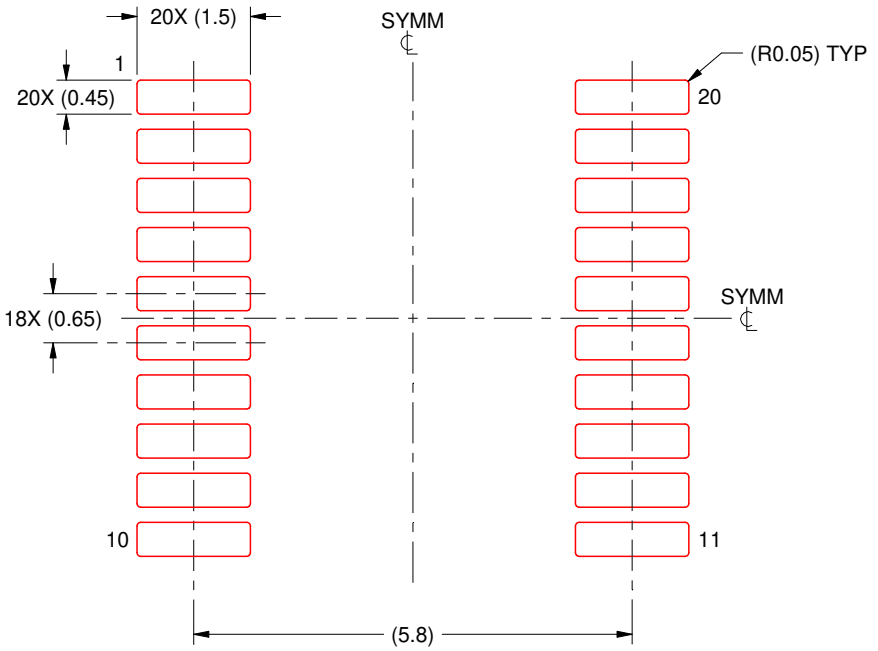



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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