SN74CB3Q3253 Dual 1-of-4 FET Multiplexer – Demultiplexer 2.5V – 3.3V Low-Voltage High-Bandwidth Bus Switch

1 Features

- High-bandwidth data path (up to 500MHz)
- 5V tolerant I/Os with device powered up or powered down
- Low and flat ON-state resistance (r_{on}) characteristics over operating range (r_{on} = 4Ω typical)
- Rail-to-rail switching on data I/O ports
  - 0 to 5V switching with 3.3V V_{CC}
  - 0 to 3.3V switching with 2.5V V_{CC}
- Bidirectional data flow with near-zero propagation delay
- Low input and output capacitance minimizes loading and signal distortion ($C_{io(OFF)}$ = 3.5pF typical)
- Fast switching frequency ($f_{\overline{OE}}$ = 20MHz maximum)
- Data and control inputs provide undershoot clamp diodes
- Low power consumption (I_{CC} = 0.6mA typical)
- V_{CC} operating range from 2.3V to 3.6V
- Data I/Os support 0V to 5V signal levels (0.8V, 1.2V, 1.5V, 1.8V, 2.5V, 3.3V, 5V)
- Control inputs can be driven by TTL or 5V and 3.3V CMOS outputs
- I_{off} supports partial-power-down mode operation
- Latch-up performance exceeds 100mA per JESD 78, class II
- ESD performance tested per JESD 22
  - 2000V Human-Body Model (A114B, Class II)
  - 1000V Charged-Device Model (C101)
- Supports both digital and analog applications: USB interface, differential signal interface bus isolation, low-distortion signal gating (for additional information regarding the performance characteristics of the CB3Q family, refer to the *CBT-C, CB3T, and CB3Q signal-switch families* application note).

2 Applications

- Video broadcasting: IP-based multi-format transcoder
- Video communications system

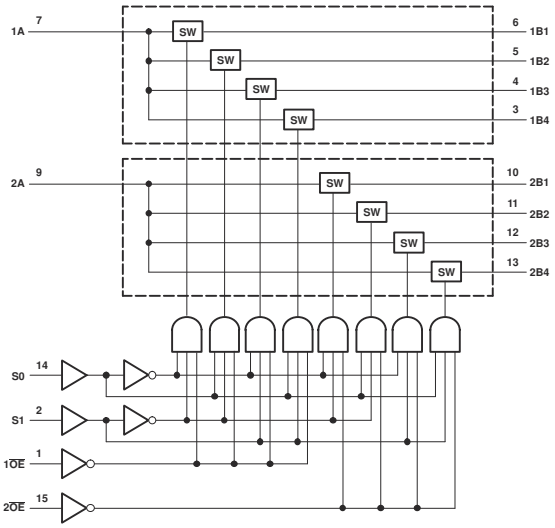
3 Description

The SN74CB3Q3253 device is a high-bandwidth FET bus switch using a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance (r_{on}). The low and flat ON-state resistance allows for minimal propagation delay and supports rail-to-rail switching on the data input and output (I/O) ports.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
SN74CB3Q3253	DBQ (SSOP, 16)	8.65mm × 6mm
	DGV (TVSOP, 16)	5mm × 6.4mm
	RGY (VQFN, 16)	4.5mm × 3.5mm
	PW (TSSOP, 16)	6.5mm × 6.4mm
	DYY (SOT-23-THN, 16)	4.2mm × 2mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Logic Diagram (Positive Logic)

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

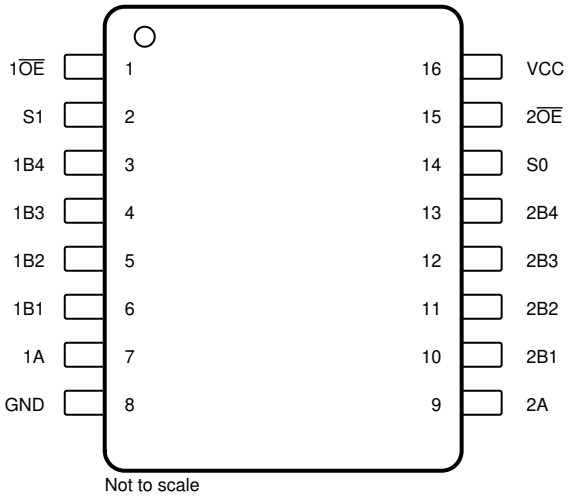


Figure 4-1. DBQ, DGV, DYY or PW Package, 16-Pin SSOP, TVSOP, SOT-23 THN or TSSOP (Top View)

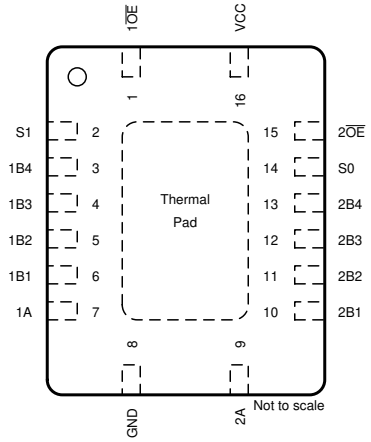


Figure 4-2. RGY Package, 16-Pin VQFN (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
1 $\overline{OE}$	1	I	Output Enable 1 Active-Low
S1	2	I	Select Pin 1
1B4	3	I/O	Channel 1I/O 4
1B3	4	I/O	Channel 1I/O 3
1B2	5	I/O	Channel 1I/O 2
1B1	6	I/O	Channel 1I/O 1
1A	7	I/O	Channel 1 common
GND	8	—	Ground
2A	9	I/O	Channel 2 common
2B1	10	I/O	Channel 2I/O 1
2B2	11	I/O	Channel 2I/O 2
2B3	12	I/O	Channel 2I/O 3
2B4	13	I/O	Channel 2I/O 4
S0	14	I	Select Pin 0
2 $\overline{OE}$	15	I	Output Enable 2 Active-Low
V_{CC}	16	—	Power

(1) I = input, O = output

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	4.6	V
V_{IN}	Control input voltage(2) (3)		–0.5	7	V
$V_{I/O}$	Switch I/O voltage(2) (3) (4)		–0.5	7	V
I_{IK}	Control input clamp current	V_{IN} < 0		–50	mA
$I_{I/OK}$	I/O port clamp current	$V_{I/O}$ < 0		–50	mA
$I_{I/O}$	ON-state switch current(5)			±64	mA
	Continuous current through V_{CC} or GND			±100	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings can be exceeded if the input and output clamp-current ratings are observed.
(4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
(5) I_I and I_O are used to denote specific conditions for $I_{I/O}$.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	+2000	V
		Charged-device model (CDM), per JEDEC specification JESD22C101(2)	+1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3V to 2.7V	1.7	5.5	V
		V_{CC} = 2.7V to 3.6V	2	5.5	
V_{IL}	Low-level control input voltage	V_{CC} = 2.3V to 2.7V	0	0.7	V
		V_{CC} = 2.7V to 3.6V	0	0.8	
$V_{I/O}$	Data input/output voltage		0	5.5	V
T_A	Operating free-air temperature	RGY, DBQ, DGV, PW packages	–40	85	°C
T_A	Operating free-air temperature	DYY package			

(1) All unused control inputs of the device must be held at V_{CC} or GND to maintain proper device operation. See also the *Implications of Slow or Floating CMOS Inputs* application note.

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5.4 Thermal Information

THERMAL METRIC[1]		SN74CB3Q3253					UNIT
		DBQ (SSOP)	DGV (TVSOP)	PW (TSSOP)	RGY (VQFN)	DYY (SOT-23-THN)	
		16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	106.4	134.2	114.3	72.3	126.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	65.1	66.1	57.9	71.9	14.9	
$R_{\theta JB}$	Junction-to-board thermal resistance	62.7	80.1	72.2	47.1	72.8	
ψ_{JT}	Junction-to-top characterization parameter	18.7	17.7	16.3	19.5	73.0	
ψ_{JB}	Junction-to-board characterization parameter	64.6	79.6	71.8	47.2	71.1	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	31.4	—	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics: RGY, PW, DBQ, DGV Packages

over recommended operating free-air temperature range (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS			MIN	TYP[2]	MAX	UNIT
V_{IK}		V_{CC} = 3.6V,	I_I = –18mA				–1.8	V
I_{IN}	Control inputs	V_{CC} = 3.6V,	V_{IN} = 0 to 5.5V				±1	µA
I_{OZ} [3]		V_{CC} = 3.6V,	V_O = 0 to 5.5V, V_I = 0,	Switch OFF, V_{IN} = V_{CC} or GND			±1	µA
I_{off}		V_{CC} = 0,	V_O = 0 to 5.5V,	V_I = 0			1	µA
I_{CC}		V_{CC} = 3.6V,	$I_{I/O}$ = 0, Switch ON or OFF,	V_{IN} = V_{CC} or GND		0.6	2	mA
ΔI_{CC} [4]	Control inputs	V_{CC} = 3.6V,	One input at 3V,	Other inputs at V_{CC} or GND			30	µA
I_{CCD} [5]	Per control input	V_{CC} = 3.6V,	A and B ports open,	$\overline{OE}$ input		0.15	0.16	mA/ MHz
		Control input switching at 50% duty cycle		S input		0.23	0.25	
C_{in}	Control inputs	V_{CC} = 3.3V,	V_{IN} = 5.5V, 3.3V, or 0			2.5	3.5	pF
$C_{io(OFF)}$	A port	V_{CC} = 3.3V,	Switch OFF, V_{IN} = V_{CC} or GND,	$V_{I/O}$ = 5.5V, 3.3V, or 0		8	11	pF
	B port	V_{CC} = 3.3V,	Switch OFF, V_{IN} = V_{CC} or GND,	$V_{I/O}$ = 5.5V, 3.3V, or 0		3.5	4.5	pF
$C_{io(ON)}$		V_{CC} = 3.3V,	Switch ON, V_{IN} = V_{CC} or GND,	$V_{I/O}$ = 5.5V, 3.3V, or 0		13	17	pF
r_{on} [6]		V_{CC} = 2.3V, TYP at V_{CC} = 2.5V	V_I = 0,	I_O = 30mA		4	10	Ω
			V_I = 1.7V,	I_O = –15mA		4.5	11	
		V_{CC} = 3V	V_I = 0,	I_O = 30mA		3.5	8	
			V_I = 2.4V,	I_O = –15mA		4	10	

(1) V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.
(2) All typical values are at V_{CC} = 3.3V (unless otherwise noted), T_A = 25°C.
(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.
(4) This parameter is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.
(5) This parameter specifies the dynamic power-supply current associated with the operating frequency of a single control input (see Figure 5-2).
(6) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

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5.6 Electrical Characteristics: DYY Package

over recommended operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS			MIN	TYP(2)	MAX	UNIT
V_{IK}		V_{CC} = 3.6V,	I_I = –18mA				–1.8	V
I_{IN}	Control inputs	V_{CC} = 3.6V,	V_{IN} = 0 to 5.5V				±1	µA
I_{OZ} (3)		V_{CC} = 3.6V,	V_O = 0 to 5.5V, V_I = 0,	Switch OFF, V_{IN} = V_{CC} or GND			±1	µA
I_{off}		V_{CC} = 0,	V_O = 0 to 5.5V,	V_I = 0			1	µA
I_{CC}		V_{CC} = 3.6V,	$I_{I/O}$ = 0, Switch ON or OFF,	V_{IN} = V_{CC} or GND		0.6	2	mA
ΔI_{CC} (4)	Control inputs	V_{CC} = 3.6V,	One input at 3V,	Other inputs at V_{CC} or GND			30	µA
I_{CCD} (5)	Per control input	V_{CC} = 3.6V,	A and B ports open,	$\overline{OE}$ input		0.15	0.16	mA/ MHz
		Control input switching at 50% duty cycle		S input		0.23	0.25	
C_{in}	Control inputs	V_{CC} = 3.3V,	V_{IN} = 5.5V, 3.3V, or 0			2.5	3.5	pF
$C_{io(OFF)}$	A port	V_{CC} = 3.3V,	Switch OFF, V_{IN} = V_{CC} or GND,	$V_{I/O}$ = 5.5V, 3.3V, or 0		8	11	pF
	B port	V_{CC} = 3.3V,	Switch OFF, V_{IN} = V_{CC} or GND,	$V_{I/O}$ = 5.5V, 3.3V, or 0		3.5	4.5	pF
$C_{io(ON)}$		V_{CC} = 3.3V,	Switch ON, V_{IN} = V_{CC} or GND,	$V_{I/O}$ = 5.5V, 3.3V, or 0		13	17	pF
r_{on} (6)		V_{CC} = 2.3V, TYP at V_{CC} = 2.5V	V_I = 0,	I_O = 30mA		4	10	Ω
			V_I = 1.7V,	I_O = –15mA		5.5	11	
		V_{CC} = 3V	V_I = 0,	I_O = 30mA		3.5	8	
			V_I = 2.4V,	I_O = –15mA		4	10	

(1) V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.
(2) All typical values are at V_{CC} = 3.3V (unless otherwise noted), T_A = 25°C.
(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.
(4) This parameter is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.
(5) This parameter specifies the dynamic power-supply current associated with the operating frequency of a single control input (see Figure 5-2).
(6) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

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5.7 Switching Characteristics: RGY, PW, DBQ, DGV Packages

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5V ± 0.2V		V_{CC} = 3.3V ± 0.3V		UNIT
			MIN	MAX	MIN	MAX	
$f_{\overline{OE}}$ or f_S (1)	$\overline{OE}$ or S	A or B		10		20	MHz
t_{pd} (2)	A or B	B or A		0.12		0.18	ns
$t_{pd(s)}$	S	A	1.5	6.7	1.5	5.9	ns
t_{en}	S	B	1.5	6.7	1.5	5.9	ns
	$\overline{OE}$	A or B	1.5	6.7	1.5	5.9	
t_{dis}	S	B	1	6.1	1	6.1	ns
	$\overline{OE}$	A or B	1	6.1	1	6.1	

(1) Maximum switching frequency for control input ($V_O > V_{CC}$, V_I = 5V, $R_L \geq 1M\Omega$, C_L = 0).
(2) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by a desired voltage source (zero output impedance).

5.8 Switching Characteristics: DYY Package

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5V ± 0.2V		V_{CC} = 3.3V ± 0.3V		UNIT
			MIN	MAX	MIN	MAX	
$f_{\overline{OE}}$ or f_S (1)	$\overline{OE}$ or S	A or B		10		20	MHz
t_{pd} (2)	A or B	B or A		0.12		0.18	ns
$t_{pd(s)}$	S	A	1.5	18	1.5	10	ns
t_{en}	S	B	1.5	12	1.5	8	ns
	$\overline{OE}$	A or B	1.5	10	1.5	7	
t_{dis}	S	B	1	12	1	11	ns
	$\overline{OE}$	A or B	1	10	1	10	

(1) Maximum switching frequency for control input ($V_O > V_{CC}$, V_I = 5V, $R_L \geq 1M\Omega$, C_L = 0).
(2) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by a desiredvoltage source (zero output impedance).

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5.9 Typical Characteristics

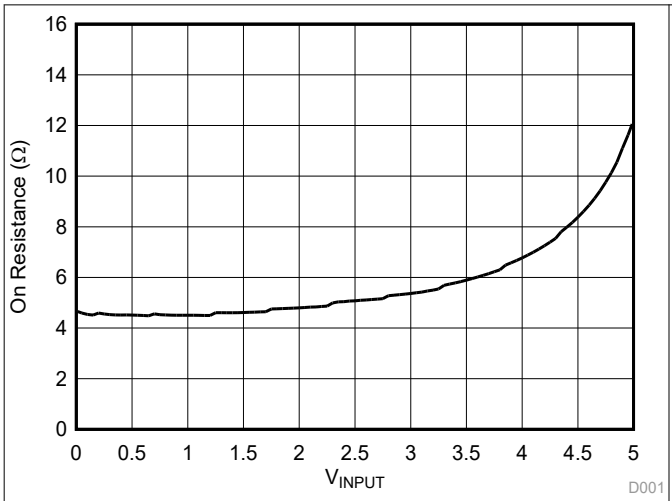


Figure 5-1. Typical r_{on} vs V_I, V_{CC} = 3.3V and I_O = –15mA

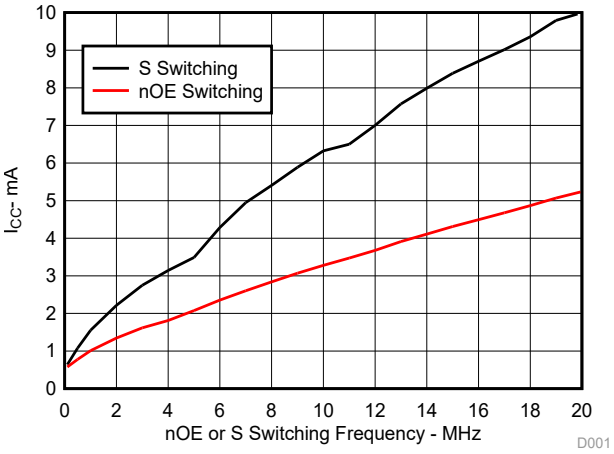
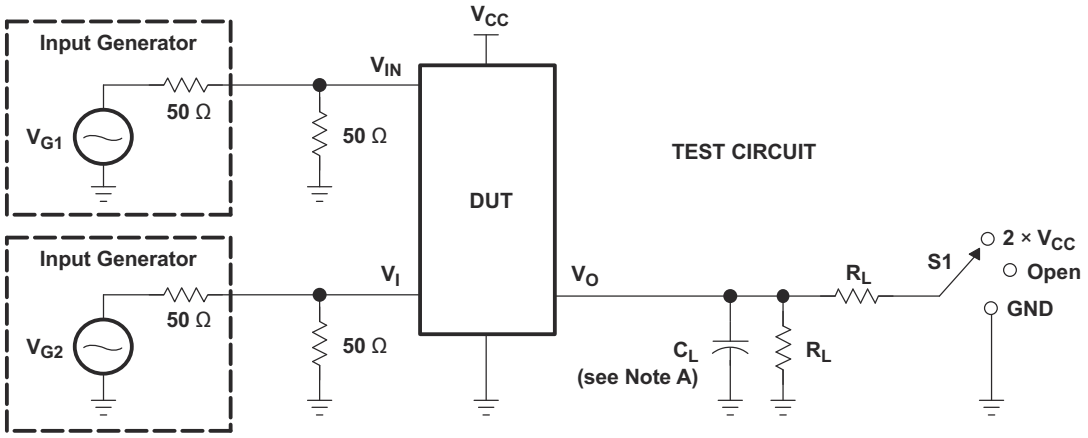


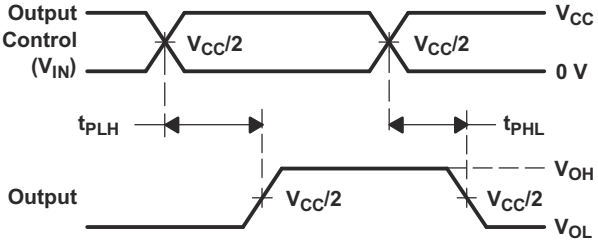
Figure 5-2. Typical I_{CC} vs $\overline{OE}$ or S Switching Frequency, V_{CC} = 3.3V

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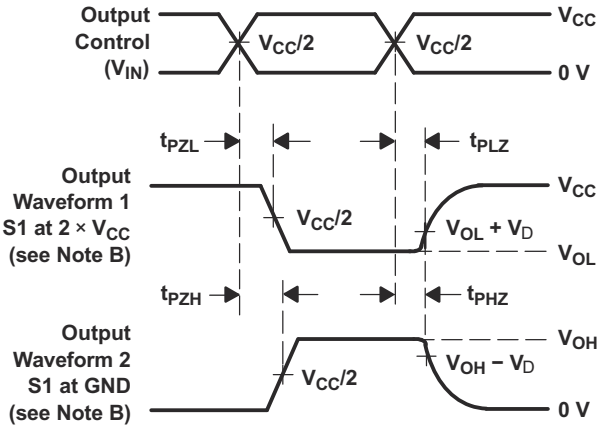
6 Parameter Measurement Information



TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	V_{CC} or GND V_{CC} or GND	30 pF 50 pF	
t_{PLZ}/t_{PZL}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	2 × V_{CC} 2 × V_{CC}	500 Ω 500 Ω	GND GND	30 pF 50 pF	0.15 V 0.3 V
t_{PHZ}/t_{PZH}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	GND GND	500 Ω 500 Ω	V_{CC} V_{CC}	30 pF 50 pF	0.15 V 0.3 V



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
H. All parameters and waveforms are not applicable to all devices.

Figure 6-1. Test Circuit and Voltage Waveforms

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7 Detailed Description

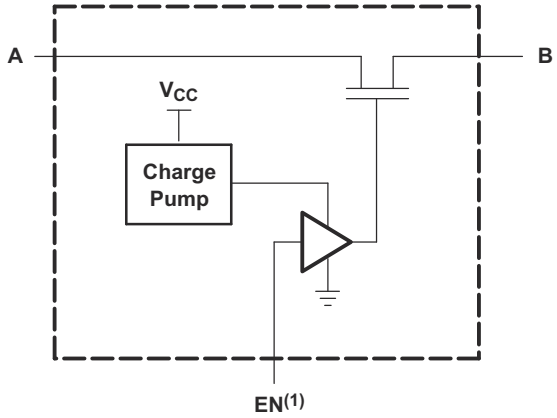
7.1 Overview

The SN74CB3Q3253 device is a high-bandwidth FET bus switch using a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance (r_{on}). The low and flat ON-state resistance allows for minimal propagation delay and supports rail-to-rail switching on the data input/output (I/O) ports. The device also features low data I/O capacitance to minimize capacitive loading and signal distortion on the data bus. Specifically designed to support high-bandwidth applications, the SN74CB3Q3253 device provides an optimized interface design designed for broadband communications, networking, and data-intensive computing systems.

The SN74CB3Q3253 device is organized as two 1-of-4 multiplexers/demultiplexers with separate output-enable (1 $\overline{OE}$, 2 $\overline{OE}$) inputs. The select (S0, S1) inputs control the data path of each multiplexer/demultiplexer. When $\overline{OE}$ is low, the associated multiplexer/demultiplexer is enabled, and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{OE}$ is high, the associated multiplexer/demultiplexer is disabled, and a high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry prevents damaging current backflow through the device when powered down. The device has isolation during power off.

To maintain the high-impedance state during power up or power down, $\overline{OE}$ must be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

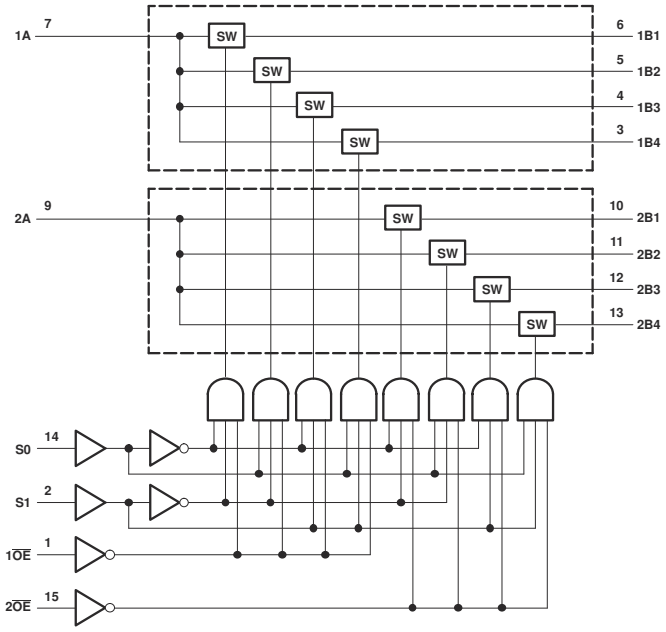


EN is the internal enable signal applied to the switch.

Figure 7-1. Simplified Schematic, Each FET Switch (SW)

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7.2 Functional Block Diagram



7.3 Feature Description

The SN74CB3Q3253 device has a high-bandwidth data path (up to 500MHz) and has 5V tolerant I/Os with the device powered up or powered down. The device also has low and flat ON-state resistance (r_{on}) characteristics over operating range (r_{on} = 4Ω Typical)

This device also has rail-to-rail switching on data I/O ports for 0- to 5V switching with 3.3V $V_{CC}$and 0- to 3.3V switching with 2.5V V_{CC}as well as bidirectional data flow with near-zero propagation delay and low input and output capacitance that minimizes loading and signal distortion ($C_{io(OFF)}$ = 3.5pF Typical)

The SN74CB3Q3253 also provides a fast switching frequency ($f_{\overline{OE}}$ = 20MHz Maximum) with data and control inputs that provide undershoot clamp diodes as well as low power consumption (I_{CC} = 0.6mA Typical)

The V_{CC} operating range is from 2.3V to 3.6V and the data I/Os support 0V to 5V signal levels of (0.8V, 1.2V, 1.5V, 1.8V, 2.5V, 3.3V, 5V)

The control inputs can be driven by TTL or 5V and 3.3V CMOS outputs as well as I_{off} Supports Partial-Power-Down Mode Operation

7.4 Device Functional Modes

Table 7-1 lists the functional modes of the SN74CB3Q3253.

Table 7-1. Function Table
(Each Multiplexer/Demultiplexer)

INPUTS			INPUT/OUTPUT	FUNCTION
$\overline{OE}$	S1	S0	A	
L	L	L	B1	A port = B1 port
L	L	H	B2	A port = B2 port
L	H	L	B3	A port = B3 port
L	H	H	B4	A port = B4 port
H	X	X	Z	Disconnect

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The SN74CB3Q3253 device can be used to multiplex and demultiplex up to 4 channels simultaneously in a 2:1 configuration.

8.2 Typical Application

The application shown is a 4-bit bus being multiplexed between two devices. The $\overline{OE}$ and S pins are used to control the chip from the bus controller. This example is a very generic example and can apply to many situations. If an application requires less than 4 bits, be sure to tie the A side to either high or low on unused channels.

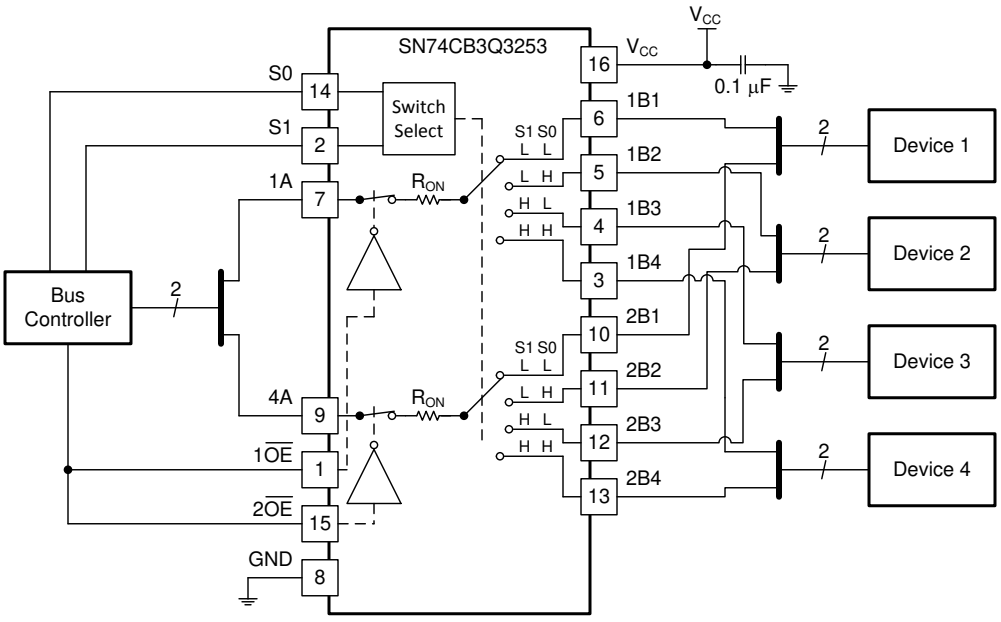


Figure 8-1. Typical Application of the SN74CB3Q3253

8.2.1 Design Requirements

The 0.1-µF capacitor must be place as close as possible to the device.

8.2.2 Detailed Design Procedure

1. Recommended input conditions:
   - For specified high and low levels, see V_{IH} and V_{IL} in *Recommended Operating Conditions*.
   - Inputs and outputs are overvoltage tolerant slowing them to go as high as 4.6V at any valid V_{CC}.
2. Recommended output conditions:
   - Load currents must not exceed ±128mA per channel.
3. Frequency selection criterion:
   - Maximum frequency tested is 500MHz.

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- Added trace resistance and capacitance can reduce maximum frequency capability; use layout practices as directed in *Layout*.

8.2.3 Application Curve

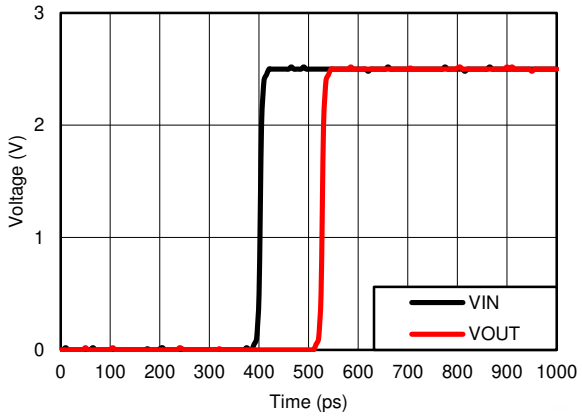


Figure 8-2. Propagation Delay (t_{pd}) Simulation Result at V_{CC} = 2.5V

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the *Absolute Maximum Ratings* table.

Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1µF bypass capacitor is recommended. If multiple pins are labeled V_{CC}, then a 0.01µF or 0.022µF capacitor is recommended for each V_{CC} because the V_{CC} pins are tied together internally. For devices with dual-supply pins operating at different voltages, for example V_{CC} and V_{DD}, a 0.1-µF bypass capacitor is recommended for each supply pin. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1µF and 1µF are commonly used in parallel. The bypass capacitor must be installed as close to the power terminal as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

Reflections and matching are closely related to the loop antenna theory but are different enough to be discussed separately from the theory. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 8-3 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

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8.4.2 Layout Example

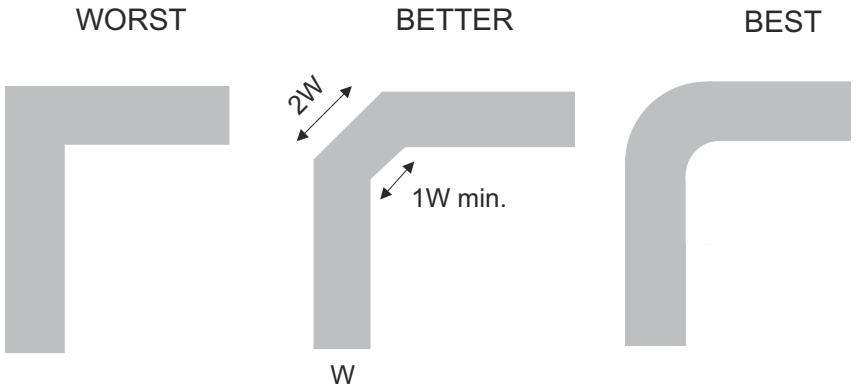


Figure 8-3. Trace Example

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9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application note
- Texas Instruments, *Selecting the Right Texas Instruments Signal Switch* application note
- Texas Instruments, *CBT-C, CB3T, and CB3Q signal-switch families* application note

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (June 2018) to Revision D (August 2026)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added the DYY package to the document	1
• Added operating free-air temperature minimum and maximum values in the *Recommended Operating Conditions* table	4
• Updated all values in the *Thermal Information* table	5
• Added the DYY package to the *Thermal Information* table	5
• Changed the typical I_{CCD} per input control value in the *Electrical Characteristics* table from 0.04 to 0.23	5
• Changed the maximum I_{CCD} per input control value in the *Electrical Characteristics* table from 0.05 to 0.25	5
• Added the *Electrical Characteristics: DYY Package* table	6
• Added the *Switching Characteristics: DYY Package* table	7
• Added the latest typical curve data to the *Typical Characteristics* section	8

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Changes from Revision B (June 2015) to Revision C (June 2018)	Page
• Changed the pinout image appearance	3

Changes from Revision A (November 2003) to Revision B (June 2015)	Page
• Removed *Ordering Information* table	1
• Added *Applications*, *Device Information* table, *Pin Configuration and Functions* section, *Storage Conditions* table, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74CB3Q3253DBQR	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BU253
SN74CB3Q3253DBQR.A	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BU253
SN74CB3Q3253DBQR.B	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BU253
SN74CB3Q3253DBQRG4	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BU253
SN74CB3Q3253DBQRG4.A	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BU253
SN74CB3Q3253DBQRG4.B	Active	Production	SSOP (DBQ) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BU253
SN74CB3Q3253DGVR	Active	Production	TVSOP (DGV) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU253
SN74CB3Q3253DGVR.B	Active	Production	TVSOP (DGV) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU253
SN74CB3Q3253DGVRG4	Active	Production	TVSOP (DGV) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU253
SN74CB3Q3253DGVRG4.B	Active	Production	TVSOP (DGV) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU253
SN74CB3Q3253PW	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	-40 to 85	BU253
SN74CB3Q3253PWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU253
SN74CB3Q3253PWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU253
SN74CB3Q3253PWR.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BU253
SN74CB3Q3253RGYR	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BU253
SN74CB3Q3253RGYR.A	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BU253
SN74CB3Q3253RGYR.B	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BU253
SN74CB3Q3253RGYRG4	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BU253
SN74CB3Q3253RGYRG4.A	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BU253
SN74CB3Q3253RGYRG4.B	Active	Production	VQFN (RGY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BU253

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

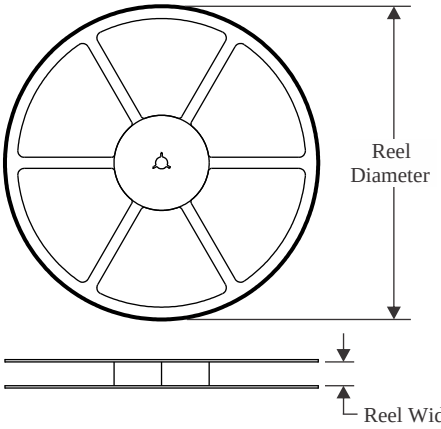
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

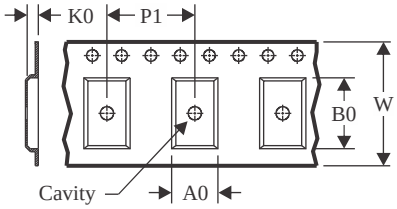
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

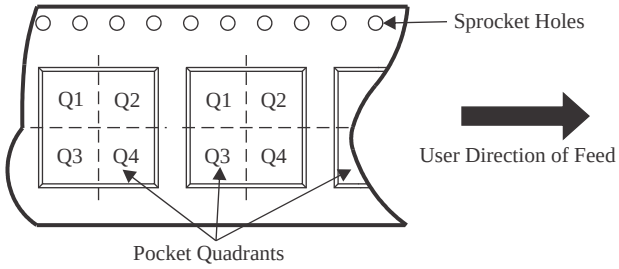


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

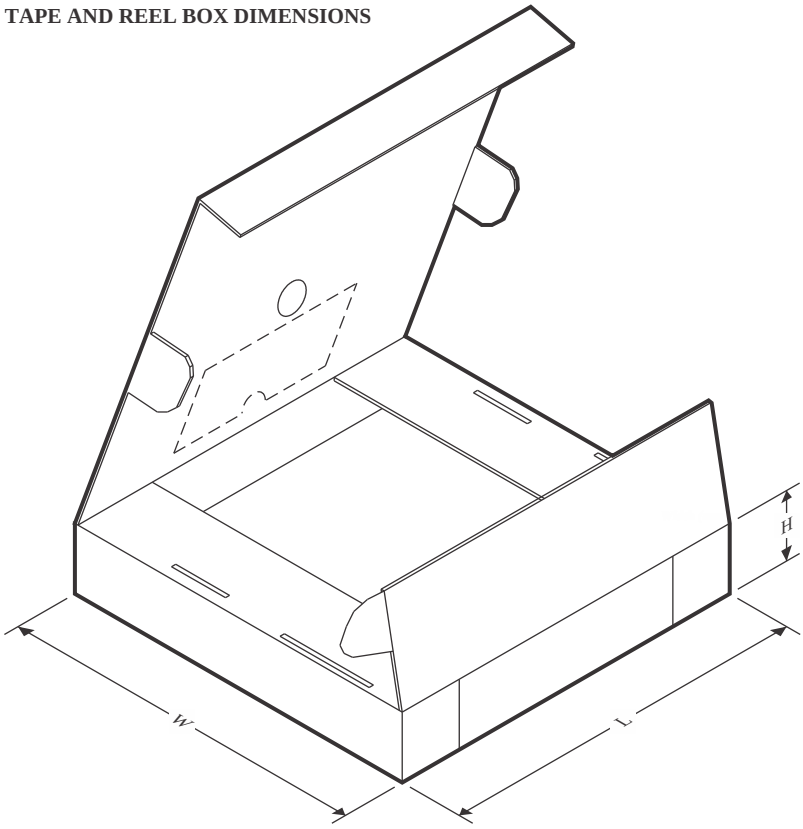
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CB3Q3253DBQR	SSOP	DBQ	16	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
SN74CB3Q3253DBQRG4	SSOP	DBQ	16	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
SN74CB3Q3253DGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74CB3Q3253DGVRG4	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74CB3Q3253PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CB3Q3253RGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
SN74CB3Q3253RGYRG4	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

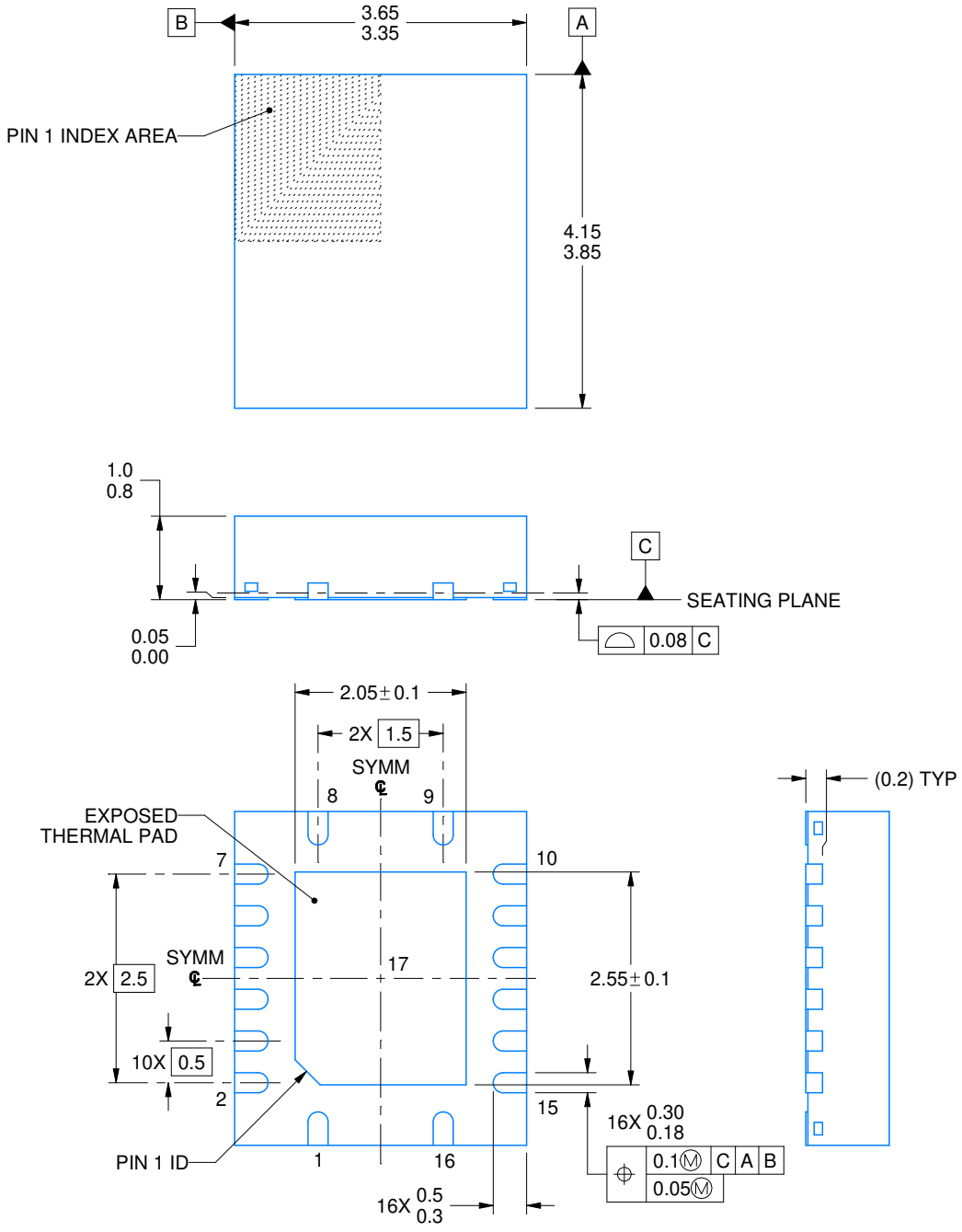
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CB3Q3253DBQR	SSOP	DBQ	16	2500	353.0	353.0	32.0
SN74CB3Q3253DBQRG4	SSOP	DBQ	16	2500	353.0	353.0	32.0
SN74CB3Q3253DGVR	TVSOP	DGV	16	2000	353.0	353.0	32.0
SN74CB3Q3253DGVRG4	TVSOP	DGV	16	2000	353.0	353.0	32.0
SN74CB3Q3253PWR	TSSOP	PW	16	2000	353.0	353.0	32.0
SN74CB3Q3253RGYR	VQFN	RGY	16	3000	353.0	353.0	32.0
SN74CB3Q3253RGYRG4	VQFN	RGY	16	3000	353.0	353.0	32.0

RGY0016A

PACKAGE OUTLINE

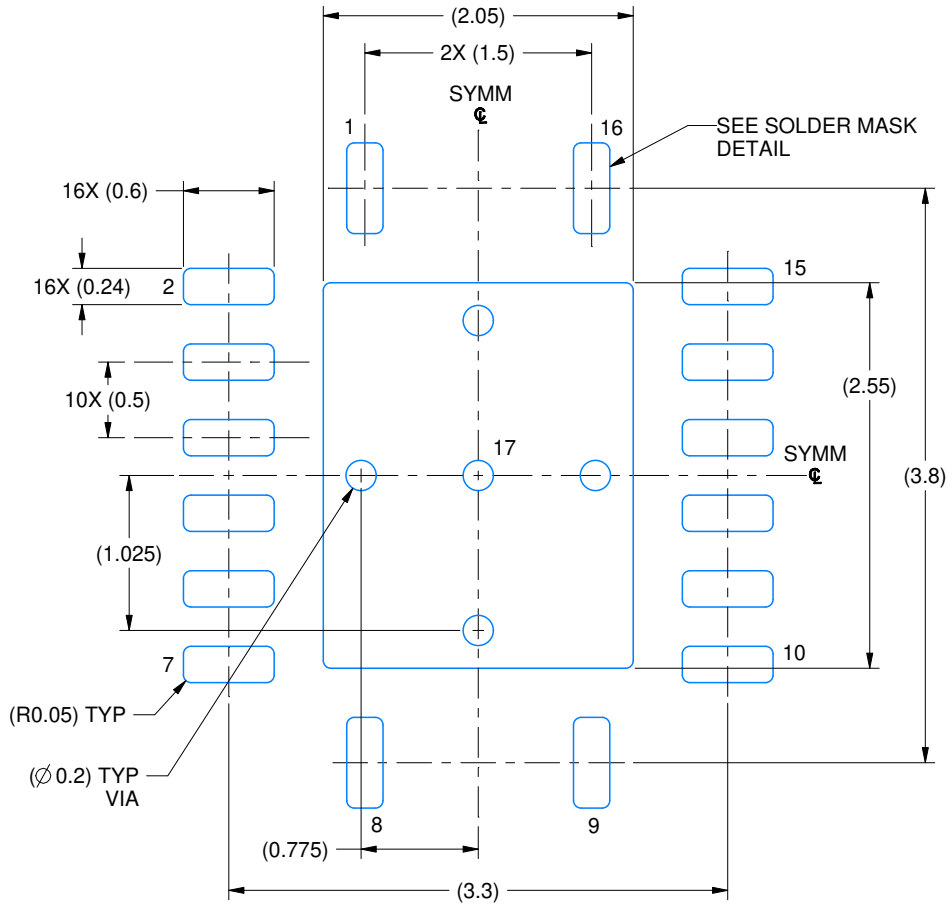
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

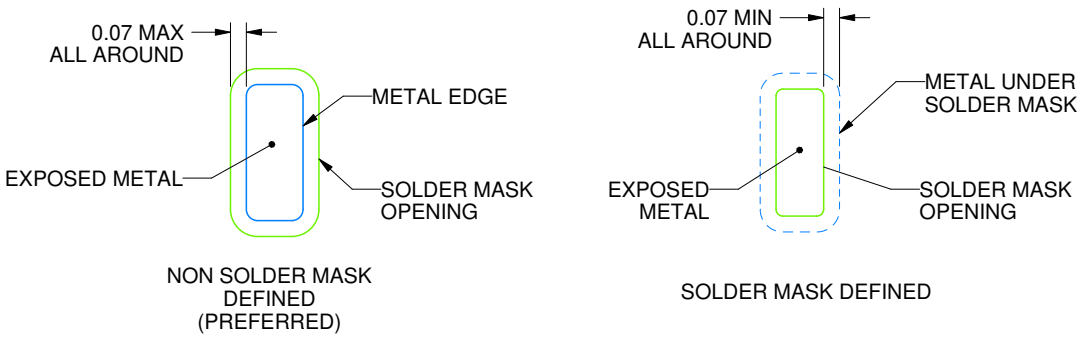


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

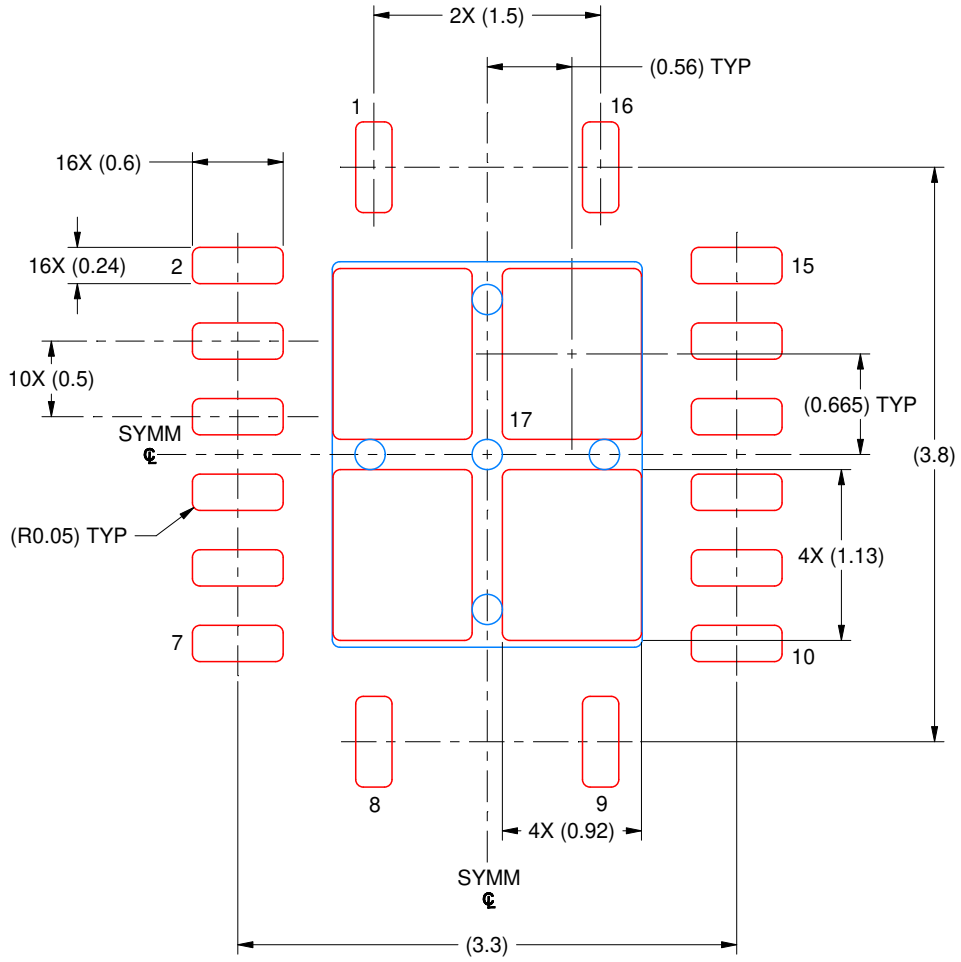


SOLDER MASK DETAILS

4225140/A 07/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 17
80% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

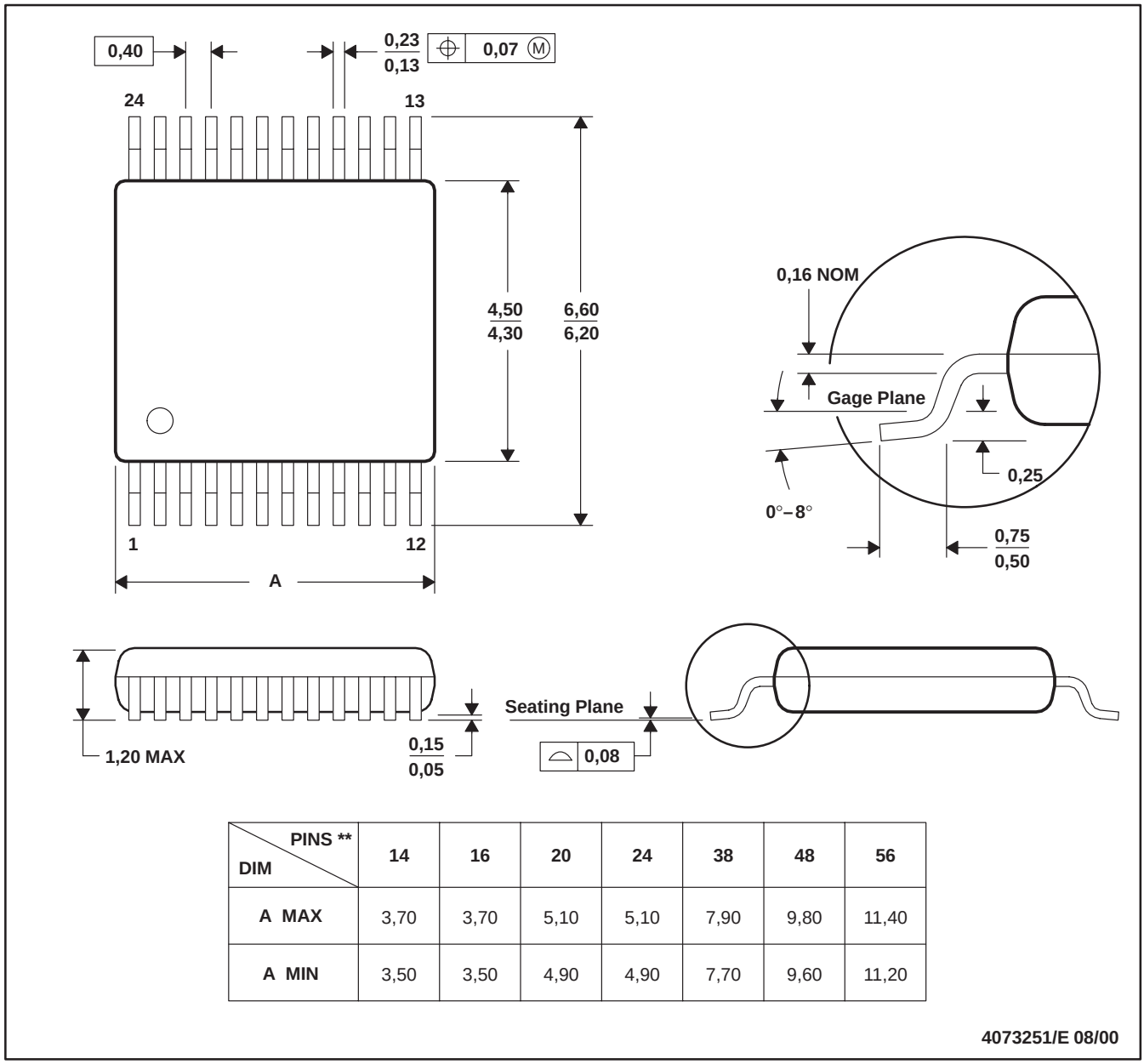
4225140/A 07/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN



DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

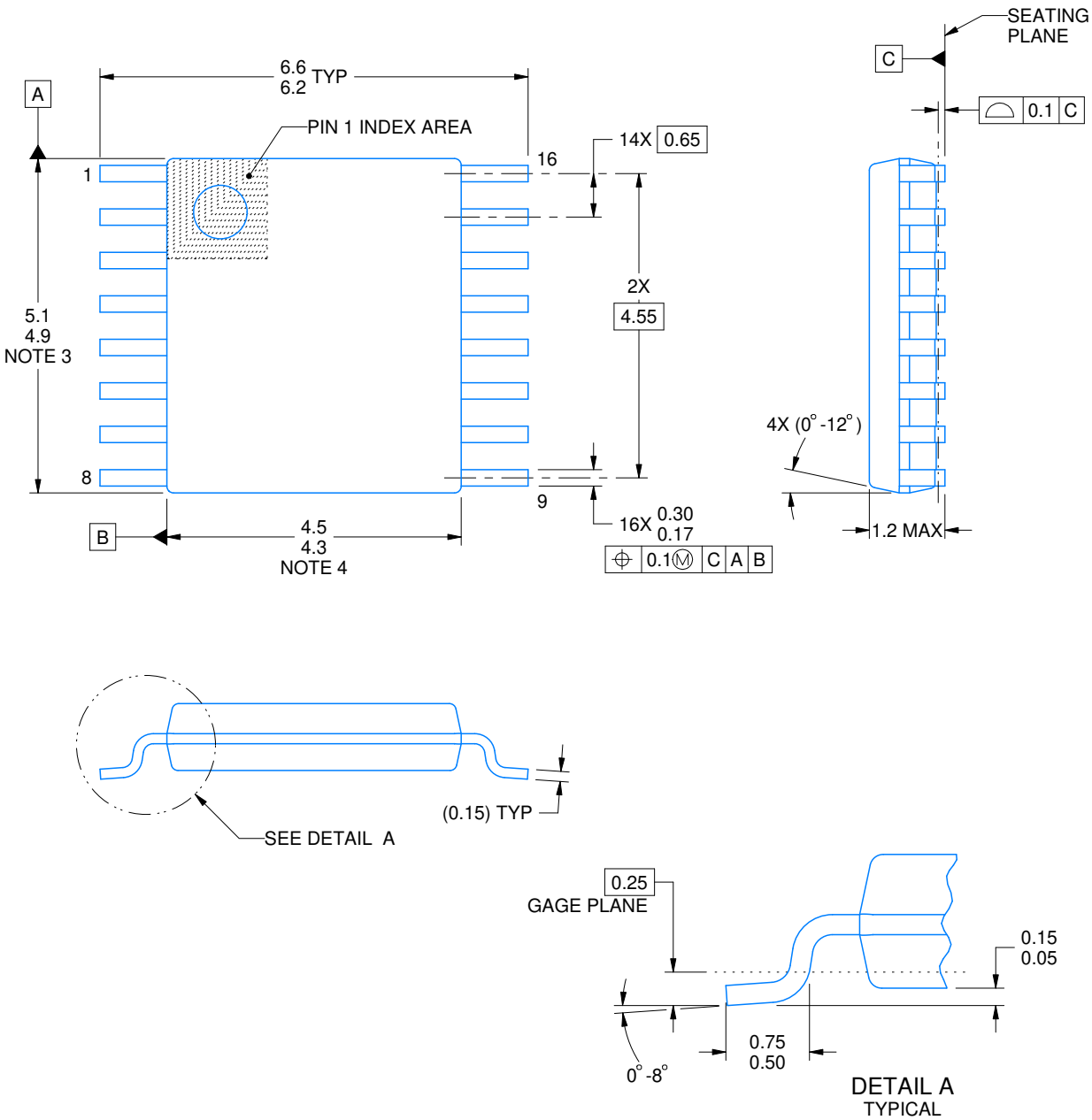
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

PACKAGE OUTLINE

PW0016A

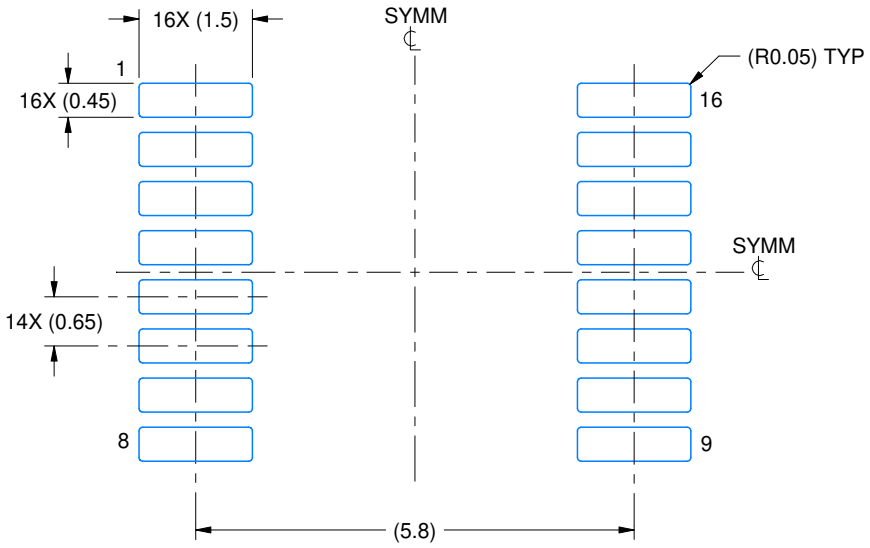
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

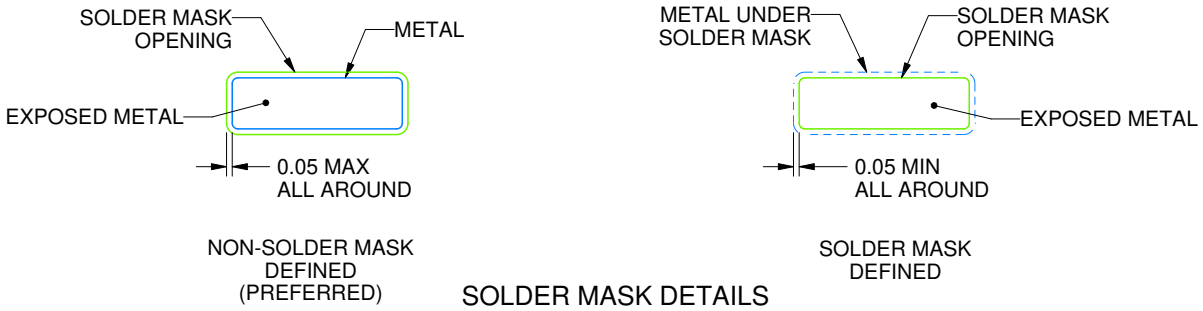


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

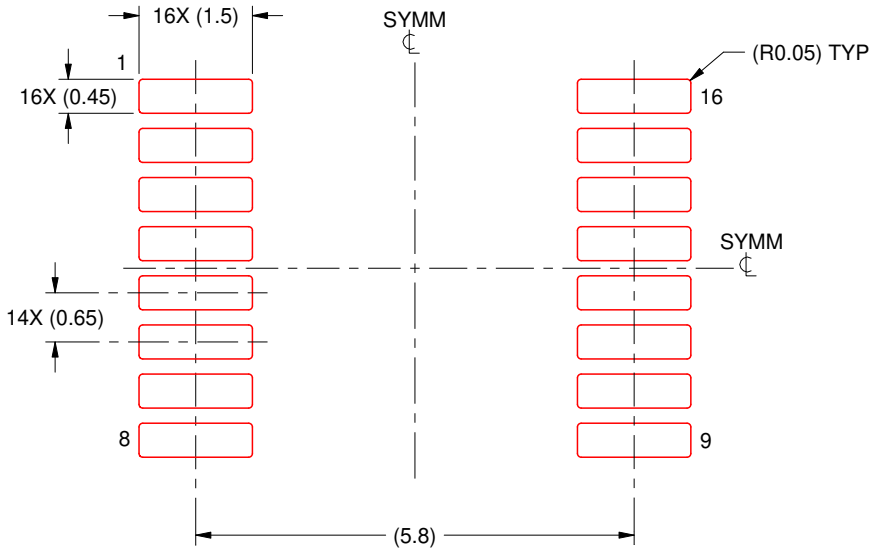


SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

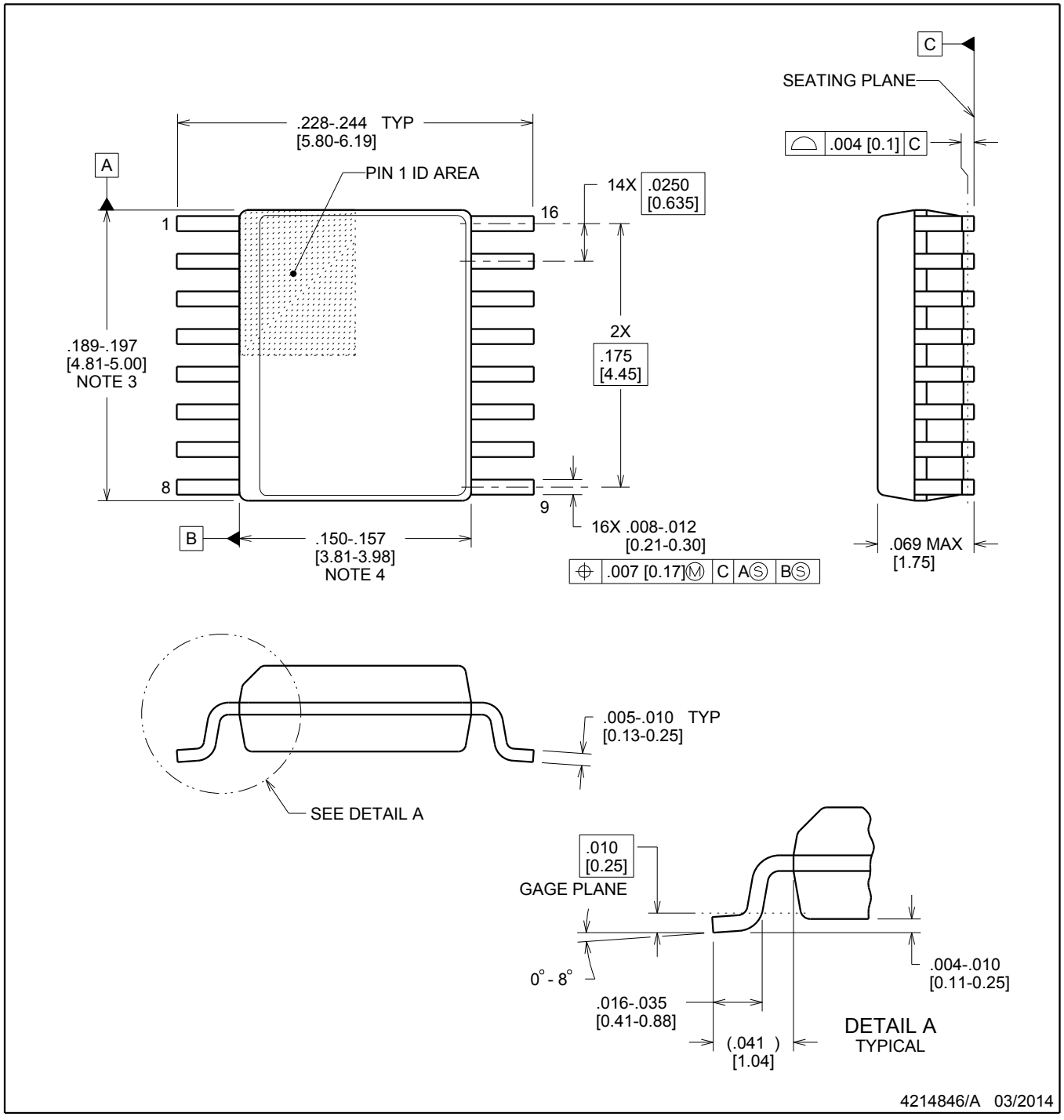


PACKAGE OUTLINE

DBQ0016A

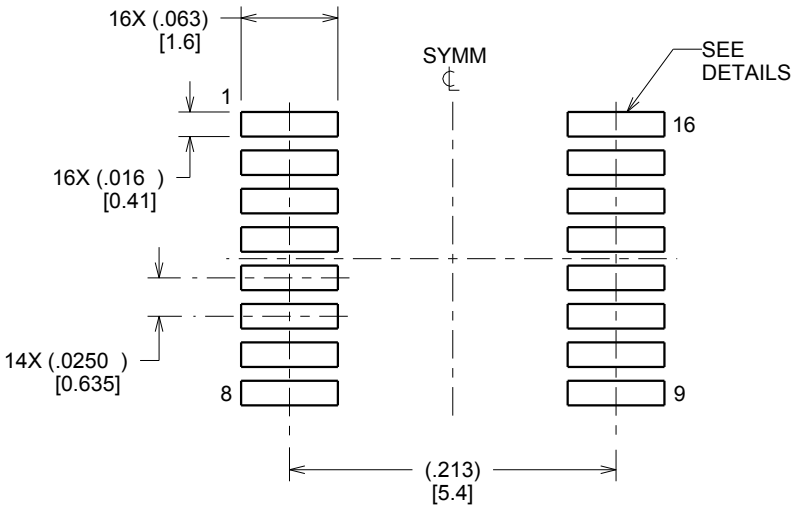
SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE

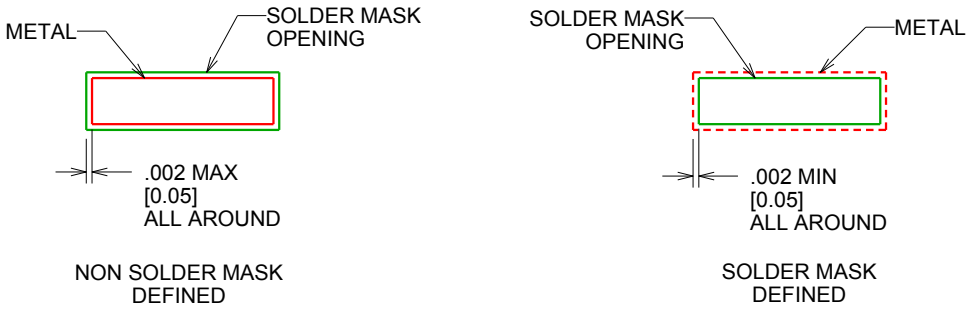


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X

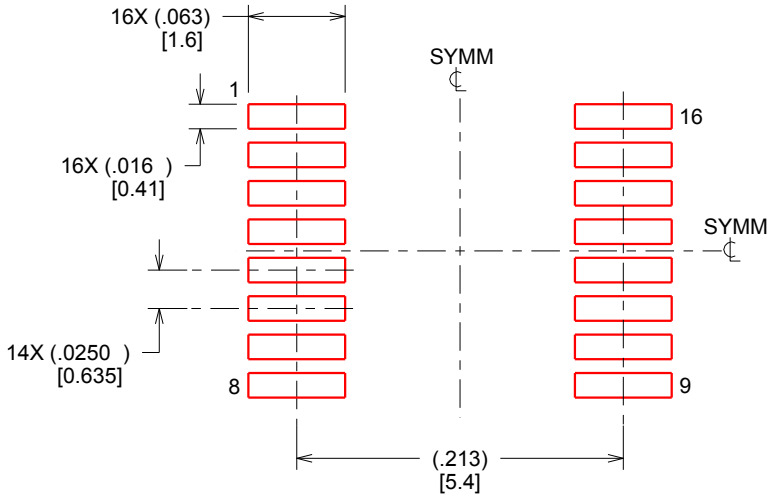


SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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