

# SN74CB3Q3244 8-Bit FET Bus Switch, 2.5V – 3.3V Low-Voltage, High-Bandwidth Bus Switch

## 1 Features

- High-bandwidth data path (up to 500MHz)
- 5V-tolerant I/Os with device powered-up or powered-down
- Low and flat ON-state resistance ( $r_{on}$ ) characteristics over operating range
- Rail-to-rail switching on data I/O ports
  - 0 to 5V switching with 3.3V  $V_{CC}$
  - 0 to 3.3V switching with 2.5V  $V_{CC}$
- Bidirectional data flow, with near-zero propagation delay
- Low input and output capacitance minimizes loading and signal distortion
- Fast switching frequency
- Data and control inputs provide undershoot clamp diodes
- Low power consumption
- $V_{CC}$  operating range from 2.3V to 3.6V
- Data I/Os support 0 to 5V signaling levels (0.8V, 1.2V, 1.5V, 1.8V, 2.5V, 3.3V, 5V)
- Control inputs can be driven by TTL or 5V/3.3V CMOS outputs
- $I_{off}$  supports partial-power-down mode operation
- Latch-up performance exceeds 100mA per JESD 78, Class II
- ESD performance tested per JESD 22
  - 2000V human-body model (A114B, Class II)
  - 1000V charged-device model (C101)
- Supports both digital and analog applications: differential signal interface, memory interleaving, bus isolation, low-distortion signal gating

## 2 Description

The SN74CB3Q3244 is a high-bandwidth FET bus switch using a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance ( $r_{on}$ ). The low and flat ON-state resistance allows for minimal propagation delay and supports rail-to-rail switching on the data input/output (I/O) ports. The device also features low data I/O capacitance to minimize capacitive loading and signal distortion on the data bus. Specifically designed to support high-bandwidth applications, the SN74CB3Q3244 provides an optimized interface design for broadband communications, networking, and data-intensive computing systems.

The SN74CB3Q3244 is organized as two 4-bit bus switches with separate output-enable (1  $\overline{OE}$ , 2  $\overline{OE}$ ) inputs. The device can be used as two 4-bit bus switches or as one 8-bit bus switch. When  $\overline{OE}$  is low, the associated 4-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When  $\overline{OE}$  is high, the associated 4-bit bus switch is OFF, and the high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry prevents damaging current backflow through the device when powered down. The device has isolation during power off.

To make sure of the high-impedance state during power up or power down,  $\overline{OE}$  must be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

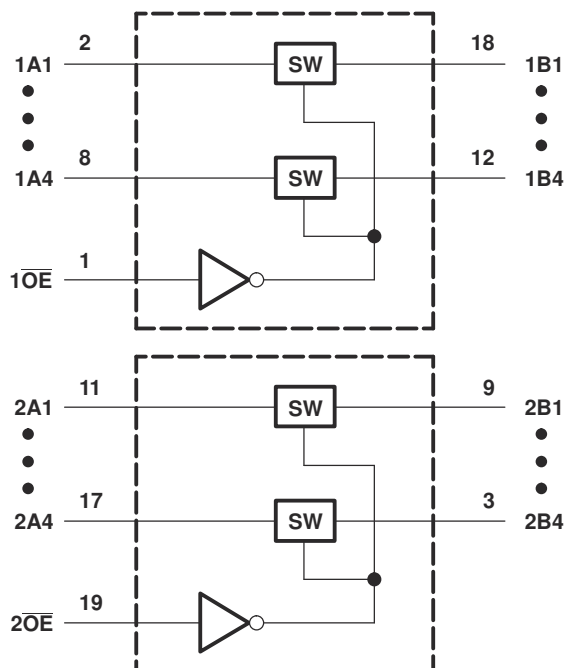
### Package Information

| PART NUMBER  | PACKAGE <sup>(1)</sup> | PACKAGE SIZE <sup>(2)</sup> |
|--------------|------------------------|-----------------------------|
| SN74CB3Q3244 | DBQ (SSOP, 20)         | 8.65mm × 6mm                |
|              | DGV (TVSOP, 20)        | 5mm × 6.4mm                 |
|              | RGY (VQFN, 20)         | 4.5mm × 3.5mm               |
|              | PW (TSSOP, 20)         | 6.5mm × 6.4mm               |
|              | DB (SSOP, 20)          | 7.2mm × 7.8mm               |
|              | DW (SOIC, 20)          | 12.8mm × 10.3mm             |

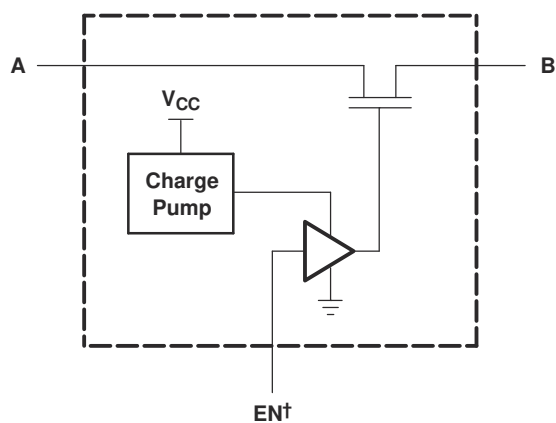
(1) For more information, see [Section 8](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.





**Logic Diagram (Positive Logic)**



† EN is the internal enable signal applied to the switch.

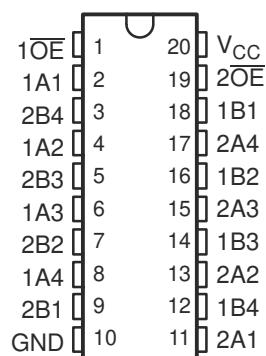
**Simplified Schematic, Each FET Switch (SW)**

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### 3 Pin Configuration and Functions

DB, DBQ, DGV, DW, OR PW PACKAGE  
(TOP VIEW)



RGY PACKAGE  
(TOP VIEW)

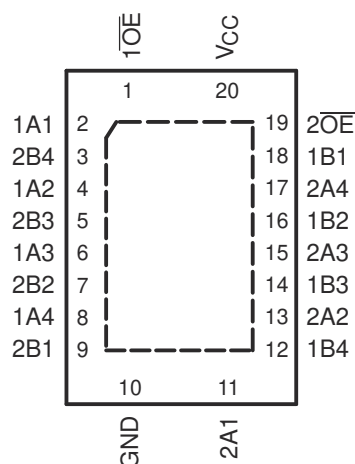


Table 3-1. Terminal Assignments

|   | 1   | 2    | 3               | 4    |
|---|-----|------|-----------------|------|
| A | 1A1 | 1 OE | V <sub>CC</sub> | 2 OE |
| B | 1A2 | 2A4  | 2B4             | 1B1  |
| C | 1A3 | 2B3  | 2A3             | 1B2  |
| D | 1A4 | 2A2  | 2B2             | 1B3  |
| E | GND | 2B1  | 2A1             | 1B4  |

Table 3-2. Pin Functions

| INPUT<br>OE | INPUT/OUTPUT<br>A <sup>(1)</sup> | FUNCTION        |
|-------------|----------------------------------|-----------------|
| L           | B                                | A port = B port |
| H           | Z                                | Disconnect      |

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

## 4 Specifications

### 4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|           |                                                     | MIN  | MAX  | UNIT |
|-----------|-----------------------------------------------------|------|------|------|
| $V_{CC}$  | Supply voltage range                                | -0.5 | 4.6  | V    |
| $V_{IN}$  | Control input voltage range <sup>(2) (3)</sup>      | -0.5 | 7    | V    |
| $V_{IO}$  | Switch I/O voltage range <sup>(2) (3) (4)</sup>     | -0.5 | 7    | V    |
| $I_{IK}$  | Control input clamp current                         |      | -50  |      |
| $I_{IOK}$ | I/O port clamp current                              |      | -50  | mA   |
| $I_{IO}$  | ON-state switch current <sup>(5)</sup>              |      | ±64  | mA   |
| $I_O$     | Continuous output current $V_{CC}$ or GND terminals |      | ±100 | mA   |
| $T_{stg}$ | Storage temperature range                           | -65  | 150  | °C   |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground unless otherwise specified.
- (3) The input and output voltage ratings can be exceeded if the input and output clamp-current ratings are observed.
- (4)  $V_I$  and  $V_O$  are used to denote specific conditions for  $V_{IO}$ .
- (5)  $I_I$  and  $I_O$  are used to denote specific conditions for  $I_{IO}$ .

### 4.2 ESD Ratings

|             |                         | VALUE                                                                         | UNIT  |
|-------------|-------------------------|-------------------------------------------------------------------------------|-------|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>             | ±2000 |
|             |                         | Charged-device model (CDM), per JEDEC specification JESD22C101 <sup>(2)</sup> | ±1000 |

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

### 4.3 Recommended Operating Conditions

See (1)

|                  |                                  |                                | MIN | MAX | UNIT |
|------------------|----------------------------------|--------------------------------|-----|-----|------|
| V <sub>CC</sub>  | Supply voltage                   |                                | 2.3 | 3.6 | V    |
| V <sub>IH</sub>  | High-level control input voltage | V <sub>CC</sub> = 2.3V to 2.7V | 1.7 | 5.5 | V    |
|                  |                                  | V <sub>CC</sub> = 2.7V to 3.6V | 2   | 5.5 |      |
| V <sub>IL</sub>  | Low-level control input voltage  | V <sub>CC</sub> = 2.3V to 2.7V | 0   | 0.7 | V    |
|                  |                                  | V <sub>CC</sub> = 2.7V to 3.6V | 0   | 0.8 |      |
| V <sub>I/O</sub> | Data input/output voltage        |                                | 0   | 5.5 | V    |
| T <sub>A</sub>   | Operating free-air temperature   |                                | –40 | 85  | °C   |

- (1) All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the *Implications of Slow or Floating CMOS Inputs* application note.

### 4.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                        | SN74CB3Q3244 |           |           |             |            |            | UNIT |
|-------------------------------|----------------------------------------|--------------|-----------|-----------|-------------|------------|------------|------|
|                               |                                        | DBQ (SSOP)   | DB (SSOP) | DW (SOIC) | DGV (TVSOP) | PW (TSSOP) | RGY (VQFN) |      |
|                               |                                        | 20 PINS      | 20 PINS   | 20 PINS   | 20 PINS     | 20 PINS    | 20 PINS    |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance | 106.4        | 70        | 58        | 92          | 114.3      | 72.3       | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics application note](#).

## 4.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                      |                   | TEST CONDITIONS                                                                                   |                                 | MIN | TYP <sup>(1)</sup> | MAX     | UNIT       |
|--------------------------------|-------------------|---------------------------------------------------------------------------------------------------|---------------------------------|-----|--------------------|---------|------------|
| $V_{IK}$                       |                   | $V_{CC} = 3.6V$ ,<br>$I_I = -18mA$                                                                |                                 |     |                    | -1.8    | V          |
| $I_{IN}$                       | Control inputs    | $V_{CC} = 3.6V$ ,<br>$V_{IN} = 0$ to 5.5V                                                         |                                 |     |                    | $\pm 1$ | $\mu A$    |
| $I_{OZ}$ <sup>(2)</sup>        |                   | $V_{CC} = 3.6V$ ,<br>$V_O = 0$ to 5.5V,<br>$V_I = 0$ ,<br>Switch OFF,<br>$V_{IN} = V_{CC}$ or GND |                                 |     |                    | $\pm 1$ | $\mu A$    |
| $I_{off}$                      |                   | $V_{CC} = 0$ ,<br>$V_O = 0$ to 5.5V,<br>$V_I = 0$                                                 |                                 |     |                    | 1       | $\mu A$    |
| $I_{CC}$                       |                   | $V_{CC} = 3.6V$ ,<br>$I_{I/O} = 0$ ,<br>Switch ON or OFF,<br>$V_{IN} = V_{CC}$ or GND             |                                 |     | 0.7                | 2       | mA         |
| $\Delta I_{CC}$ <sup>(3)</sup> | Control inputs    | $V_{CC} = 3.6V$ ,<br>One input at 3V,<br>Other inputs at $V_{CC}$ or GND                          |                                 |     |                    | 30      | $\mu A$    |
| $I_{CCD}$ <sup>(4)</sup>       | Per control input | $V_{CC} = 3.6V$ ,<br>A and B ports open,<br>Control input switching at 50% duty cycle             |                                 |     | 0.3                | 0.45    | mA/<br>MHz |
| $C_{in}$                       | Control inputs    | $V_{CC} = 3.3V$ ,<br>$V_{IN} = 5.5V, 3.3V$ , or 0                                                 |                                 |     | 2.5                | 3.5     | pF         |
| $C_{io(OFF)}$                  |                   | $V_{CC} = 3.3V$ ,<br>Switch OFF,<br>$V_{IN} = V_{CC}$ or GND,<br>$V_{I/O} = 5.5V, 3.3V$ , or 0    |                                 |     | 3.5                | 5       | pF         |
| $C_{io(ON)}$                   |                   | $V_{CC} = 3.3V$ ,<br>Switch ON,<br>$V_{IN} = V_{CC}$ or GND,<br>$V_{I/O} = 5.5V, 3.3V$ , or 0     |                                 |     | 9                  | 11      | pF         |
| $r_{on}$ <sup>(5)</sup>        |                   | $V_{CC} = 2.3V$ ,<br>TYP at $V_{CC} = 2.5V$                                                       | $V_I = 0$ ,<br>$I_O = 30mA$     |     | 4                  | 8       | $\Omega$   |
|                                |                   |                                                                                                   | $V_I = 1.7V$ ,<br>$I_O = -15mA$ |     | 5                  | 9       |            |
|                                |                   | $V_{CC} = 3V$                                                                                     | $V_I = 0$ ,<br>$I_O = 30mA$     |     | 4                  | 6       |            |
|                                |                   |                                                                                                   | $V_I = 2.4V$ ,<br>$I_O = -15mA$ |     | 5                  | 8       |            |

- (1) All typical values are at  $V_{CC} = 3.3V$  (unless otherwise noted),  $T_A = 25^\circ C$ .
- (2) For I/O ports, the parameter  $I_{OZ}$  includes the input leakage current.
- (3) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than  $V_{CC}$  or GND.
- (4) This parameter specifies the dynamic power-supply current associated with the operating frequency of a single control input (see Figure 4-2).
- (5) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

## 4.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Section 5)

| PARAMETER               | FROM<br>(INPUT) | TO<br>(OUTPUT) | $V_{CC} = 2.5V \pm 0.2V$ |      | $V_{CC} = 3.3V \pm 0.3V$ |     | UNIT |
|-------------------------|-----------------|----------------|--------------------------|------|--------------------------|-----|------|
|                         |                 |                | MIN                      | MAX  | MIN                      | MAX |      |
| $f_{OE}$ <sup>(1)</sup> | $\overline{OE}$ | A or B         |                          | 10   |                          | 20  | MHz  |
| $t_{pd}$ <sup>(2)</sup> | A or B          | B or A         |                          | 0.12 |                          | 2   | ns   |
| $t_{en}$                | $\overline{OE}$ | A or B         | 2.8                      | 7.1  | 2.5                      | 5.9 | ns   |
| $t_{dis}$               | $\overline{OE}$ | A or B         | 1                        | 7.4  | 1.5                      | 6.8 | ns   |

- (1) Maximum switching frequency for control input ( $V_O > V_{CC}$ ,  $V_I = 5V$ ,  $R_L \geq 1M\Omega$ ,  $C_L = 0$ )
- (2) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by a desired voltage source (zero output impedance).

## 4.7 Typical Characteristics

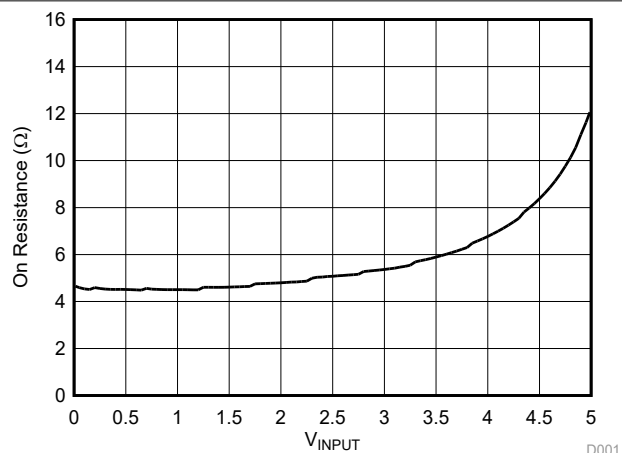


Figure 4-1. Typical  $r_{on}$  vs  $V_I$ ,  $V_{CC} = 3.3V$  and  $I_O = -15mA$

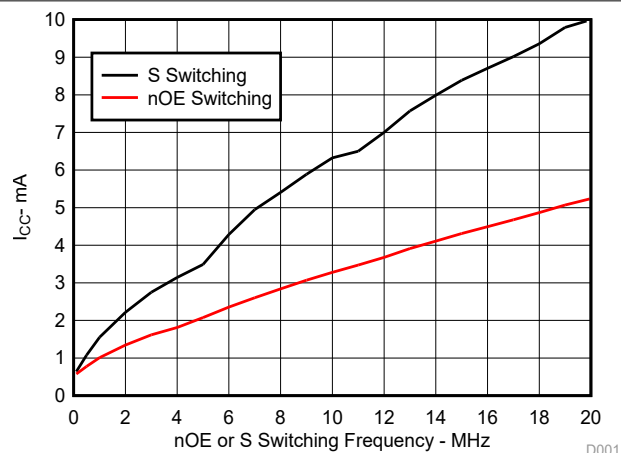
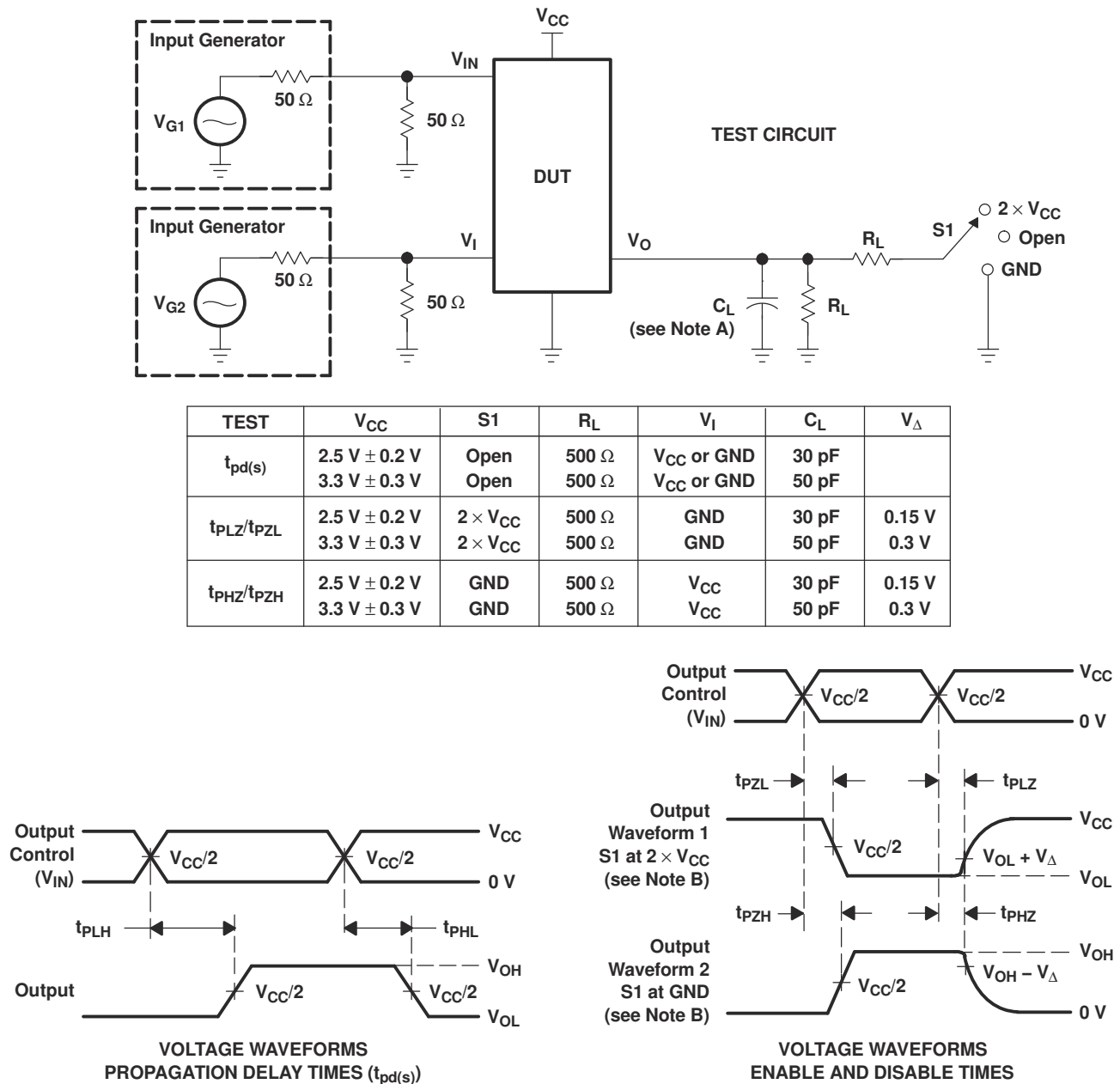


Figure 4-2. Typical  $I_{CC}$  vs  $\overline{OE}$  Switching Frequency,  $V_{CC} = 3.3V$

## 5 Parameter Measurement Information



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd(s)}$ . The  $t_{pd}$  propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
  - H. All parameters and waveforms are not applicable to all devices.

**Figure 5-1. Test Circuit and Voltage Waveforms**

## 6 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 6.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 6.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 6.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 6.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision B (December 2004) to Revision C (August 2026)                                                          | Page |
|------------------------------------------------------------------------------------------------------------------------------|------|
| • Updated the numbering format for tables, figures, and cross-references throughout the document .....                       | 1    |
| • Deleted the <i>Ordering Information</i> table from the document.....                                                       | 1    |
| • Deleted the GQN package from the document.....                                                                             | 4    |
| • Added the <i>ESD Ratings</i> table.....                                                                                    | 5    |
| • Added the <i>Thermal Information</i> table and moved $R_{\theta JA}$ to the table.....                                     | 6    |
| • Changed the typical $I_{CCD}$ per input control value in the <i>Electrical Characteristics</i> table from 0.14 to 0.3..... | 7    |
| • Changed the maximum $I_{CCD}$ per input control value in the <i>Electrical Characteristics</i> table from 0.15 to 0.45...  | 7    |
| • Updated the maximum $V_{CC}$ values for $t_{dis}$ in the <i>Switching Characteristics</i> table.....                       | 7    |
| • Added the latest typical curve data to the <i>Typical Characteristics</i> section.....                                     | 8    |

## 8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number            | Status<br>(1) | Material type<br>(2) | Package   Pins   | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|----------------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">SN74CB3Q3244DBQR</a> | Active        | Production           | SSOP (DBQ)   20  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | CB3Q3244            |
| SN74CB3Q3244DBQR.A               | Active        | Production           | SSOP (DBQ)   20  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | CB3Q3244            |
| SN74CB3Q3244DBQR.B               | Active        | Production           | SSOP (DBQ)   20  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | CB3Q3244            |
| SN74CB3Q3244DBQRG4               | Active        | Production           | SSOP (DBQ)   20  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | CB3Q3244            |
| SN74CB3Q3244DBQRG4.A             | Active        | Production           | SSOP (DBQ)   20  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | CB3Q3244            |
| SN74CB3Q3244DBQRG4.B             | Active        | Production           | SSOP (DBQ)   20  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | CB3Q3244            |
| <a href="#">SN74CB3Q3244DGVR</a> | Active        | Production           | TVSOP (DGV)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | BU244               |
| SN74CB3Q3244DGVR.B               | Active        | Production           | TVSOP (DGV)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | BU244               |
| <a href="#">SN74CB3Q3244PW</a>   | Obsolete      | Production           | TSSOP (PW)   20  | -                     | -           | Call TI                              | Call TI                           | -40 to 85    | BU244               |
| <a href="#">SN74CB3Q3244PWR</a>  | Active        | Production           | TSSOP (PW)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | BU244               |
| SN74CB3Q3244PWR.A                | Active        | Production           | TSSOP (PW)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | BU244               |
| SN74CB3Q3244PWR.B                | Active        | Production           | TSSOP (PW)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | BU244               |
| SN74CB3Q3244PWRG4                | Active        | Production           | TSSOP (PW)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | BU244               |
| SN74CB3Q3244PWRG4.A              | Active        | Production           | TSSOP (PW)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | BU244               |
| SN74CB3Q3244PWRG4.B              | Active        | Production           | TSSOP (PW)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | BU244               |
| <a href="#">SN74CB3Q3244RGYR</a> | Active        | Production           | VQFN (RGY)   20  | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | BU244               |
| SN74CB3Q3244RGYR.A               | Active        | Production           | VQFN (RGY)   20  | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | BU244               |
| SN74CB3Q3244RGYR.B               | Active        | Production           | VQFN (RGY)   20  | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | BU244               |
| SN74CB3Q3244RGYRG4               | Active        | Production           | VQFN (RGY)   20  | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | BU244               |
| SN74CB3Q3244RGYRG4.A             | Active        | Production           | VQFN (RGY)   20  | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | BU244               |
| SN74CB3Q3244RGYRG4.B             | Active        | Production           | VQFN (RGY)   20  | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | BU244               |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

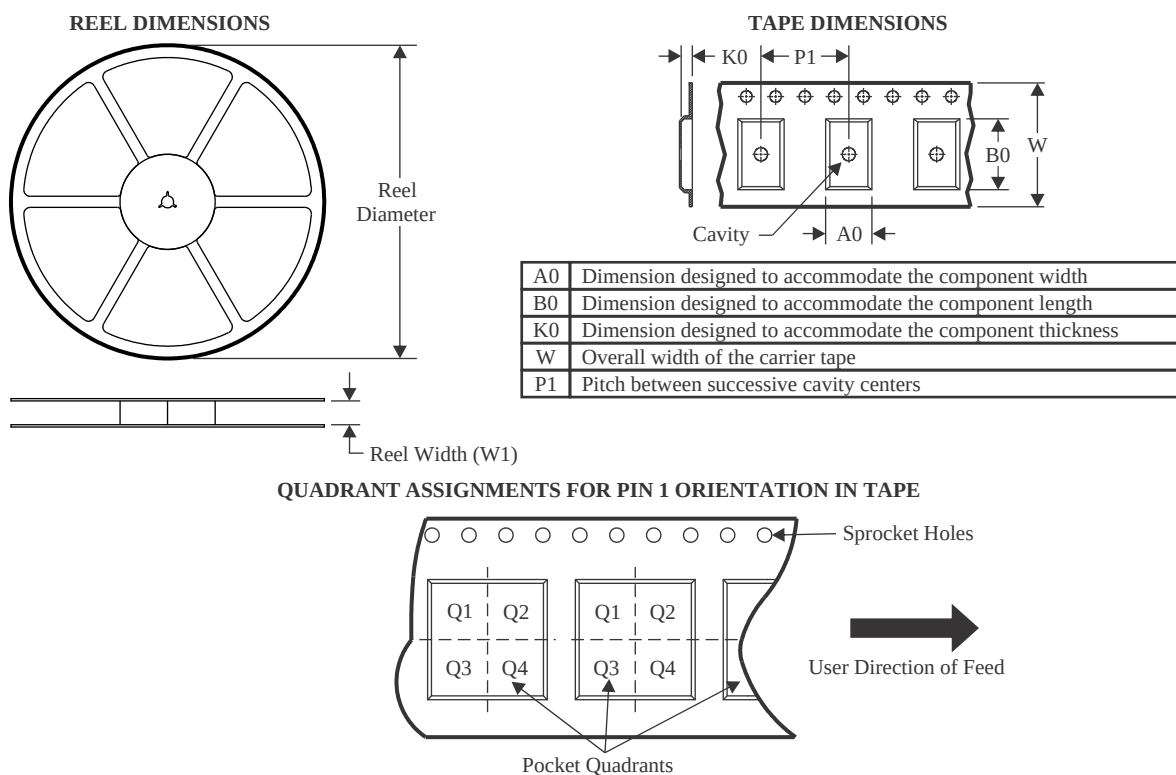
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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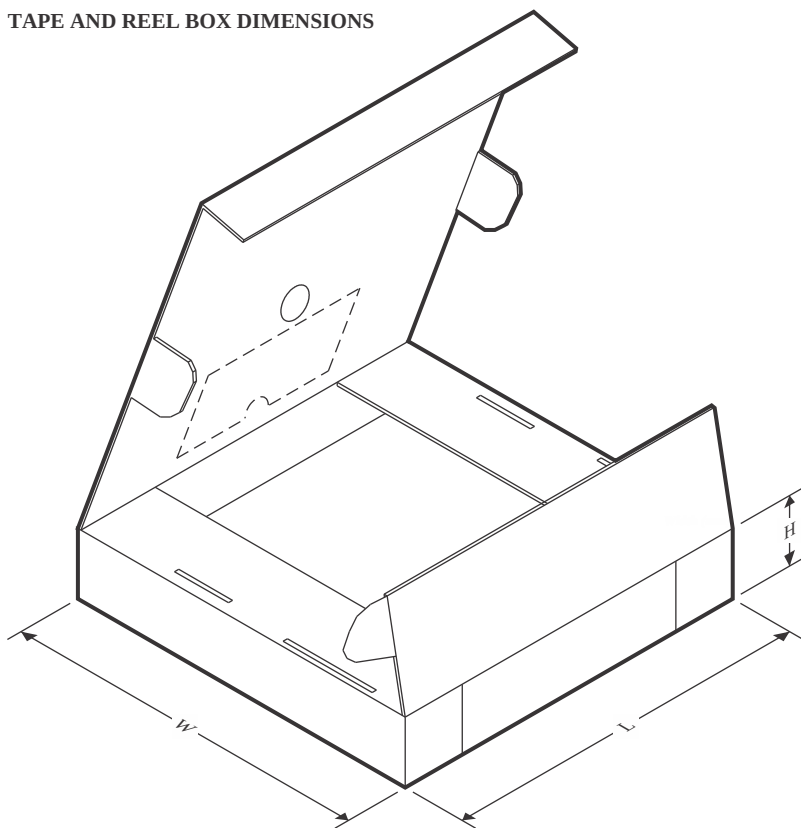
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device             | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74CB3Q3244DBQR   | SSOP         | DBQ             | 20   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74CB3Q3244DBQRG4 | SSOP         | DBQ             | 20   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74CB3Q3244DGVR   | TVSOP        | DGV             | 20   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74CB3Q3244PWR    | TSSOP        | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.0     | 1.4     | 8.0     | 16.0   | Q1            |
| SN74CB3Q3244PWRG4  | TSSOP        | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.0     | 1.4     | 8.0     | 16.0   | Q1            |
| SN74CB3Q3244RGYR   | VQFN         | RGY             | 20   | 3000 | 330.0              | 12.4               | 3.71    | 4.71    | 1.1     | 8.0     | 12.0   | Q1            |
| SN74CB3Q3244RGYRG4 | VQFN         | RGY             | 20   | 3000 | 330.0              | 12.4               | 3.71    | 4.71    | 1.1     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS

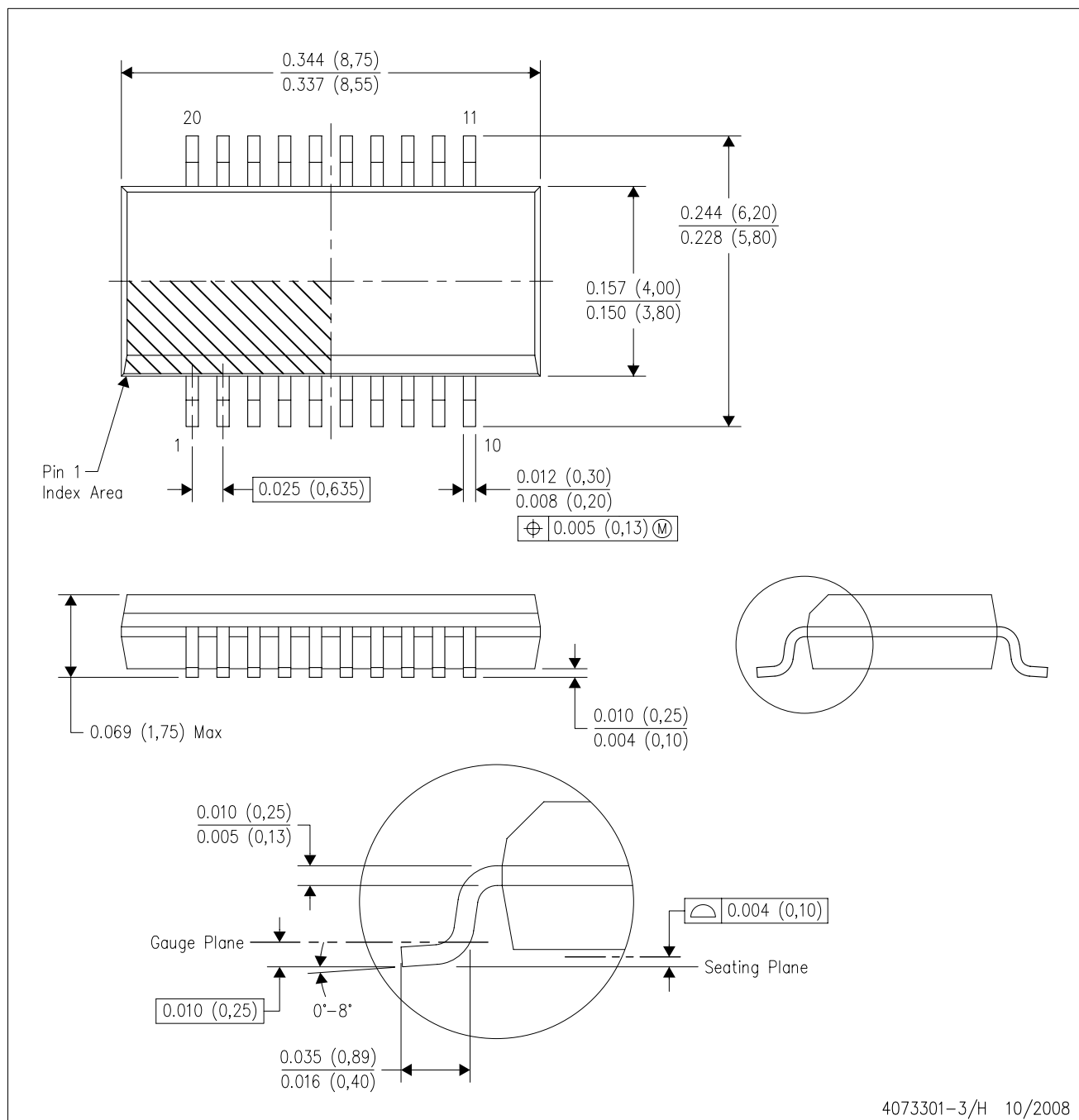


\*All dimensions are nominal

| Device             | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74CB3Q3244DBQR   | SSOP         | DBQ             | 20   | 2500 | 353.0       | 353.0      | 32.0        |
| SN74CB3Q3244DBQRG4 | SSOP         | DBQ             | 20   | 2500 | 353.0       | 353.0      | 32.0        |
| SN74CB3Q3244DGVR   | TVSOP        | DGV             | 20   | 2000 | 353.0       | 353.0      | 32.0        |
| SN74CB3Q3244PWR    | TSSOP        | PW              | 20   | 2000 | 353.0       | 353.0      | 32.0        |
| SN74CB3Q3244PWRG4  | TSSOP        | PW              | 20   | 2000 | 353.0       | 353.0      | 32.0        |
| SN74CB3Q3244RGYR   | VQFN         | RGY             | 20   | 3000 | 353.0       | 353.0      | 32.0        |
| SN74CB3Q3244RGYRG4 | VQFN         | RGY             | 20   | 3000 | 353.0       | 353.0      | 32.0        |

DBQ (R-PDSO-G20)

# PLASTIC SMALL-OUTLINE PACKAGE

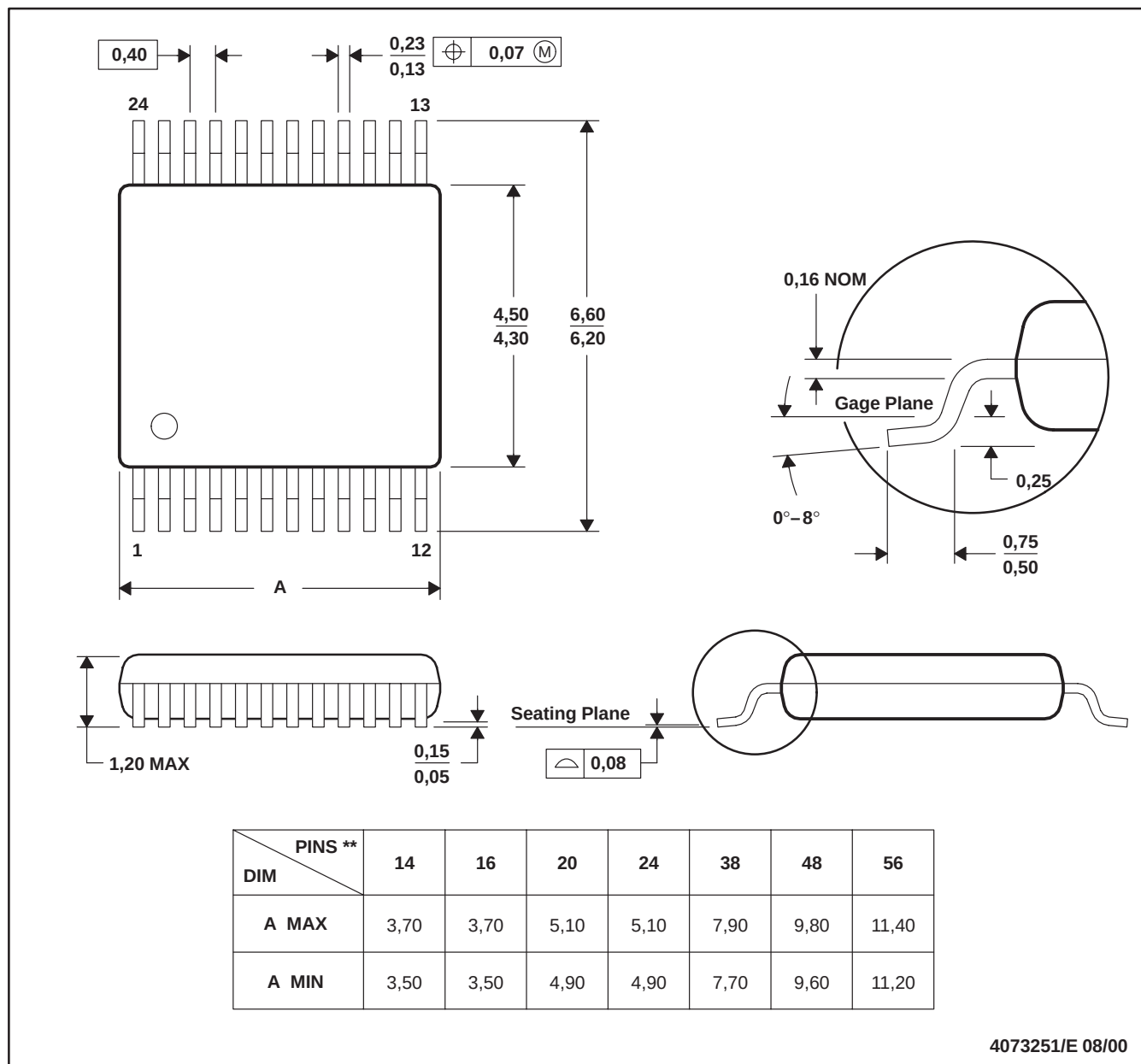


- NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.  
D. Falls within JEDEC MO-137 variation AD.

## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

## GENERIC PACKAGE VIEW

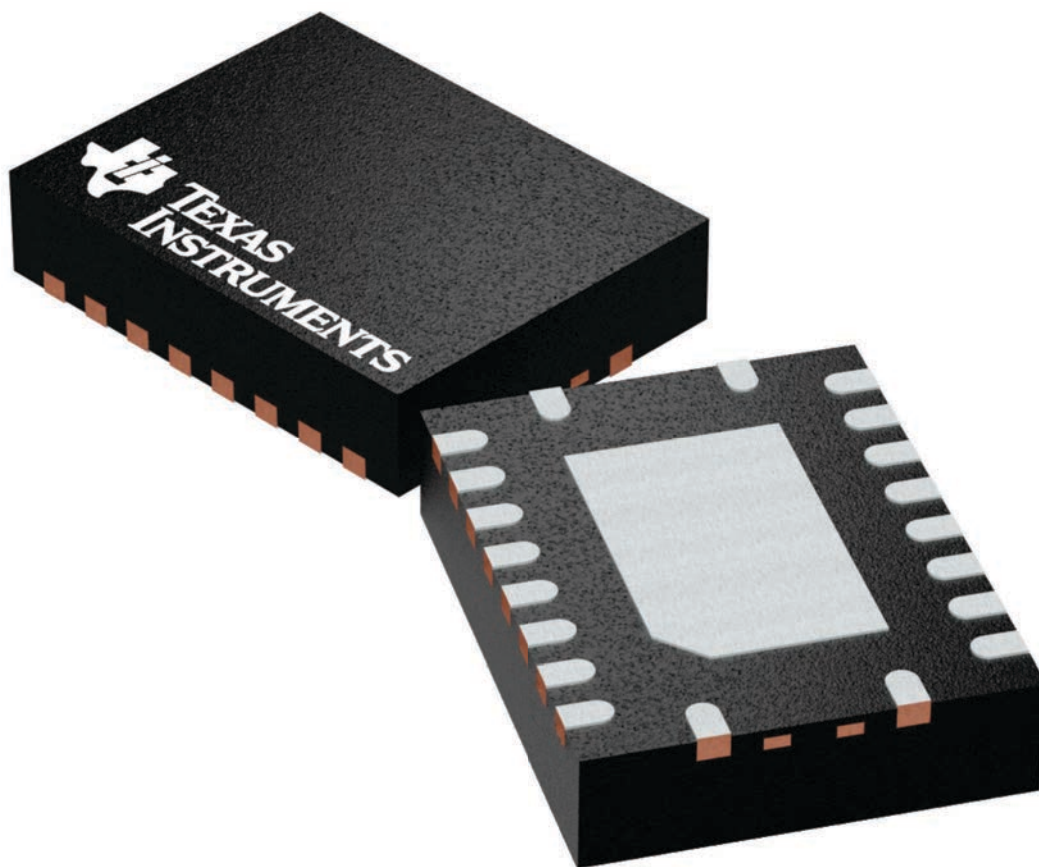
**RGY 20**

**VQFN - 1 mm max height**

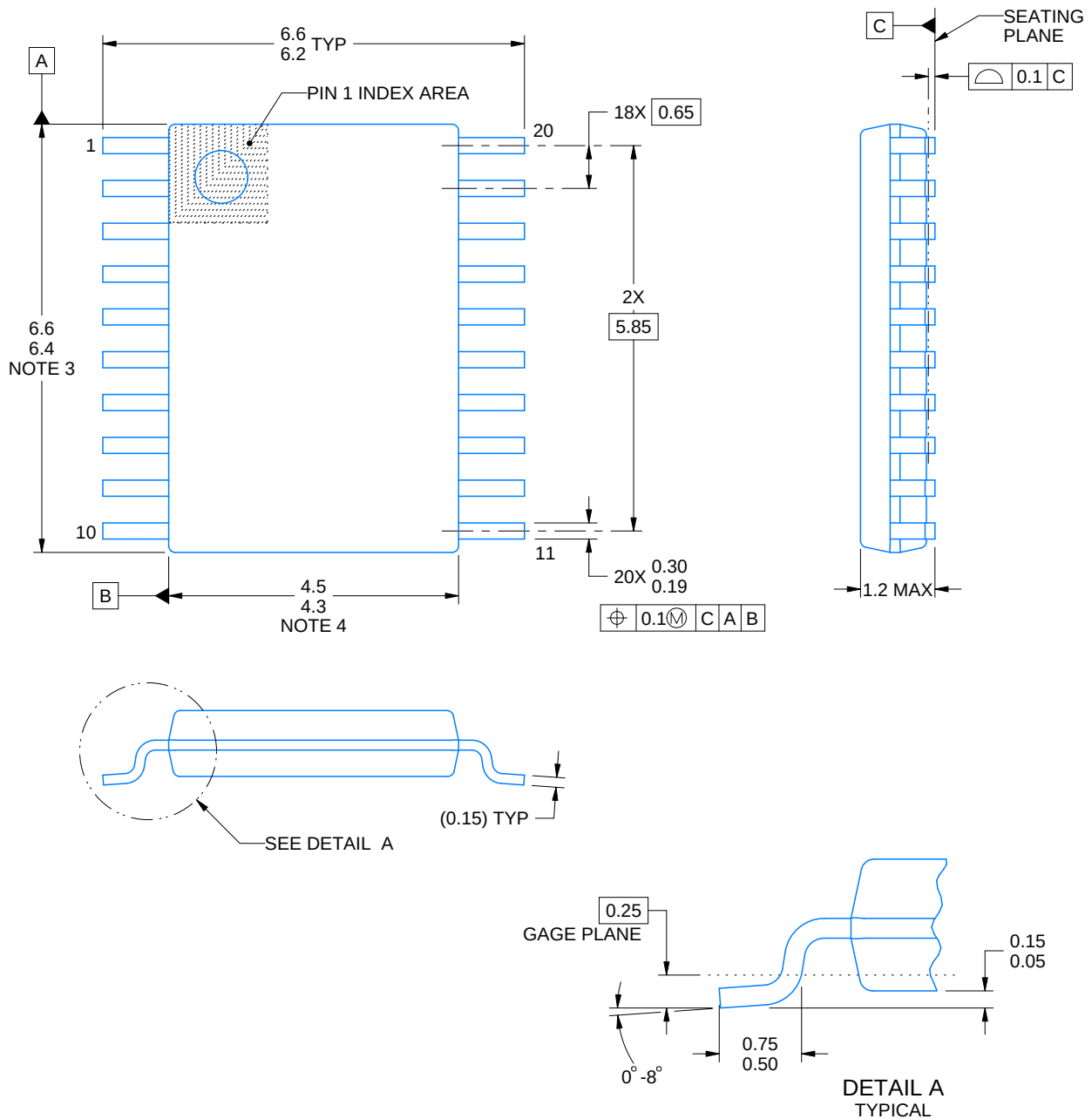
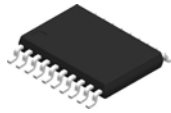
3.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FGLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4225264/A



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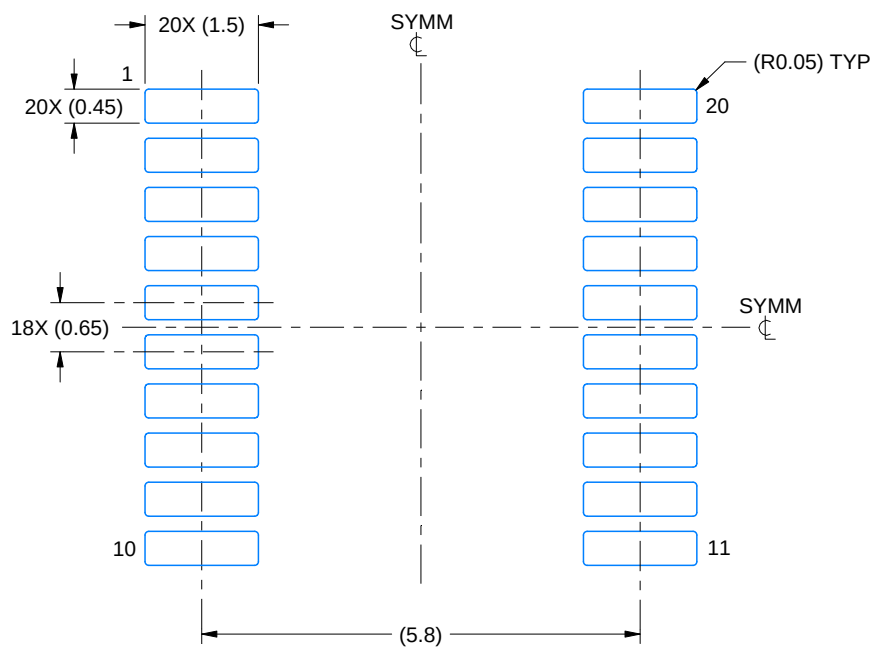
## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

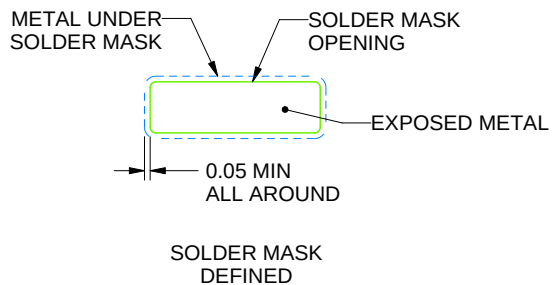
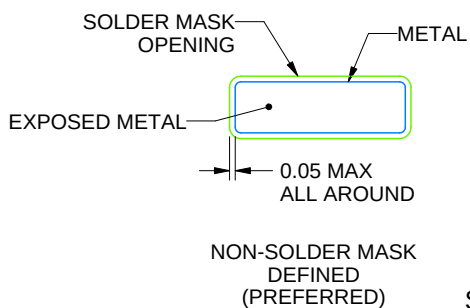
**PW0020A**

**TSSOP - 1.2 mm max height**

## SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



## SOLDER MASK DETAILS

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NOTES: (continued)

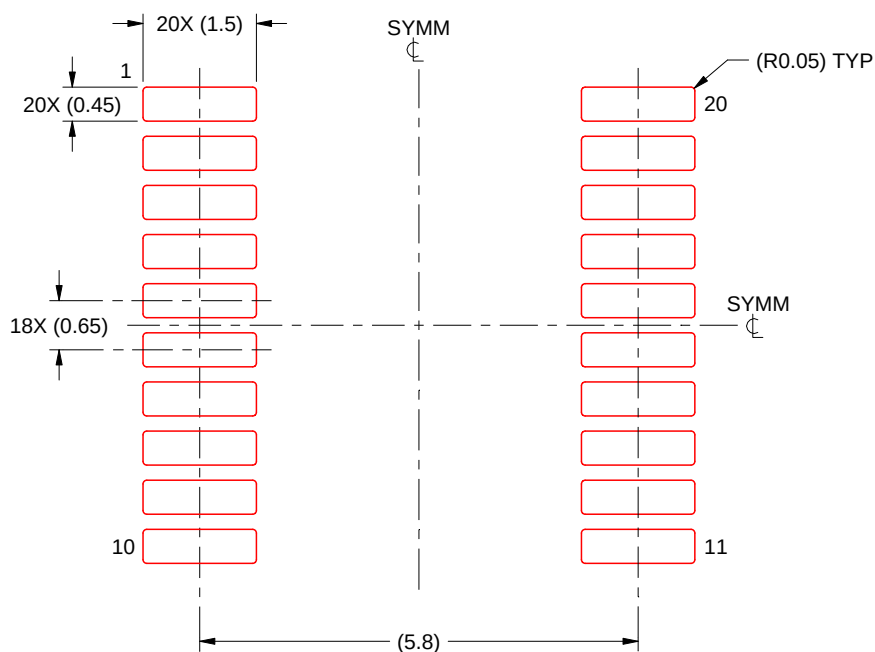
6. Publication IPC-7351 may have alternate designs.  
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025