Primary-side Regulation Off-line PWM Controller

# SFA0006A

Data Sheet

## Description

SFA0006A is the current mode PWM control IC with a primary-side regulation suitable for the automotive system controllers. By employing the primary-side regulation, the IC realizes low component counts and the downsizing the power supply circuit. For supporting the low consumption power and the low standby power, the IC has an automatic standby function. The IC automatically switches to the PWM mode in normal operation, and to the burst oscillation mode at standby. The IC achieves power supply systems to be more cost effective with fewer external components.

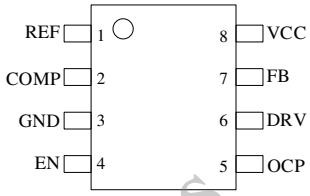
## Features

- AEC-Q100 Qualified
- Bare Lead Frame: Pb-free (RoHS Compliant)
- Primary-side Regulation
  Optocoupler is Unnecessary
  Output Voltage is Set by External Resistor and Transformer Winding Ratio
- Current Mode PWM Control
- Constant Voltage (CV) and Constant Current (CC) Controls
- Automatic Standby Function
- Operation Modes:
  Normal Operation: PWM Mode
  Light Load Operation: Green Mode
  Standby Operation: Burst Oscillation Mode
- Enable Function
  (IC Operation Stops when the EN Pin is Low Level)
- Random Switching Function
- Slope Compensation Function
  (Subharmonic Oscillation Prevention)
- Leading Edge Blanking Function
- Protections:
  Overcurrent Protection (OCP): Pulse-by-Pulse
  Overload Protection (OLP) with Timer: Auto-restart
  Overvoltage Protection (OVP): Auto-restart
  Thermal Shutdown (TSD): Auto-restart

## Package

SOP8






Not to scale

## Specifications

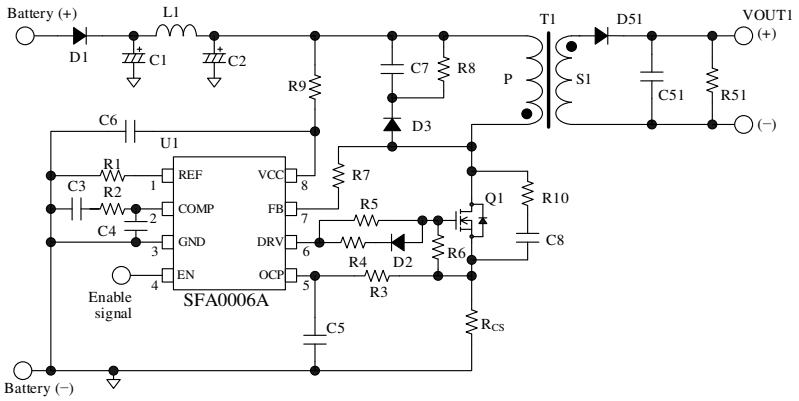
- Maximum VCC Pin Voltage: 40 V
- DRV Pin Source Current (Peak): −270 mA
- DRV Pin Sink Current (Peak): 540 mA

## Applications

For following automotive switching power supply circuits connected to 12 V or 24 V battery:

- Auxiliary Power Supply
- Buck Converter Circuit

## Typical Application




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## 1. Absolute Maximum Ratings

Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

Unless otherwise specified, $T_A$ = 25 °C.

| Parameter | Symbol | Conditions | Pin | Rating | Unit |
|---|---|---|---|---|---|
| REF Pin Voltage | $V_{REF}$ | | 1–3 | −0.3 to 5.5 | V |
| COMP Pin Voltage | $V_{COMP}$ | | 2–3 | −0.3 to 5.5 | V |
| EN Pin Voltage | $V_{EN}$ | | 4–3 | −0.3 to 40 | V |
| OCP Pin Voltage | $V_{OCP}$ | | 5–3 | −2.0 to 40 | V |
| DRV Pin Voltage | $V_{DRV}$ | | 6–3 | −0.3 to 9.0 | V |
| DRV Pin Source Current (Peak) | $I_{DRV(SO)}$ | | 6–3 | −270 | mA |
| DRV Pin Source Current (DC) | $I_{DRV(SO)DC}$ | | 6–3 | −90 | mA |
| DRV Pin Sink Current (Peak) | $I_{DRV(SI)}$ | | 6–3 | 540 | mA |
| DRV Pin Sink Current (DC) | $I_{DRV(SI)DC}$ | | 6–3 | 180 | mA |
| FB Pin Voltage | $V_{FB}$ | | 7–3 | −2.0 to 40 | V |
| FB Pin Current | $I_{FB}$ | | 7–3 | 1.0 | mA |
| VCC Pin Voltage | $V_{CC}$ | | 8–3 | −0.3 to 40 | V |
| Control Part Power Dissipation | $P_D$ | * | — | 1.04 | W |
| Operating Ambient Temperature | $T_{OP}$ | | — | −40 to 125 | °C |
| Storage Temperature | $T_{STG}$ | | — | −40 to 150 | °C |
| Junction Temperature | $T_J$ | | — | 150 | °C |

* The IC is mounted on the glass-epoxy board (PCB: 42 mm × 32 mm in size, 1 mm in thickness).

## 2. Recommended Operating Conditions

| Parameter | Symbol | Conditions | Pin | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| VCC Pin Voltage | $V_{CC}$ | | 8–3 | 5.5 | — | 32 | V |

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## 3. Electrical Characteristics

The following electrical characteristics in $T_A$ = −40 °C to 125 °C are guaranteed by design. Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

| Parameter | Symbol | Conditions | Pin | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| **Power Supply Startup Operation** | | | | | | | |
| Operation Start Voltage | $V_{CC(ON)}$ | | 8–3 | 4.4 | 4.80 | 5.3 | V |
| Operation Stop Voltage | $V_{CC(OFF)}$ | | 8–3 | 4.0 | 4.40 | 4.8 | V |
| Operation Voltage Hysteresis | $V_{CC(HYS)}$ | | 8–3 | 0.19 | 0.40 | 0.63 | V |
| Circuit Current before Startup | $I_{CC(OFF)}$ | $V_{CC}$ = 14 V | 8–3 | 76 | 250 | 525 | µA |
| Circuit Current in Operation | $I_{CC(OP)}$ | $V_{CC}$ = 14 V, $C_{DRV}$ = 2 nF | 8–3 | 0.49 | 2.90 | 5.00 | mA |
| Circuit Current in Enable Operation | $I_{CC(EN)}$ | $V_{CC}$ = 14 V | 8–3 | — | — | 6 | µA |
| **Enable Operation** | | | | | | | |
| EN Pin On Threshold Voltage | $V_{EN(ON)}$ | | 4–3 | 0.43 | 1.88 | 2.94 | V |
| EN Pin Off Threshold Voltage | $V_{EN(OFF)}$ | | 4–3 | 0.38 | 1.28 | 2.10 | V |
| EN Pin Hysteresis Voltage | $V_{EN(HYS)}$ | | 4–3 | — | 0.60 | 1.26 | V |
| EN Pin Resistor | $R_{EN}$ | | 4–3 | 0.38 | 1.00 | 2.10 | MΩ |
| **Feedback Operation** | | | | | | | |
| Current Ratio between FB–REF Pins | $I_{REF}/I_{FB}$ | | 7–3 | 96 | 100 | — | % |
| FB Pin Open Protection Mask Period (Internal Clock Cycle) | $t_{FB(OPEN)}$ | | 7–3 | — | 3 | 4 | Cycles |
| **REF Pin Operation** | | | | | | | |
| REF Pin Reference Voltage | $V_{REF}$ | | 1–3 | 1.268 | 1.300 | 1.333 | V |
| REF Pin Overvoltage Threshold Voltage | $V_{REF(OVP)}$ | | 1–3 | 1.71 | 1.90 | 2.10 | V |
| REF Pin Mask Time | $t_{MASK}$ | | 1–3 | 0.70 | 1.00 | 1.33 | µs |
| **COMP Operation** | | | | | | | |
| COMP Pin Sink Current | $I_{COMP(SI)}$ | | 2–3 | 13.3 | 20.0 | 28.4 | µA |
| COMP Pin Source Current | $I_{COMP(SO)}$ | | 2–3 | −28.4 | −20.0 | −13.3 | µA |
| COMP Pin Overload Threshold Voltage | $V_{COMP(OLP)}$ | | 2–3 | 2.38 | 2.80 | 3.26 | V |
| Frequency Adjustable Start Voltage | $V_{FDOWN(H)}$ | | 2–3 | 1.05 | 1.20 | 1.37 | V |
| Frequency Adjustable Stop Voltage | $V_{FDOWN(L)}$ | | 2–3 | 0.50 | 0.60 | 0.70 | V |
| Oscillation Stop COMP pin Threshold Voltage | $V_{COMP(OFF)}$ | | 2–3 | 0.42 | 0.50 | 0.59 | V |
| **DRV Operation** | | | | | | | |
| DRV Pin Output Voltage | $V_{DRV}$ | | 6–3 | 6.7 | 8.0 | 9.0 | V |
| Minimum Drive Voltage | $V_{DRIVE(MIN)}$ | $V_{CC}$ = 5.2 V | 6–3 | 4.8 | — | — | V |
| DRV Pin Internal Source Resistor | $R_{DRV(SO)}$ | | 6–3 | 0.45 | 5.0 | 22.1 | Ω |
| DRV Pin Internal Sink Resistor | $R_{DRV(SI)}$ | | 6–3 | 0.45 | 4.5 | 21.1 | Ω |
| Output Voltage at DRV Pin in Non-operation | $V_{DRV(OFF)}$ | | 6–3 | 0.095 | 0.800 | 1.200 | V |

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| Parameter | Symbol | Conditions | Pin | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| DRV Pin Rising Time* | $t_{r(DRV)}$ | $C_{DRV}$ = 2 nF | 6–3 | — | 60 | — | ns |
| DRV Pin Falling Time* | $t_{f(DRV)}$ | $C_{DRV}$ = 2 nF | 6–3 | — | 30 | — | ns |
| **PWM Operation** | | | | | | | |
| Average Oscillation Frequency | $f_{OSC(AVG)}$ | $V_{COMP}$ = 2 V | 6–3 | 50.0 | 60.0 | 70.0 | kHz |
| Minimum Oscillation Frequency | $f_{OSC(MIN)}$ | $V_{COMP}$ = 0.5 V | 6–3 | 16.0 | 20.0 | 24.0 | kHz |
| Maximum Duty Cycle | $D_{MAX}$ | | 6–3 | 72.0 | 81.5 | 88.0 | % |
| Frequency Fluctuation Width* | $\Delta f$ | | 6–3 | — | 5.4 | — | kHz |
| Soft-start Period | $t_{SS}$ | | 6–3 | 9.9 | 13.5 | 18.4 | ms |
| OLP Delay Time | $t_{OLP(ON)}$ | | 6–3 | 59.0 | 93.1 | 140.0 | ms |
| OLP Stop Time | $t_{OLP(OFF)}$ | | 6–3 | 1.292 | 1.730 | 2.300 | s |
| **OCP Operation** | | | | | | | |
| OCP Threshold Voltage at 35% Duty Cycle | $V_{OCP(H)}$ | | 5–3 | 247 | 300 | 347 | mV |
| OCP Threshold Voltage at LEB ($t_{BW}$) | $V_{OCP(LEB)}$ | | 5–3 | 455 | 600 | 770 | mV |
| OCP Compensation Duty Cycle* | $D_{DPC}$ | | 5–3 | — | 35 | — | % |
| OCP Threshold Voltage at Zero Duty Cycle | $V_{OCP(L)}$ | | 5–3 | 228 | 270 | 315 | mV |
| OCP Pin Source Current | $I_{OCP}$ | $V_{OCP}$ = 0 V | 5–3 | 0.95 | 14.5 | 47.0 | µA |
| Leading Edge Blanking Time* | $t_{LEB}$ | | 5–3 | 170 | 300 | 420 | ns |
| **TSD Operation** | | | | | | | |
| TSD Operating Temperature* | $T_{TSD}$ | | 8–3 | 150 | 165 | 180 | °C |
| TSD Hysteresis Temperature* | $T_{TSD(HYS)}$ | | 8–3 | — | 13 | — | °C |

* Guaranteed by design

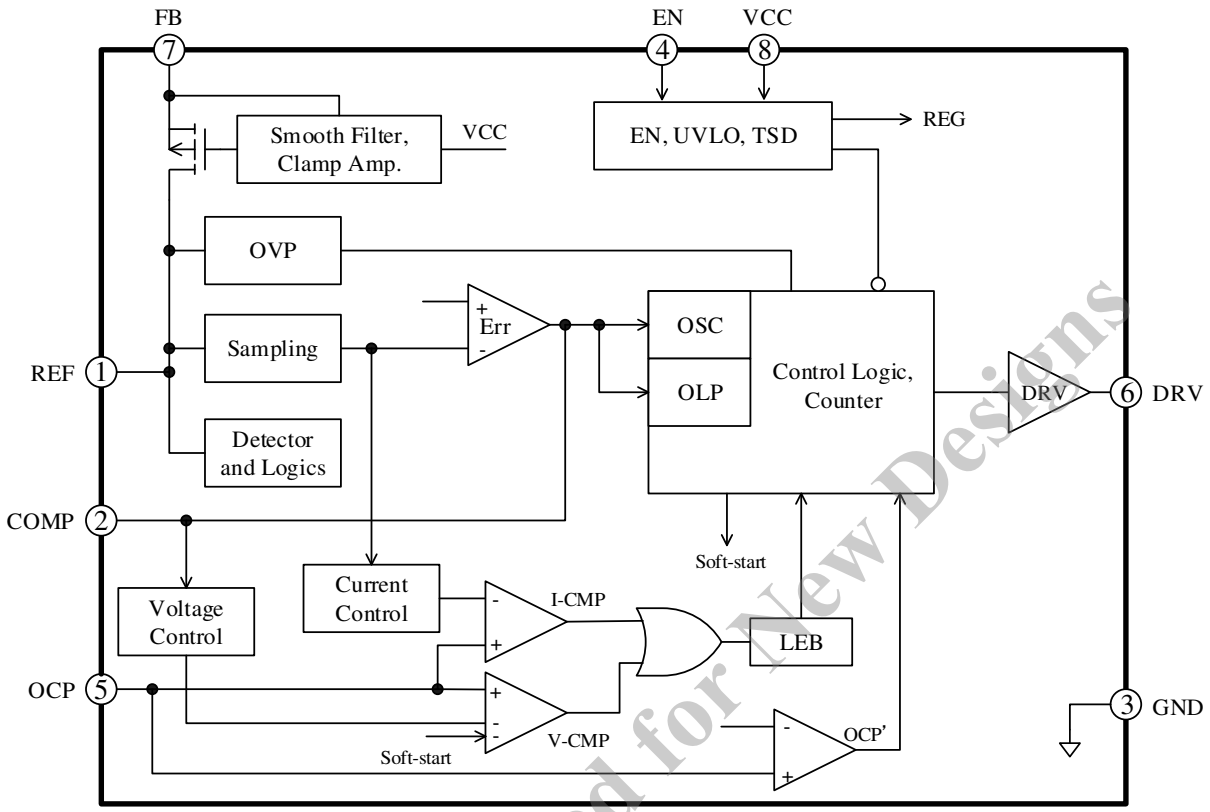
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## 4. Mechanical Characteristics

| Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Package Weight | | — | 0.084 | — | g |

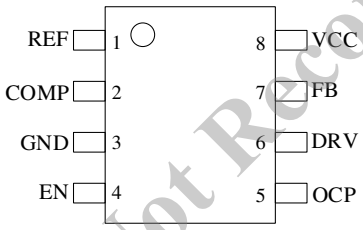

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## 5. Block Diagram




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## 6. Pin Configuration Definitions




| Pin No. | Pin Name | Description |
|---|---|---|
| 1 | REF | Output voltage setting |
| 2 | COMP | Phase compensation |
| 3 | GND | Circuit ground |
| 4 | EN | Enable signal input |
| 5 | OCP | Overcurrent signal input |
| 6 | DRV | Gate drive output |
| 7 | FB | Power MOSFET drain voltage detection |
| 8 | VCC | Power supply input |


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## 7. Typical Application

Figure 7-1 shows the circuit example using the IC. In a power supply specification such that the drain pin of external power MOSFET has large transient surge voltages, to reduce the surge voltage, add one or more of the following snubbers:

- Adding a clamp snubber circuit, which is a capacitor-resistor-diode (C7, R8, and D3) combination, on the primary winding, P.
- Adding a damper snubber circuit, which is a capacitor or a resistor-capacitor (R10 and C8) combination, between the drain and source pins of the power MOSFET.

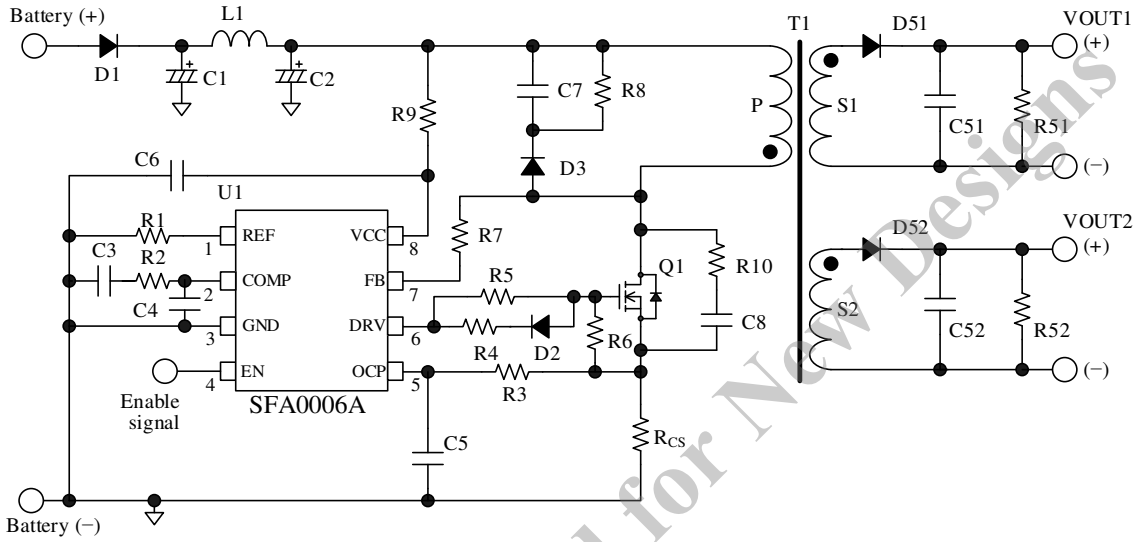


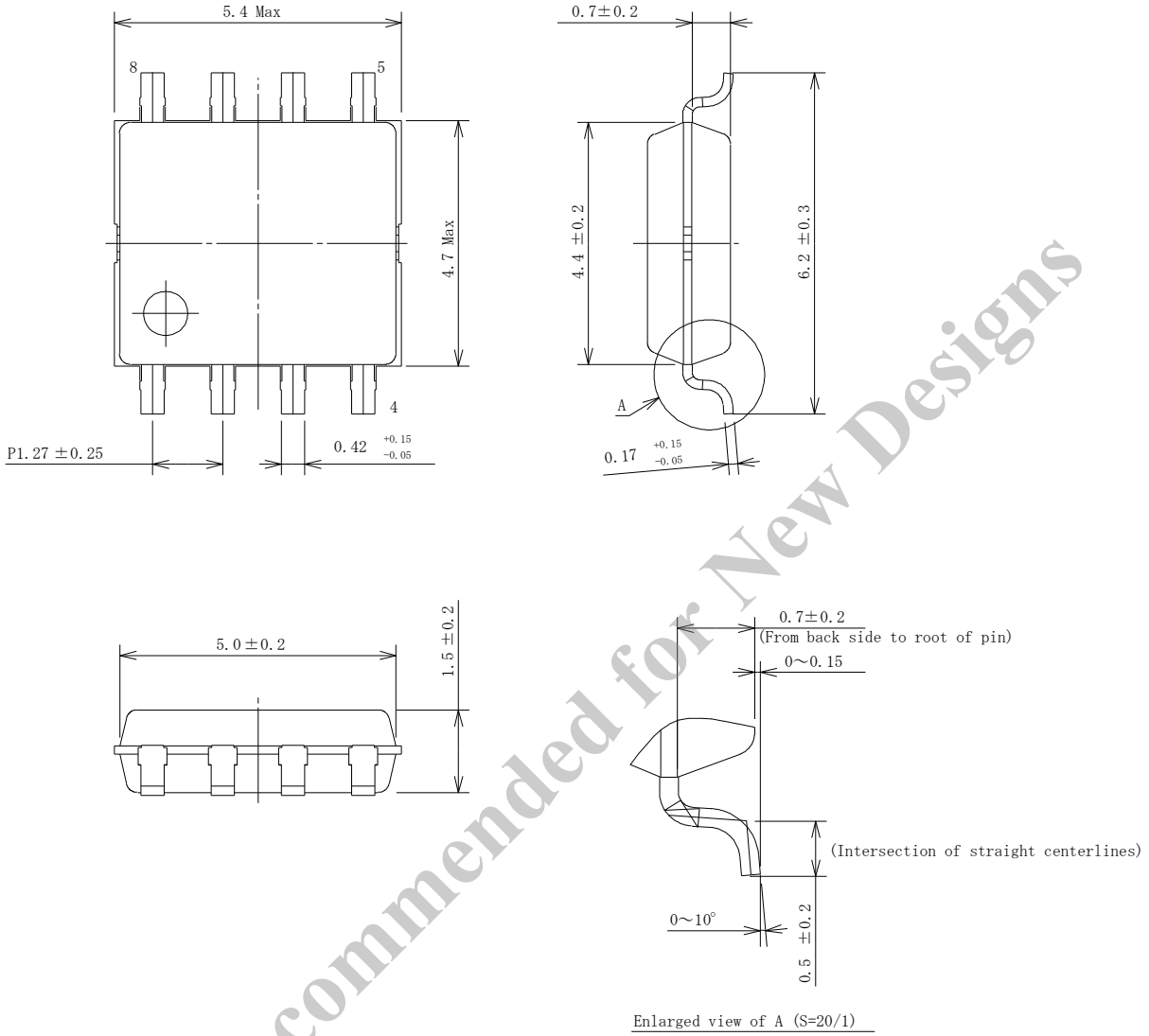

Figure 7-1. Circuit Detecting Drain Voltage

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## 8. Physical Dimensions

● **SOP8 Package**



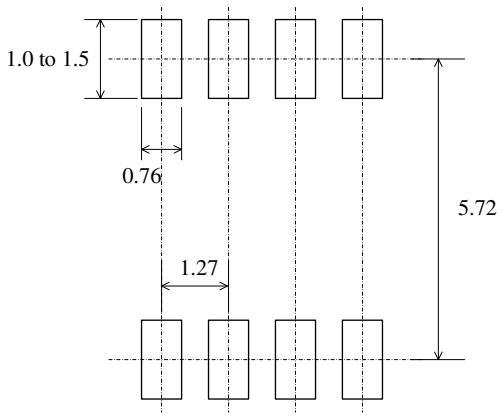

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**NOTE:**

- Dimensions in millimeters
- Bare lead frame: Pb-free (RoHS compliant)
- Reflow (MSL3)


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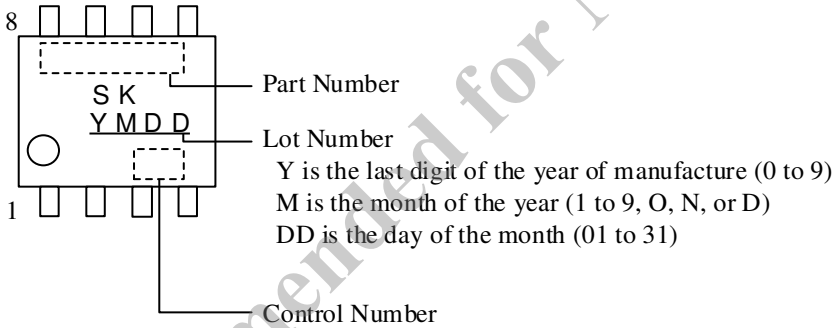
● **Land Pattern Example**




**NOTE:**

- Dimensions in millimeters

## 9. Marking Diagram




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## 10. Operational Description

All the characteristic values given in this section are typical values, unless they are specified as minimum or maximum. Current polarities are defined as follows: current going into the IC (sinking) is positive current (+); current coming out of the IC (sourcing) is negative current (−).

### 10.1. Start/Stop Operation and Enable Function

Figure 10-1 shows the internal circuit of the VCC and EN pins. Figure 10-2 shows the operational waveforms at startup.

At startup, when the VCC pin voltage increases to the Operation Start Voltage, $V_{CC(ON)}$ = 4.80 V, or more, and the EN pin voltage reaches the On Threshold Voltage, $V_{EN(ON)}$ = 1.88 V, the internal power supply (regulator) operates. When the regulator operates, the internal oscillator and the soft start function (see Section 10.2) are activated. Then, the circuit current increases as shown in Figure 10-3.

When the VCC pin voltage decreases to the Operation Stop Voltage, $V_{CC(OFF)}$ = 4.40 V, or less, the control circuit operation is stopped by the undervoltage lockout (UVLO) circuit. Then, the IC returns to the state before startup.

The IC has the enable function. When the on/off signal is input to the EN pin while the VCC pin voltage is higher than the $V_{CC(OFF)}$, the IC is activated/stopped. As shown is Figure 10-2, when the EN pin voltage reaches the On Threshold Voltage, $V_{EN(ON)}$ = 1.88 V, the IC starts the operation. When the EN pin voltage decreases to the Off Threshold Voltage, $V_{EN(OFF)}$ = 1.28 V, or less, the IC stops the operation.

When not using the enable function, the EN pin must be shorted to the VCC pin.

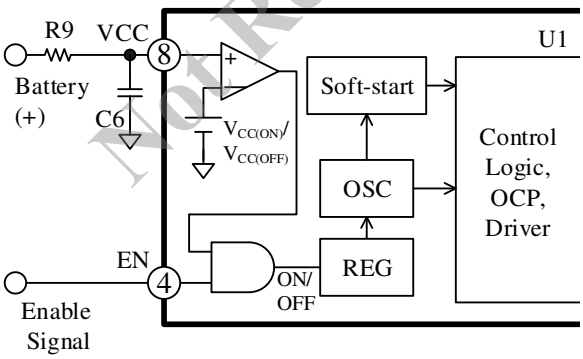



Figure 10-1. Operation Circuit of VCC and EN Pins

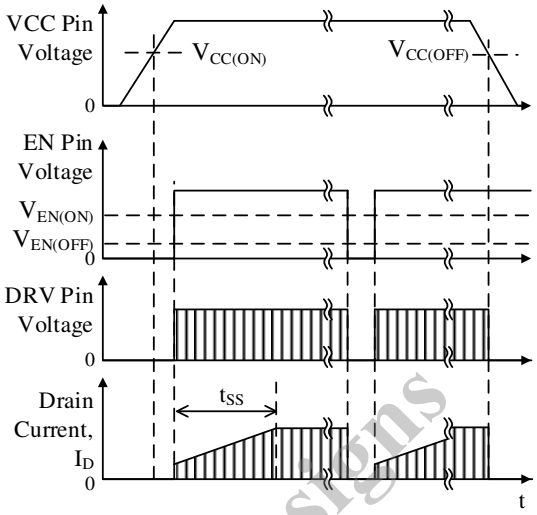



Figure 10-2. Operational Waveforms at Startup

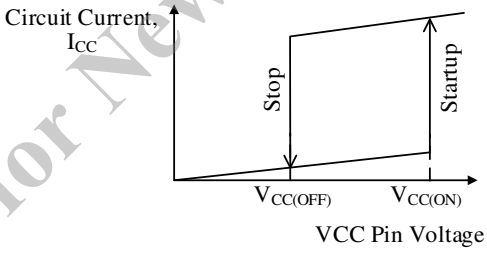



Figure 10-3. VCC Pin Voltage and Circuit Current ($V_{EN} \geq V_{EN(ON)}$)

### 10.2. Soft Start Function

The IC is activated by the soft-start operation in startup. This reduces the voltage and current stresses of the external components such as a power MOSFET and a secondary rectifier diode. In the power supply startup, when the VCC pin voltage increases to $V_{CC(ON)}$ or more, and the EN pin voltage increases to $V_{EN(ON)}$ or more, the IC starts the oscillation by the soft-start operation. Thus, the drain current gradually increases. The soft-start period, $t_{SS}$, is 13.5 ms, which is set internally in advance.

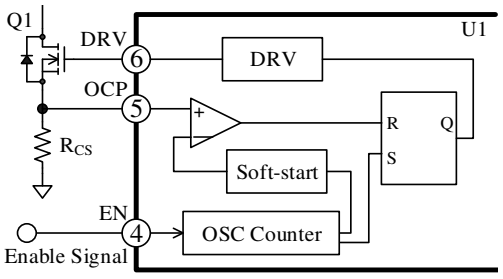



Figure 10-4. Soft-start Operation

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## 10.3. Primary-side Regulation (PSR)

The IC employs the primary-side regulation (PSR) method. In the PSR method, the primary-side winding voltage is input to the FB pin via the resistor as shown in Figure 10-5. Then, the output voltage is controlled to be constant using the FB pin voltage.

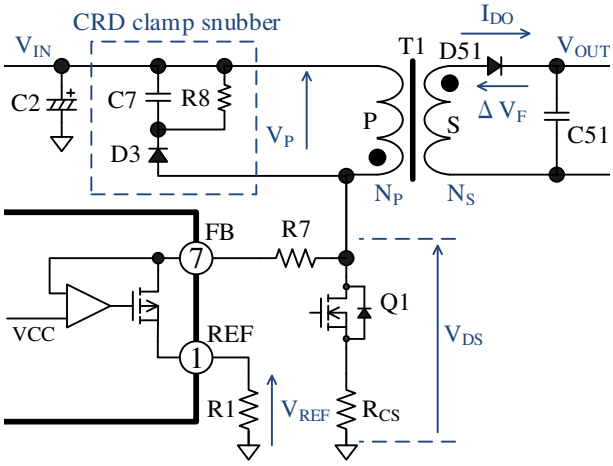



Figure 10-5. Primary-side Regulation Circuit

Figure 10-6 shows the detection timing of the drain voltage, $V_{DS}$. When the power MOSFET is turned off, the energy stored in the transformer is supplied to the secondary side, and then the current, $I_{DO}$, flows to the secondary-side rectifier diode. Even after the transformer energy is released, $V_{DS}$ oscillates freely because the power MOSFET continues to be turned off. $I_{DO}$ is 0 A during this free oscillation period.

The IC generates a feedback signal that is minimized the influence of $\Delta V_F$ of the secondary-side rectifier diode by sampling the $V_{DS}$ waveform from the point A in Figure 10-6 of the REF pin voltage, $V_{REF}$. The IC requires a sampling period of about 1.65 µs or more including $t_{MASK}$. Even in the burst operation (see Section 10.7) where the sampling period is the shortest, be sure to have a period of ≥1.65 µs from the point the VSP pin turns off to the point the REF pin voltage starts to fall (see Figure 10-6). Figure 10-6 shows an ideal $V_{DS}$ waveform. To reduce the surge voltage at turn-off, add a CRD clamp snubber circuit on the primary winding, P, as shown in Figure 10-5.

To increase the sampling accuracy, the IC has a sample delay time, $t_{MASK}$, not to respond the surge of $V_{REF}$ occurred at turning off. When the surge width exceeds $t_{MASK}$, it is required the peak and width of the surge are reduced to $t_{MASK}$ or less by adjusting C7 and R8. The rising time is affected by the values of the following resistors: R1 for the REF pin; R4 and R5 for the DRV pin.. R1, R4, and R5 must be adjusted so that the rising time can be shorter than $t_{MASK}$= 0.70 µs (min.). The rising time means the period from when the DRV pin becomes low level until when the VREF reaches its maximum voltage.

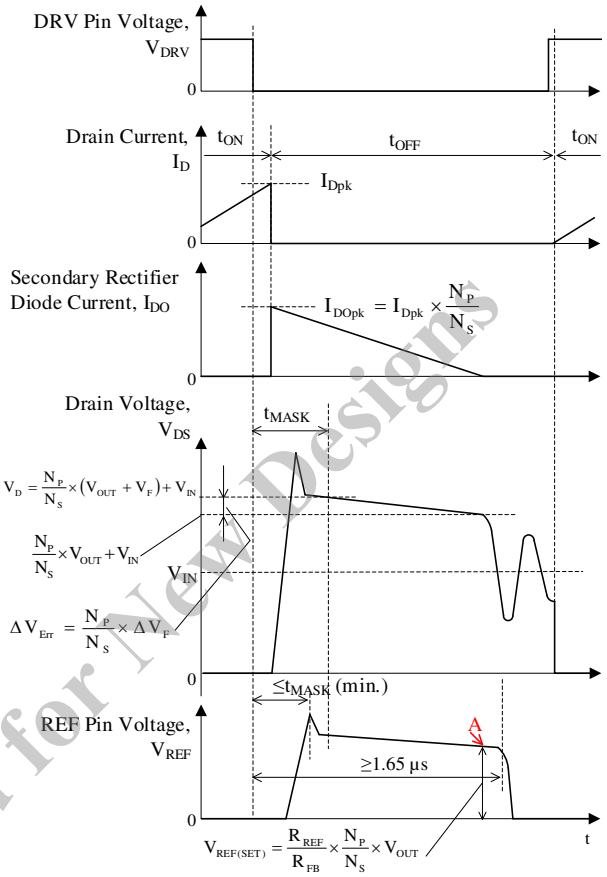



Figure 10-6. Detection Timing of Primary-side Winding Voltage

## 10.4. Constant Voltage (CV) Control

For the constant voltage (CV) control of the output voltage, the IC uses a peak current mode control that provides high speed transient response and stable operation. The IC compares $V_{RCS}$ with the internal reference voltage, $V_{KCOMP}$, by the internal comparator (OCPv's), and controls so that the peak value of $V_{RCS}$ gets close to $V_{KCOMP}$. Where, $V_{RCS}$ is the voltage across of the current detection resistor, $R_{CS}$. The REF pin voltage is generated from the FB pin voltage. $V_{KCOMP}$ is a value obtained by inverting the sampled REF pin voltage by the error amplifier (see Figure 10-7 and Figure 10-8). The following equation shows the relation between the REF pin voltage and the FB pin current:

$$V_{REF} = I_{FB} \times R_{REF} \quad (1)$$

- Light Load Operation

In a light load condition, the output voltage increases, and the sampling value of the REF pin also increases.

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Thus, $V_{KCOMP}$ decreases, and the IC controls the peak value of $V_{RCS}$ to decrease. This decreases the peak value of drain current, and prevents the output voltage increasing.

- Heavy Load Operation

In a heavy load condition, the IC performs the inverse operation to that described above, i.e., $V_{KCOMP}$ increases. This increases the peak value of drain current, and prevents the output voltage decreasing.

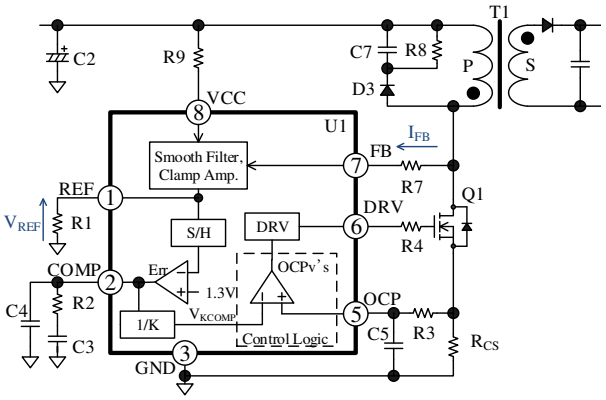



Figure 10-7. Constant Voltage Control Circuit

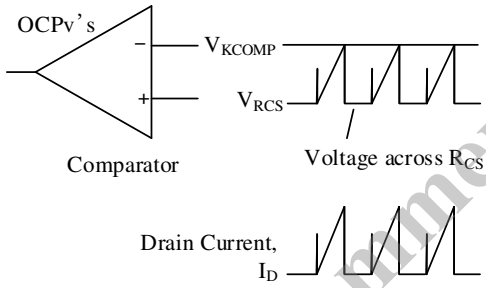



Figure 10-8. $I_D$ and OCPv's Comparator Operation in Normal Operation

When the PWM control of peak current mode operates a continuous mode, the drain current waveform becomes trapezoidal. This causes the subharmonic oscillation because the on-time varies according to the initial drain current even if the drain peak current determined by control amount (target voltage, $V_{KCOMP}$) is constant. The subharmonic oscillation is an operation in which the on-period fluctuates at an integral multiple of the switching period. To prevent this, the IC controls to suppress the subharmonic oscillation using the signal that is a target voltage, $V_{KCOMP}$, generated by adding the slope compensation signal to the OCP pin voltage signal. Occurrence of the subharmonic oscillation in out of feedback control, which is a power supply transient state such as startup, overload, and load shorted, does not affect for the IC operation.

## 10.5. Constant Current (CC) Operation

When the output current increases, the drain current of the power MOSFET is limited to the value set by the current detection resistor, $R_{CS}$. When the limited state continues for the continues for the OLP Delay Time, $t_{OLP(ON)}$ = 93.1 ms, or more, the IC switches to the constant current (CC) control from the constant voltage (CV) control. Figure 10-9 shows the CV/CC Characteristics.

When the drain current is limited due to increasing the output current, the output voltage decreases. The current is controlled to be constant by decreasing the oscillation frequency and the drain current limitation value according to the output voltage decreasing.

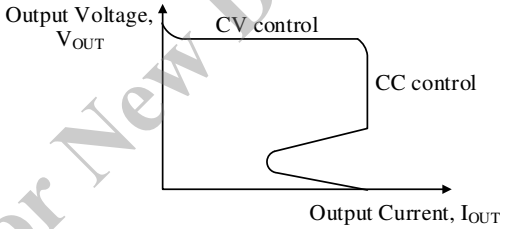



Figure 10-9. CV/CC Characteristic

## 10.6. Random Switching Function

The IC has a function to superimpose the frequency fluctuation on the PWM average oscillation frequency, $f_{OSC\ (AVG)}$. During the switching operation, the IC performs a slight fluctuation randomly to $f_{OSC\ (AVG)}$. This reduces conduction noises, and simplifies the noise filter of the input section.

## 10.7. Automatic Standby Function

The IC has the automatic standby function to improve the efficiency in a light load.

The automatic standby function of the SFA0006A switches automatically from the normal operation to the green mode or the burst oscillation mode according to the output load decreasing (see Figure 10-10). The switching loss in a light load is reduced by the green mode and the burst oscillation mode. In the green mode, the frequency gradually decreases (60.0 kHz to 20.0 kHz) according to $I_D$ decreasing. Where, $I_D$ is the drain current of the power MOSFET. In the burst oscillation mode, the IC repeats oscillation and oscillation stop as shown in Figure 10-11. The cycle of the burst oscillation operation is about 1.16 ms. The frequency during the burst oscillation is $f_{OSC(MIN)}$ = 20.0 kHz. In the burst oscillation mode, the oscillator that determines the cycle is not synchronized with the oscillator that determines

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the oscillation frequency. Therefore, the oscillation frequency may become high when switching to the burst oscillation mode.

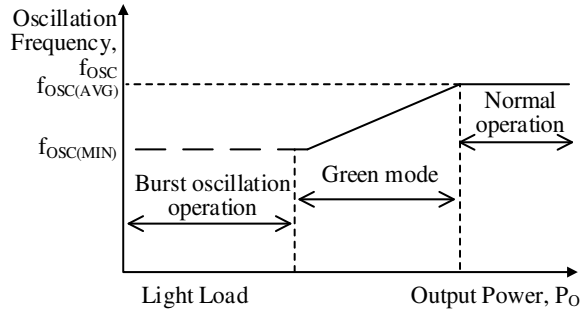



Figure 10-10. Automatic Standby Function

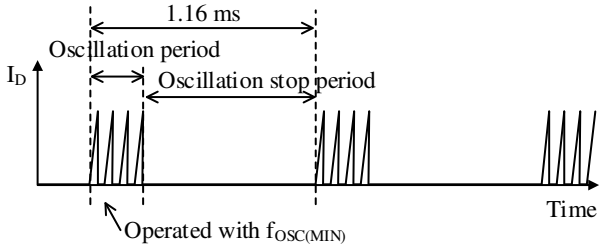



Figure 10-11. Operational Waveform of Burst Oscillation

## 10.8. Overcurrent Protection (OCP) and Overload Protection (OLP)

The overcurrent protection (OCP) controls an output power by pulse-by-pulse method. When the peak value of the drain current flowing through the external power MOSFET reaches the limitation value (OCP operating point) set by the current detection resistor, $R_{CS}$, the power MOSFET is turned off. When the OCP state continues, the COMP pin voltage increases. When the state where the COMP pin voltage exceeds the COMP Pin Overload Threshold Voltage, $V_{COMP(OLP)}$ = 2.80 V, continues for the OLP Delay Time, $t_{OLP(ON)}$ = 93.1 ms, or more, the OLP is activated. Then, the IC switches to the constant current (CC) control (see Section 10.5). When the abnormal condition is removed, the IC automatically returns to normal operation.

The OCP has the leading edge blanking function and the input compensation function. These details are described in Section 10.8.1 and 10.8.2, respectively.

### 10.8.1. Leading Edge Blanking Function

The IC uses a peak-current-mode control method for controlling the output voltage to be constant. In this control method, the overcurrent protection circuit responds to a steep surge generated when the power MOSFET is turned on, and then the power MOSFET may be turned off. To prevent this, the IC has the Leading Edge Blanking Time, $t_{LEB}$ = 300 ns, not to respond the drain current surge occurred at turning on..

### 10.8.2. Input Compensation Function

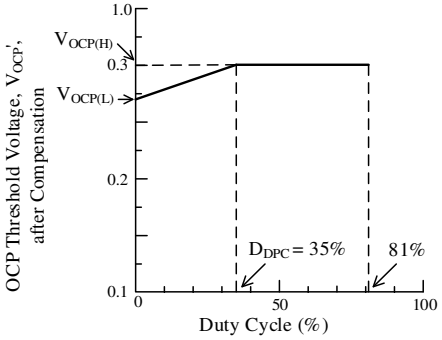
The input compensation function is a function that adjusts the OCP operating point according to input voltages. The control system circuits of a general PWM control IC have propagation delays; therefore, the higher an input voltage increases, the steeper the slope of a drain current becomes. This causes an actual drain peak current to be larger than the peak current at the OCP operating point. To reduce such peak current variation, the input compensation function works as follows: a compensation signal having a constant slope, shown in Figure 10-12, is superimposed on a detection signal of the drain current inside the IC. As a result, the internal threshold voltage is adjusted.

To reduce the difference between an OCP threshold voltage when an input voltage is high (i.e., the duty cycle is small) and it when an input voltage is low (i.e., the duty cycle is large), an OCP threshold voltage is compensated so that it becomes high when an input voltage is low (see Figure 10-12).

The amount of the compensation signal depends on the duty cycle. The OCP threshold voltage, $V_{OCP}$', after compensation corresponding to the duty cycle is calculated by the following equation. Note that $V_{OCP}$' becomes constant when the duty cycle, $D_{DPC}$, is 35% or more.

$$V_{OCP}{}' = \frac{V_{OCP(H)} - V_{OCP(L)}}{D_{DPC}} \times \text{Duty} + V_{OCP(L)} \qquad (2)$$

Where:
$V_{OCP(H)}$ is the OCP Threshold Voltage at 35% Duty Cycle (300 mV),
$V_{OCP(L)}$ is the OCP Threshold Voltage at Zero Duty Cycle (270 mV),
$D_{DPC}$ is the OCP Compensation Duty Cycle (35%), and
Duty is a duty cycle (%).




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Figure 10-12. Duty Cycle and Current Limit Threshold Voltage Value

## 10.9. Overvoltage Protection (OVP)

The IC has the REF pin overvoltage protection (OVP). When the REF pin voltage reaches the Overvoltage Threshold Voltage, $V_{REF(OVP)}$ = 1.90 V, the OVP is activated, and then the switching operation is stopped. After $t_{OLP(OFF)}$ = 1.730 s from activating the OVP, the IC automatically restarts the oscillation.

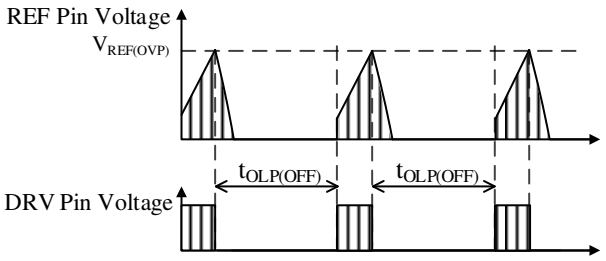



Figure 10-13. OVP Operational Waveforms

## 10.10.FB Pin Open Protection

The IC has the FB pin open protection. When traces connected to the FB pin become open for some reason, and this state continues for the period when the DRV pin outputs the high signal 3 times, this function is activated. Then, the switching operation is stopped. After $t_{OLP(OFF)}$ = 1.730 s from stopping the switching operation, the IC automatically restarts the oscillation.

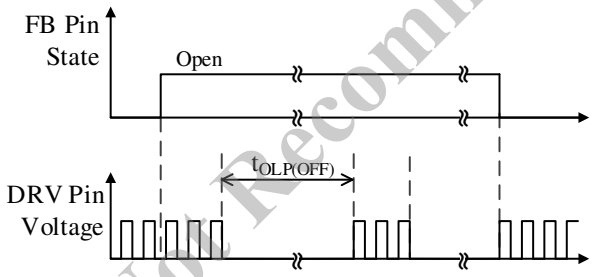



Figure 10-14. FB Pin Open Protection

## 10.11.Thermal Shutdown (TSD)

The IC has the thermal shutdown (TSD) circuit with hysteresis. When the junction temperature of the IC reaches the TSD Operating Temperature, $T_{TSD}$ = 165 °C, the TSD is activated. Then, the switching operation is stopped. When the junction temperature decreases to $T_{TSD} - T_{TSD(HYS)}$ or less, the IC is activated again.

# 11. Design Notes

## 11.1. External Components

Components fit for the use condition should be used.

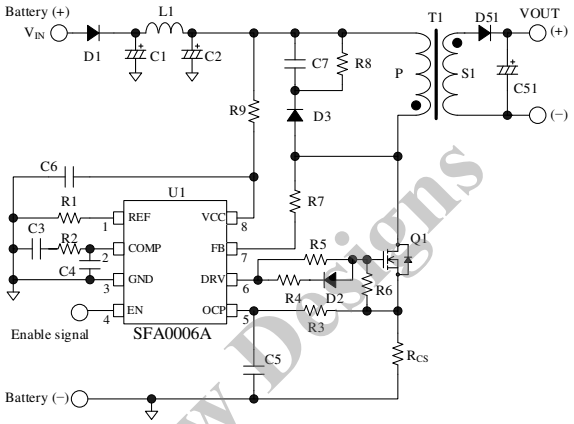



Figure 11-1. Peripheral Circuit of IC

### 11.1.1. Input/Output Smoothing Electrolytic Capacitor

For input/output smoothing electrolytic capacitor, it is required to apply the proper derating to ripple current, voltage, and temperature rising. To reduce the ripple voltage of the output electrolytic capacitor, it is recommended to use the low ESR type suitable for switching power supply.

### 11.1.2. VCC Pin Peripheral Circuit

The resistor, R9, and the capacitor, C6, in Figure 11-1 are for the noise reduction. R9 value is 1 Ω to 10 Ω or less. C6 value is 0.01 μF to 0.1 μF. Adjust R9 and C6 so that the voltage fluctuation time of the VCC pin voltage is ≤ 3 V/μs under all operating conditions including power startup and shutdown.

### 11.1.3. FB and REF Pins Peripheral Circuit

The rising time is affected by the values of the following resistors: R1 for the REF pin; R4 and R5 for the DRV pin. Therefore, R1, R4, and R5 must be adjusted so that the rising time can be shorter than $t_{MASK}$ = 0.70 μs (min.). The rising time means the period from when the DRV pin becomes low level until when the REF pin reaches its maximum voltage (see Figure 11-2). For sampling the REF pin voltage, a sampling period of about 1.65 μs or more is required after the

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DRV pin becomes low level. R1 value is 2.7 kΩ to 3.9 kΩ.

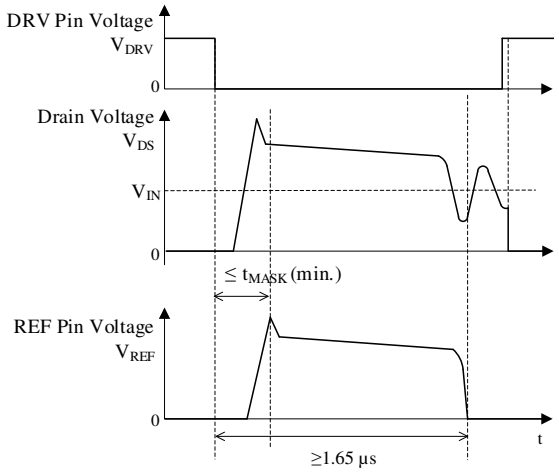



Figure 11-2. REF Pin Voltage

### 11.1.4. COMP Pin Peripheral Circuit

Figure 11-3 shows the COMP pin peripheral circuit.

The capacitors (C3 and C4) and the resistor (R2) between the COMP and GND pins are for high-frequency noise reduction and phase compensation. These components should be connected to the COMP and GND pins with a minimal length of traces. C4 is about 1000 pF to 1500 pF. C3 is about 0.01 µF. R2 is about 220 kΩ to 820 kΩ.

Be sure to confirm the actual operation in the application, and adjust these values. Also, care should be taken in measuring the waveform with oscilloscope because the internal impedance of the COMP pin is high. Especially in a light load, connecting the probe directly to the COMP pin may affect the control. Therefore, when measuring the waveform, connect the voltage follower (buffer) circuit composed of an operational amplifier with high impedance to the COMP pin as shown in Figure 11-3.

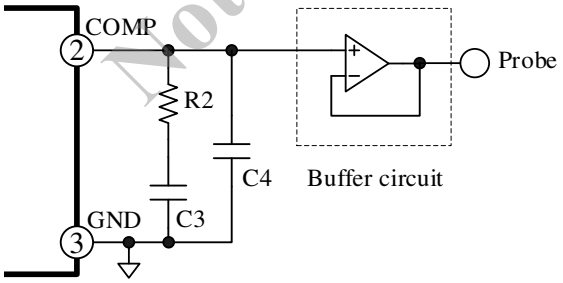



Figure 11-3. Measuring Waveform of COMP Pin

### 11.1.5. OCP Pin Peripheral Circuit

The OCP pin detects the drain current flowing through the external power MOSFET with the resistor, $R_{CS}$. C5 and R3 are the filter circuits for noise reduction when turning on the power MOSFET. Set R3 to 50 Ω or less, and adjust C5.

The components between the OCP and GND pins should be connected with a minimal length of trace. The trace should be as small loop as possible.

### 11.1.6. DRV Pin Peripheral Circuit

The DRV pin is the gate drive pin for an external power MOSFET. The characteristics of the DRV pin are as follows: the output voltage, $V_{DRV}$ = 8.0 V; the peak source current, $I_{DRV(SO)}$ = −270 mA; and the peak sink current, $I_{DRV(SI)}$ = 540 mA. Select the power MOSFET whose gate threshold voltage, $V_{GS(th)}$, is sufficiently smaller than $V_{DRV}$ over the entire operating temperature range.

The internal resistance of the DRV pin is as follows: $R_{DRV(SO)}$ = 5.0 Ω for source side, and $R_{DRV(SI)}$ = 4.5 Ω for sink side.

For R4, R5, and D2 in Figure 11-1, confirm the power MOSFET loss, the gate waveform (e.g., ringing reduction by traces), and the EMI noise, based on the actual operation in the application, and adjust these values. R6 is for preventing the malfunctions due to steep dv/dt at turn-off the power MOSFET. R6 (the reference value is 10 kΩ to 100 kΩ) should be connected close to the gate and source pins of the power MOSFET.

Also, when the input voltage, $V_{IN}$, steeply rises from the state where no voltage is applied to the VCC pin, the gate voltage rises due to the parasitic capacitance between the drain and the gate of the external power MOSFET. Then, the power MOSFET may be turned on. To avoid this event, an internal circuit that clamps the gate voltage to less than 1 V (maximum current is 5 mA) is connected to the DRV pin. Therefore, the sink resistor, $R_{G(SI)}$, connected to the power MOSFET gate should be set to satisfy the following equation:

$$R_{G(SI)} < \frac{V_{TH} - (1\ V + V_F)}{5\ mA} \quad (3)$$

Where:

$R_{G(SI)}$ is the sink resistor value,

$$R_{G(SI)} = \frac{R4 \times R5}{R4 + R5}$$

$V_{TH}$ is the maximum value of the power MOSFET threshold voltage, and

$V_F$ is the forward voltage of D2.

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## 11.2. PCB Layout

Figure 11-4 shows the peripheral circuit example around the IC. The switching power supply circuit includes high frequency and high voltage current paths that affect the IC operation, noise interference, and power dissipation. Therefore, the trace layouts and component placements on the PCB play an important role in circuit designing. High frequency and high voltage current loops must be as small as possible with wide trace in order to maintain a low-impedance state. In addition, ground traces should be as wide and short as possible so that the radiated EMI levels can be reduced.

In addition, the following contents should be taken into account in the design of PCB trace layout.

1) Main Circuit

This is the main traces flowing switching current, and thus it should be as wide trace and small loop as possible.

2) Control Ground

Since the operation of the IC may be affected from the large current of the main trace that flows in control ground traces, the control ground traces should be separated from main traces, and connected at a single point as close to the GND pin as possible.

3) VCC Pin

Since the traces are for supplying power to the IC, the traces should be as small loop as possible. The capacitor, C6, should be connected near the VCC pin and the GND pin.

4) Peripheral Components of the IC

The control components connected to the IC should be placed near the IC, and connected to the corresponding pin of the IC with a minimal length of traces.

5) Secondary Rectifier Smoothing Circuit

This is the main traces flowing switching currents, and thus it should be as wide trace and small loop as possible.

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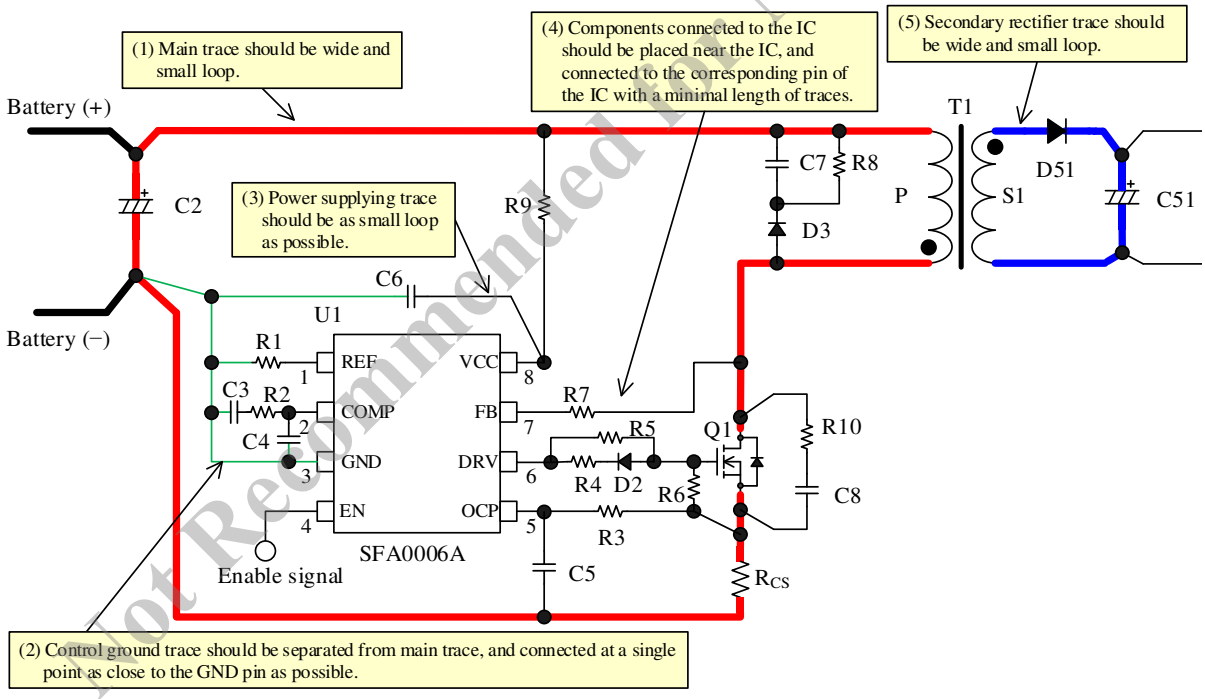



Figure 11-4. Peripheral Circuit Example around IC


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