FINAL DATA SHEET

Si5397/Si5396: Dual/Quad DSPLL® Any-Frequency, Any-Output Jitter Attenuators

The Si5397 is a high-performance, 8-output jitter-attenuating clock multiplier which integrates four any-frequency DSPLLs for applications that require maximum integration and independent timing paths. The Si5396 is a dual DSPLL version with either four or twelve outputs. Each DSPLL has access to any of the four inputs and can provide low jitter clocks on any of the device outputs. Device grades J/K/L/M have an integrated reference to save board space, improve system reliability and reduces the effect of acoustic emissions noise caused by temperature ramps. Grades A/B/C/D use an external crystal (XTAL) or crystal oscillator (XO) reference.

Based on 4th generation DSPLL technology, these devices provide any-frequency con- version with typical jitter performance of 95 fs. Each DSPLL supports independent free-run, holdover modes of operation, as well as automatic and hitless input clock switching. The Si5397/96 is programmable via a serial interface with in-circuit programmable non-volatile memory so that it always powers up in a known configuration.

Programming the Si5397/Si5396 is easy with Skyworks ClockBuilder Pro™ software. Factory pre-programmed devices are also available.

Applications

- OTN muxponders and transponders
- 10/40/100/400GbE
- Synchronous Ethernet (ITU-T G.8262)
- 10/25/100G Carrier Ethernet switches
- Broadcast video

Key Features

- Each DSPLL generates any output frequency from any input frequency
- Four or two DSPLLs to synchronize to multiple time domains
- Ultra-low phase jitter of 95 fs rms
- Enhanced hitless switching minimizes output phase transients
- Input frequency range:
  - Differential: 8 kHz to 750 MHz
  - LVCMOS: 8 kHz to 250 MHz
- Output frequency range:
  - Differential: 100 Hz to 720 MHz
  - LVCMOS: 100 Hz 250 MHz
- Status Monitoring
- Si5397: 4-PLL, 8/4 output, 64-QFN/LGA
- Si5396: 2-PLL, 4 output, 44-QFN/LGA and 12 output, 64-QFN/LGA
- External reference: Grades A/B/C/D
- Integrated reference: Grades J/K/L/M
- Drop-in compatible with Si5347/46
- For RoHS and other product compliance information, see the Skyworks Certificate of Conformance.

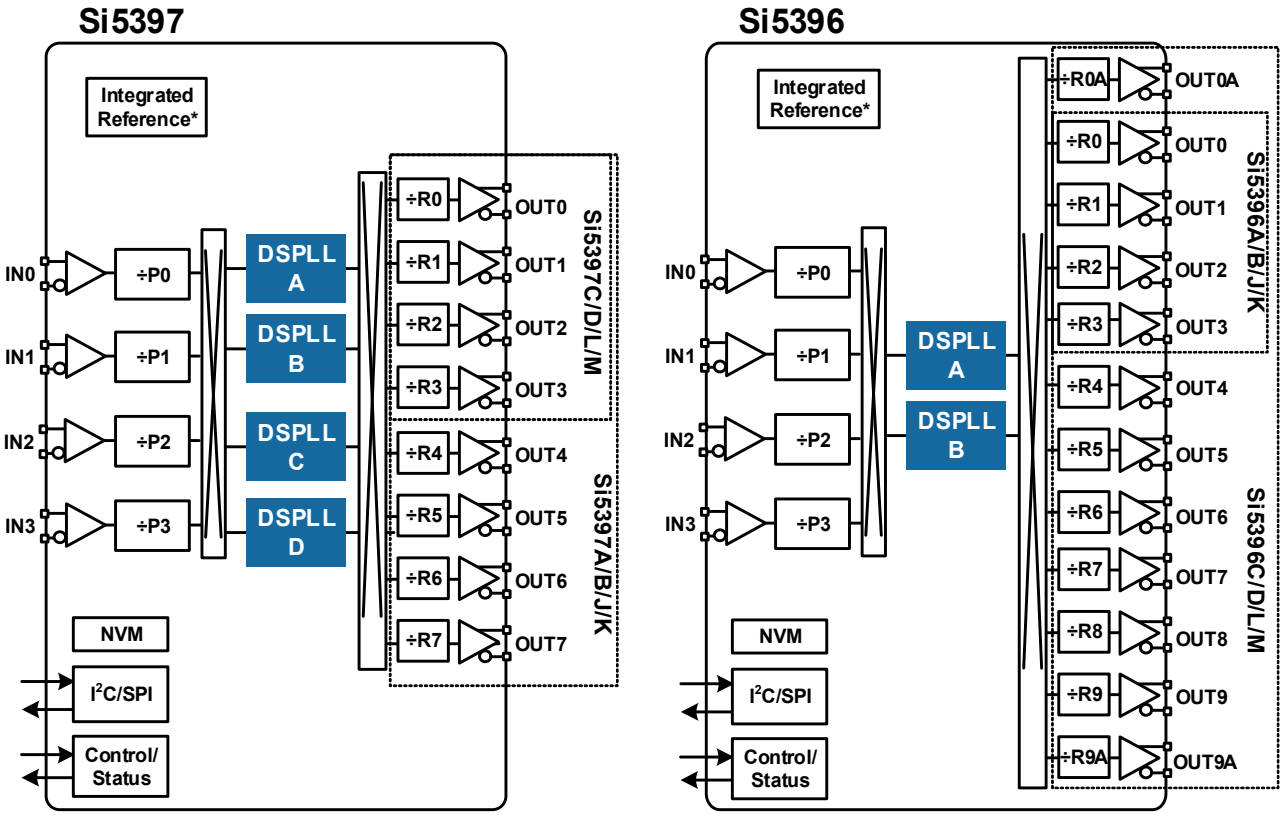


Figure 1. Si5397/Si5396

1. Feature List

The Si5397/Si5396 features are listed below:

- Generates any output frequency in any format from any input frequency
- External XTAL or XO reference (A/B/C/D)
- Integrated reference (J/K/L/M)
- Ultra-low phase jitter of 95 fs rms
- Four or two DSPLLs to synchronize to multiple inputs
- Input frequency range:
  - Differential: 8 kHz to 750 MHz
  - LVCMOS: 8 kHz to 250 MHz
- Output frequency range:
  - Differential: up to 720 MHz
  - LVCMOS: up to 250 MHz
- Flexible crosspoints route any input to any output clock
- Programmable jitter attenuation bandwidth per DSPLL: 0.1 Hz to 4 kHz
- Highly configurable outputs compatible with LVDS, LVPECL, LVCMOS, CML, and HCSL with programmable signal amplitude
- Status monitoring (LOS, OOF, LOL)
- Enhanced hitless switching minimizes output phase transients for 8 kHz, 19.44 MHz, 25 MHz, and other input frequencies
- Drop-in compatible with Si5347/46
- Locks to gapped clock inputs
- Automatic free-run and holdover modes
- Fastlock feature for low nominal bandwidths
- Independent Frequency-on-the-fly for each DSPLL
- DCO mode: as low as 0.01 ppb steps per DSPLL
- Core voltage:
  - VDD: 1.8 V ±5%
  - VDDA: 3.3 V ±5%
- Independent output clock supply pins: 3.3, 2.5, or 1.8 V
- Serial interface: I2C or SPI
- In-circuit programmable with non-volatile OTP memory
- ClockBuilder™ Pro software tool simplifies device configuration
- Si5397 (4-PLL): 4 input, 8 output
  - Grade A/B: 64-QFN 9×9 mm
  - Grade J/K: 64-LGA 9x9 mm
- Si5397 (4-PLL): 4 input, 4 output
  - Grade C/D: 64-QFN 9×9 mm
  - Grade L/M: 64-LGA 9x9 mm
- Si5396 (2-PLL): 4 input, 4 output
  - Grade A/B: 44-QFN 7×7 mm
  - Grade J/K: 44-LGA 7x7 mm
- Si5396 (2-PLL): 4 input, 12 output
  - Grade C/D: 64-QFN 9×9 mm
  - Grade L/M: 64-LGA 9x9 mm
- Temperature range: –40 to +85 °C
- Pb-free, RoHS-6 compliant

2. Related Documents

Table 1. Related Documentation and Software

Document / Resource	Web Address URL
Si5397/96 Family Reference Manual	https://www.skyworksinc.com/-/media/Skyworks/SL/documents/public/reference-manuals/si5397-96-family.pdf The reference manual is intended to be used in conjunction with this data sheet, which contains more detailed explanations about the operation of the device.
Crystal Reference Manual (Grades A/B/C/D only)	https://www.skyworksinc.com/-/media/Skyworks/SL/documents/public/reference-manuals/si534x-8x-9x-recommended-crystals-rm.pdf
UG336: Si5396 Evaluation Board User's Guide	https://www.skyworksinc.com/-/media/Skyworks/SL/documents/public/user-guides/ug336-si5396-evb.pdf
UG353: Si5397 Evaluation Board User's Guide	https://www.skyworksinc.com/-/media/Skyworks/SL/documents/public/user-guides/ug353-si5397evb.pdf
AN1151: Using the Si539x in 56G SerDes Applications	https://www.skyworksinc.com/-/media/Skyworks/SL/documents/public/application-notes/an1151-using-si539x.pdf
AN1155: Differences between Si5342-47 and Si5392-97	https://www.skyworksinc.com/-/media/SkyWorks/SL/documents/public/application-notes/an1155-differences-between-si5342-47-and-si5392-97.pdf
AN1178: Frequency-On-the-Fly for Skyworks Jitter Attenuators and Clock Generators	https://www.skyworksinc.com/-/media/Skyworks/SL/documents/public/application-notes/an1178-frequency-otf-jitter-atten-clock-gen.pdf
Quality and Reliability	https://www.skyworksinc.com/Quality
Development Kits	https://www.skyworksinc.com/en/Products/Timing
ClockBuilder Pro (CBPro) Software	https://www.skyworksinc.com/en/Application-Pages/Clockbuilder-Pro-Software

3. Ordering Guides

Table 2. Si5397/Si5396 A/B/C/D Ordering Guide
(External Reference)

Ordering Part Number (OPN)	Number of DSPLLs	Number of Input/ Output Clocks	Output Clock Frequency Range	Package	Reference
Si5397					
Si5397A-A-GM[1,2]	4	4/8	0.0001 to 720 MHz	64-QFN 9 × 9 mm	External
Si5397B-A-GM[1,2]			0.0001 to 350 MHz		
Si5397C-A-GM[1,2]		4/4	0.0001 to 720 MHz		
Si5397D-A-GM[1,2]			0.0001 to 350 MHz		
Si5397A-A-EVB	—	8-Output	—	Evaluation Board	
Si5396					
Si5396A-A-GM[1,2]	2	4/4	0.0001 to 720 MHz	44-QFN 7 × 7 mm	External
Si5396B-A-GM[1,2]			0.0001 to 350 MHz		
Si5396C-A-GM[1,2]	2	4/12	0.0001 to 720 MHz	64-QFN 9 × 9 mm	
Si5396D-A-GM[1,2]			0.0001 to 350 MHz		
Si5396C-A-EVB	—		—	Evaluation Board	

1. Add an R at the end of the OPN to denote tape and reel ordering options.
2. Custom, factory preprogrammed devices are available. Ordering part numbers are assigned by Skyworks and the ClockBuilder Pro software utility. Custom part number format is “Si5397A-Axxxxx-GM" or “Si5396A-Axxxxx-GM" where "xxxxx" is a unique numerical sequence representing the preprogrammed configuration.

Table 3. Si5397/Si5396 J/K/L/M Ordering Guide
(Integrated Reference)

Ordering Part Number (OPN)	Number of DSPLLs	Number of Input/ Output Clocks	Output Clock Frequency Range	Package	Reference
Si5397					
Si5397J-A-GM[1,2]	4	4/8	0.0001 to 720 MHz	64-LGA 9 x 9 mm	Internal
Si5397K-A-GM[1,2]			0.0001 to 350 MHz		
Si5397L-A-GM[1,2]		4/4	0.0001 to 720 MHz		
Si5397M-A-GM[1,2]			0.0001 to 350 MHz		
Si5397J-A-EVB	—	8-Output	—	Evaluation Board	
Si5396					
Si5396J-A-GM[1,2]	2	4/4	0.0001 to 720 MHz	44-LGA 7 × 7 mm	Internal
Si5396K-A-GM[1,2]			0.0001 to 350 MHz		
Si5396J-A-EVB	—			Evaluation Board	
Si5396L-A-GM[1,2]	2	4/12	0.0001 to 720 MHz	64-LGA 9 × 9 mm	
Si5396M-A-GM[1,2]			0.0001 to 350 MHz		
Si5396L-A-EVB	—		—	Evaluation Board	

1. Add an R at the end of the OPN to denote tape and reel ordering options.
2. Custom, factory preprogrammed devices are available. Ordering part numbers are assigned by Skyworks and the ClockBuilder Pro software utility. Custom part number format is “Si5397A-Axxxxx-GM" or “Si5396A-Axxxxx-GM" where "xxxxx" is a unique numerical sequence representing the preprogrammed configuration.

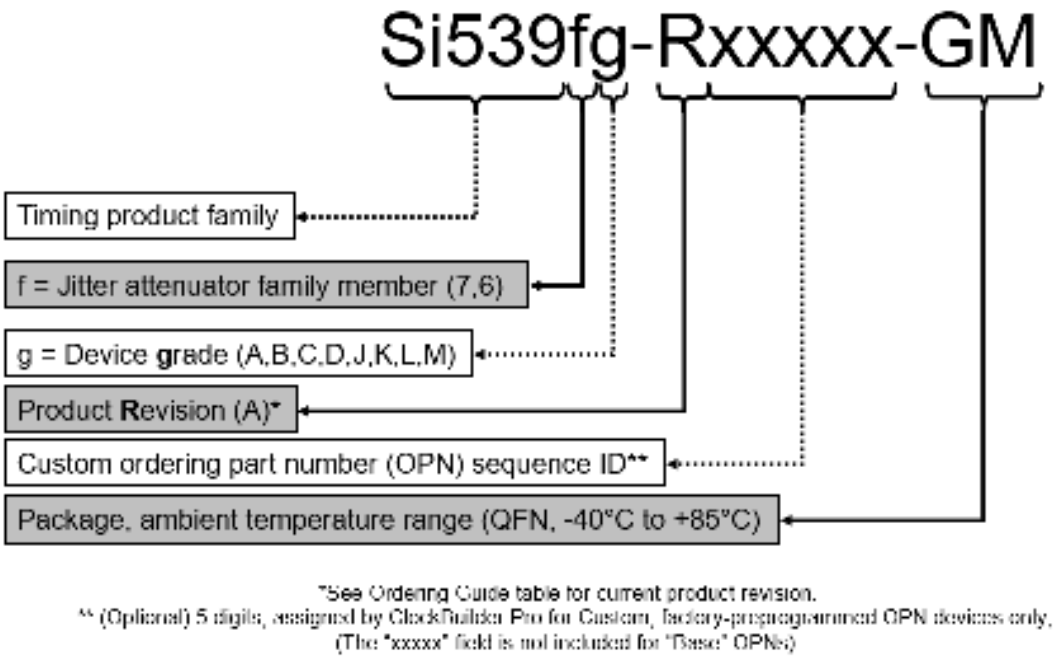


Figure 2. Ordering Part Number Fields

4. Functional Description

The Si5397/Si5396 multi-PLL Jitter attenuators take advantage of Skyworks 4th generation DSPLL technology to offer the industry's most integrated and flexible jitter attenuating clock generator solution. Each of the DSPLLs operate independently from each other and are controlled through a common serial interface. Each DSPLL has access to any of the four inputs (IN0 to IN3) with manual or automatic input selection. The Si5397 has 4-DSPLLs and has either 4 or 8 outputs while the Si5396 has 2-DSPLLs and comes with either 4 or 12 outputs. Any of the output clocks can be configured to any of the DSPLLs using a flexible crosspoint connection.

4.1. Frequency Configuration

The frequency configuration for each of the DSPLLs is programmable through the serial interface and can also be stored in non-volatile memory. The combination of fractional input dividers (Pn/Pd), fractional frequency multiplication (Mn/Md), and integer output division (Rn) allows each of the DSPLLs to lock to any input frequency and generate virtually any output frequency. All divider values for a specific frequency plan are easily determined using the ClockBuilder Pro utility.

4.2. DSPLL Loop Bandwidth

The DSPLL loop bandwidth determines the amount of input clock jitter attenuation. Register-configurable DSPLL loop bandwidth settings in the range of 0.1 Hz to 4 kHz are available for selection for each of the DSPLLs. Since the loop bandwidth is controlled digitally, each of the DSPLLs will always remain stable with less than 0.1 dB of peaking regardless of the loop bandwidth selection.

4.3. Fastlock Feature

Selecting a low DSPLL loop bandwidth (e.g. 0.1 Hz) will generally lengthen the lock acquisition time. The fastlock feature allows setting a temporary Fastlock Loop Bandwidth that is used during the lock acquisition process. Higher fastlock loop bandwidth settings will enable the DSPLLs to lock faster. Fastlock Loop Bandwidth settings in the range of 100 Hz to 4 kHz are available for selection. The DSPLL will revert to its normal loop bandwidth once lock acquisition has completed.

4.4. Modes of Operation

Once initialization is complete, each of the DSPLLs operates independently in one of four modes: Free-run Mode, Lock Acquisition Mode, Locked Mode, or Holdover Mode. A state diagram showing the modes of operation is shown in the figure below. The following sections describe each of these modes in greater detail.

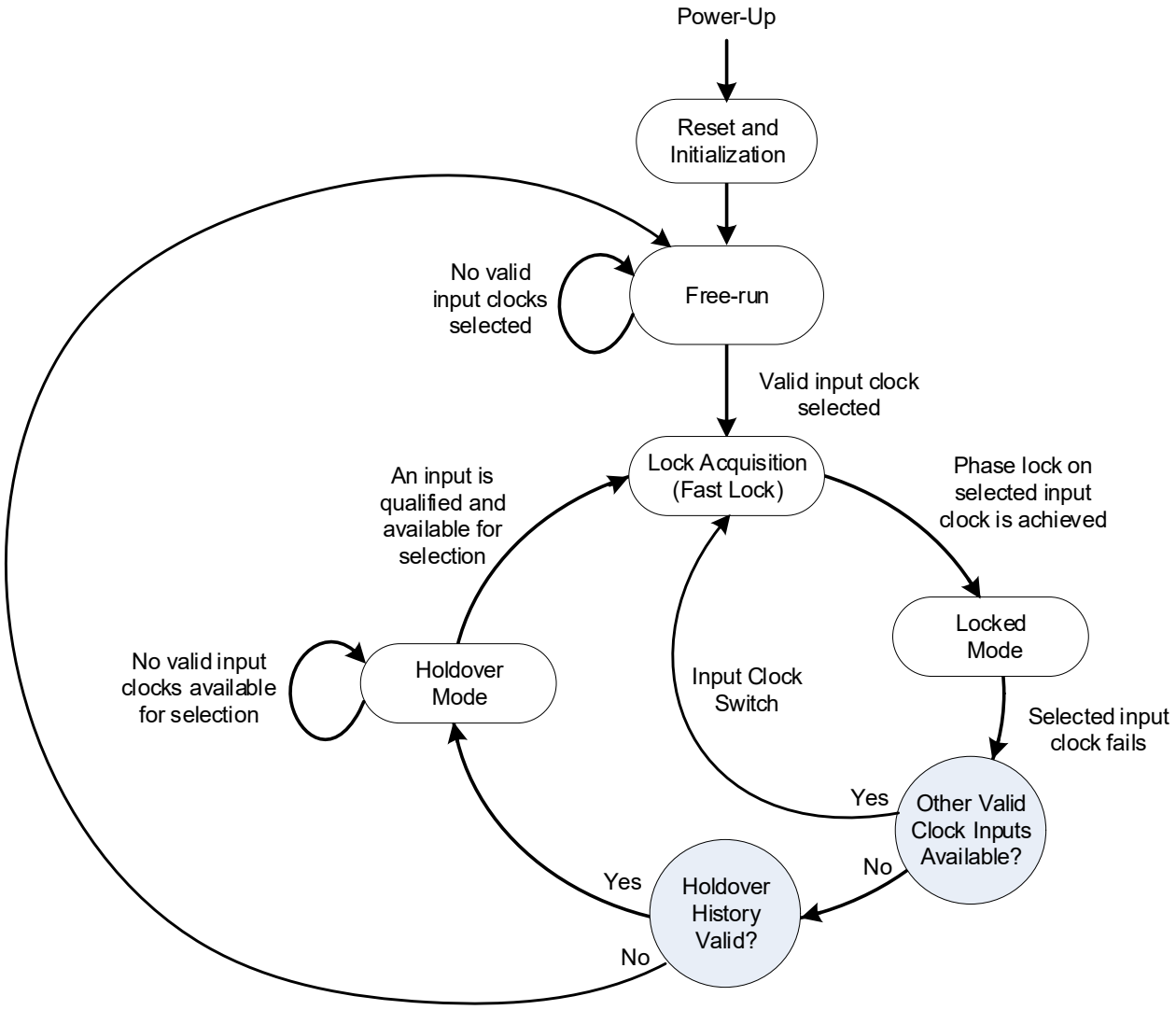


Figure 3. Modes of Operation

4.4.1. Initialization and Reset

Once power is applied, the device begins an initialization period where it downloads default register values and configuration data from NVM and performs other initialization tasks. Communicating with the device through the serial interface is possible once this initialization period is complete. No clocks will be generated until the initialization is complete.

Clocks that feature the integrated crystal may require a slightly longer settling time compared to the external crystal device. See the Reference Manual for more details.

There are two types of resets available. A hard reset is functionally similar to a device power-up. All registers will be restored to the values stored in NVM, and all circuits including the serial interface will be restored to their initial state. A hard reset is initiated using the RSTb pin or by asserting the hard reset register bit.

A soft reset bypasses the NVM download. It is simply used to initiate register configuration changes.

4.4.2. Freerun Mode

All four DSPLLs will automatically enter freerun mode once power is applied to the device and initialization is complete. The frequency accuracy of the generated output clocks in freerun mode is entirely dependent on the frequency accuracy of the external crystal or reference clock on the XA/XB pins. For example, if the crystal frequency is ±100 ppm, then all the output clocks will be generated at their configured frequency ±100 ppm in freerun mode. Any drift of the crystal frequency will be tracked at the output clock frequencies. A TCXO or OCXO is recommended for applications that need better frequency accuracy and stability while in freerun mode or holdover mode.

4.4.3. Lock Acquisition Mode

Each of the DSPLLs independently monitors its configured inputs for a valid clock. If at least one valid clock is available for synchronization, a DSPLL will automatically start the lock acquisition process.

If the fast lock feature is enabled, a DSPLL will acquire lock using the fastlock loop bandwidth setting and then transition to the DSPLL Loop Bandwidth setting when lock acquisition is complete. During lock acquisition the outputs will generate a clock that follows the VCO frequency change as it pulls-in to the input clock frequency.

4.4.4. Locked Mode

Once locked, the DSPLL will generate output clocks that are both frequency and phase locked to their selected input clocks. At this point, any XTAL frequency drift will not affect the output frequency. A loss of lock pin (LOL) and status bit indicate when lock is achieved. See 4.8.4. LOL Detection for more details on the operation of the loss-of-lock circuit.

4.4.5. Holdover Mode

Each of the DSPLLs will automatically enter holdover mode when the selected input clock becomes invalid and no other valid input clocks are available for selection. The DSPLLs use an averaged input clock frequency as its final holdover frequency to minimize the disturbance of the output clock phase and frequency when an input clock suddenly fails. The holdover circuit for the DSPLL stores up to 120 seconds of historical frequency data while locked to a valid clock input. The final averaged holdover frequency value is calculated from a programmable window within the stored historical frequency data. Both the window size and the delay are programmable as shown in the figure below. The window size determines the amount of holdover frequency averaging. The delay value allows ignoring frequency data that may be corrupt just before the input clock failure.

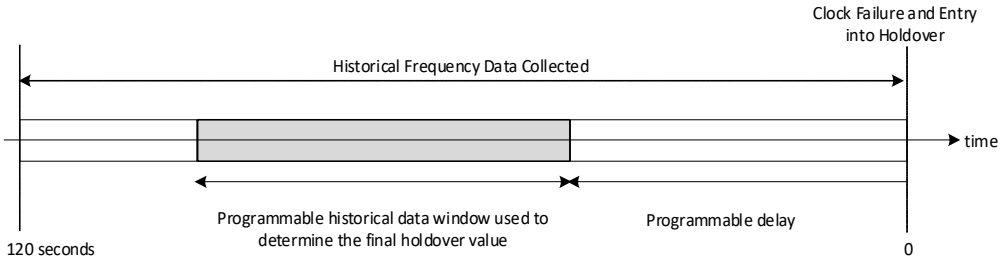


Figure 4. Programmable Holdover Window

When entering holdover, the DSPLL will pull its output clock frequency to the calculated averaged holdover frequency. While in holdover, the output frequency drift is entirely dependent on the external crystal or external reference clock connected to the XA/XB pins. If the clock input becomes valid, the DSPLL will automatically exit the holdover mode and re-acquire lock to the new input clock. This process involves pulling the output clock frequency to achieve frequency and phase lock with the input clock. This pull-in process is glitchless and its rate is controlled by the DSPLL or the fastlock bandwidth. These options are register programmable.

The DSPLL output frequency when exiting holdover can be ramped (recommended). Just before the exit is initiated, the difference between the current holdover frequency and the new desired frequency is measured. Using the calculated difference and a user-selectable ramp rate, the output is linearly ramped to the new frequency. The ramp rate can be 0.2 ppm/s, 40,000 ppm/s, or any of about 40 values in between. The DSPLL loop BW does not limit or affect ramp rate selections (and vice versa). CBPro defaults to ramped exit from holdover. The same ramp rate settings are used for both exit from holdover and ramped input switching. For more information on ramped input switching, see 4.7.5. Frequency Ramped Input Switching.

NOTE: If ramped holdover exit is not selected, the holdover exit is governed either by (1) the DSPLL loop BW or (2) a user-selectable holdover exit BW.

4.4.6. Frequency-on-the-Fly (FOTF)

The Si5397/Si5396 use register writes to support configuration on the fly to allow certain characteristics to be changed on one DSPLL without affecting the clocks generated from other DSPLLs. These characteristics include Input/Output Frequencies, PLL bandwidth, LOL, and OOF settings. See the Si5397/96 Family Reference Manual and AN1178: Frequency-On-the-Fly for Skyworks Jitter Attenuators and Clock Generators for more details.

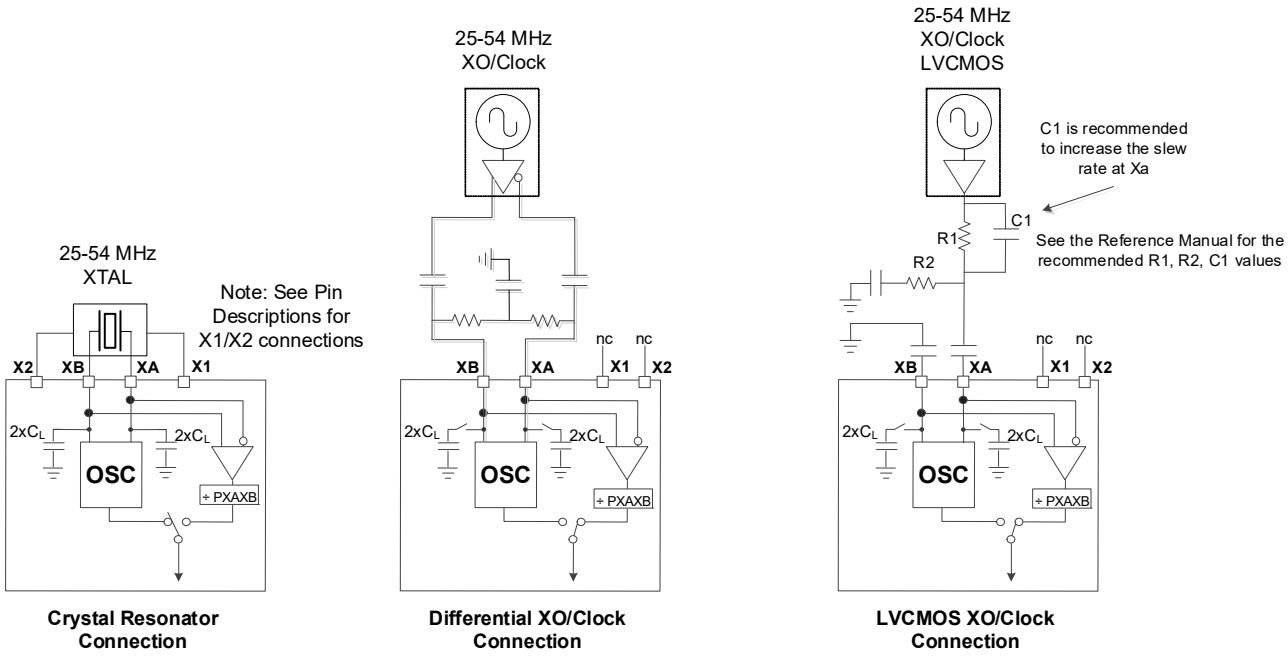
4.5. Digitally Controlled Oscillator (DCO) Mode

The DSPLLs support a DCO mode where their output frequencies are adjustable in predefined steps defined by frequency step words (FSW).The frequency adjustments are controlled through the serial interface or by pin control using frequency increment (FINC) or decrement (FDEC). A FINC will add the frequency step word to the DSPLL output frequency, while a FDEC will decrement it.

4.6. External Reference (Grade A/B/C/D Only)

An external crystal (XTAL) is used in combination with the internal oscillator (OSC) to produce an ultra-low jitter reference clock for the DSPLLs and for providing a stable reference for the Free-run and Holdover Modes. A simplified diagram is shown in the figure below. The device includes internal XTAL loading capacitors, which eliminates the need for external capacitors and also has the benefit of reduced noise coupling from external sources. Refer to Table 17, External Crystal Specifications for Grades A/B/C/D for crystal specifications. A crystal in the range of 48 MHz to 54 MHz is recommended for best jitter performance. The Si5397/96 Family Reference Manual provides additional information on PCB layout recommendations for the crystal to ensure optimum jitter performance.

To achieve optimal jitter performance and minimize BOM cost, a crystal is recommended on the XA/XB reference input. For SyncE line card PLL applications (e.g. loop bandwidth set to 0.1 Hz), a TCXO is required on the XA/XB reference to minimize wander and to provide a stable holdover reference. See the Si5397/96 Family Reference Manual or more information. Selection between the external XTAL or REFCLK is controlled by register configuration. The internal crystal loading capacitors (CL) are disabled in the REFCLK mode. Refer to Table 8, Input Clock Specifications for REFCLK requirements when using this mode. The Si5397/96 Family Reference Manual provides additional information on PCB layout recommendations for the crystal to ensure optimum jitter performance. A PREF divider is available to accommodate external clock frequencies higher than 54 MHz. Although the REFCLK frequency range of 25 MHz to 54 MHz is supported, frequencies in the range of 48 MHz to 54 MHz will achieve the best output jitter performance.



Note: XA and XB must not exceed the maximum input voltage listed in Table 8. Input Clock Specifications.

Figure 5. Crystal Resonator and External Reference Clock Connection Options

Note that connecting an external reference to a device that already has an integrated reference (grades J/K/L/M) is not allowed. Doing so could lead to internal damage to the circuits.

4.7. Inputs (IN0, IN1, IN2, IN3)

The Si5397 has four inputs that can be synchronized with four DSPLLs. The Si5396 has four inputs that can be synchronized with two DSPLLs. The inputs accept both differential and single-ended clocks. A crosspoint between the inputs and the DSPLLs allows any of the inputs to connect to any of the DSPLLs.

4.7.1. Input Selection

Input selection for each of the DSPLLs can be made manually through register control or automatically using an internal state machine.

4.7.2. Manual Input Selection

In manual mode, the input selection is made by writing to a register. If there is no clock signal on the selected input, the DSPLL will automatically enter holdover mode.

4.7.3. Automatic Input Selection

When configured in this mode, the DSPLL automatically selects a valid input that has the highest configured priority. The priority scheme is independently configurable for each DSPLL and supports revertive or non-revertive selection.

All inputs are continuously monitored for loss of signal (LOS) and/or invalid frequency range (OOF). Only inputs that do not assert both the LOS and OOF monitors can be selected for synchronization by the automatic state machine. The DSPLL(s) will enter the Holdover mode if there are no valid inputs available.

4.7.4. Hitless Input Switching

Hitless switching is a feature that prevents a phase offset from propagating to the output when switching between two clock inputs that have a fixed phase relationship. A hitless switch can only occur when the two input frequencies are frequency locked, meaning that they have to be exactly at the same frequency, or at an integer frequency relationship to each other. When hitless switching is enabled, the DSPLL simply absorbs the phase difference between the two input clocks during an input switch. When disabled, the phase difference between the two inputs is propagated to the output at a rate determined by the DSPLL Loop Bandwidth. The hitless switching feature supports clock frequencies down to the minimum input frequency of 8 kHz; however, for optimum hitless switching performance, higher input frequencies are recommended. Hitless switching can be enabled on a per DSPLL basis.

4.7.5. Frequency Ramped Input Switching

The ramped input switching feature is enabled/disabled depending on both the frequency of the Phase-Frequency detector (Fpfd) and the difference in input frequencies (Zero-PPM vs non-zero PPM). The table below shows the selection criteria to enable ramped input switching. The same ramp rate settings are used for both holdover exit and clock switching. For more information on ramped exit from holdover, see 4.4.5. Holdover Mode and the Si5397/96 Family Reference Manual.

Table 4. Recommended Ramped Input Switching Settings for Internal Clock Switches

Maximum Input Frequency Difference	Fpfd[1] < 500 kHz	Fpfd[1] ≥ 500 kHz
0 ppm Frequency locked	Ramped exit from holdover	
≤ 10 ppm	Ramped input switching and ramped exit from holdover	Ramped exit from holdover
> 10 ppm	Ramped input switching and ramped exit from holdover	

1. The Fpfd value is determined by various requirements of the frequency plan and is displayed in the CBPro project file.

Always enable hitless switching and enable phase buildout on holdover exit.

4.7.6. Glitchless Input Switching

The DSPLLs have the ability of switching between two input clock frequencies that are up to ±500 ppm apart. The DSPLL will pull-in to the new frequency using the DSPLL Loop Bandwidth or using the Fastlock Loop Bandwidth if it is enabled. The loss of lock (LOL) indicator will assert while the DSPLL is pulling-in to the new clock frequency. There will be no output runt pulses generated at the output during the transition.

4.7.7. Typical Hitless Switching Scenarios

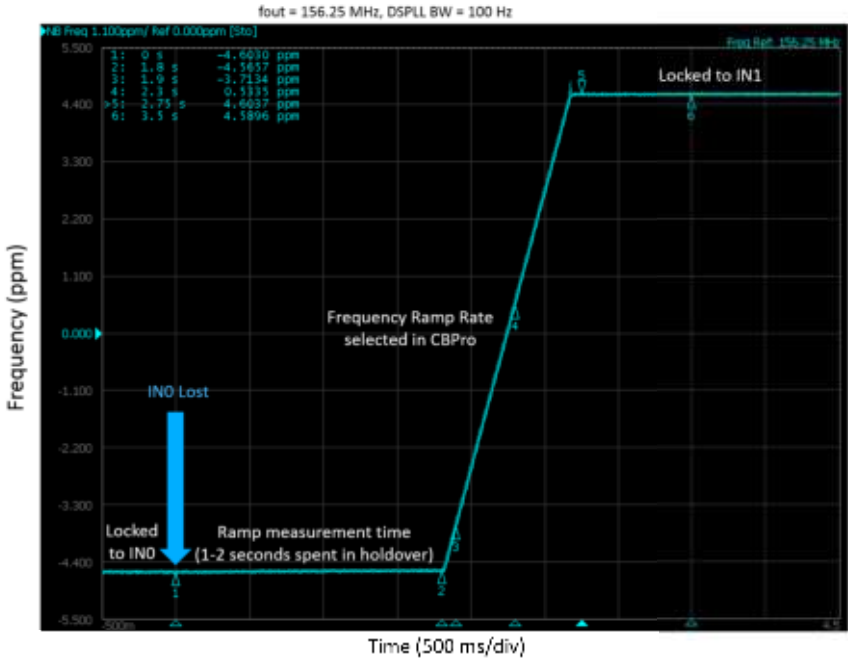


Figure 6. Output Frequency Transient — Ramped Switching Between Two 8 kHz Inputs (±4.6 ppm Offset)

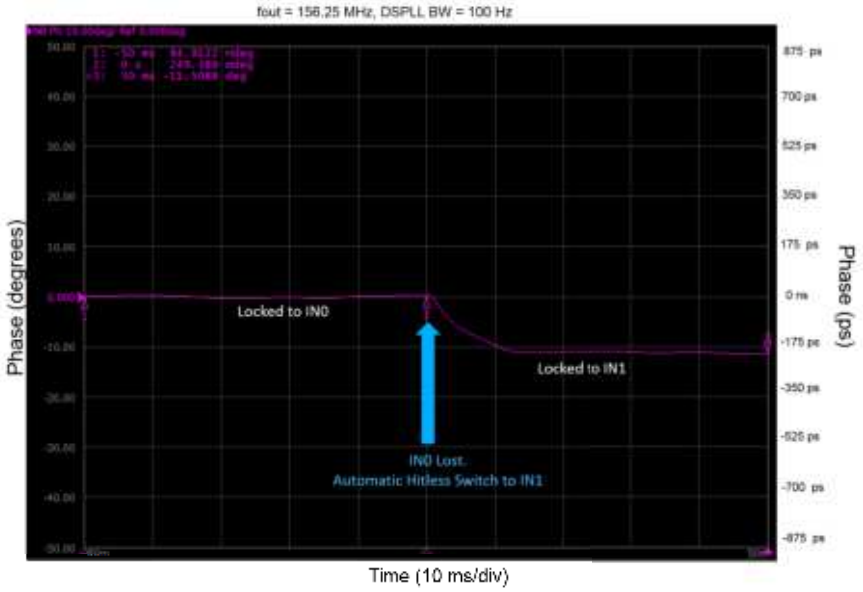


Figure 7. Output Phase Transient-Hitless Switching between Two 25 MHz Inputs (0 ppm, 180 Degree Phase Shift)

4.7.8. Synchronizing to Gapped Input Clocks

Each of the DSPLLs support locking to an input clock that has missing periods. This is also referred to as a gapped clock. The purpose of gapped clocking is to modulate the frequency of a periodic clock by selectively removing some of its cycles. Gapping a clock severely increases its jitter, so a phase-locked loop with high jitter tolerance and low loop bandwidth is required to produce a low-jitter periodic clock. The resulting output will be a periodic non-gapped clock with an average frequency of the input with its missing cycles. For example, an input clock of 100 MHz with one cycle removed every 10 cycles will result in a 90 MHz periodic non-gapped output clock, as shown in Figure 8. For more information on gapped clocks, see AN561: Introduction to Gapped Clocks and PLLs.

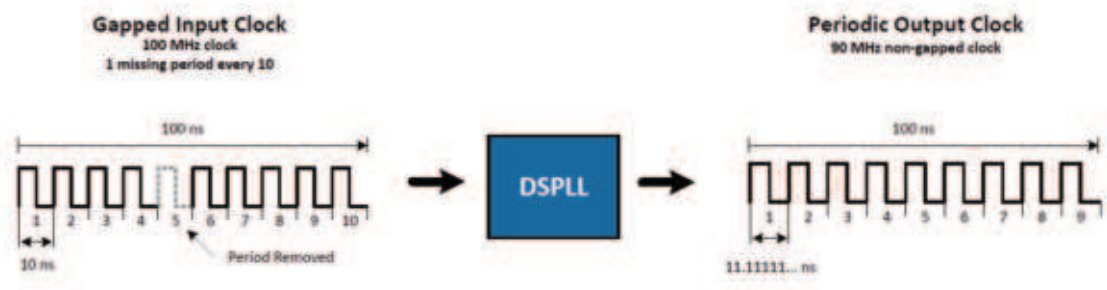


Figure 8. Generating an Averaged Clock Output Frequency from a Gapped Clock Input

A valid gapped clock input must have a minimum frequency of 10 MHz with a maximum of two missing cycles out of every eight. Locking to a gapped clock will not trigger the LOS, OOF, and LOL fault monitors. Clock switching between gapped clocks may violate the hitless switching specification in Table 13, Performance Characteristics when the switch occurs during a gap in either input clock.

4.8. Fault Monitoring

All four input clocks (IN0, IN1, IN2, IN3) are monitored for LOS and OOF, as shown in the figure below. The reference at the XA/XB pins is also monitored for LOS since it provides a critical reference clock for the DSPLLs. Each of the DSPLLs also has an LOL indicator, which is asserted when synchronization is lost with their selected input clock.

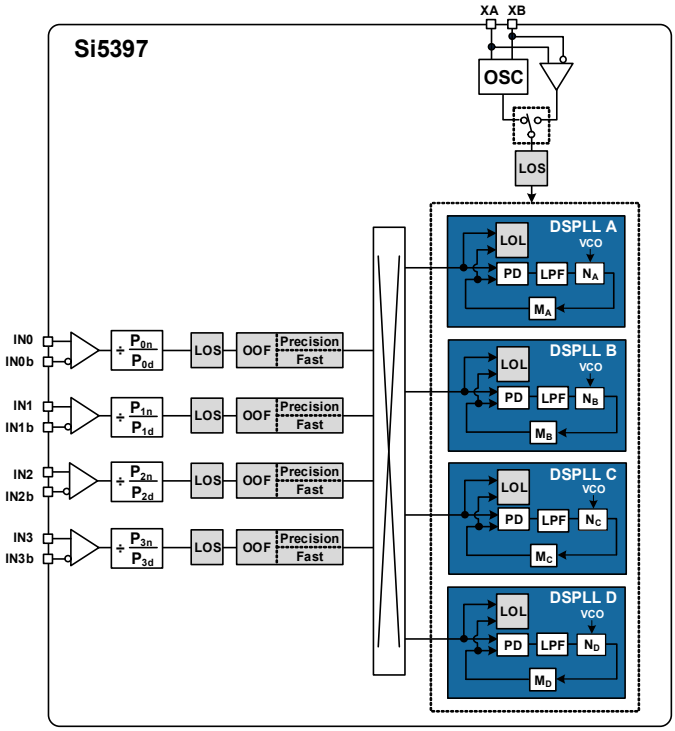


Figure 9. Si5397 Fault Monitors

4.8.1. Input LOS Detection

The loss of signal monitor measures the period of each input clock cycle to detect phase irregularities or missing clock edges. Each of the input LOS circuits has its own programmable sensitivity which allows ignoring missing edges or intermittent errors. Loss of signal sensitivity is configurable using the ClockBuilder Pro utility. The LOS status for each of the monitors is accessible by reading a status register. The live LOS register always displays the current LOS state and a sticky register always stays asserted until cleared. An option to disable any of the LOS monitors is also available.

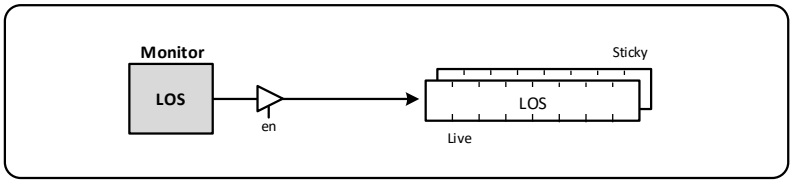


Figure 10. LOS Status Indicators

4.8.2. XA/XB LOS Detection

A LOS monitor is available to ensure that the external crystal or reference clock is valid. By default the output clocks are disabled when XAXB_LOS is detected. This feature can be disabled such that the device will continue to produce output clocks when XAXB_LOS is detected.

4.8.3. OOF Detection

Each input clock is monitored for frequency accuracy with respect to an OOF reference, which it considers as its "0_ppm" reference. This OOF reference can be selected as either:

- XA/XB pins
- Any input clock (IN0, IN1, IN2, IN3)

The final OOF status is determined by the combination of both a precise OOF monitor and a fast OOF monitor as shown in the figure below. An option to disable either monitor is also available. The live OOF register always displays the current OOF state, and its sticky register bit stays asserted until cleared.

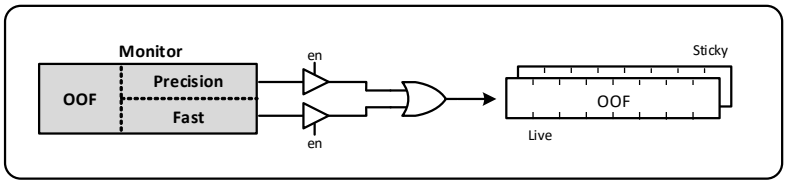


Figure 11. OOF Status Indicator

4.8.3.1. Precision OOF Monitor

The precision OOF monitor circuit measures the frequency of all input clocks to within 1/16 ppm accuracy with respect to the selected OOF frequency reference. A valid input clock frequency is one that remains within the OOF frequency range, which is register configurable up to ±512 ppm in steps of 1/16 ppm. A configurable amount of hysteresis is also available to prevent the OOF status from toggling at the failure boundary. An example is shown in the figure below. In this case, the OOF monitor is configured with a valid frequency range of ±6 ppm and with 2 ppm of hysteresis. An option to use one of the input pins (IN0 - IN3) as the 0 ppm OOF reference instead of the XA/XB pins is available. This option is register-configurable.

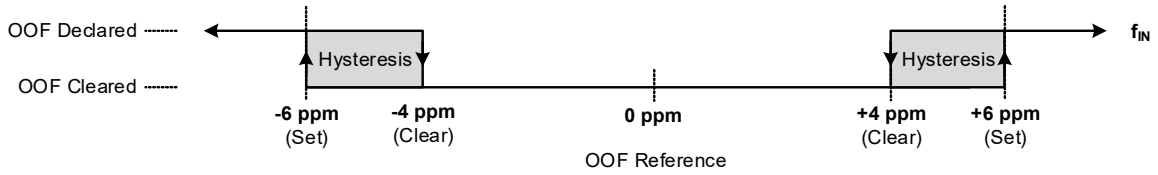


Figure 12. Example of Precise OOF Monitor Assertion and Deassertion Triggers

4.8.3.2. Fast OOF Monitor

Because the precision OOF monitor needs to provide 1/16 ppm of frequency measurement accuracy, it must measure the monitored input clock frequencies over a relatively long period of time. This may be too slow to detect an input clock that is quickly ramping in frequency. An additional level of OOF monitoring called the Fast OOF monitor runs in parallel with the precision OOF monitors to quickly detect a ramping input frequency. The Fast OOF monitor asserts OOF on an input clock frequency that has changed by greater than ±4000 ppm.

4.8.4. LOL Detection

There is an LOL monitor for each of the DSPLLs. The LOL monitor asserts an LOL register bit when a DSPLL has lost synchronization with its selected input clock. There is also a dedicated loss of lock pin that reflects the loss of lock condition for each of the DSPLLs (LOL_Ab, LOL_Bb, LOL_Cb, LOL_Db). The LOL monitor functions by measuring the frequency difference between the input and feedback clocks at the phase detector. There are two LOL frequency monitors, one that sets the LOL indicator (LOL Set) and another that clears the indicator (LOL Clear). An optional timer is available to delay clearing of the LOL indicator to allow additional time for the DSPLL to completely lock to the input clock. The timer is also useful to prevent the LOL indicator from toggling or chattering as the DSPLL completes lock acquisition. A block diagram of the LOL monitor is shown in the figure below. The live LOL register always displays the current LOL state and a sticky register always stays asserted until cleared. The LOLb pin reflects the current state of the LOL monitor.

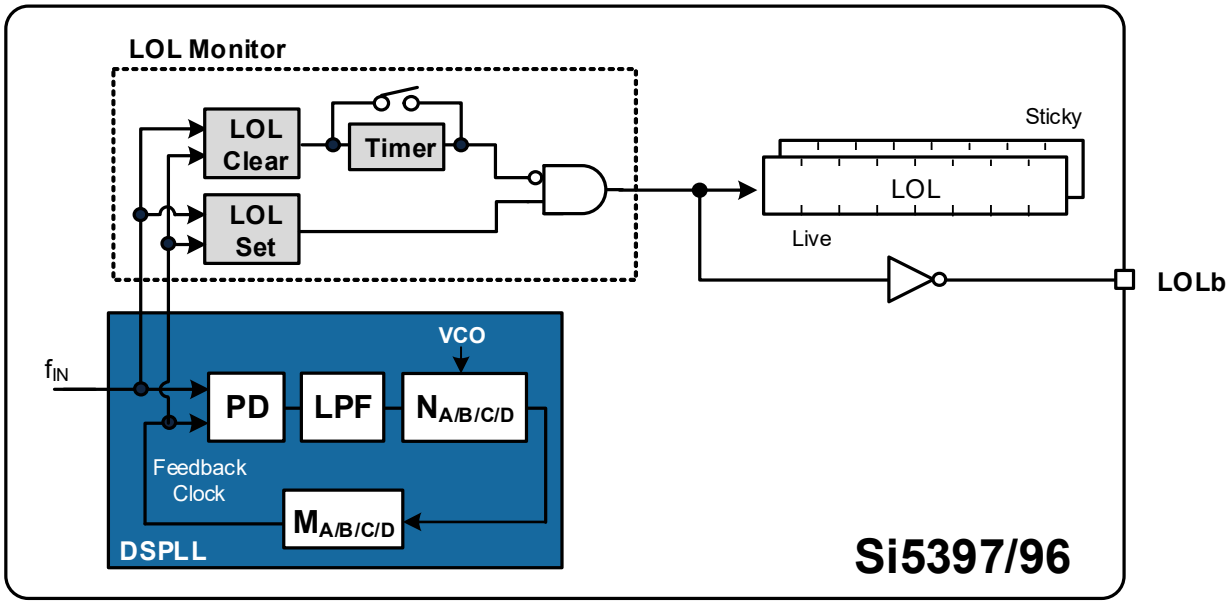


Figure 13. LOL Status Indicators

Each of the LOL frequency monitors has adjustable sensitivity, which is register-configurable from 0.1 ppm to 10,000 ppm. Having two separate frequency monitors allows for hysteresis to help prevent chattering of LOL status. An example configuration where LOCK is indicated, when there is less than 0.1 ppm frequency difference at the inputs of the phase detector and LOL is indicated when there is more than 1 ppm frequency difference, is shown in the following figure.

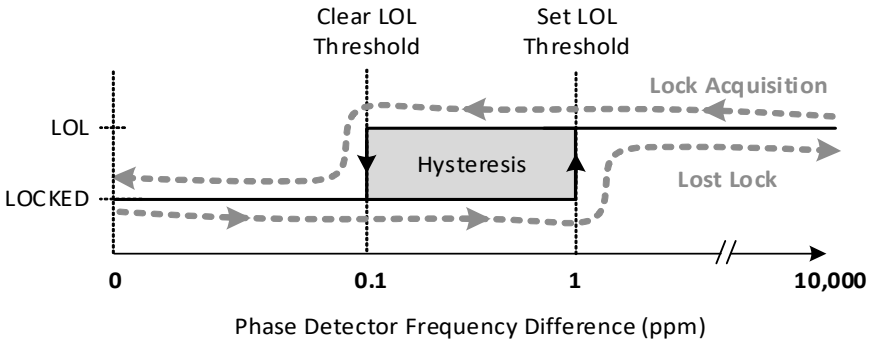


Figure 14. LOL Set and Clear Thresholds

An optional timer is available to delay clearing of the LOL indicator to allow additional time for the DSPLL to completely lock to the input clock. The timer is also useful to prevent the LOL indicator from toggling or chattering as the DSPLL completes lock acquisition. The configurable delay value depends on frequency configuration and loop bandwidth of the DSPLL and is automatically calculated using the ClockBuilder Pro utility.

4.8.5. Interrupt Pin (INTRb)

An interrupt pin (INTRb) indicates a change in state of the status indicators (LOS, OOF, LOL, HOLD). Any of the status indicators are maskable to prevent assertion of the interrupt pin. The state of the INTRb pin is reset by clearing the status register that caused the interrupt.

4.9. Outputs

The Si5397 supports up to eight differential output drivers and the Si5396 supports up to twelve outputs. Each driver has a configurable voltage amplitude and common mode voltage covering a wide variety of differential signal formats including LVPECL, LVDS, HCSL, and CML. In addition to supporting differential signals, any of the outputs can be configured as single-ended LVCMOS (3.3 V, 2.5 V, or 1.8 V) providing up to 24 single-ended outputs, or any combination of differential and single-ended outputs.

4.9.1. Output Crosspoint

A crosspoint allows any of the output drivers to connect with any of the DSPLLs. The crosspoint configuration is programmable and can be stored in NVM so that the desired output configuration is ready at power-up.

4.9.2. Output Signal Format

The differential output amplitude and common mode voltage are both fully programmable and compatible with a wide variety of signal formats, including LVDS and LVPECL. In addition to supporting differential signals, any of the

outputs can be configured as LVCMOS (3.3 V, 2.5 V, or 1.8 V) drivers providing up to 24 single-ended outputs or any combination of differential and single-ended outputs.

4.9.3. Programmable Common Mode Voltage For Differential Outputs

The common mode voltage (VCM) for the differential modes is programmable and depends on the voltage available at the output's VDDO pin. Setting the common mode voltage is useful when dc-coupling the output drivers.

4.9.4. LVCMOS Output Impedance Selection

Each LVCMOS driver has a configurable output impedance to accommodate different trace impedances and drive strengths. A source termination resistor is recommended to help match the selected output impedance to the trace impedance. There are three programmable output impedance selections for each VDDO option, as shown in the table below. Note that selecting a lower source impedance may result in higher output power consumption.

Table 5. Typical Output Impedance (Z_S)

VDDO	CMOS Drive Selections		
	OUTx_CMOS_DRV = 1	OUTx_CMOS_DRV = 2	OUTx_CMOS_DRV = 3
3.3 V	38 Ω	30 Ω	22 Ω
2.5 V	43 Ω	35 Ω	24 Ω
1.8 V	—	46 Ω	31 Ω

4.9.5. LVCMOS Output Signal Swing

The signal swing (VOL/VOH) of the LVCMOS output drivers is set by the voltage on the VDDO pins. Each output driver has its own VDDO pin allowing a unique output voltage swing for each of the LVCMOS drivers.

4.9.6. LVCMOS Output Polarity

When a driver is configured as an LVCMOS output, it generates a clock signal on both pins (OUTx and OUTxb). By default the clock on the OUTxb pin is generated with the same polarity (in phase) with the clock on the OUTx pin. The polarity of these clocks is configurable, which enables complementary clock generation and/or inverted polarity with respect to other output drivers.

4.9.7. Output Enable/Disable

The Si5397/96 allows enabling/disabling outputs by pin or register control, or a combination of both. Two output enable pins are available (OE0b, OE1b). The output enable pins can be mapped to any of the outputs (OUTx) through register configuration. By default OE0b controls all of the outputs while OE1b remains unmapped and has no effect until configured.

Enabling and disabling outputs can also be controlled by register control. This allows disabling one or more output when the OEb pin(s) has them enabled. By default the output enable register settings are configured to allow the OEb pins to have full control.

4.9.8. Output Disable During LOL

By default a DSPLL that is out of lock will generate either free-running clocks or generate clocks in holdover mode. There is an option to disable the outputs when a DSPLL is LOL. This option can be useful to force a downstream PLL into holdover.

4.9.9. Output Disable During XAXB_LOS

The internal oscillator circuit (OSC) in combination with the external crystal (XTAL) provides a critical function for the operation of the DSPLLs. In the event of a crystal failure the device will assert an XAXB_LOS alarm. By default all outputs will be disabled during assertion of the XAXB_LOS alarm. There is an option to leave the outputs enabled during an XAXB_LOS alarm, but the frequency accuracy and stability will be indeterminate during this fault condition.

4.9.10. Output Driver State When Disabled

The disabled state of an output driver is register configurable as disable low or disable high.

4.9.11. Synchronous/Asynchronous Output Disable

Outputs can be configured to disable synchronously or asynchronously. In synchronous disable mode the output will wait until a clock period has completed before the driver is disabled. This prevents unwanted runt pulses from occurring when disabling an output. In asynchronous disable mode, the output clock will disable immediately without waiting for the period to complete.

4.9.12. Output Divider (R) Synchronization

All the output R dividers are reset to a known state during the power-up initialization period. This ensures consistent and repeatable phase alignment across all output drivers. Resetting the device using the RSTb pin or asserting the hard reset bit will have the same result.

4.10. Power Management

Unused inputs and output drivers can be powered down when unused. Consult the Si5397/96 Family Reference Manual and ClockBuilder Pro configuration utility for details.

4.11. In-Circuit Programming

The Si5397/96 is fully configurable using the serial interface (I2C or SPI). At power-up the device downloads its default register values from internal non-volatile memory (NVM). Application specific default configurations can be written into NVM allowing the device to generate specific clock frequencies at power-up. Writing default values to NVM is in-circuit programmable with normal operating power supply voltages applied to its VDD and VDDA pins. The NVM is two time writable. Once a new configuration has been written to NVM, the old configuration is no longer accessible. Refer to the Si5397/96 Family Reference Manual for a detailed procedure for writing registers to NVM.

4.12. Serial Interface

Configuration and operation of the Si5397/96 is controlled by reading and writing registers using the I2C or SPI interface. The I2C_SEL pin selects I2C or SPI operation. Communication with both 3.3 V and 1.8 V host is supported. The SPI mode operates in either 4-wire or 3-wire mode. See the Si5397/96 Family Reference Manual for details.

4.13. Custom Factory Preprogrammed Parts

For applications where a serial interface is not available for programming the device, custom preprogrammed parts can be ordered with a specific configuration written into NVM. A factory preprogrammed part will generate clocks at power-up. Custom, factory-preprogrammed devices are available. The ClockBuilder Pro custom part number wizard can be used to quickly and easily generate a custom part number for your configuration.

In less than three minutes, you will be able to generate a custom part number with a detailed data sheet addendum matching your design's configuration. Once you receive the confirmation email with the data sheet addendum, simply place an order with your local Skyworks sales representative. Samples of your pre-programmed device will typically ship in about two weeks.

4.14. Register Map

The register map is divided into multiple pages where each page has 256 addressable registers. Page 0 contains frequently accessible registers, such as alarm status, resets, device identification, etc. Other pages contain registers that need less frequent access, such as frequency configuration and general device settings. Refer to the Si5397/96 Family Reference Manual for a complete list of register descriptions and settings. It is strongly recommended that ClockBuilder Pro be used to create and manage register settings.

5. Electrical Specifications

Table 6. Recommended Operating Conditions[1]

Parameter	Symbol	Min	Typ	Max	Unit
Ambient temperature	T_A	–40	25	85	°C
Junction temperature	TJ_{MAX}	—	—	125	°C
Core supply voltage	V_{DD}	1.71	1.80	1.89	V
	V_{DDA}	3.14	3.30	3.47	V
Clock output driver supply voltage	V_{DDO}	3.14	3.30	3.47	V
		2.37	2.50	2.62	V
		1.71	1.80	1.89	V
Status pin supply voltage	V_{DDS}	3.14	3.30	3.47	V
		1.71	1.80	1.89	V

1. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise noted.

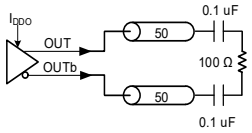
Table 7. DC Characteristics

V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDIO}/V_{DDS} = 3.3 V ±5%, 1.8 V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = -40 to 85 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Core Supply Current[1,2,3]	I_{DD}	Si5397, 4 DSPLLs	—	320	520	mA
		S5397, 1 DSPLL	—	200	360	mA
		Si5396, 2 DSPLLs	—	180	290	mA
	I_{DDA}	Si5397, 4 DSPLLs	—	155	195	mA
		Si5397, 1 DSPLL	—	125	140	mA
		Si5396, 2 DSPLLs	—	120	150	mA
Output Buffer Supply Current	I_{DDO}	2.5 V LVPECL Output[4]	—	22	26	mA
		2.5 V LVDS Output[4]	—	15	18	mA
		3.3 V LVCMOS Output[5]	—	22	30	mA
		2.5 V LVCMOS Output[5]	—	18	23	mA
		1.8 V LVCMOS Output[5]	—	12	16	mA
Total Power Dissipation[6]	P_d	Si5397, 4 DSPLLs[1]	—	1400	1950	mW
		Si5397, 2 DSPLLs[1]	—	1100	1550	mW
		Si5396 A/B/J/K, 2 DSPLLs[2]	—	870	1200	mW
		Si5396 C/D/L/M, 2 DSPLLs[3]	—	1100	1850	mW

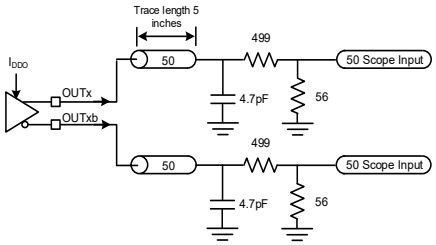
1. Si5397 test configuration: 7×2.5 V LVDS outputs enabled @156.25 MHz. Excludes power in termination resistors.
2. Si5396A/B/J/K test configuration: 4×2.5 V LVDS outputs enabled @ 156.25 MHz. Excludes power in termination resistors.
3. Si5396C/D/L/M test configuration: 12 x 2.5 V LVPECL outputs enabled @ 156.25 MHz. Excludes power in termination resistors.
4. Differential outputs terminated into an ac-coupled 100 Ω load.

Differential Output Test Configuration



5. LVCMOS outputs measured into a 5-inch 50 ? PCB trace with 5 pF load. The LVCMOS outputs were set to OUTx_CMOS_DRV = 3, which is the strongest driver setting. Refer to the Si5397/96 Family Reference Manual for more details on register settings..

LVCMOS Output Test Configuration

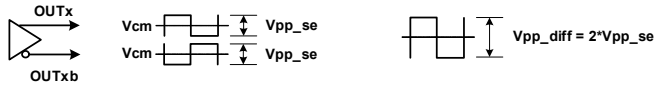


6. Detailed power consumption for any configuration can be estimated using ClockBuilder Pro when an evaluation board (EVB) is not available. All EVBs support detailed current measurements for any configuration.

Table 8. Input Clock Specifications
V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, T_A = –40 to 85 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Standard Differential or Single-Ended - AC Coupled Input Buffer (IN0/IN0b, IN1/IN1b, IN2/IN2b, IN3/IN3b)						
Input frequency range	f_{IN}	Differential	0.008	—	750	MHz
		All Single-ended signals, including LVCMOS	0.008	—	250	MHz
Voltage swing[1]	V_{IN}	Differential AC-coupled, f_{IN} < 250 MHz	100	—	1800	mVpp_se
		Differential AC-coupled, 250 MHz < f_{IN} < 750 MHz	225	—	1800	mVpp_se
		Single-ended AC-coupled, f_{IN} < 250 MHz	100	—	3600	mVpp_se
Slew rate[2,3]	SR		400	—	—	V/µs
Duty cycle	DC		40	—	60	%
Input capacitance	C_{IN}		—	2.4	—	pF
Input resistance differential	R_{IN_DIFF}		—	16	—	kΩ
Input resistance single-ended	R_{IN_SE}		—	8	—	kΩ
LVCMOS / Pulsed CMOS DC-Coupled Input Buffer (IN0, IN1, IN2, IN3)[4]						
Input frequency	f_{IN_CMOS}	Standard CMOS and non-standard CMOS	0.008	—	250	MHz
		Pulsed CMOS	0.008	—	1	MHz
Input voltage[5]	V_{IL}	Standard CMOS	—	—	0.5	V
		Non-standard CMOS and pulsed CMOS	—	—	0.4	V
	V_{IH}	Standard CMOS	1.3	—	—	V
		Non-standard CMOS and pulsed CMOS	0.8	—	—	V
Slew rate[2,3]	SR		400	—	—	V/µs
Duty cycle	DC	Standard CMOS and non-standard CMOS	40	—	60	%
		Pulsed CMOS	5		95	
Minimum pulse width	PW	Standard CMOS and non-standard CMOS (250 MHz @ 40% duty cycle)	1.6	—	—	ns
		Pulsed CMOS (1 MHz @ 40% duty cycle)	50	—	—	
Input resistance	R_{IN}		—	8	—	kΩ
REFCLK (Applied to XA/XB)						
REFCLK frequency	f_{IN_REF}	Full operating range, jitter performance may be reduced	24.97	—	54.06	MHz
		Range for best jitter	48	—	54	MHz
Input voltage swing	V_{IN_DIFF}		365	—	2000	mVpp_se
	V_{IN_SE}		365		2500	mVpp_diff
Slew rate[2,3]	SR		400	—	—	V/µs
Duty cycle	DC		40	—	60	%

1. Voltage swing is specified as single-ended mVpp.



2. Recommended for specified jitter performance. Slew rate can go lower, but jitter performance could degrade if the minimum slew rate specification is not met (see the Si5397/96 Family Reference Manual).
3. Rise and fall times can be estimated using the following simplified equation: $tr/tf_{80\text{-}20} = ((0.8 – 0.2) \times V_{IN_Vpp_se}) / SR$.
4. Standard, non-standard and pulsed CMOS refer to different formats of CMOS each with a voltage swing of 1.8V, 2.5V or 3.3V +/-5%.
   - Standard CMOS refers to the industry standard LVCMOS signal.
   - Non-standard CMOS refers to a signal that has been attenuated/level-shifted in order to comply with the specified non-standard VIL and VIH specifications.
   - Pulsed CMOS refers to a signal that has been attenuated/level-shifted and has a low/high duty cycle and must be dc coupled. A typical application example is a low-frequency video frame sync pulse.

   Refer to the Si5397/96 Family Reference Manual for the recommended connections/termination for the different modes.
5. CMOS signals that exceed 3.3 V + 5% can be used as inputs as long as a resistive attenuation network is used to guarantee that the input voltage at the pin does not violate the device's input ratings. Please refer to the Si5397/96 Family Reference Manual for the recommended connections/termination for this mode.

Table 9. Serial and Control Input Pin Specifications
V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDIO}/V_{DDS} = 3.3 V ±5%, 1.8 V ±5%, T_A = –40 to 85 °C

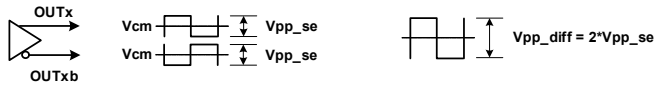
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si5397 Serial and Control Input Pins (I2C_SEL, RSTb, OE0b, A1/SDO, SCLK, A0/CSb, FINC, A0/CSb, SDA/SDIO, DSPLL_SEL[1:0])						
Input voltage	V_{IL}		—	—	0.3 x V_{DDIO}[1]	V
	V_{IH}		0.7 × V_{DDIO}[1]	—	—	V
Input capacitance	C_{IN}		—	2	—	pF
Input resistance	R_L		—	20	—	kΩ
Minimum pulse width	PW	RSTb and FINC	100	—	—	ns
Update rate	F_{UR}	FINC	—	—	1	MHz
Si5397 Control Input Pins (FDEC, OE1b)						
Input voltage	V_{IL}		—	—	0.3 x V_{DDS}	V
	V_{IH}		0.7 × V_{DDS}	—	—	V
Input capacitance	C_{IN}		—	2	—	pF
Minimum pulse width	PW	FDEC	100	—	—	ns
Update rate	F_{UR}	FDEC	—	—	1	MHz
Si5396 Serial and Control Input Pins (I2C_SEL, RSTb, OE0b, OE1b, A1/SDO, SCLK, A0/CSb, SDA/SDIO)						
Input voltage	V_{IL}		—	—	0.3 x V_{DDIO}[1]	V
	V_{IH}		0.7 × V_{DDIO}[1]	—	—	V
Input capacitance	C_{IN}		—	2	—	pF
Input resistance	R_L		—	20	—	kΩ
Minimum pulse width	PW	RSTb	100	—	—	ns

1. V_{DDIO} is determined by the IO_VDD_SEL bit. It is selectable as V_{DDA} or V_{DD}.

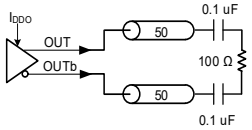
Table 10. Differential Clock Output Specifications
V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Output frequency	f_{OUT}			0.0001	—	720	MHz
Duty cycle	DC	f_{OUT} < 400 MHz		48	—	52	%
		400 MHz < f_{OUT} <= 720 MHz		45	—	55	%
Output voltage amplitude[1]	V_{OUT}	V_{DDO} = 3.3 V, 2.5 V, 1.8 V	LVDS	350	450	530	mVpp_se
		V_{DDO} = 3.3 V, 2.5 V	LVPECL	630	750	950	mVpp_se
Common mode voltage[1, 2] (100 Ω load line-to-line)	V_{CM}	V_{DDO} = 3.3 V	LVDS	1.1	1.2	1.3	V
			LVPECL	1.9	2.0	2.1	V
		V_{DDO} = 2.5 V	LVPECL LVDS	1.1	1.2	1.3	V
		V_{DDO} = 1.8 V	sub-LVDS	0.8	0.9	1.0	V
Output-to-output skew (same DSPLL, different outputs)	T_{SKS}	f_{OUT} = 720 MHz (LVDS differential)		—	0	75	ps
Out-outb skew (same output)	T_{SK_OUT}	Measured from positive to negative output pins		—	0	50	ps
Rise and fall times	$t_{r/tf}$	f_{OUT} > 100 MHz (20% to 80%)		—	100	200	ps
Differential output impedance	Z_O			—	100	—	Ω
Power supply noise rejection[2]	PSRR	10 kHz sinusoidal noise		—	–101	—	dBc
		100 kHz sinusoidal noise		—	–96	—	dBc
		500 kHz sinusoidal noise		—	–99	—	dBc
		1 MHz sinusoidal noise		—	–97	—	dBc
Output-to-output crosstalk[3]	XTALK	Si5397		—	–72	—	dBc
		Si5396		—	–88	—	dBc

1. Output amplitude and common-mode settings are programmable through register settings and can be stored in NVM. Each output driver can be programmed independently. Note that the maximum LVDS single-ended amplitude can be up to 110 mV higher than the TIA/EIA-644 maximum. Refer to the Si5397/96 Family Reference Manual for more suggested output settings. Not all combinations of voltage amplitude and common mode voltages settings are possible.



Differential Output Test Configuration



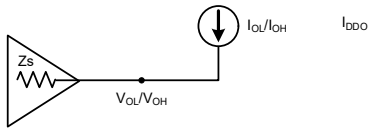
2. Measured for 156.25 MHz carrier frequency. 100 mVpp sinewave noise added to VDDO = 3.3 V and noise spur amplitude measured.
3. Measured across two adjacent outputs, both in LVDS mode, with the victim running at 155.52 MHz and the aggressor at 156.25 MHz. Refer to AN862: Optimizing Si534x Jitter Performance in Next Generation Internet Infrastructure Systems for guidance on crosstalk optimization. Note that all active outputs must be terminated when measuring crosstalk.

Table 11. LVCMOS Clock Output Specifications
V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Output frequency	f_{OUT}			0.0001	—	250	MHz
Duty cycle	DC	f_{OUT} <100 MHz		48	—	52	%
		100 MHz < f_{OUT} < 250 MHz		44	—	56	%
Output voltage high[1,2,3]	V_{OH}	**V_{DDO} = 3.3 V**					
		OUTx_CMOS_DRV = 1	I_{OH} = –10 mA	V_{DDO} x 0.85	—	—	V
		OUTx_CMOS_DRV = 2	I_{OH} = –12 mA	V_{DDO} x 0.85	—	—	V
		OUTx_CMOS_DRV = 3	I_{OH} = –17 mA	V_{DDO} x 0.85	—	—	V
		V_{DDO} = 2.5 V					
		OUTx_CMOS_DRV = 1	I_{OH} = –6 mA	V_{DDO} x 0.85	—	—	V
		OUTx_CMOS_DRV = 2	I_{OH} = –8 mA	V_{DDO} x 0.85	—	—	V
		OUTx_CMOS_DRV = 3	I_{OH} = –11 mA	V_{DDO} x 0.85	—	—	V
		V_{DDO} = 1.8 V					
		OUTx_CMOS_DRV = 2	I_{OH} = –4 mA	V_{DDO} x 0.85	—	—	V
		OUTx_CMOS_DRV = 3	I_{OH} = –5 mA	V_{DDO} x 0.85	—	—	V
Output voltage low[1,2,3]	V_{OL}	**V_{DDO} = 3.3 V**					
		OUTx_CMOS_DRV = 1	I_{OL} = 10 mA	—	—	V_{DDO} x 0.15	V
		OUTx_CMOS_DRV = 2	I_{OL} = 12 mA	—	—	V_{DDO} x 0.15	V
		OUTx_CMOS_DRV = 3	I_{OL} = 17 mA	—	—	V_{DDO} x 0.15	V
		V_{DDO} = 2.5 V					
		OUTx_CMOS_DRV = 1	I_{OL} = 6 mA	—	—	V_{DDO} x 0.15	V
		OUTx_CMOS_DRV = 2	I_{OL} = 8 mA	—	—	V_{DDO} x 0.15	V
		OUTx_CMOS_DRV = 3	I_{OL} = 11 mA	—	—	V_{DDO} x 0.15	V
		V_{DDO} = 1.8 V					
		OUTx_CMOS_DRV = 2	I_{OL} = 4 mA	—	—	V_{DDO} x 0.15	V
		OUTx_CMOS_DRV = 3	I_{OL} = 5 mA	—	—	V_{DDO} x 0.15	V
Rise and fall times[3]	t_r/t_f	(20% to 80%)	V_{DDO} = 3.3 V	—	400	600	ps
			V_{DDO} = 2.5 V	—	450	600	ps
			V_{DDO} = 1.8 V	—	550	750	ps

1. Driver strength is a register programmable setting and stored in NVM. Options are OUTx_CMOS_DRV = 1, 2, 3. Refer to the Si5397/96 Family Reference Manual for more details on register settings.
2. I_{OL}/I_{OH} is measured at V_{OL}/V_{OH} as shown in the DC test configuration.

DC Test Configuration



3. A series termination resistor (Rs) is recommended to help match the source impedance to a 50 Ω PCB trace. A 4.7 pF capacitive load is assumed. The LVCMOS outputs were set to OUTx_CMOS_DRV = 3 at 156.25 MHz.

LVCMOS Output Test Configuration

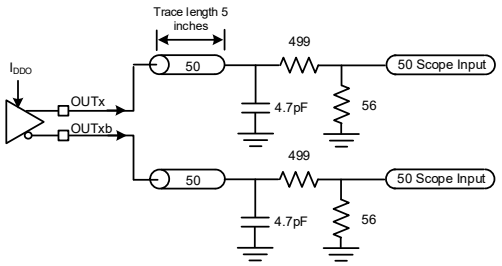


Table 12. Output Serial and Status Pin Specifications

V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDIO}/V_{DDS} = 3.3 V ±5%, 1.8 V ±5%, T_A = –40 to 85 °C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Si5397 Serial and Status Output Pins (LOL_Ab, LOL_Bb, LOL_Cb, LOL_Db, INTRb, LOS_XAXBb, SDA/SDIO[1], A1/SDO)						
Output voltage	V_{OH}	I_{OH} = –2 mA	V_{DDIO}[2] x 0.85	—	—	V
	V_{OL}	I_{OL} = 2 mA	—	—	V_{DDIO}[2] x 0.15	V
Si5396 Status Output Pins (INTRb, LOS_XAXBb, SDA/SDIO[1], A1/SDO)						
Output voltage	V_{OH}	I_{OH} = –2 mA	V_{DDIO}[2] x 0.85	—	—	V
	V_{OL}	I_{OL} = 2 mA	—	—	V_{DDIO}[2] x 0.15	V
Si5396 Status Output Pins (LOL_Ab, LOL_Bb)						
Output Voltage	V_{OH}	I_{OH} = –2 mA	V_{DDS} x 0.85	—	—	V
	V_{OL}	I_{OL} = 2 mA	—	—	V_{DDS} x 0.15	V

1. The V_{OH} specification does not apply to the open-drain SDA/SDIO output when the serial interface is in I^2C mode or is unused with I^2C_SEL pulled high. V_{OL} remains valid in all cases.
2. V_{DDIO} is determined by the IO_VDD_SEL bit. It is selectable as V_{DDA} or V_{DD}. Users normally select this option in ClockBuilder Pro. Alternatively, refer to the Si5397/96 Family Reference Manual for more details on the proper register settings.

Table 13. Performance Characteristics
V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
PLL loop bandwidth programming range[1]	f_{BW}		0.1	—	4000	Hz
Initial start-up time	t_{START}	Time from power-up to when the device generates free-running clocks	—	30	45	ms
PLL lock time[2]	t_{ACQ}	With Fastlock enabled, f_{IN} = 19.44 MHz	—	280	300	ms
POR to serial interface ready[3]	t_{RDY}		—	—	15	ms
Maximum phase transient during a hitless switch[4]	t_{SWITCH}	Single automatic/manual switch between two 8 kHz inputs, DSPLL BW = 40 Hz	—	—	0.8	ns
		Single automatic/manual switch between two 2 MHz inputs, DSPLL BW = 400 Hz	—	—	0.3	ns
Input-to-Output Delay Variation[5]	$t_{IODELAY}$	$f_{IN} = f_{OUT}$ = 2 MHz DSPLL BW = 4 kHz	—	—	0.55	ns
		$f_{IN} = f_{OUT}$ = 62 kHz DSPLL BW = 4 kHz	—	—	0.75	ns
		$f_{IN} = f_{OUT}$ = 8 kHz DSPLL BW = 4 kHz	—	—	3	ns
Jitter peaking	J_{PK}	Measured with a frequency plan running a 25 MHz input, 25 MHz output, and a loop bandwidth of 4 Hz	—	—	0.1	dB
Jitter tolerance	J_{TOL}	Compliant with G.8262 options 1 and 2 for 1G, 10G or 25G synchronous Ethernet, jitter modulation frequency = 10 Hz	—	3180	—	UI pk-pk
Pull-in range	ω_P		—	500	—	ppm
RMS phase jitter[6]	J_{GEN}	12 kHz to 20 MHz	—	95	125	fs

1. Actual loop bandwidth might be lower; please refer to CBPro for actual value for your frequency plan.
2. Lock Time can vary significantly depending on several parameters, such as bandwidths, LOL thresholds, etc. For this case, lock time was measured with nominal bandwidth set to 100 Hz, fastlock bandwidth set to 1 kHz, LOL set/clear thresholds of 6/0.6 ppm respectively, using IN0 as clock reference by removing the reference and enabling it again, then measuring the delta time between the first rising edge of the clock reference and the LOL indicator deassertion.
3. Measured as time from valid V_{DD}/V_{DDA} rails (90% of their value) to when the serial interface is ready to respond to commands.
4. Higher input frequencies will typically result in higher Fpfd frequencies, which, in turn, will result in better hitless switching performance. It is recommended to use higher input frequencies for the best hitless switching performance.
5. Delay is dependent on frequency configuration. Using f_{PFD} < 128 kHz will result in higher delay values. Input clock rise time must be <200 ps.
6. Test conditions: f_{IN} = 19.44 MHz, f_{OUT} = 156.25 MHz LVPECL, loop bandwidth = 100 Hz, fXTAL = 48 MHz.

Table 14. I²C Timing Specifications (SCL, SDA)
V_{DD}= 1.8 V ±5%, V_{DDA}= 3.3 V ±5%, V_{DDS}/V_{DDIO}= 3.3 V ±5%, 1.8 V ±5%, T_A= –40 to 85 °C

Parameter	Symbol	Test Condition	Standard Mode100 kbps		Fast Mode 400 kbps		Unit
			Min	Max	Min	Max	
SCL clock frequency	f_{SCL}		—	100	—	400	kHz
SMBus timeout	—		25	35	25	35	ms
Hold time (repeated) start condition	$t_{HD:STA}$		4.0	—	0.6	—	µs
Low period of the SCL clock	t_{LOW}		4.7	—	1.3	—	µs
HIGH period of the SCL clock	t_{HIGH}		4.0	—	0.6	—	µs
Setup time for a repeated start condition	$t_{SU:STA}$		4.7	—	0.6	—	µs
Data hold time	$t_{HD:DAT}$		100	—	100	—	ns
Data setup time	$t_{SU:DAT}$		250	—	100	—	ns
Rise time of both SDA and SCL signals	t_r		—	1000	20	300	ns
Fall time of both SDA and SCL signals	t_f		—	300	—	300	ns
Setup time for stop condition	$t_{SU:STO}$		4.0	—	0.6	—	µs
Bus free time between a stop and start condition	t_{BUF}		4.7	—	1.3	—	µs
Data valid time	$t_{VD:DAT}$		—	3.45	—	0.9	µs
Data valid acknowledge time	$t_{VD:ACK}$		—	3.45	—	0.9	µs

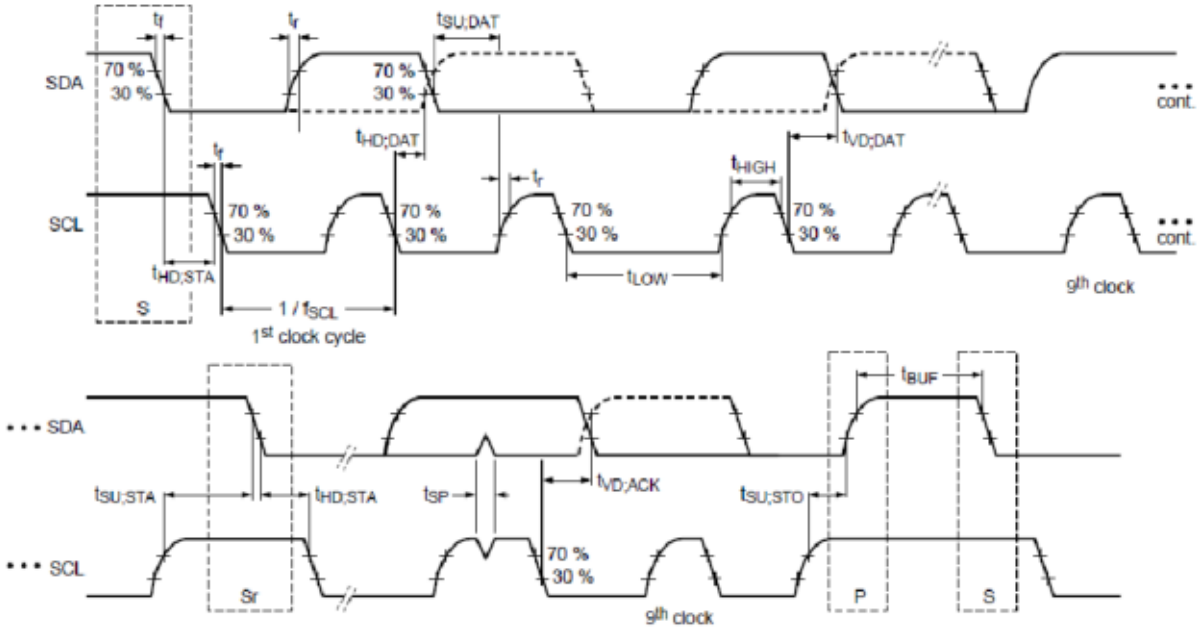


Figure 15. I²C Serial Port Timing Standard and Fast Modes

Table 15. SPI Timing Specifications (4-Wire)
V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3V ±5%, V_{DDIO}= 3.3 V ±5%, 1.8 V ±5%, T_A = –40 to 85 °C

Parameter	Symbol	Min	Typ	Max	Unit
SCLK frequency	f_{SPI}	—	—	20	MHz
SCLK duty cycle	T_{DC}	40	—	60	%
SCLK period	T_C	50	—	—	ns
Delay time, SCLK fall to SDO active	T_{D1}	—	—	18	ns
Delay time, SCLK fall to SDO	T_{D2}	—	—	15	ns
Delay time, CSb rise to SDO tri-state	T_{D3}	—	—	15	ns
Setup time, CSb to SCLK	T_{SU1}	5	—	—	ns
Hold time, SCLK fall to CSb	T_{H1}	5	—	—	ns
Setup time, SDI to SCLK rise	T_{SU2}	5	—	—	ns
Hold time, SDI to SCLK rise	T_{H2}	5	—	—	ns
Delay time between chip selects (CSb)	T_{CS}	95	—	—	ns

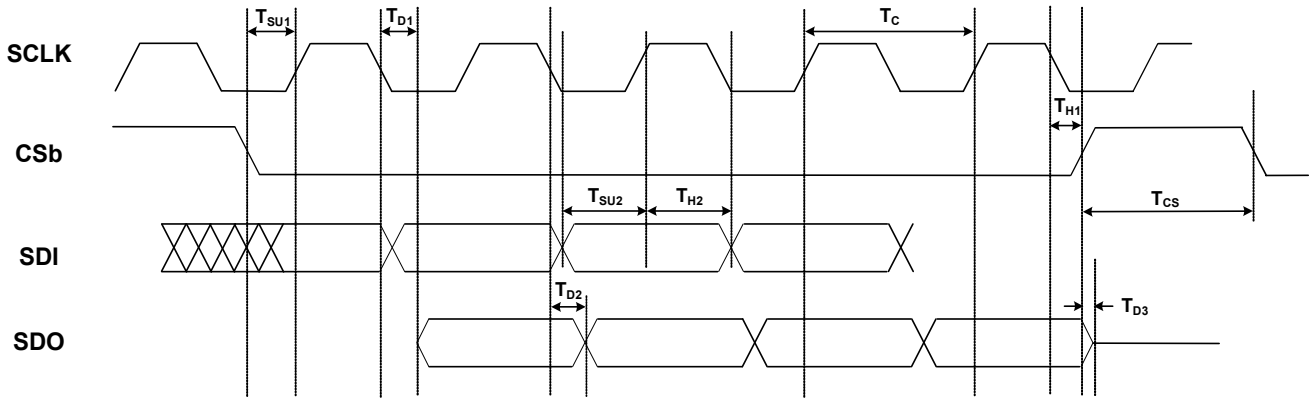


Figure 16. 4-Wire SPI Serial Interface Timing

Table 16. SPI Timing Specifications (3-Wire)
V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3V ±5%, V_{DDIO}= 3.3 V ±5%, 1.8 V ±5%, T_A = –40 to 85 °C

Parameter	Symbol	Min	Typ	Max	Unit
SCLK frequency	f_{SPI}	—	—	20	MHz
SCLK duty cycle	T_{DC}	40	—	60	%
SCLK period	T_C	50	—	—	ns
Delay time, SCLK fall to SDIO turn-on	T_{D1}	—	12.5	18	ns
Delay time, SCLK fall to SDIO next-bit	T_{D2}	—	10	15	ns
Delay time, CSb rise to SDIO tri-state	T_{D3}	—	10	15	ns
Setup time, CSb to SCLK	T_{SU1}	5	—	—	ns
Hold time, CSb to SCLK fall	T_{H1}	5	—	—	ns
Setup time, SDI to SCLK rise	T_{SU2}	5	—	—	ns
Hold time, SDI to SCLK rise	T_{H2}	5	—	—	ns
Delay time between chip selects (CSb)	T_{CS}	95	—	—	ns

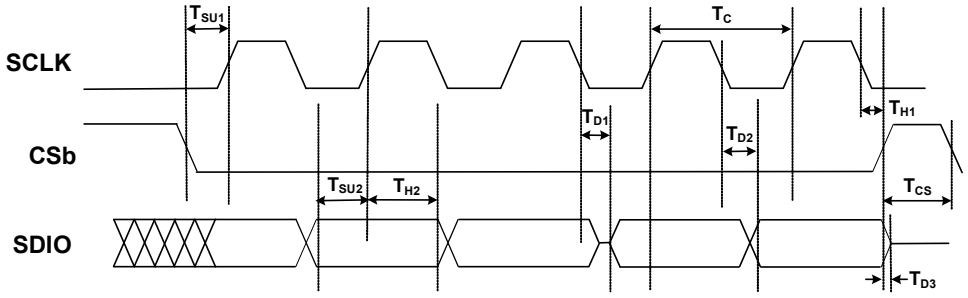


Figure 17. 3-Wire SPI Serial Interface Timing

Table 17. External Crystal Specifications for Grades A/B/C/D[1]

Parameter	Symbol	Test Condition	Mix	Typ	Max	Unit
Crystal frequency range	f_{XTAL} (A/B/C/D)	Full operating range, jitter performance may be reduced	24.97	—	54.06	MHz
		Range for best jitter	48	—	54	MHz
Load capacitance	C_L		—	8	—	pF
Crystal drive level	d_L		—	—	200	µW
Equivalent series resistance	r_{ESR}	Refer to the Si5397/96 Family Reference Manual to determine ESR and shunt capacitance values.				
Shunt capacitance	C_O					

1. Refer to the Si534x/8x/9x Jitter Attenuators Recommended Crystal, TCXO and OCXOs Reference Manual for recommended 48 to 54 MHz crystals.

Table 18. Internal Reference Specifications for Grade J/K/L/M[1,2]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Initial accuracy	—		–8	—	+8	ppm
Frequency characteristics across temperature	—	Inclusive of temperature range of –40 to 125 °C, aging at 115 °C and reflow	–88	—	+88	ppm
Activity dip	—	Frequency perturbations	–2	—	+2	ppm
Overall accuracy	—	Inclusive of initial accuracy, frequency characteristics across temperature and activity dips (all items listed above)	–98	—	+98	ppm

1. These devices with integrated reference have been tuned with an internal 48 MHz reference to deliver optimum performance. It is important to note that connecting an external reference to a device that already has an integrated reference is not allowed. Doing so could lead to internal damage to the circuits.
2. Clocks that feature the integrated crystal may require a slightly longer settling time compared to the external crystal device. See the reference manual for more details.

Table 19. Thermal Characteristics 44-QFN and 44-LGA (Si5396)

Parameter	Symbol	Test Condition	Min	Typ	Max
Thermal resistance junction to ambient	θ_{JA}	Still air[1,2]	22.3	25.49	°C/W
		Air flow 1 m/s[1,2]	19.4	22.14	°C/W
		Air flow 2 m/s[1,2]	18.4	21.13	°C/W
Thermal resistance junction to case	θ_{JC}		10.9	9.87	°C/W
Thermal resistance junction to board	θ_{JB}		9.3	9.52	°C/W
	Ψ_{JB}		9.2	9.58	°C/W
Thermal resistance junction to top center	Ψ_{JT}		0.23	0.81	°C/W

1. 44-QFN: Based on PCB Dimension: 3" x 4.5" PCB Thickness: 1.6 mm, PCB Land/Via: 36, Number of Cu Layers: 4.
2. 44-LGA: Based on 4 layer PCB with dimension 4" x 4.5", PCB Thickness of 1.6 mm, per JEDEC. PCB Center Land with 16 Via to top internal plane of PCB.

Table 20. Thermal Characteristics 64-QFN and 64-LGA (Si5397)

Parameter	Symbol	Test Condition	64-QFN	64-LGA	Unit
Thermal resistance junction to ambient	θ_{JA}	Still air[1,2]	22	22.3	°C/W
		Air flow 1 m/s[1,2]	19.4	19.4	°C/W
		Air flow 2 m/s[1,2]	18.3	18.4	°C/W
Thermal resistance junction to case	θ_{JC}		9.5	10.9	°C/W
Thermal resistance junction to board	θ_{JB}		9.4	9.3	°C/W
	Ψ_{JB}		9.3	9.2	°C/W
Thermal resistance junction to top center	Ψ_{JT}		0.2	0.23	°C/W

1. 64-QFN: Based on PCB Dimension: 3" x 4.5" PCB Thickness: 1.6 mm, PCB Land/Via: 36, Number of Cu Layers: 4.
2. 64-LGA: Based on 4 layer PCB with dimension 4" x 4.5", PCB Thickness of 1.6 mm, per JEDEC. PCB Center Land with 16 Via to top internal plane of PCB.

Table 21. Absolute Maximum Ratings[1,2,3]

Parameter	Symbol	Test Condition	Value	Unit
DC supply voltage	V_{DD}		–0.5 to 3.8	V
	V_{DDA}		–0.5 to 3.8	V
	V_{DDO}		–0.5 to 3.8	V
	V_{DDS}		–0.5 to 3.8	V
Input voltage range	V_{I1}[4]	IN0 – IN3	–1.0 to 3.8	V
	V_{I2}	RSTb, OE0b, OE1b, I2C_SEL, FINC, FDEC, PLL_SEL[1:0] SDA/SDIO, A1/SDO, SCLK,A0/CSb	–0.5 to 3.8	V
	V_{I3}	XA/XB	–0.5 to 2.7	V
Latch-up tolerance	LU		JESD78 Compliant	
ESD tolerance	HBM	100 pF, 1.5 kΩ	2.0	kV
Max junction temperature in operation	T_{JCT}		125	°C
Storage temperature range	T_{STG}		–55 to 150	°C
Soldering temperature (Pb-free profile)[5]	T_{PEAK}		260	°C
Soldering temperature time at T_{PEAK} (Pb-free profile)[5]	T_P		20 to 40	s

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. 64-QFN/LGA and 44-QFN/LGA packages are RoHS compliant.
3. For detailed packaging information, go to www.skyworksinc.com.
4. The minimum voltage at these pins can be as low as –1.0 V when an ac input signal of 8 kHz or greater is applied. See Table 8, Input Clock Specifications for single-ended ac-coupled f_{IN} < 250 MHz.
5. The device is compliant with JEDEC J-STD-020.

6. Typical Application Schematic

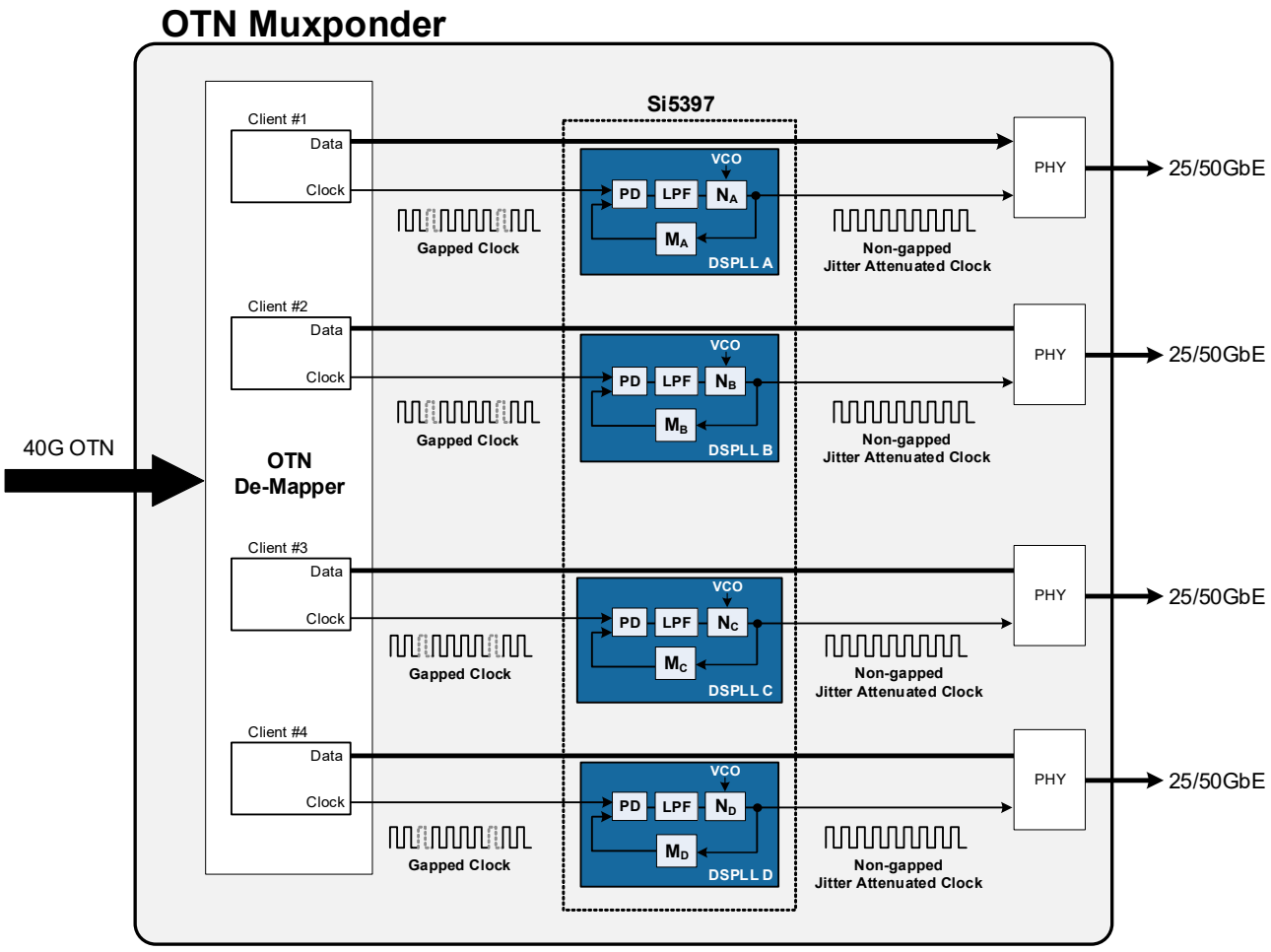


Figure 18. Using the Si5397 to Clean Gapped Clocks in an OTN Application

7. Detailed Block Diagrams

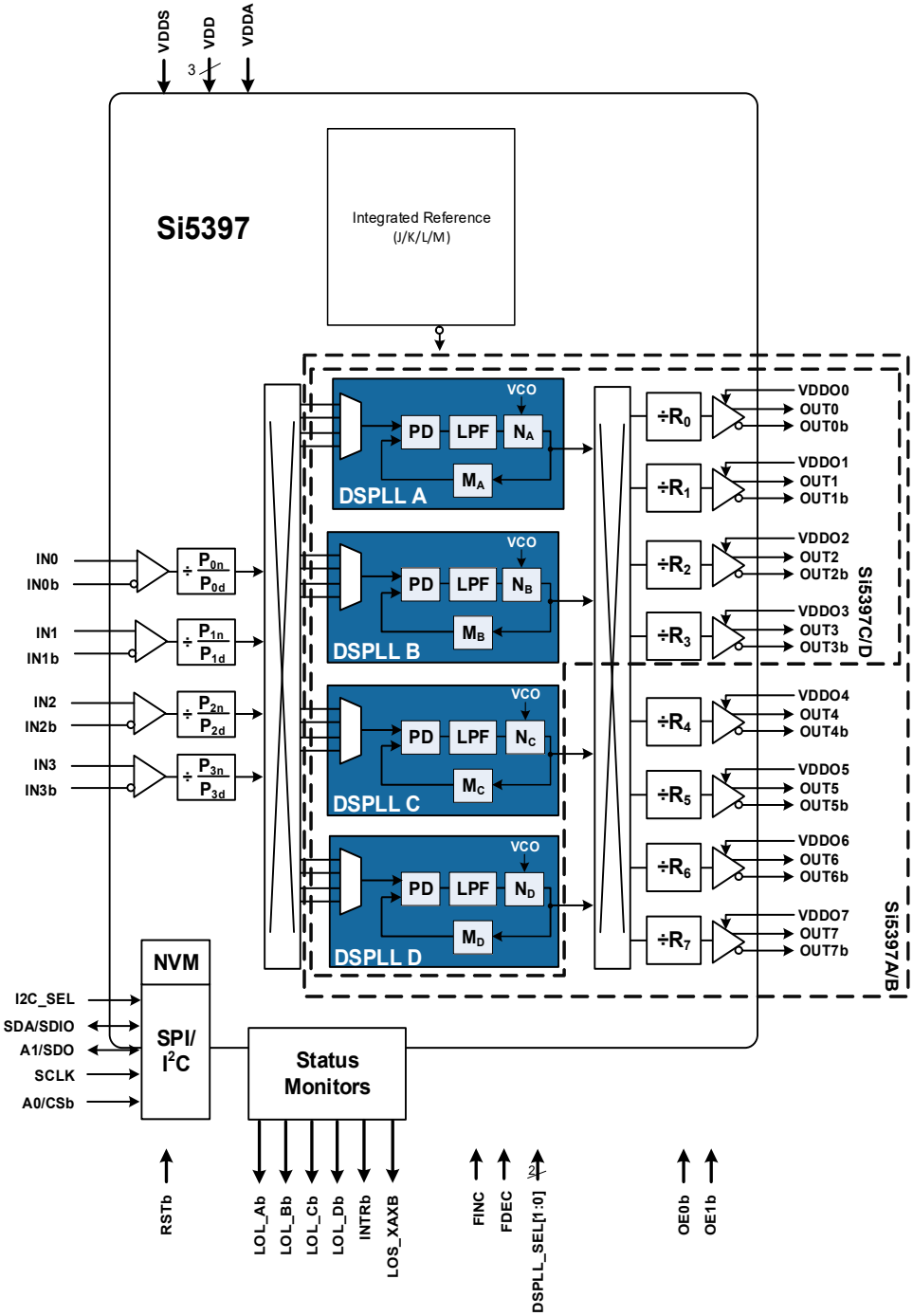


Figure 19. Si5397 Block Diagram

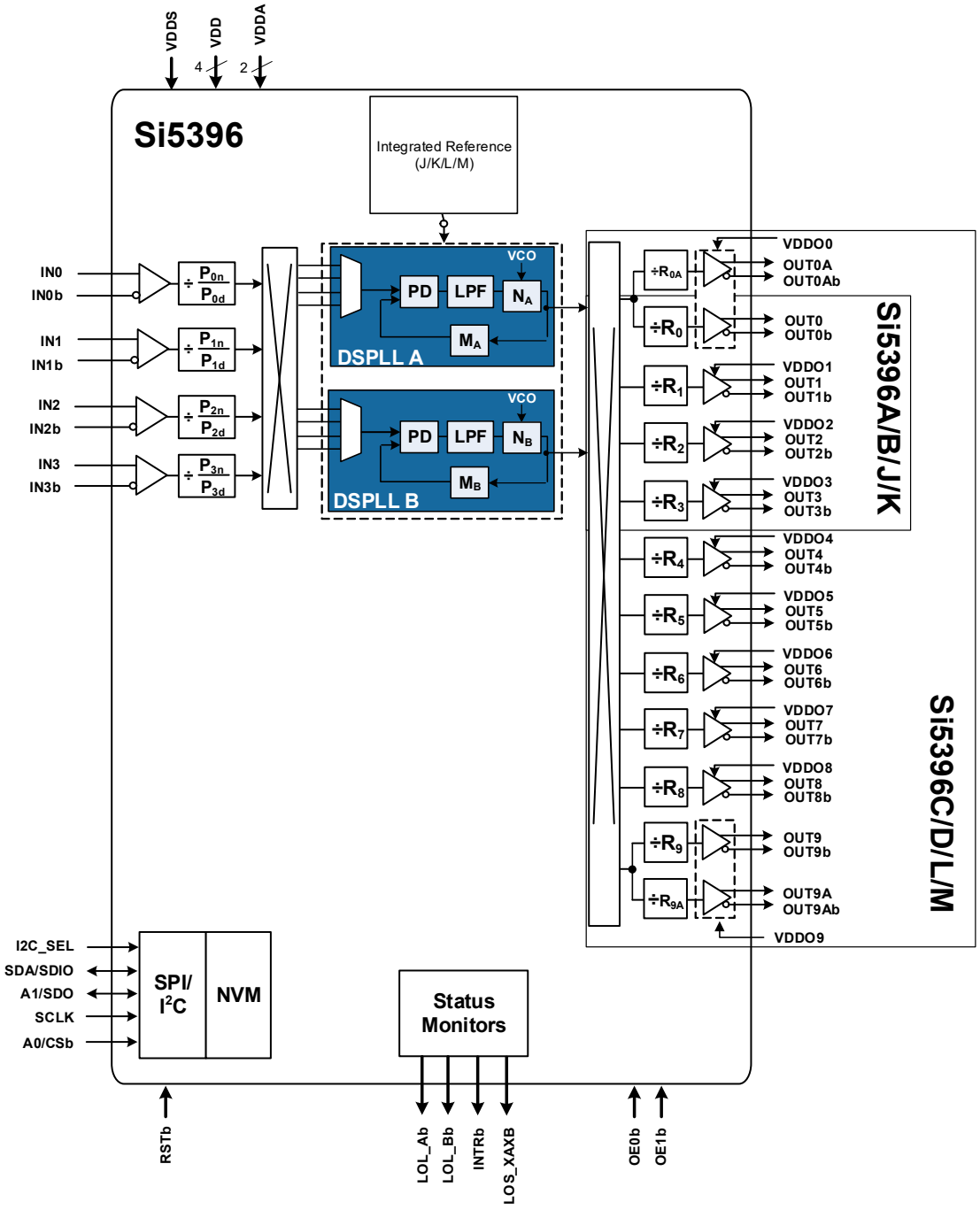


Figure 20. Si5396 Block Diagram

8. Typical Operating Characteristics (Jitter and Phase Noise)

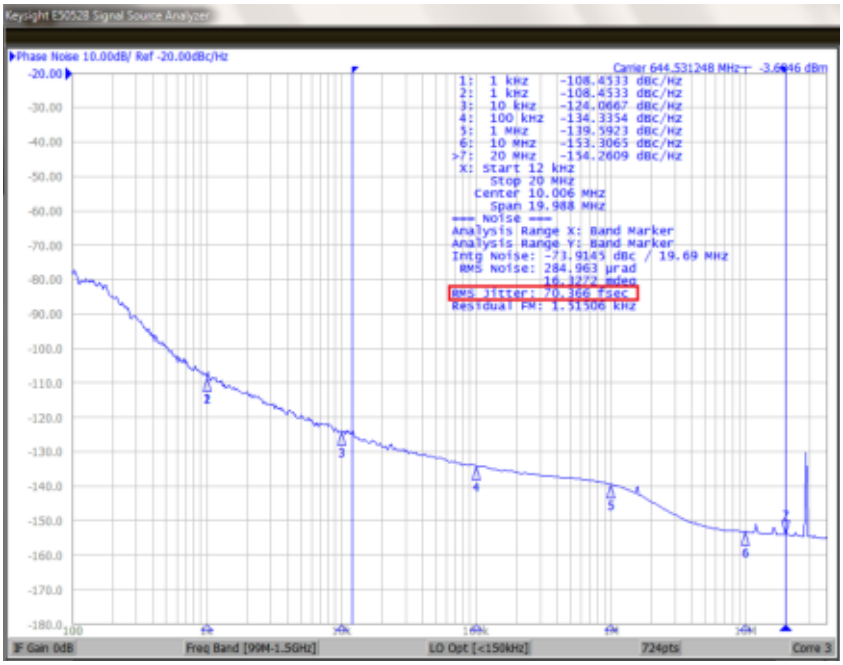


Figure 21. Input = 19.44 MHz; Output = 644.531248 MHz, 2.5 V LVDS

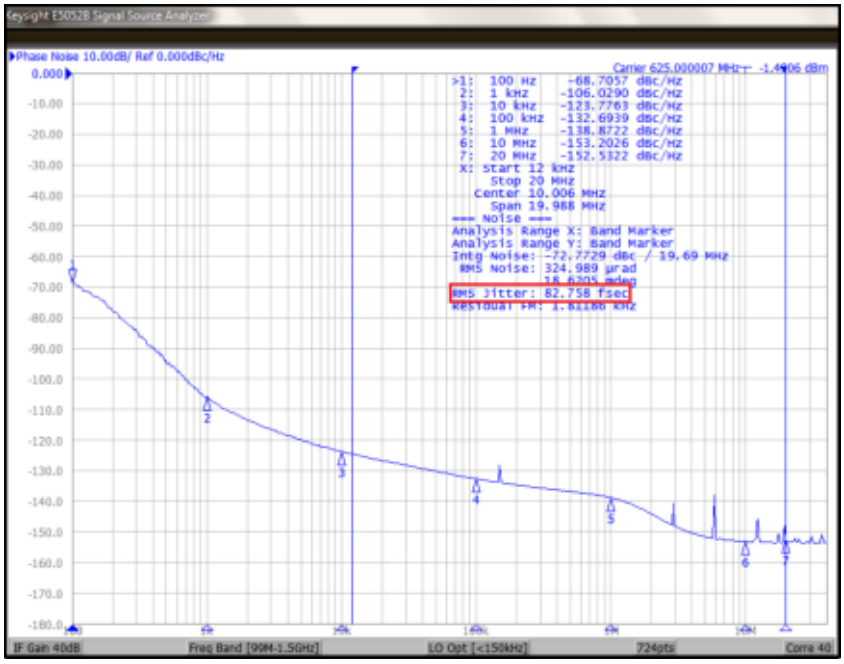


Figure 22. Input = 25 MHz; Output = 625 MHz, 2.5 V LVDS

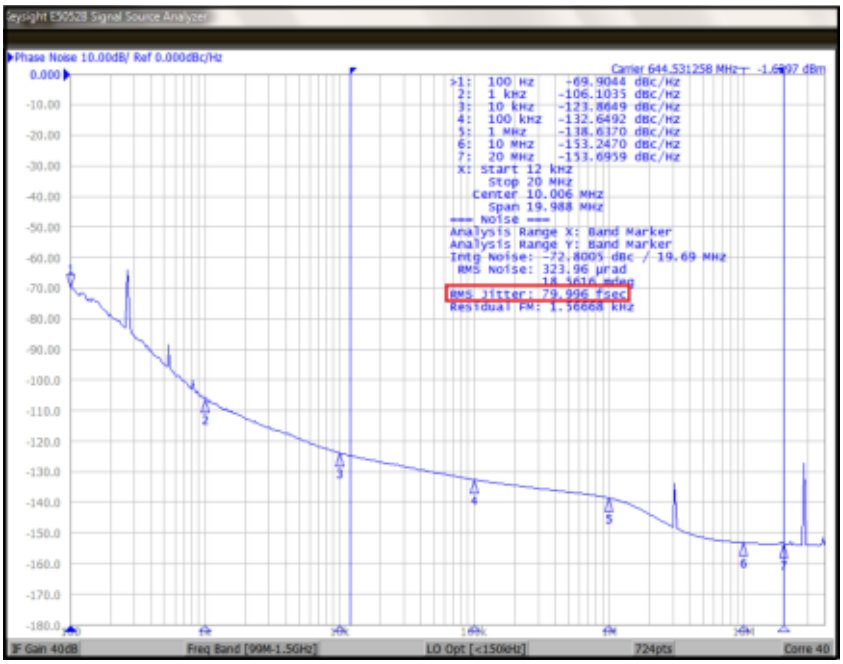


Figure 23. Input = 19.44 MHz; Output = 644.53125 MHz, 2.5 V LVDS

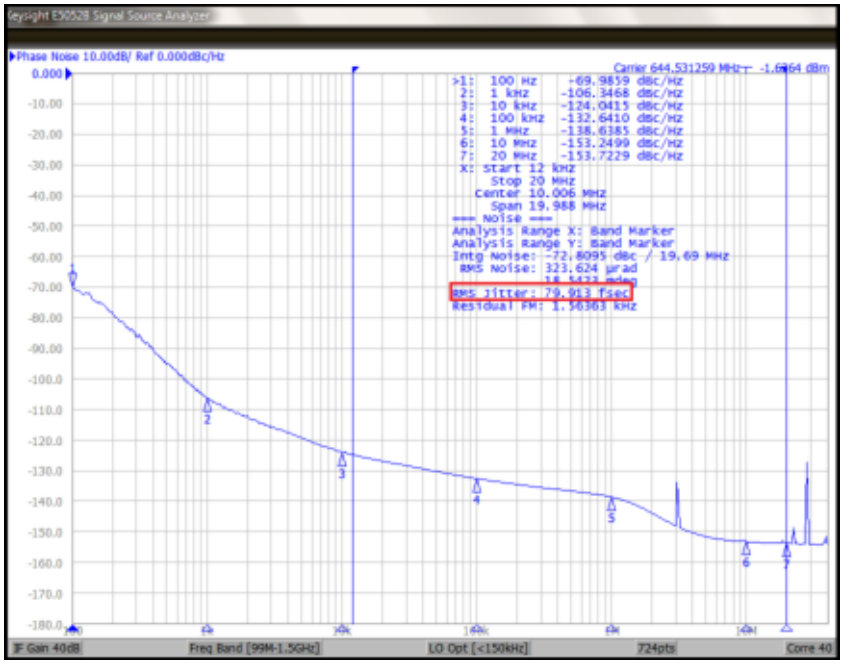


Figure 24. Input = 25 MHz; Output = 644.53125 MHz, 2.5 V LVDS

9. Pin Descriptions

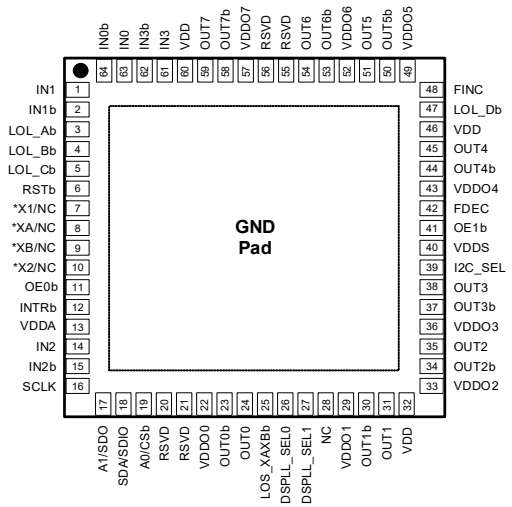


Figure 25. Si5397 A/B/J/K (64-QFN and 64-LGA) Top View

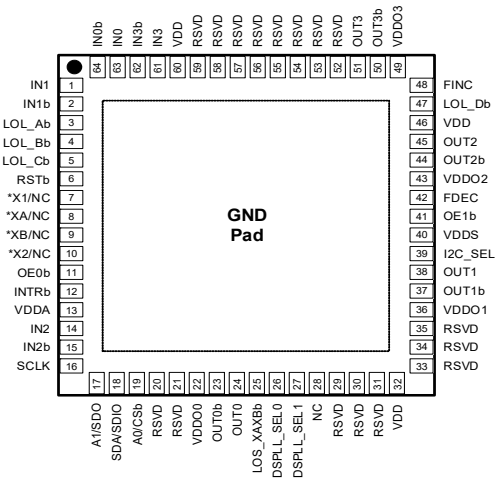


Figure 26. Si5397 C/D/L/M (64-QFN and 64-LGA) Top View

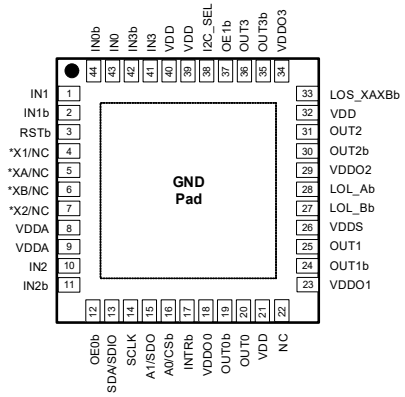


Figure 27. Si5396 A/B/J/K (44-QFN and 44-LGA) Top View

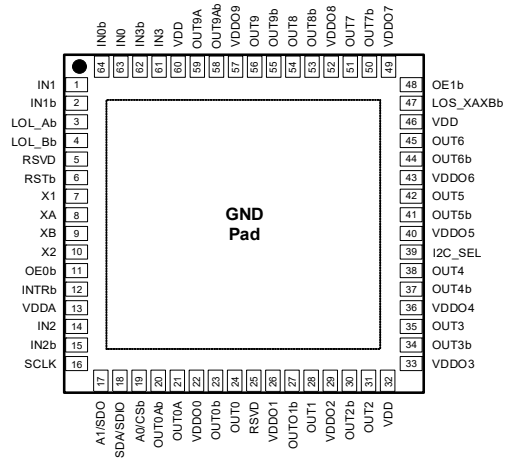


Figure 28. Si5396 C/D/L/M (64-QFN and 64-LGA) Top View

NOTE: Grades A/B/C/D require external references so these pins can be connected to those references (XTAL, XO, etc.). Connecting an external reference to a device that already has an internal reference is not recommended and could lead to internal damage to the circuits.

Table 22. Si5397/Si5396 Pin Descriptions[1]

Pin Name	Pin Number				Pin Type[2]	Function
	Si5397 A/B/J/K	Si5397 C/D/J/K	Si5396 A/B/J/K	Si5396 C/D/L/M		
Inputs						
XA/NC	8	8	5	8	I	**Crystal Input for Grade A/B/C/D** Input pins for external crystal (XTAL). Alternatively these pins can be driven with an external reference clock (REFCLK). An internal register bit selects XTAL or REFCLK mode. Default is XTAL mode. **NC (No-Connect) for Grades J/K/L/M** These devices have an integrated reference and these pins cannot be connected to an external reference. They should be left floating to avoid damage or interference to the internal reference.
XB/NC	9	9	6	9	I	
X1/NC	7	7	4	7	I	**XTAL Shield for Grade A/B/C/D** Connect these pins directly to the XTAL ground pins. X1, X2 and the XTAL ground pins should be separated from the PCB ground plane. Refer to the Si5397/96 Family Reference Manual for layout guidelines. **NC (No-Connect) for Grades J/K/L/M or external reference clocks** These pins should be left disconnected for Grades J/K/L/M with integrated reference or when connecting XA/XB pins to an external reference clock (REFCLK)
X2/NC	10	10	7	10	I	
IN0	63	63	43	63	I	**Clock Inputs** These pins accept an input clock for synchronizing the device. They support both differential and single-ended clock signals. Refer to the Si5397/96 Family Reference Manual for input termination options. These pins are high-impedance and must be terminated externally. The negative side of the differential input must be grounded through a capacitor when accepting a single-ended clock.
IN0b	64	64	44	64	I	
IN1	1	1	1	1	I	
IN1b	2	2	2	2	I	
IN2	14	14	10	14	I	
IN2b	15	15	11	15	I	
IN3	61	61	41	61	I	
IN3b	62	62	42	62	I	
Outputs						
OUT0Ab	—	—	—	20	O	**Output Clocks** These output clocks support a programmable signal swing and common mode voltage. Desired output signal format is configurable using register control. Termination recommendations are provided in the Si5397/96 Family Reference Manual. Unused outputs should be left unconnected.
OUT0A	—	—	—	21	O	
OUT0	24	24	20	24	O	
OUT0b	23	23	19	23	O	
OUT1	31	38	25	28	O	
OUT1b	30	37	24	27	O	
OUT2	35	45	31	31	O	
OUT2b	34	44	30	30	O	
OUT3	38	51	36	35	O	
OUT3b	37	50	35	34	O	
OUT4	45	—	—	38	O	
OUT4b	44	—	—	37	O	
OUT5	51	—	—	42	O	
OUT5b	50	—	—	41	O	
OUT6	54	—	—	45	O	
OUT6b	53	—	—	44	O	
OUT7	59	—	—	51	O	
OUT7b	58	—	—	50	O	
OUT8	—	—	—	54	O	
OUT8b	—	—	—	53	O	

Table 22. Si5397/Si5396 Pin Descriptions[1] (Continued)

Pin Name	Pin Number				Pin Type[2]	Function
	Si5397 A/B/J/K	Si5397 C/D/J/K	Si5396 A/B/J/K	Si5396 C/D/L/M		
OUT9	—	—	—	56	O	
OUT9b	—	—	—	55	O	
OUT9A	—	—	—	59	O	
OUT9Ab	—	—	—	58	O	
Serial Interface						
I2C_SEL	39	39	38	39	I	**I²C Select**[3] This pin selects the serial interface mode as I²C (I2C_SEL = 1) or SPI (I2C_SEL = 0). This pin is internally pulled high.
SDA/SDIO	18	18	13	18	I/O	**Serial Data Interface**[3] This is the bidirectional data pin (SDA) for the I²C mode, or the bidirectional data pin (SDIO) in the 3-wire SPI mode, or the input data pin (SDI) in 4- wire SPI mode. When in I2C mode, this is an open-drain output and must be pulled-up using an external resistor of at least1 kΩ. No pull-up resistor is needed when in SPI mode, as the output is a push- pull driver. Tie low when unused.
A1/SDO	17	17	15	17	I/O	**Address Select 1/Serial Data Output**[3] In I²C mode, this pin is open-drain and functions as the A1 address input pin. It does not have an internal pull-up or pull-down resistor. In 4-wire SPI mode this output is a push-pull driver and functions as the serial data output (SDO) pin. It drives high to the voltage selected by the IO_VDD_SEL bit. Leave disconnected when unused.
SCLK	16	16	14	16	I	**Serial Clock Input**[3] This pin functions as the serial clock input for both I²C and SPI modes. When in I²C mode, this pin must be pulled-up using an external resistor of at least 1 kΩ. No pull-up resistor is needed when in SPI mode.
A0/CSb	19	19	16	19	I	**Address Select 0/Chip Select**[3] This pin functions as the hardware controlled address A0 in I²C mode. In SPI mode, this pin functions as the chip select input (active low). This pin is internally pulled-up.
Control Status						
INTRb	12	12	17	12	O	**Interrupt**[3] This pin is asserted low when a change in device status has occurred. It should be left unconnected when not in use.
RSTb	6	6	3	6	I	**Device Reset**[3] Active low input that performs power-on reset (POR) of the device. Resets all internal logic to a known state and forces the device registers to their default values. Clock outputs are disabled during reset. This pin is internally pulled-up and can be left unconnected when not in use.
OE0b	11	12	12	11	I	**Output Enable 0**[3] This pin is used to enable (when held low) and disable (when held high) the output clocks. By default this pin controls all outputs. It can also be configured to control a subset of outputs. See 4.9.7. Output Enable/Disable for details. This pin is internally pulled-down.
OE1b	41	41	—	48		**Output Enable 1 (Si5397)**[4] This is an additional output enable pin that can be configured to control a subset of outputs. By default it has no control on the outputs until configured. See 4.9.7. Output Enable/Disable for details. There is no internal pull-up/pull- down for this pin. This pin must be pulled up or down externally (do not leave floating when not in use).
	—	—	37			**Output Enable 1 (Si5396)**[3] This is an additional output enable pin that can be configured to control a subset of outputs. By default it has no control on the outputs until configured. See 4.9.7. Output Enable/Disable for details. This pin is internally pulled-down.
LOL_Ab	3	3	28	3	O	**Loss Of Lock_A/B/C/D**[3,4] These output pins indicate when DSPLL A, B, C, D is out-of-lock (low) or locked (high). They can be left unconnected when not in use. Si5397: see note 3, Si5396: see note 4.
LOL_Bb	4	4	27	4	O	
LOL_Cb	5	5	—	—	O	
LOL_Db	47	47	—	—	O	

Table 22. Si5397/Si5396 Pin Descriptions[1] (Continued)

Pin Name	Pin Number				Pin Type[2]	Function
	Si5397 A/B/J/K	Si5397 C/D/J/K	Si5396 A/B/J/K	Si5396 C/D/L/M		
LOS_XAXBb	25	25	33	47	O	**Status Pins[3]** This pin indicates a loss of signal alarm on the XA/XB pins. This either indicates a XTAL failure or a loss of external signal on the XA/XB pins. This pin can be left unconnected when unused.
DSPLL_SEL0	26	26	—		I	**DSPLL Select Pins (Si5397 only)[3]** These pins are used in conjunction with the FINC and FDEC pins. The DSPLL_SEL[1:0] pins determine which DSPLL is affected by a frequency change using the FINC and FDEC pins. See 4.5. Digitally Controlled Oscillator (DCO) Mode for details. These pins are internally pulled-down.
DSPLL_SEL1	27	27	—		I	
FDEC	42	42	—		I	**Frequency Decrement Pin (Si5397 only)[4]** This pin is used to step-down the output frequency of a selected DSPLL. The frequency change step size is register configurable. The DSPLL that is affected by the frequency change is determined by the DSPLL_SEL[1:0] pins. This pin must be pulled up or down externally (do not leave floating when not in use).
FINC	48	48	—		I	**Frequency Increment Pin (Si5397 only)[3]** This pin is used to step-up the output frequency of a selected DSPLL. The frequency change step size is register configurable. The DSPLL that is affected by the frequency change is determined by the DSPLL_SEL[1:0] pins. This pin is pulled low internally and can be left unconnected when not in use.
RSVD	20	20	—	5	—	**Reserved** These pins are connected to the die. Leave disconnected.
	21	21	—	25	—	
	—	29	—	—	—	
	—	30	—	—	—	
	—	31	—	—	—	
	—	33	—	—	—	
	—	34	—	—	—	
	—	35	—	—	—	
	—	52	—	—	—	
	—	53	—	—	—	
	—	54	—	—	—	
	55	55	—	—	—	
	56	56	—	—	—	
	—	57	—	—	—	
	—	58	—	—	—	
	—	59	—	—	—	
NC	28	28	22		—	**No Connect** These pins are not connected to the die. Leave disconnected.
Power						
VDD	32	21	21	32	P	**Core Supply Voltage** The device operates from a 1.8 V supply. Refer to the Si5397/96 Family Reference Manual for power supply filtering recommendations. A 0402 1 µF capacitor should be placed very near each of these pins.
	46	46	32	46		
	60	60	39	60		
	—	—	40	—		
VDDA	13	13	8	13	P	**Core Supply Voltage 3.3 V** This core sup- ply pin requires a 3.3 V power source. See the Si5397/96 Family Reference Manual for power supply filtering recommendations. A 0402 1 µF capacitor should be placed very near each of these pins.
	—	—	9	—		
VDDS	40	40	26	—	P	**Status Output Voltage** The voltage on this pin determines VOL/VOH on the Si5396 LOL_Ab and LOL_Bb outputs. On the Si5397, this pin determines VIL/VIH for the FDEC and OE1b inputs. Connect to either 3.3 V or 1.8 V. A 0.1 µF bypass capacitor should be placed very close to this pin.

Table 22. Si5397/Si5396 Pin Descriptions[1] (Continued)

Pin Name	Pin Number				Pin Type[2]	Function
	Si5397 A/B/J/K	Si5397 C/D/J/K	Si5396 A/B/J/K	Si5396 C/D/L/M		
VDDO0	22	22	18	22	P	**Output Clock Supply Voltage 0 to 7** Supply voltage (3.3 V, 2.5 V, 1.8 V) for OUTn, OUTnb outputs. A 0.1 uF bypass capacitor should be placed very close to this pin. Leave VDDO pins of unused output drivers unconnected. An alternate option is to connect the VDDO pin to a power supply and disable the output driver to minimize current consumption. A 0402 1 µF capacitor should be placed very near each of these pins.
VDDO1	29	36	23	26	P	
VDDO2	33	43	29	29	P	
VDDO3	36	49	34	33	P	
VDDO4	43	—	—	36	P	
VDDO5	49	—	—	40	P	
VDDO6	52	—	—	43	P	
VDDO7	57	—	—	49	P	
VDDO8				52	P	
VDDO9				57	P	
GND PAD	—	—	—	—	P	**Ground Pad** This pad provides connection to ground and must be connected for proper operation. Use as many vias as practical and keep the via length to an internal ground plane as short as possible.

1. Refer to the Si5397/96 Family Reference Manual for more information on register setting names.
2. I = Input, O = Output, P = Power.
3. The IO_VDD_SEL control bit (0x0943 bit 0) selects 3.3 V or 1.8 V operation.
4. The voltage on the VDDS pin(s) determines 3.3 V or 1.8 V operation.

NOTE: All status pins except I^2C and SPI are push-pull.

10. Packaging

10.1. Package Outlines

10.1.1. Si5397 A/B/C/D and Si5396 C/D (External Reference) 9 x 9 mm 64-QFN Package

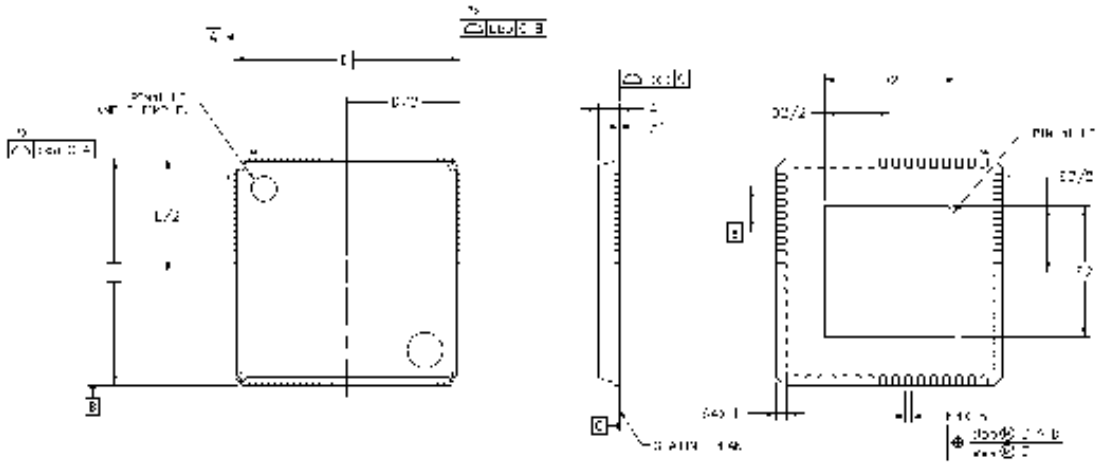


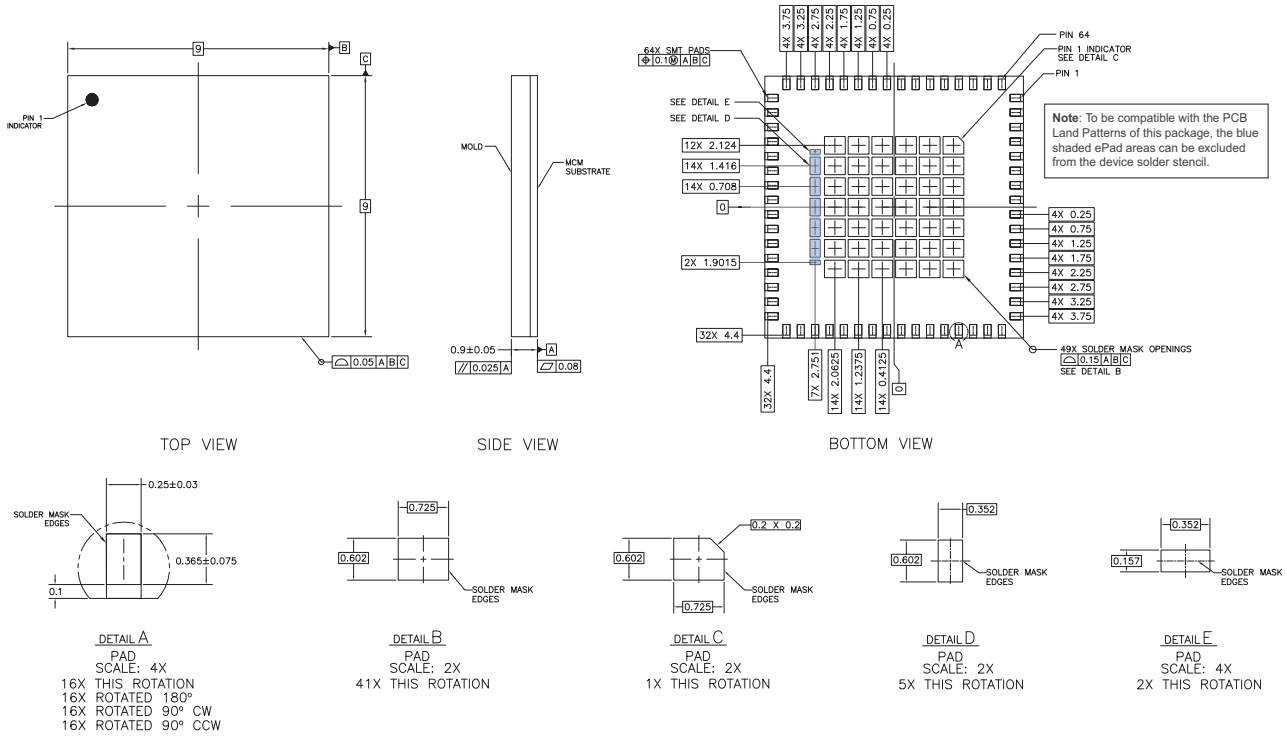
Figure 29. Si5397 A/B/C/D and Si5396 C/D (External Reference) Package Diagram

Table 23. Si5397 A/B/C/D and Si5396 C/D (External Reference) Package Dimensions[1]

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0	0.02	0.05
b	0.18	0.25	0.30
D		9 BSC	
D2	5.10	5.20	5.30
e		0.50 BSC	
E		9 BSC	
E2	5.10	5.20	5.30
L	0.30	0.40	0.50
aaa	—	—	0.15
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10

1. All dimensions shown are in millimeters (mm) unless otherwise noted. Dimensioning and tolerancing per ANSI Y14.5M-1994. This drawing conforms to JEDEC Solid State Outline MO-220. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for small body components.

10.1.2. Si5397 J/K/L/M and Si5396 L/M (Internal Reference) 9 x 9 mm 64-LGA Package



NOTE: Unless otherwise specified, dimensioning and tolerance in accordance with ASME Y14.5M-1994.

Figure 30. Si5397 J/K/L/M and Si5396 L/M (Internal Reference) Package Diagram

Table 24. Si5397 J/K/L/M and Si5396 L/M (Internal Reference) Package Dimensions

Dimension	Symbol	Min	Typ	Max
Total Thickness	A	0.85	0.90	0.95
Substrate Thickness			0.25 REF	
Mold Thickness			0.65 REF	
Solder Mask Thickness			0.015 REF	
Exposed Pad Grid Opening	Detail B		0.602 x 0.725 REF	
	Detail C		0.602 x 0.725 REF	
	Detail D		0.602 x 0.352 REF	
	Detail E		0.157 x 0.352 REF	
Body Size	B		9.0 BSC	
	C		9.0 BSC	
Lead Pitch			0.5 BSC	
Lead Length	Detail A	0.29	0.365	0.44
Lead Width		0.22	0.25	0.28
Package Edge Tolerance		0.05		
Mold Flatness		0.025		
Coplanarity		0.08		
Lead Pullback from PKG Edge		0.1		

10.1.3. Si5396 A/B (External Reference) 7 x 7 mm 44-QFN Package

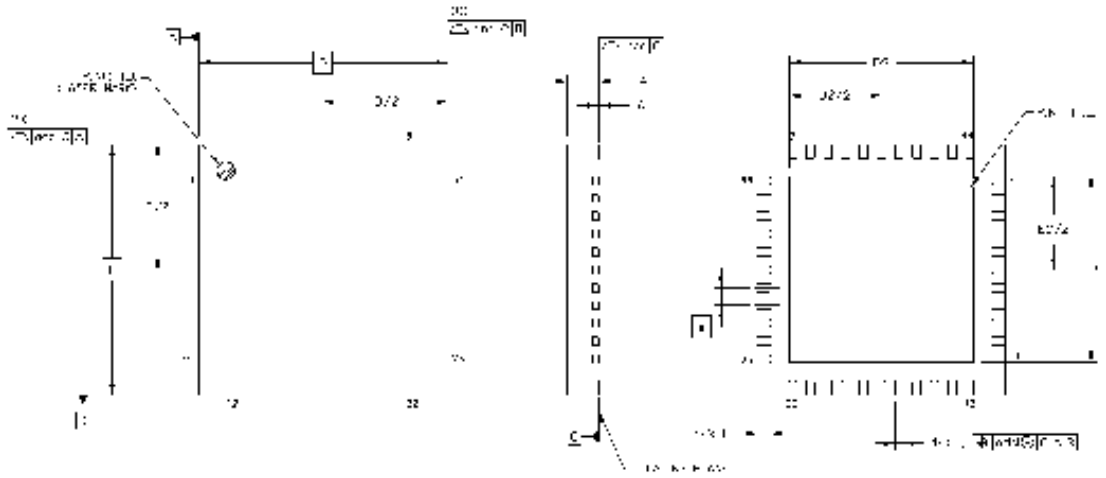


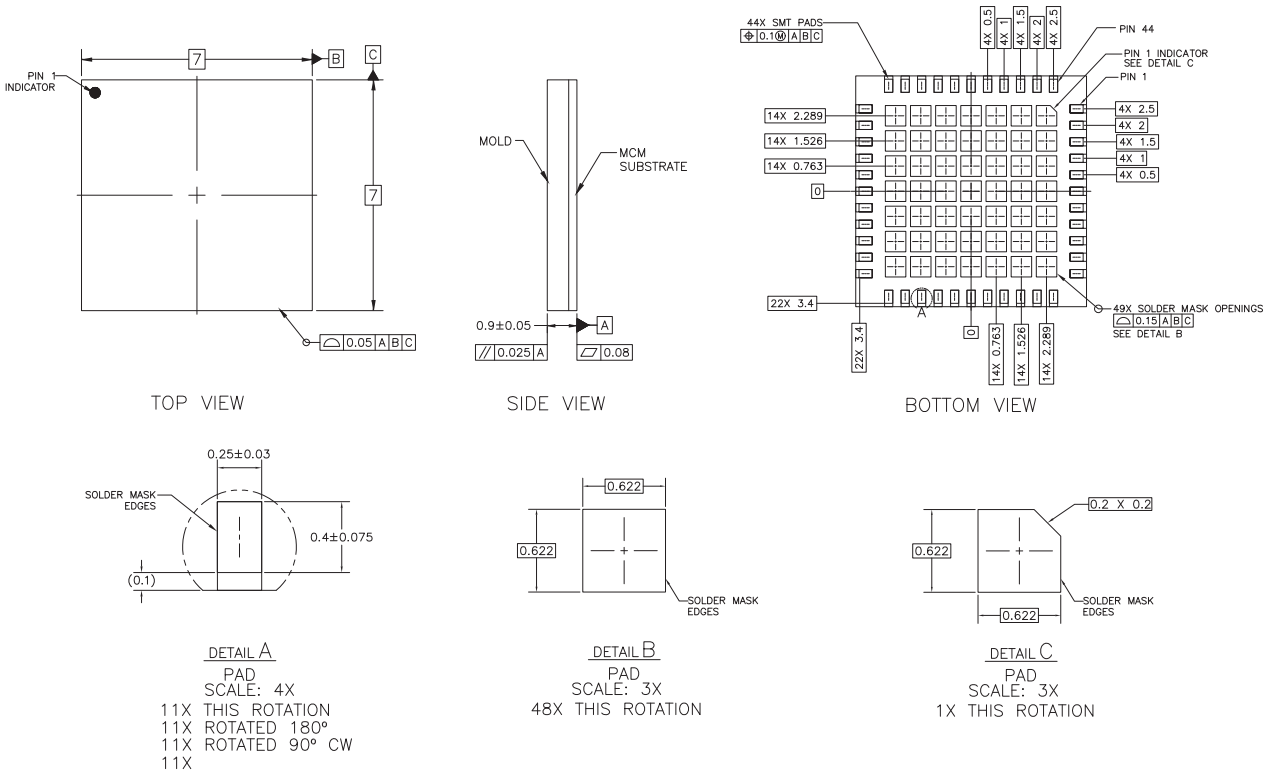
Figure 31. Si5396 A/B (External Reference) Package Diagram

Table 25. Si5396 A/B (External Reference) Package Dimensions[1]

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0	0.02	0.05
b	0.18	0.25	0.30
D		7 BSC	
D2	5.10	5.20	5.30
e		0.50 BSC	
E		7 BSC	
E2	5.10	5.20	5.30
L	0.30	0.40	0.50
aaa	—	—	0.15
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10

1. All dimensions shown are in millimeters (mm) unless otherwise noted. Dimensioning and tolerancing per ANSI Y14.5M-1994. This drawing conforms to JEDEC Solid State Outline MO-220. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for small body components.

10.1.4. Si5396 J/K (Internal Reference) 7 x 7 mm 44-LGA Package



NOTE: Unless otherwise specified, dimensioning and tolerance in accordance with ASME Y14.5M-1994.

Figure 32. Si5396 J/K (Internal Reference) Package Diagram

Table 26. Si5396 J/K (Internal Reference) Package Dimensions

Dimensions	Symbol	Min	Typ	Max
Total Thickness	A	0.85	0.90	0.95
Substrate Thickness			0.25 REF	
Mold Thickness			0.65 REF	
Solder Mask Thickness			0.015 REF	
Exposed Pad Grid Opening	Detail B		0.622x0.622 REF	
	Detail C			
Body Size	B		7.0 BSC	
	C		7.0 BSC	
Lead Pitch			0.5 BSC	
Lead Length	Detail A	0.325	0.4	0.475
Lead Width		0.22	0.25	0.28
Package Edge Tolerance		0.05		
Mold Flatness		0.025		
Coplanarity		0.08		
Lead Pullback from PKG Edge		0.1		

10.2. PCB Land Pattern

The figure below illustrates the PCB land pattern details for the devices. The table below lists the values for the dimensions shown in the illustration. Refer to the Si5397/96 Family Reference Manual for information about thermal via recommendations.

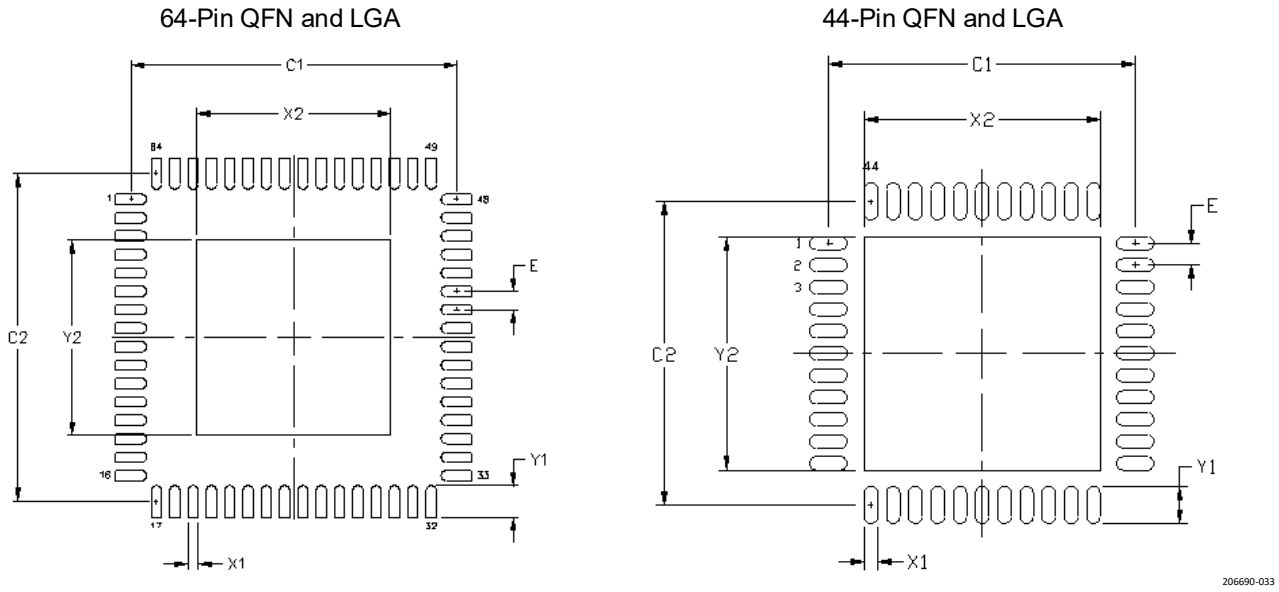


Figure 33. Si5397/Si5396 PCB Land Patterns

Table 27. Si5397/Si5396 PCB Land Pattern Dimensions

Dimensions	Si5397 (Max)	Si5396 (Max)	Notes
C1	8.90	6.90	**General** All dimensions shown are in millimeters (mm). This Land Pattern Design is based on the IPC-7351 guidelines. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a fabrication allowance of 0.05 mm. **Solder Mask Design** All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 mm minimum, all the way around the pad. **Stencil Design** A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release. The stencil thickness should be 0.125 mm (5 mils). The ratio of stencil aperture to land pad size should be 1:1 for all pads. The stencil design will need to match the respective ground pads as shown in the Package outline. The stencil aperture to land pad size recommendation is 70% paste coverage. **Card Assembly** A No-Clean, Type-3 solder paste is recommended. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for small body components.
C2	8.90	6.90	
E	0.50	0.50	
X1	0.30	0.30	
Y1	0.85	0.85	
X2	5.30	5.30	
Y2	5.30	5.30	

10.3. Top Marking



Figure 34. Si5396C/D and Si5397A/B/C/D QFN 9x9 mm Package



Figure 35. Si5396A/B – QFN 7x7 mm Package, SI5396J/K – LGA 7x7 mm Package, Si5396L/M and Si5397J/K/L/M – LGA 9x9 mm Package

Table 28. Si5397/Si5396 Top Marking Explanation

Line	Characters	Description
1	Si5397g- Si5396g-	Base part number and device grade: Si5397: Quad PLL Si5396: Dual PLL g = Device Grade (A/B/C/D/J/K/L/M). See 3. Ordering Guides for more information. – = Dash character.
2	Rxxxxx-GM	R = Product revision. (Refer to See 3. Ordering Guides for latest revision). xxxxx = Customer specific NVM sequence number. Optional NVM code as- signed for custom, factory pre-programmed devices. Characters are not included for standard, factory default configured devices. See 3. Ordering Guides for more information. -GM = Package (QFN/LGA) and temperature range (–40 to +85 °C)
3	YYWWTTTTTT	YYWW = Characters correspond to the year (YY) and work week (WW) of package assembly. TTTTTT = Manufacturing trace code.
4	CC	CC = country of origin (ISO Abbreviation) = KR (South Korea) or TW (Taiwan).

11. Revision History

Revision	Date	Description
A	February, 2025	• Section 10.1.2 Si5397 J/K/L/M and Si5396 L/M (Internal Reference) 9 x 9 mm 64-LGA Package. - Updated the package diagram in Figure 30. - Updated the package dimensions in Table 24. • Section 10.1.4 Si5396 J/K (Internal Reference) 7 x 7 mm 44-LGA Package. - Updated the package diagram in Figure 32. - Updated the package dimensions in Table 26. • Section 10.3 Top Marking. - Updated the top marking in Figure 38. - Updated the country of origin explanation in Table 29.
1.2	January, 2021	• Launch of Si5396C/D/L/M 2-PLL, 12-output grade option.
1.1	July, 2020	• Reduced maximum Phase jitter spec from 140 fs to 125 fs based on additional characterization data. • The single center pad on the 7 x 7 mm 44-LGA Package is divided by solder-mask into 9 pads (3 x 3 grid array) to increase mechanical support to the center of the package-there is no change to the PCB layout made or to any of the metal layers of the package.
1.0	June, 2019	• Add Integrated reference options J/K/L/M • Updated Figure 4.3. Crystal Resonator and External Reference Clock Connection Options • Table 5.2 DC Characteristics - Core supply current IDD/IDDA limits clarified for each device - Output Buffer supply conditions clarified - Total power dissipation numbers updated - Updated test configuration diagrams • Table 5.3 Input clock specifications - Updated Input voltage section of "LVCMOS / Pulsed CMOS DC-Coupled Input Buffer" to include standard CMOS • Table 5.5 Differential Clock Output Specifications - Increased max Rise and Fall times from 150ps to 200ps based on final characterization • Table 5.6. LVCMOS Clock Output Specifications - Updated Min and Max limits for duty cycle - Updated test configuration diagrams • Table 5.8. Performance Characteristics - Updated hitless switching specifications • Updated Table 5.10. SPI Timing Specifications (4-Wire) table and timing diagram • Updated Table 5.11. SPI Timing Specifications (3-Wire) • Changed NC/XA, NC/XB, NC/X1, NC/X2 to XA, XB, X1, X2 respectively since integrated crystal devices are getting their own data sheet
0.96	June, 2018	• Preliminary data sheet

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