# Ultra Series™ Crystal Oscillator (VCXO) Si565 Data Sheet

## Ultra Low Jitter Any-Frequency VCXO (100 fs), 0.2 to 3000 MHz

The Si565 Ultra Series™ voltage-controlled crystal oscillator utilizes Skyworks Solutions' advanced 4th generation DSPLL® technology to provide an ultra-low jitter, low phase noise clock at any output frequency. The device is factory-programmed to any frequency from 0.2 to 3000 MHz with <1 ppb resolution and maintains exceptionally low jitter for both integer and fractional frequencies across its operating range. On-chip power supply filtering provides industry-leading power supply noise rejection, simplifying the task of generating low jitter clocks in noisy systems that use switched-mode power supplies. Offered in industry-standard footprints, the Si565 has a dramatically simplified supply chain that enables Silicon Labs to ship custom frequency samples 1-2 weeks after receipt of order. Unlike a traditional XO, where a different crystal is required for each output frequency, the Si565 uses one simple crystal and a DSPLL IC-based approach to provide the desired output frequency. The Si565 is factory-configurable for a wide variety of user specifications, including frequency, output format, and OE pin location/polarity. Specific configurations are factory-programmed at time of shipment, eliminating the long lead times associated with custom oscillators.

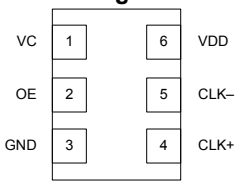



5 x 7 mm and 3.2 x 5 mm



2.5 x 3.2 mm

**Pin Assignments**




(Top View)

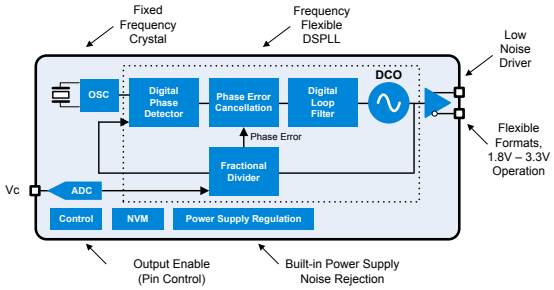
**KEY FEATURES**

- Available with any frequency from 200 kHz to 3000 MHz
- Ultra low jitter: 100 fs RMS typical (12 kHz – 20 MHz)
- Excellent PSNR and supply noise immunity: –80 dBc Typ
- 3.3 V, 2.5 V and 1.8 V $V_{DD}$ supply operation from the same part number
- LVPECL, LVDS, CML, HCSL, CMOS, and Dual CMOS output options
- 2.5x3.2, 3.2x5, 5x7 mm package options
- Samples available with 1-2 week lead times

**APPLICATIONS**

- 100G/200G/400G OTN, coherent optics
- 10G/25G/40G/100G Ethernet
- 56G/112G PAM4 clocking
- 3G-SDI/12G-SDI/24G-SDI broadcast video
- Servers, switches, storage, NICs, search acceleration
- Test and measurement
- FPGA/ASIC clocking

| Pin # | Descriptions |
|---|---|
| 1 | VC = Voltage Control Pin |
| 2 | OE = Output enable |
| 3 | GND = Ground |
| 4 | CLK+ = Clock output |
| 5 | CLK- = Complementary clock output. Not used for CMOS. |
| 6 | VDD = Power supply |



# 1. Ordering Guide

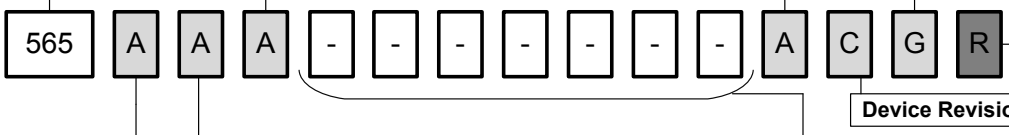
The Si565 VCXO supports a variety of options including frequency, output format, and OE pin location/polarity, as shown in the chart below. Specific device configurations are programmed into the part at time of shipment, and samples are available in 1-2 weeks. Skyworks Solutions provides an online part number configuration utility to simplify this process. Refer to https://www.skyworksinc.com/en/Products/Timing-Oscillators to access this tool and for further ordering instructions.

| VCXO Series | Description |
|---|---|
| 565 | Single Frequency VCXO |

| Code | OE Pin | OE Polarity |
|---|---|---|
| A | Pin 2 | Active High |
| B | Pin 2 | Active Low |

| | Package |
|---|---|
| A | 5x7 mm |
| B | 3.2x5 mm |
| C | 2.5x3.2 mm |

| | Temperature Grade |
|---|---|
| G | -40 to 85 °C |




Device Revision

| Code | Reel |
|---|---|
| R | Tape and Reel |
| <Blank> | Coil Tape |

| Signal Format | VDD Range | Order Option |
|---|---|---|
| LVPECL | 2.5, 3.3 V | A |
| LVDS | 1.8, 2.5, 3.3 V | B |
| CMOS | 1.8, 2.5, 3.3 V | C |
| CML | 1.8, 2.5, 3.3 V | D |
| HCSL | 1.8, 2.5, 3.3 V | E |
| Dual CMOS (In-Phase) | 1.8, 2.5, 3.3 V | F |
| Dual CMOS (Complementary) | 1.8, 2.5, 3.3 V | G |
| HCSL-Fast | 1.8, 2.5, 3.3 V | H |
| Custom | 1.8, 2.5, 3.3 V | X |

| | Temperature Stability = ± 20 ppm | | | |
|---|---|---|---|---|
| | Vc Tuning Slope Kv [ppm/V] | Min APR [± ppm] at VDD [3] | | |
| | | 3.3V | 2.5V | 1.8V |
| A | 60 | 20 | -- | -- |
| B | 75 | 40 | 20 | -- |
| C | 105 | 70 | 40 | 20 |
| D | 150 | 115 | 75 | 45 |
| E | 180 | 145 | 100 | 65 |
| F | 225 | 190 | 135 | 85 |

| Frequency Code [2] | Description |
|---|---|
| Mxxxxxx | $F_{CLK} < 1$ MHz |
| xMxxxxx | 1 MHz ≤ $F_{CLK} < 10$ MHz |
| xxMxxxx | 10 MHz ≤ $F_{CLK} < 100$ MHz |
| xxxMxxx | 100 MHz ≤ $F_{CLK} < 1000$ MHz |
| xxxxMxx | 1000 MHz ≤ $F_{CLK} < 3000$ MHz |
| xxxxxx | Custom code if $F_{CLK} >$ 6 digits |

**Notes:**

1. Contact Skyworks for non-standard configurations.
2. Create custom part numbers at https://www.skyworksinc.com/en/Products/Timing-Oscillators.
3. Min Absolute Pull Range (APR) includes temp stability, initial accuracy, load pulling, VDD variation, and 20 year aging at 70 °C.
   a. For best jitter and phase noise performance, always choose the smallest Kv that meets the application's minimum APR requirements. Unlike SAW-based solutions which require higher Kv values to account for their higher temperature dependence, the Si56x series provides lower Kv options to minimize noise coupling and jitter in real-world PLL designs.
   b. APR is the ability of a VCXO to track a signal over the product lifetime. A VCXO with an APR of ±20 ppm is able to lock to a clock with a ±20 ppm stability over 20 years over all operating conditions.
   c. APR (±) = (0.5 x VDD x tuning slope) - (initial accuracy + temp stability + load pulling + VDD variation + aging).
   d. Minimum APR values noted above include absolute worst case values for all parameters.
   e. See application note, "AN266: VCXO Tuning Slope (Kv), Stability, and Absolute Pull Range (APR)" for more information.

## 1.1 Technical Support

| | |
|---|---|
| Oscillator Phase Noise Lookup Utility | https://www.skyworksinc.com/tools/oscillator-phase-noise |
| Quality and Reliability | https://www.skyworksinc.com/quality |
| Development Kits | https://www.skyworksinc.com/en/Products/Timing |

## 2. Electrical Specifications

**Table 2.1. Electrical Specifications**

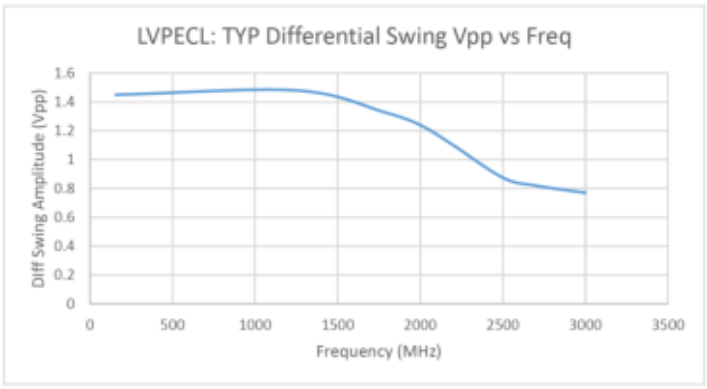
$V_{DD}$ = 1.8 V, 2.5 or 3.3 V ± 5%, $T_A$ = –40 to 85 ºC

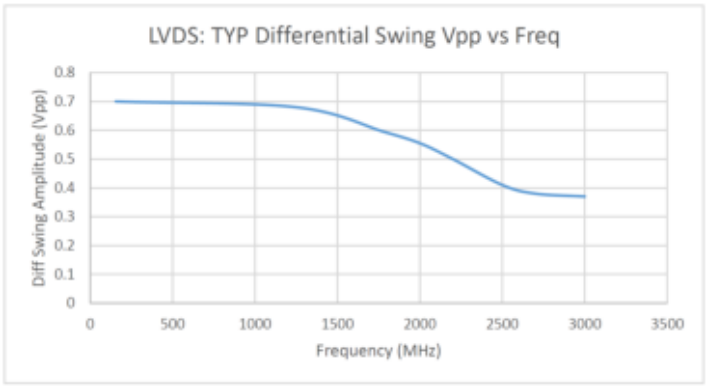
| Parameter | Symbol | Test Condition/Comment | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Temperature Range | $T_A$ | | –40 | — | 85 | ºC |
| Frequency Range | $F_{CLK}$ | LVPECL, LVDS, CML | 0.2 | — | 3000 | MHz |
| | | HCSL | 0.2 | — | 400 | MHz |
| | | CMOS, Dual CMOS | 0.2 | — | 250 | MHz |
| Supply Voltage | $V_{DD}$ | 3.3 V | 3.135 | 3.3 | 3.465 | V |
| | | 2.5 V | 2.375 | 2.5 | 2.625 | V |
| | | 1.8 V | 1.71 | 1.8 | 1.89 | V |
| Supply Current | $I_{DD}$ | LVPECL (output enabled) | — | 120 | 170 | mA |
| | | LVDS/CML (output enabled) | — | 100 | 140 | mA |
| | | HCSL (output enabled) | — | 95 | 140 | mA |
| | | HCSL-Fast (output enabled) | — | 103 | 152 | mA |
| | | CMOS (output enabled) | — | 95 | 145 | mA |
| | | Dual CMOS (output enabled) | — | 105 | 155 | mA |
| | | Tristate Hi-Z (output disabled) | — | 83 | — | mA |
| Temperature Stability[1] | | -40 to 85 °C | –20 | — | 20 | ppm |
| Rise/Fall Time (20% to 80% $V_{PP}$) | $T_R/T_F$ | LVPECL/LVDS/CML | — | — | 350 | ps |
| | | CMOS / Dual CMOS ($C_L$ = 5 pF) | — | 0.5 | 1.5 | ns |
| | | HCSL, $F_{CLK}$ > 50 MHz | — | — | 550 | ps |
| | | HCSL-Fast, $F_{CLK}$ > 50 MHz | — | — | 275 | ps |
| Duty Cycle | $D_C$ | All formats | 45 | — | 55 | % |
| Output Enable (OE)[2] | $V_{IH}$ | | 0.7 × $V_{DD}$ | — | — | V |
| | $V_{IL}$ | | — | — | 0.3 × $V_{DD}$ | V |
| | $T_D$ | Output Disable Time, $F_{CLK}$ > 10 MHz | — | — | 3 | µs |
| | $T_E$ | Output Enable Time, $F_{CLK}$ > 10 MHz | — | — | 20 | µs |
| Powerup Time | $t_{OSC}$ | Time from 0.9 × $V_{DD}$ until output frequency ($F_{CLK}$) within spec | — | — | 10 | ms |
| Powerup VDD Ramp Rate | $V_{RAMP}$ | Fastest $V_{DD}$ ramp rate allowed on startup | — | — | 100 | V/ms |
| LVPECL Output Option[3] | $V_{OC}$ | Mid-level | $V_{DD}$ – 1.42 | — | $V_{DD}$ – 1.25 | V |
| | $V_O$ | Swing (diff, $F_{CLK}$ ≤ 1.5 GHz) | 1.1 | — | 1.9 | $V_{PP}$ |
| | | Swing (diff, $F_{CLK}$ > 1.5 GHz)[6] | 0.55 | — | 1.7 | $V_{PP}$ |

| Parameter | Symbol | Test Condition/Comment | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| LVDS Output Option[4] | $V_{OC}$ | Mid-level (2.5 V, 3.3 V VDD) | 1.125 | 1.20 | 1.275 | V |
| | | Mid-level (1.8 V VDD) | 0.8 | 0.9 | 1.0 | V |
| | $V_O$ | Swing (diff, $F_{CLK}$ ≤ 1.4 GHz) | 0.6 | 0.7 | 0.9 | $V_{PP}$ |
| | | Swing (diff, $F_{CLK}$ > 1.4 GHz)[6] | 0.25 | 0.5 | 0.8 | $V_{PP}$ |
| HCSL Output Option[5]<br>HCSL-Fast Output Option[5] | $V_{OH}$ | Output voltage high | 660 | 800 | 850 | mV |
| | $V_{OL}$ | Output voltage low | –150 | 0 | 150 | mV |
| | $V_C$ | Crossing voltage | 250 | 410 | 550 | mV |
| CML Output Option (AC-Coupled) | $V_O$ | Swing (diff, $F_{CLK}$ ≤ 1.5 GHz) | 0.6 | 0.8 | 1.0 | $V_{PP}$ |
| | | Swing (diff, $F_{CLK}$ > 1.5 GHz)[6] | 0.3 | 0.55 | 0.9 | $V_{PP}$ |
| CMOS Output Option | $V_{OH}$ | $I_{OH}$ = 8/6/4 mA for 3.3/2.5/1.8 V VDD | 0.85 × $V_{DD}$ | — | — | V |
| | $V_{OL}$ | $I_{OL}$ = 8/6/4 mA for 3.3/2.5/1.8 V VDD | — | — | 0.15 × $V_{DD}$ | V |

**Notes:**

1. Min APR includes temperature stability, initial accuracy, load pulling, VDD variation, and aging for 20 yrs at 70 ºC.
2. OE includes a 50 kΩ pull-up to VDD for OE active high, or includes a 50 kΩ pull-down to GND for OE active low.
3. $R_{term}$ = 50 Ω to $V_{DD}$ – 2.0 V (see Figure 4.1). Additional DC current from the output driver will flow through the 50 Ω resistors, resulting in a shift in common mode voltage. The measurements in this table have accounted for this.
4. $R_{term}$ = 100 Ω (differential) (see Figure 4.2).
5. $R_{term}$ = 50 Ω to GND (see Figure 4.2).
6. Refer to the figure below for Typical Clock Output Swing Amplitudes vs Frequency.



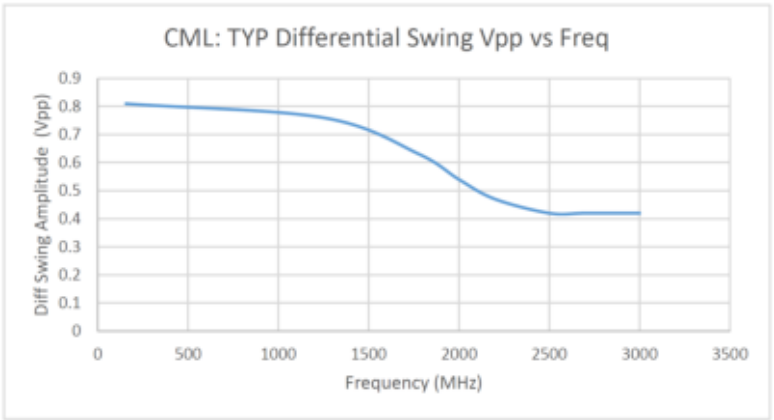




**Figure 2.1. Typical Clock Output Swing Amplitudes vs. Frequency**

**Table 2.2. $V_C$ Control Voltage Input**

$V_{DD}$ = 1.8, 2.5 or 3.3 V ± 5%, $T_A$ = –40 to 85 ºC

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Control Voltage Range | $V_C$ | | 0.1 x VDD | VDD/2 | 0.9 x VDD | V |
| Control Voltage Tuning Slope (Vc = 10% VDD to 90% VDD) | Kv | Positive slope, ordering option | 60, 75, 105, 150, 180, 225 | | | ppm/V |
| Kv Variation | Kv_var | | — | — | ±10 | % |
| Control Voltage Linearity | LVC | Best Straight Line fit | –1.5 | ±0.5 | +1.5 | % |
| Modulation Bandwidth | BW | | — | 10 | — | kHz |
| Vc Input Impedance | ZVC | | 500 | — | — | kΩ |

**Table 2.3. Clock Output Phase Jitter and PSNR**

$V_{DD}$ = 1.8 V, 2.5 or 3.3 V ± 5%, $T_A$ = –40 to 85 ºC

| Parameter | Symbol | Test Condition/Comment | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Phase Jitter (RMS, 12 kHz - 20 MHz)[1] All Differential Formats, $F_{CLK}$ ≥ 200 MHz | ϕJ | Kv = 60 ppm/V | — | 100 | 150 | fs |
| | | Kv = 75 ppm/V | — | 103 | — | fs |
| | | Kv = 105 ppm/V | — | 110 | — | fs |
| | | Kv = 150 ppm/V | — | 123 | — | fs |
| | | Kv = 180 ppm/V | — | 132 | — | fs |
| | | Kv = 225 ppm/V | — | 150 | — | fs |
| Phase Jitter (RMS, 12 kHz - 20 MHz) [1] All Diff Formats, 100 MHz ≤ $F_{CLK}$ < 200 MHz | ϕJ | Kv = 60 ppm/V | — | 115 | 180 | fs |
| | | Kv = 75 ppm/V | — | 118 | — | fs |
| | | Kv = 105 ppm/V | — | 125 | — | fs |
| | | Kv = 150 ppm/V | — | 138 | — | fs |
| | | Kv = 180 ppm/V | — | 147 | — | fs |
| | | Kv = 225 ppm/V | — | 165 | — | fs |
| Phase Jitter (RMS, 12 kHz - 20 MHz)[1] LVDS, $F_{CLK}$ = 156.25 MHz | ϕJ | Kv = 60 ppm/V | — | 110 | 130 | fs |
| | | Kv = 75 ppm/V | — | 113 | — | fs |
| | | Kv = 105 ppm/V | — | 120 | — | fs |
| | | Kv = 150 ppm/V | — | 133 | — | fs |
| | | Kv = 180 ppm/V | — | 142 | — | fs |
| | | Kv = 225 ppm/V | — | 160 | — | fs |
| Phase Jitter (RMS, 12 kHz - 20 MHz)[1] CMOS / Dual CMOS Formats | ϕJ | 10 MHz ≤ $F_{CLK}$ < 250 MHz | — | 200 | — | fs |

| Parameter | Symbol | Test Condition/Comment | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Spurs Induced by External Power Supply Noise, 50 mVpp Ripple. LVDS 156.25 MHz Output | PSNR | 100 kHz sine wave | | -83 | | dBc |
| | | 200 kHz sine wave | | -83 | | |
| | | 500 kHz sine wave | | -82 | | |
| | | 1 MHz sine wave | | -85 | | |

**Note:**
1. Guaranteed by characterization. Jitter inclusive of any spurs.

**Table 2.4. 3.2 x 5 mm Clock Output Phase Noise (Typical)**

| Offset Frequency (f) | 156.25 MHz LVDS | 200 MHz LVDS | 644.53125 MHz LVDS | Unit |
|---|---|---|---|---|
| 100 Hz | –73 | –71 | –60 | |
| 1 kHz | –102 | –102 | –93 | |
| 10 kHz | –130 | –128 | –118 | |
| 100 kHz | –141 | –139 | –129 | dBc/Hz |
| 1 MHz | –150 | –148 | –138 | |
| 10 MHz | –159 | –160 | –153 | |
| 20 MHz | –160 | –162 | –154 | |
| **Offset Frequency (f)** | **156.25 MHz LVPECL** | **200 MHz LVPECL** | **644.53125 MHz LVPECL** | **Unit** |
| 100 Hz | –72 | –71 | –60 | |
| 1 kHz | –103 | –101 | –92 | |
| 10 kHz | –130 | –127 | –117 | |
| 100 kHz | –142 | –139 | –129 | dBc/Hz |
| 1 MHz | –150 | –148 | –138 | |
| 10 MHz | –160 | –162 | –154 | |
| 20 MHz | –161 | –162 | –156 | |

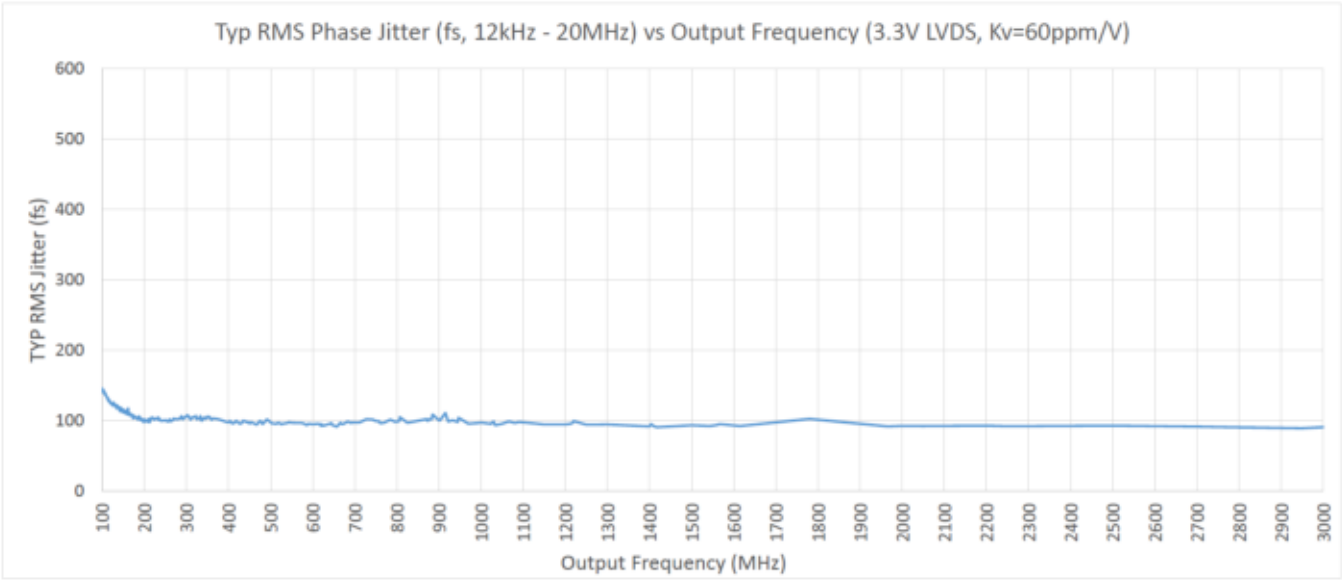



**Figure 2.2. Phase Jitter vs. Output Frequency**

Phase jitter measured with Agilent E5052 using a differential-to-single ended converter (balun or buffer). Measurements collected for >700 commonly used frequencies. Phase noise plots for specific frequencies are available using our free, online Oscillator Phase Noise Lookup Tool at https://www.skyworksinc.com/en/Products/Timing-Oscillators.

**Table 2.5. Environmental Compliance and Package Information**

| Parameter | Test Condition |
|---|---|
| Mechanical Shock | MIL-STD-883, Method 2002 |
| Mechanical Vibration | MIL-STD-883, Method 2007 |
| Solderability | MIL-STD-883, Method 2003 |
| Gross and Fine Leak | MIL-STD-883, Method 1014 |
| Resistance to Solder Heat | MIL-STD-883, Method 2036 |
| Moisture Sensitivity Level (MSL): 3.2 x 5, 5 x 7 packages | 1 |
| Moisture Sensitivity Level (MSL): 2.5 x 3.2 package | 2 |
| Contact Pads: 3.2x5, 5x7 packages | Au/Ni (0.3 - 1.0 µm / 1.27 - 8.89 µm) |
| Contact Pads: 2.5x3.2 packages | Au/Pd/Ni (0.03 - 0.12 µm / 0.1 - 0.2 µm / 3.0 - 8.0 µm) |

**Note:**

1. For additional product information not listed in the data sheet (e.g. RoHS Certifications, MDDS data, qualification data, REACH Declarations, ECCN codes, etc.), refer to our "Corporate Request For Information" portal found here: www.skyworksinc.com/quality.

**Table 2.6. Thermal Conditions[1]**

Max Junction Temperature = 125° C

| Package | Parameter | Symbol | Test Condition | Value | Unit |
|---|---|---|---|---|---|
| 2.5 x 3.2 mm 6-pin DFN[2] | Thermal Resistance Junction to Ambient | $\Theta_{JA}$ | Still Air, 85 °C | 72 | °C/W |
| | Thermal Parameter Junction to Board | $\Psi_{JB}$ | Still Air, 85 °C | 38 | °C/W |
| | Thermal Parameter Junction to Top Center | $\Psi_{JT}$ | Still Air, 85 °C | 15 | °C/W |
| 3.2 × 5 mm 6-pin CLCC | Thermal Resistance Junction to Ambient | $\Theta_{JA}$ | Still Air, 85 °C | 55 | °C/W |
| | Thermal Parameter Junction to Board | $\Psi_{JB}$ | Still Air, 85 °C | 20 | °C/W |
| | Thermal Parameter Junction to Top Center | $\Psi_{JT}$ | Still Air, 85 °C | 20 | °C/W |
| 5 × 7 mm 6-pin CLCC | Thermal Resistance Junction to Ambient | $\Theta_{JA}$ | Still Air, 85 °C | 53 | °C/W |
| | Thermal Parameter Junction to Board | $\Psi_{JB}$ | Still Air, 85 °C | 26 | °C/W |
| | Thermal Parameter Junction to Top Center | $\Psi_{JT}$ | Still Air, 85 °C | 26 | °C/W |

**Note:**

1. Based on PCB Dimensions: 4.5" x 7", PCB Thickness: 1.6 mm, Number of Cu Layers: 4.
2. For best 2.5x3.2mm thermal performance, use 2 GND vias as shown in the Si5xxUC-EVB eval board layout

**Table 2.7. Absolute Maximum Ratings[1]**

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Maximum Operating Temp. | $T_{AMAX}$ | 95 | ºC |
| Storage Temperature | $T_S$ | –55 to 125 | ºC |
| Supply Voltage | $V_{DD}$ | –0.5 to 3.8 | ºC |
| Input Voltage | $V_{IN}$ | –0.5 to $V_{DD}$ + 0.3 | V |
| ESD HBM (JESD22-A114) | HBM | 2.0 | kV |
| Solder Temperature[2] | $T_{PEAK}$ | 260 | ºC |
| Solder Time at $T_{PEAK}$[2] | $T_P$ | 20–40 | sec |

**Notes:**

1. Stresses beyond those listed in this table may cause permanent damage to the device. Functional operation specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. The device is compliant with JEDEC J-STD-020.

## 3. Dual CMOS Buffer

Dual CMOS output format ordering options support either complementary or in-phase signals for two identical frequency outputs. This feature enables replacement of multiple VCXOs with a single Si565 device.

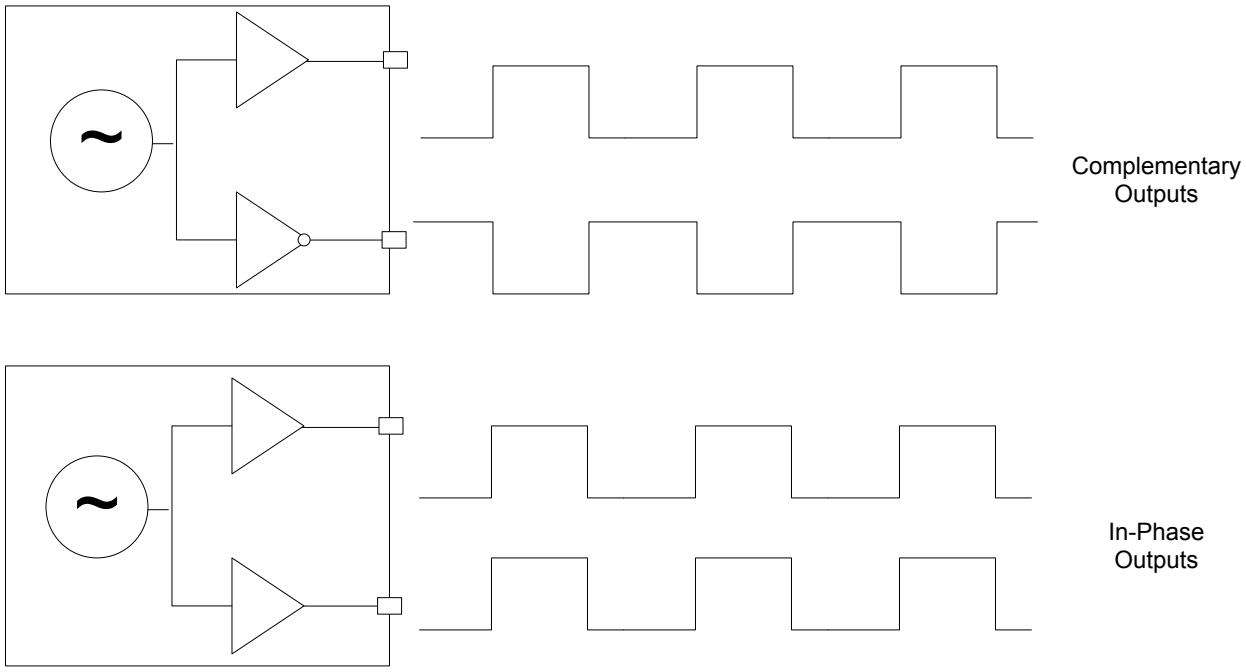



**Figure 3.1. Integrated 1:2 CMOS Buffer Supports Complementary or In-Phase Outputs**

## 4. Recommended Output Terminations

The output drivers support both AC-coupled and DC-coupled terminations as shown in figures below.

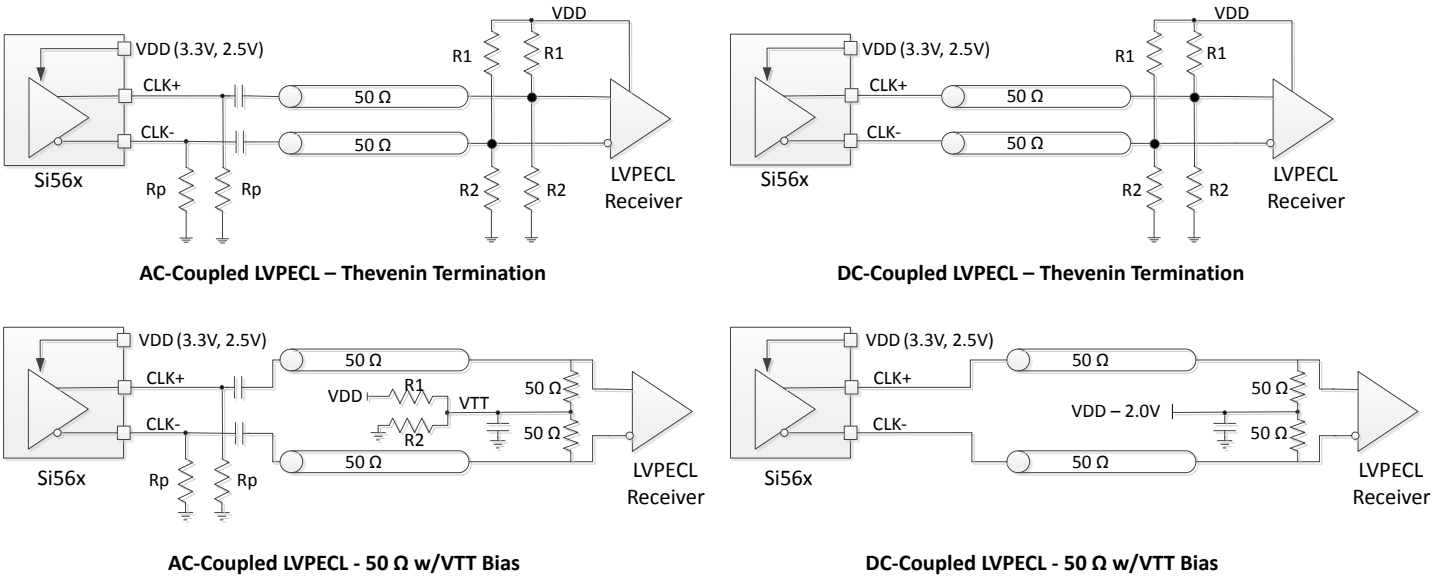



**Figure 4.1. LVPECL Output Terminations**

| AC-Coupled LVPECL Termination Resistor Values | | | |
|---|---|---|---|
| **VDD** | R1 | R2 | Rp |
| **3.3 V** | 82.5 Ω | 127 Ω | 130 Ω |
| **2.5 V** | 62.5 Ω | 250 Ω | 90 Ω |

| DC-Coupled LVPECL Termination Resistor Values | | |
|---|---|---|
| **VDD** | R1 | R2 |
| **3.3 V** | 127 Ω | 82.5 Ω |
| **2.5 V** | 250 Ω | 62.5 Ω |

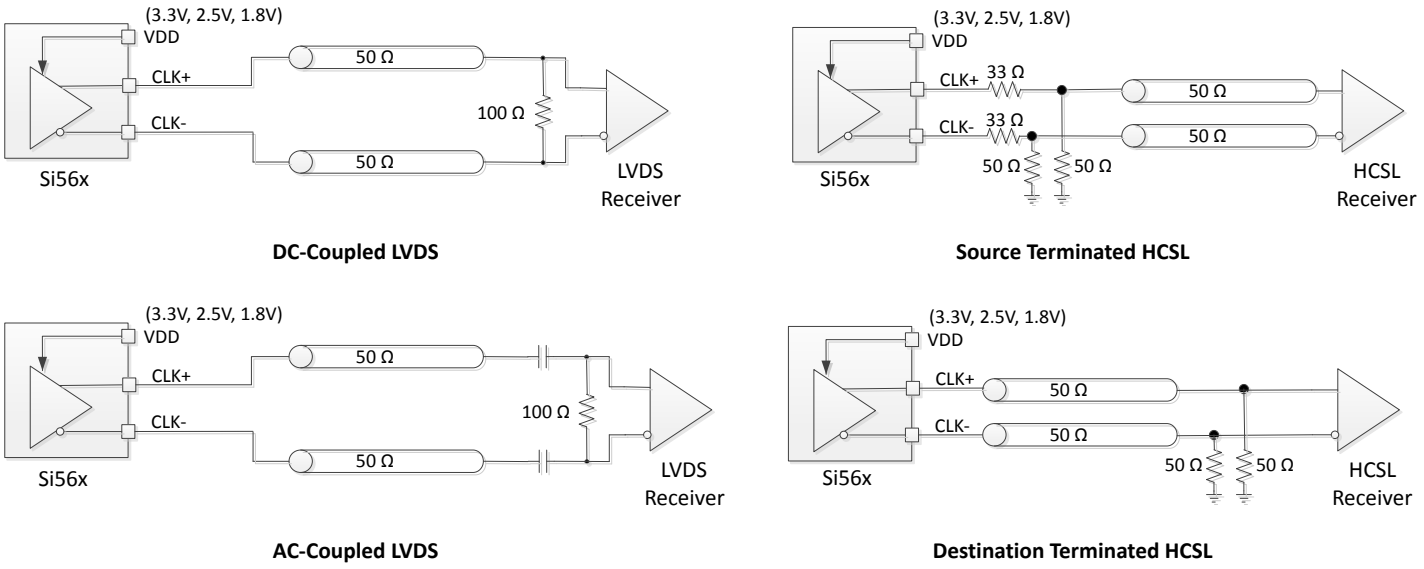



**Figure 4.2. LVDS and HCSL Output Terminations**

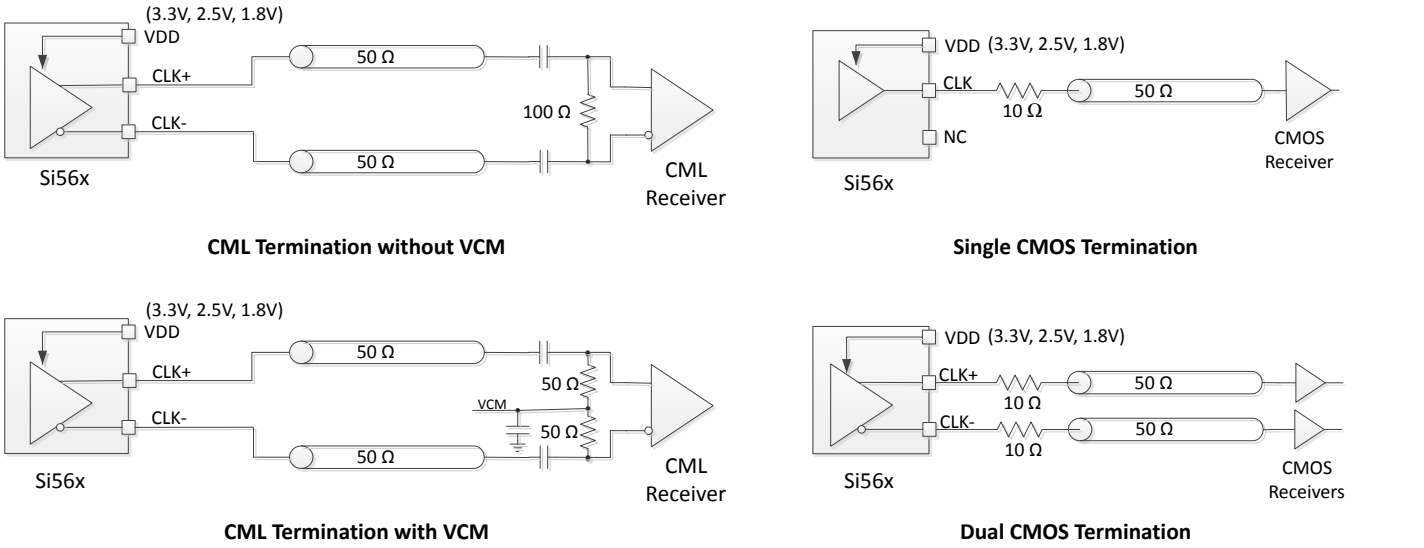



**Figure 4.3. CML and CMOS Output Terminations**

# 5. Package Outline

## 5.1 Package Outline (5×7 mm)

The figure below illustrates the package details for the 5×7 mm Si565. The table below lists the values for the dimensions shown in the illustration.

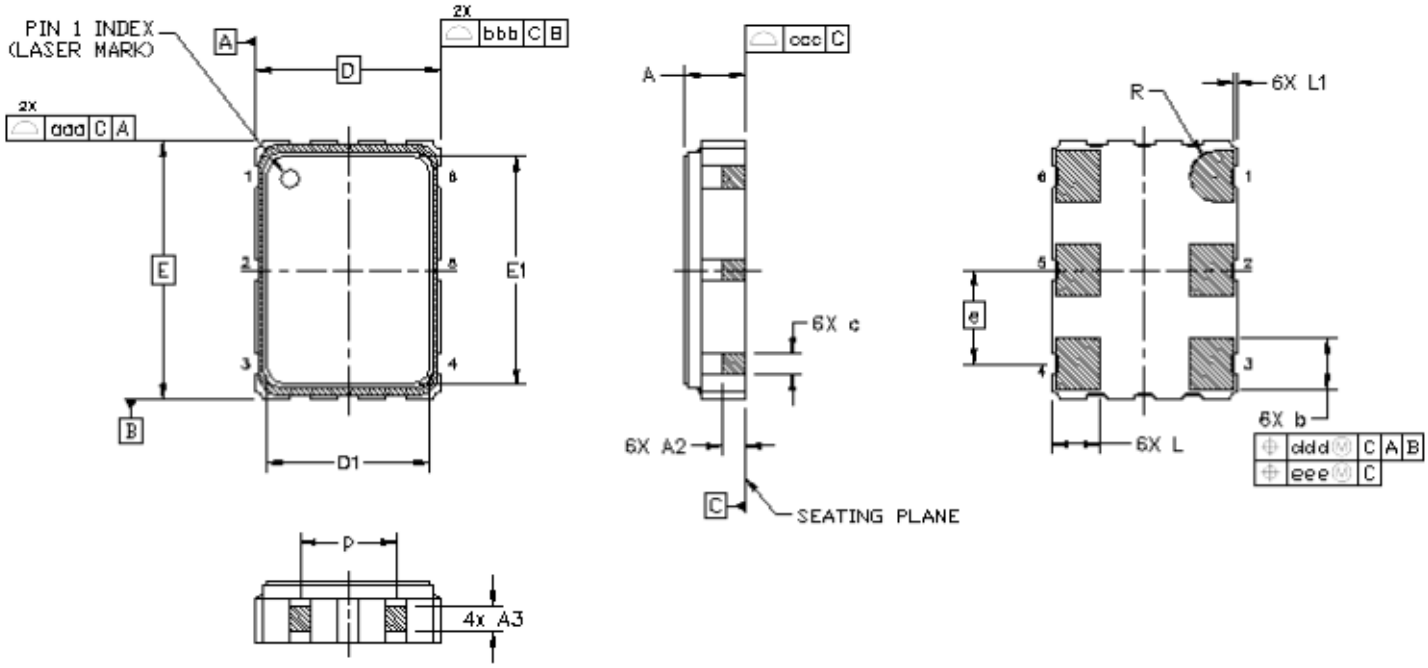



**Figure 5.1. Si565 (5×7 mm) Outline Diagram**

**Table 5.1. Package Diagram Dimensions (mm)**

| Dimension | Min | Nom | Max | | Dimension | Min | Nom | Max |
|---|---|---|---|---|---|---|---|---|
| A | 1.13 | 1.28 | 1.43 | | L | 1.17 | 1.27 | 1.37 |
| A2 | 0.50 | 0.55 | 0.60 | | L1 | 0.05 | 0.10 | 0.15 |
| A3 | 0.50 | 0.55 | 0.60 | | p | 1.70 | — | 1.90 |
| b | 1.30 | 1.40 | 1.50 | | R | 0.70 REF | | |
| c | 0.50 | 0.60 | 0.70 | | aaa | 0.15 | | |
| D | 5.00 BSC | | | | bbb | 0.15 | | |
| D1 | 4.30 | 4.40 | 4.50 | | ccc | 0.08 | | |
| e | 2.54 BSC | | | | ddd | 0.10 | | |
| E | 7.00 BSC | | | | eee | 0.05 | | |
| E1 | 6.10 | 6.20 | 6.30 | | | | | |

**Notes:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

## 5.2 Package Outline (3.2×5 mm)

The figure below illustrates the package details for the 3.2×5 mm Si565. The table below lists the values for the dimensions shown in the illustration.

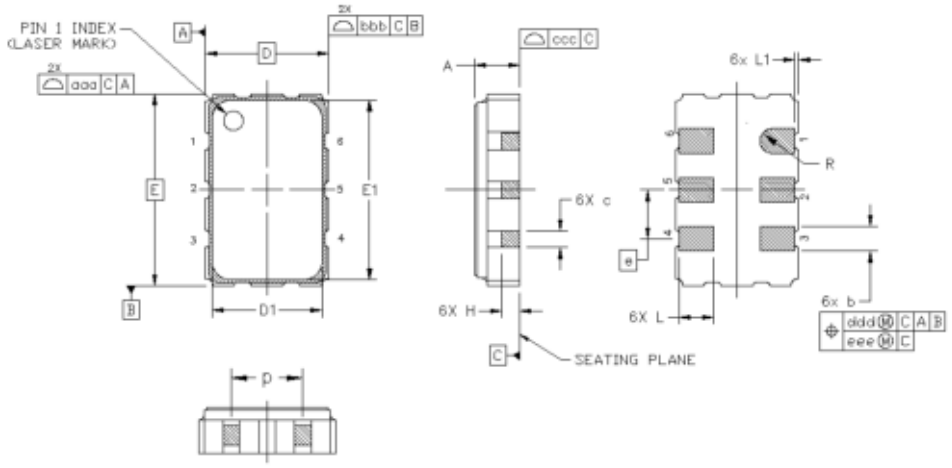



**Figure 5.2. Si565 (3.2×5 mm) Outline Diagram**

**Table 5.2. Package Diagram Dimensions (mm)**

| Dimension | Min | Nom | Max |
|---|---|---|---|
| A | 1.06 | 1.17 | 1.33 |
| b | 0.54 | 0.64 | 0.74 |
| c | 0.35 | 0.45 | 0.55 |
| D | | 3.20 BSC | |
| D1 | 2.55 | 2.60 | 2.65 |
| e | | 1.27 BSC | |
| E | | 5.00 BSC | |
| E1 | 4.35 | 4.40 | 4.45 |
| H | 0.45 | 0.55 | 0.65 |
| L | 0.80 | 0.90 | 1.00 |
| L1 | 0.05 | 0.10 | 0.15 |
| p | 1.36 | 1.46 | 1.56 |
| R | | 0.32 REF | |
| aaa | | 0.15 | |
| bbb | | 0.15 | |
| ccc | | 0.08 | |
| ddd | | 0.10 | |
| eee | | 0.05 | |

**Notes:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

## 5.3 Package Outline (2.5x3.2 mm)

The figure below illustrates the package details for the 2.5x3.2 mm Si565. The table below lists the values for the dimensions shown in the illustration.

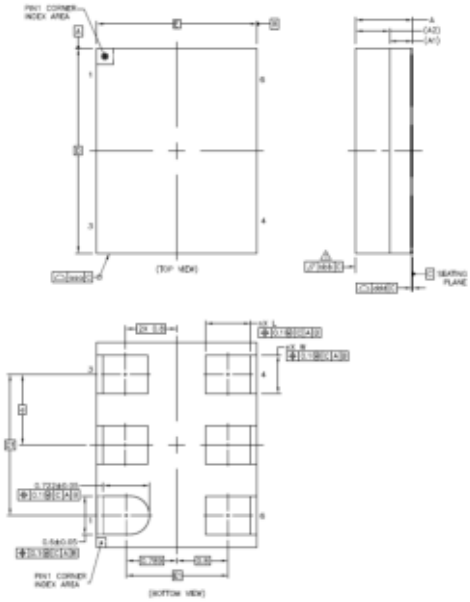


**Figure 5.3. Si565 (2.5×3.2 mm) Outline Diagram**

**Table 5.3. Package Diagram Dimensions (mm)**

| Dimension | Min | Nom | Max |
|---|---|---|---|
| A | 0.85 | 0.90 | 1.00 |
| A1 | | 0.36 REF | |
| A2 | | 0.53 REF | |
| W | 0.55 | 0.60 | 0.65 |
| D | | 3.2 BSC | |
| E | | 2.5 BSC | |
| e | | 1.10 BSC | |
| L | 0.65 | 0.70 | 0.75 |
| n | | 5 | |
| D1 | | 2.2 BSC | |
| E1 | | 1.589 BSC | |
| aaa | | 0.10 | |
| bbb | | 0.10 | |
| ddd | | 0.08 | |

**Notes:**

1. The dimensions in parentheses are reference.
2. All dimensions in millimeters (mm).
3. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

# 6. PCB Land Pattern

## 6.1 PCB Land Pattern (5×7 mm)

The figure below illustrates the 5×7 mm PCB land pattern for the Si565. The table below lists the values for the dimensions shown in the illustration.

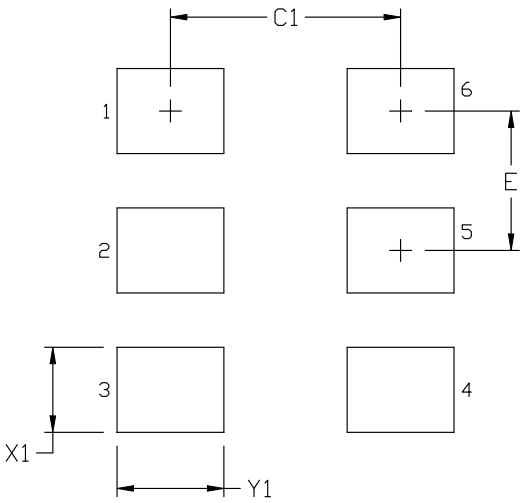



**Figure 6.1. Si565 (5×7 mm) PCB Land Pattern**

**Table 6.1. PCB Land Pattern Dimensions (mm)**

| Dimension | (mm) |
|---|---|
| C1 | 4.20 |
| E | 2.54 |
| X1 | 1.55 |
| Y1 | 1.95 |

**Notes:**

**General**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

**Solder Mask Design**

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

**Stencil Design**

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1.

**Card Assembly**

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

## 6.2 PCB Land Pattern (3.2×5 mm)

The figure below illustrates the 3.2×5.0 mm PCB land pattern for the Si565. The table below lists the values for the dimensions shown in the illustration.

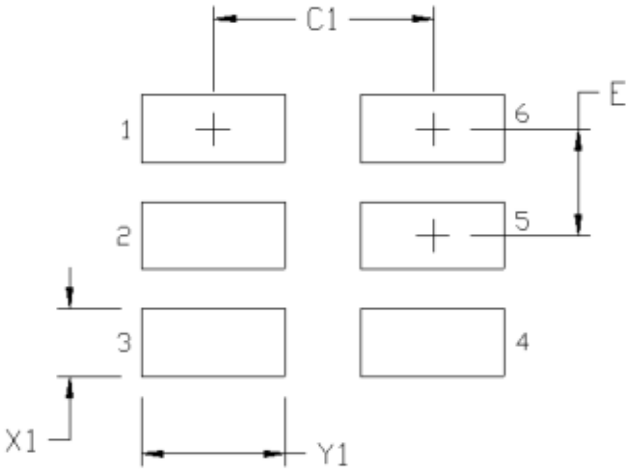



**Figure 6.2. Si565 (3.2×5 mm) PCB Land Pattern**

**Table 6.2. PCB Land Pattern Dimensions (mm)**

| Dimension | (mm) |
|---|---|
| C1 | 2.60 |
| E | 1.27 |
| X1 | 0.80 |
| Y1 | 1.70 |

**Notes:**

**General**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

**Solder Mask Design**

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

**Stencil Design**

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1.

**Card Assembly**

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

### 6.3 PCB Land Pattern (2.5×3.2 mm)

The figure below illustrates the 2.5×3.2 mm PCB land pattern for the Si565. The table below lists the values for the dimensions shown in the illustration.

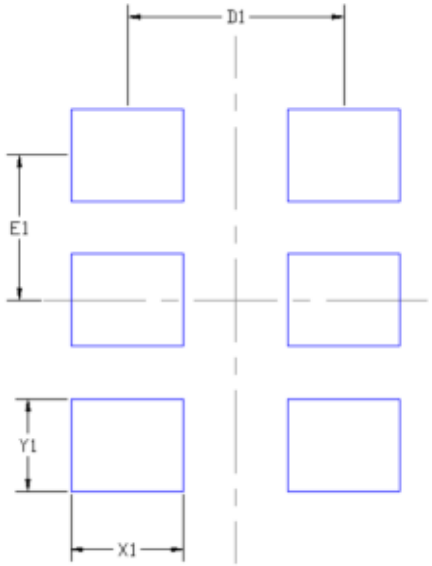



**Figure 6.3. Si565 (2.5×3.2 mm) PCB Land Pattern**

**Table 6.3. PCB Land Pattern Dimensions (mm)**

| Dimension | Description | Value (mm) |
|---|---|---|
| X1 | Width - leads on long sides | 0.85 |
| Y1 | Height - leads on long sides | 0.7 |
| D1 | Pitch in X directions of XLY1 leads | 1.639 |
| E1 | Lead pitch XLY1 leads | 1.10 |

**Notes:** The following notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine-tune their SMT process as required for their application and tooling.

**General**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

**Solder Mask Design**

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

**Stencil Design**

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 0.8:1 for the pads.

**Card Assembly**

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

# 7. Top Markings

## 7.1 Top Marking (5x7 and 3.2x5 Packages)

The figure below illustrates the mark specification for the Si565 5x7 and 3.2x5 package sizes. The table below lists the line information.

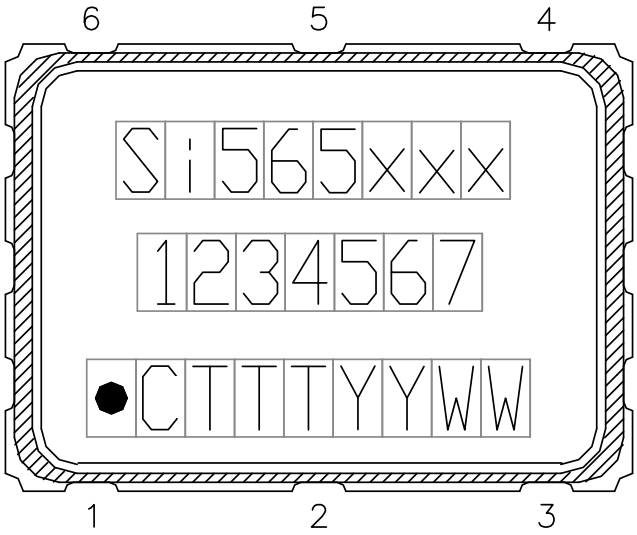



**Figure 7.1. Mark Specification**

**Table 7.1. Si565 Top Mark Description**

| Line | Position | Description |
|---|---|---|
| 1 | 1–8 | "Si565", xxx = Ordering Option 1, Option 2, Option 3 (e.g. Si565AAA) |
| 2 | 1–7 | Frequency Code<br>(e.g. 100M000 or 6-digit custom code as described in the Ordering Guide) |
| 3 | **Trace Code** | |
| | Position 1 | Pin 1 orientation mark (dot) |
| | Position 2 | Product Revision (C) |
| | Position 3–5 | Tiny Trace Code (3 alphanumeric characters per assembly release instructions) |
| | Position 6–7 | Year (last two digits of the year), to be assigned by assembly site (ex: 2017 = 17) |
| | Position 8–9 | Calendar Work Week number (1–53), to be assigned by assembly site |

### 7.2 Top Marking (2.5x3.2 Package)

The figure below illustrates the mark specification for the Si565 2.5x3.2 package sizes. The table below lists the line information.

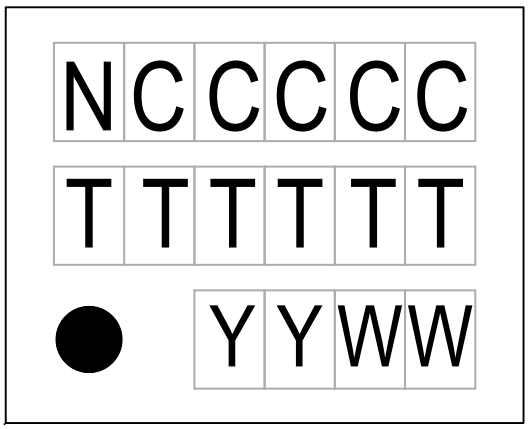



**Figure 7.2. Mark Specification**

**Table 7.2. Si565 Top Mark Description**

| Line | Position | Description |
|---|---|---|
| 1 | 1–6 | N = Si565, CCCCC = Custom Mark Code |
| 2 | **Trace Code** | |
| | 1–6 | Six-digit trace code per assembly release instructions |
| 3 | Position 1 | Pin 1 orientation mark (dot) |
| | Position 2–3 | Year (last two digits of the year), to be assigned by assembly site (exp: 2017 = 17) |
| | Position 4–5 | Calendar Work Week number (1–53), to be assigned by assembly site |

# 8. Revision History

**Revision 206622A**

May, 2023

- Updated Min and Nom package diagram dimensions specs in 5.3 Package Outline (2.5x3.2 mm).

**Revision 1.3**

June, 2021

- Updated Ordering Guide and Top Mark for Rev C silicon.
- Added HCSL-Fast (faster $t_R/t_F$) ordering option.
- Updated Table 2.1, Powerup VDD Ramp Rate.

**Revision 1.2**

September, 2020

- Added 2.5 x 3.2 mm package option.
- Updated Table 2.1, Powerup VDD Ramp Rate and LVDS Swing.

**Revision 1.0**

June, 2018

- Initial draft

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