Si720x Switch/Latch Hall Effect Magnetic Position Sensor Data Sheet

Not Recommended for New Designs

The Si7201/2/3/4/5/6 family of Hall effect magnetic sensors switches and latches from Silicon Labs combines a chopper-stabilized Hall element with a low-noise analog amplifier, 13-bit analog-to-digital converter, and a flexible comparator circuit. Leveraging Silicon Labs' proven CMOS design techniques, the Si720x family incorporates digital signal processing to provide precise compensation for temperature and offset drift.

Compared with existing Hall effect sensors, the Si720x family offers industry-leading sensitivity, which enables use with larger air gaps and smaller magnets. For battery-powered applications, the Si720x family offers very low power consumption to improve operating life.

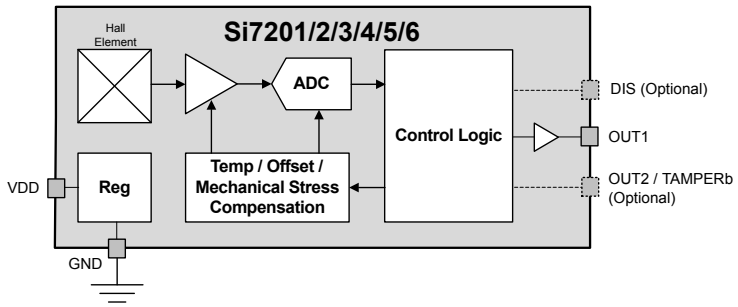
The Si720x devices are offered in 3-pin SOT23, 5-pin SOT23, and TO-92 packages, with power, ground, a single output pin that goes high or low as the magnetic field increases, and with the 5-pin parts a disable(sleep) pin, and a tamper output pin. With the three-pin package, tamper indication is by the pin going back to its zero field level at high magnetic field.

Applications:

- Replacement of reed switches in consumer, and security applications
- Position sensing of HVAC knob, door locks, windows, and other mechanical devices
- BLDC motor control
- Camera image stabilization, zoom, and autofocus
- Fluid level sensing
- Control knobs and selector switches
- General-purpose mechanical position sensing

FEATURES

- High-Sensitivity Hall Effect Sensor
  - Maximum B_{OP} operating point/minimum field strength of <1.1 mT
  - Omnipolar or unipolar operation
  - Integrated digital signal processing for temperature and offset drift compensation
- Low 400 nA Typical Current Consumption at 5 samples per second
- Selectable Sensitivity, Hysteresis, Output Polarity and Sample Rate
- Sensitivity Drift < ±3% over Temperature
- Wide Power Supply Voltage
  - 1.71 to 5.5 V
  - 3.3 to 26.5 V
- Selectable Output Options
  - Open-drain output
  - Digital high/low output
- Industry-Standard Packaging
  - Surface mount SOT-23 (3 or 5 pin)
  - Through hole TO-92 (3-pin)



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1. Electrical Specifications

Unless otherwise specified, all min/max specifications apply over the recommended operating conditions.

Table 1.1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power Supply	V_{DD}	Si7201/2/3/4	1.71		5.5[1]	V
Power Supply	V_{DD}	Si7205/6	3.3		26.5	V
Temperature	T_A	I grade	-40		+125[2]	°C

Note:
1. 3.6 V for most sensitive parts (see Chapter 5. Ordering Guide).
2. 0-70°C for most sensitive parts (F grade) (see Chapter 5. Ordering Guide).

Table 1.2. General Specifications[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Voltage High	V_{IH}	DIS pin	0.7 x V_{DD}	-	-	V
Input Voltage Low	V_{IL}	DIS pin	-	-	0.3 x V_{DD}	V
Input voltage Range	V_{IN}	DIS pin	0		V_{DD}	V
Input Leakage	I_{IL}	DIS pin			1	µA
Output Voltage Low	V_{OL}	TAMPERb pin I_{OL} = 3 mA V_{DD} > 2 V			0.4	V
		TAMPERb pin I_{OL} = 2 mA V_{DD} > 1.71 V			0.2	V
		TAMPERb pin I_{OL} = 6 mA V_{DD} > 2 V			0.6	V
Output Voltage High	V_{OH}	TAMPERb pin I_{OH} = 2 mA V_{DD} > 2.25 V	V_{DD} – 0.4			V

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Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current Consumption Average power depends on the sample rate and percent of time spent sampling versus sleep mode or idle mode. See the ordering guide for average power calculations for specific devices.	I_{DD}	Sleep timer enabled average at V_{DD} = 3.3 V and 200 msec sleep time		0.4		µA
		Sleep mode V_{DD} = 3.3 V, T = 25 °C V_{DD} = 3.3 V, T = 70 °C V_{DD} = 5.5 V, T = 125 °C		50	 1000 5000	 nA nA nA
		Conversion in progress V_{DD} = 1.8V V_{DD} = 3.3 V V_{DD} = 5.5 V		 3.5 5 6.8	 5.5 6 8.0	mA
		Conversion in progress high voltage parts V_{DD} = 3.3 to 26.5 V		6.5	8.5	mA
		Idle mode low voltage parts V_{DD} = 1.71 to 5.5 V		0.6	1	mA
		Idle mode high voltage parts V_{DD} = 3.3 to 26.5 V		0.9	1.2	mA
Conversion Time	T_{CONV}	First conversion when waking from sleep or idle		11		µs
		Additional conversions in a burst		8.8		µs
Sample Rate	F_{SAMPLE}	Parts can be configured for sleep or idle between samples. Sleep is lower power, but the fastest sampling rate is 8 kHz. Idle allows sampling rate to be configured to be as high as 113 kHz. See the ordering guide for details.		-		
Wake Up Time	T_{WAKE}	Time from V_{DD} > 1.71 V to first measurement			1	msec

Note:

1. TAMPERb and DIS pin specifications apply when the pin is present (Si7203/4).
2. Idle time can be factory programmed from 13.2 µsec to 206 msec ±10% or set to zero in which case conversions are done every 8.8 µsec. Normally idle time is only used at higher sample speeds.
3. For high voltage parts (V_{DD} = 26.5 V maximum), the power on ramp should be faster than 10 V per second in the start-up region from 2 to 3 V.

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Table 1.3. Output Pin Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si7201/2/3/4						
Output Voltage Low Open Drain or Push Pull	V_{OL}	I_{OL} = 3 mA V_{DD} > 2 V			0.4	V
		I_{OL} = 2 mA V_{DD} > 1.71V			0.2	V
		I_{OL} = 6 mA V_{DD} > 2 V			0.6	V
Leakage Output High Output Pin Open Drain	I_{OH}				1	µA
Output Voltage High Output Pin Push Pull	V_{OH}	I_{OH} = 2 mA V_{DD} > 2.25 V	V_{DD} – 0.4			V
Slew Rate	T_{SLEW}			5		$\%V_{DD}$/ns
Si7205/6						
Output Voltage Low	V_{OL}	I_{OL} = 11.4 mA V_{DD} > 6 V			0.4	V
Safe Continuous Sink Current					20	mA
Leakage Output High Output Pin Open Drain	I_{OH}				1	µA
Slew Rate Digital Output Mode	T_{SLEW}			5		$\%V_{DD}$/ns
Output Pin Shorted to V_{DD}	I_{SHORT}	V_{DD} = 12 V Average current as pin cycles		4		mA

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The Si7205 and Si7206 can be configured to signal the status equivalent to output high or low by modulating the power supply current. If configured in this way, the following are the specifications for the amount of current that will be drawn for the “output high” state.

Table 1.4. I_{DD} Signaling

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
I_{DD} Signaling Current	I_{DO}	V_{DDH} > 6 V	8	10	12	mA

Table 1.5. Magnetic Sensor[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Offset	B_{OFF}	20 mT scale V_{DD} = 1.71 to 3.6 V 0-70°C		±150	±250	µT
		20 mT scale V_{DD} = 1.71 to 5.5 V Full temperature range		±250	+450, -350	µT
Gain Accuracy		0-70°C			5	%
		Full temperature range			10	%
RMS Noise[2]		Room temp, 20 mT range, V_{DD} = 5 V		30		µT rms

Note:

1. See the Magnetic Sensors Selector Guide for operating release points. These are defined as maximum operating point and minimum release point over the operating temperature range and do not include the effect of noise.
2. For a single conversion. This can be reduced by the square root of N by filtering over N samples. See ordering guide for samples taken per measurement.

Table 1.6. Temperature Compensation

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Bop and Brp vs Temperature		Flat Tempco. 0-70°C		< ±0.05		%/°C
		Neodymium compensation		-0.12		%/°C
		Ceramic compensation		-0.2		%/°C

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Table 1.7. Thermal Characteristics

Parameter	Symbol	Test Condition	Value	Unit
Junction to Air Thermal Resistance	θ_{JA}	JEDEC 4 layer board no airflow SOT23-5	212.8	°C/W
Junction to Board Thermal Resistance	θ_{JB}	JEDEC 4 layer board no airflow SOT23-5	45	°C/W
Junction to Air Thermal Resistance	θ_{JA}	JEDEC 4 layer board no airflow SOT23-3	254.6	°C/W
Junction to Board Thermal Resistance	θ_{JB}	JEDEC 4 layer board no airflow SOT23-3	54.8	°C/W

Table 1.8. Absolute Maximum Ratings[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Temperature Under Bias			-55		125	°C
Storage Temperature			-65		150	°C
Si7201/2/3/4						
Voltage on I/O Pins			-0.3		V_{DD}+0.3	V
Voltage on V_{DD} with Respect to Ground			-0.3		6	V
ESD Tolerance		HBM			2	kV
		CDM			500	V
Si7205/6						
Voltage on Ouput pin[2]			-21		40	V
Voltage on V_{DD} with Respect to Ground[3]			-21		40	V
ESD Tolerance		HBM			8	kV
		CDM			500	V

Notes:

1. Absolute maximum ratings are stress ratings only, operation at or beyond these conditions is not implied and may shorten the life of the device or alter its performance.
2. The output pin can withstand EMC transients per ISO 7637-2-2-11 and Ford EMC-CS-2009.1 with a current limiting resistor of 220 Ω to a local bypass cap of 0.1 µF and additional 22 Ω between the capacitor and ground..
3. V_{DD} can withstand automotive EMC transients per ISO 7637-2-2-11 and Ford EMC-CS-2009.1 with a current limiting resistor of 220 Ω.

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2. Functional Description

The Si7201/2/3/4/5/6 family of Hall Effect magnetic sensors digitize the component of the magnetic field in the z axis of the device (positive field is defined as pointing into the device from the bottom). The digitized field is compared to a pre-programmed threshold and the output pin goes high or low if the threshold is crossed. The parts are normally used to detect the presence or absence of a magnet in security systems, as position sensors or for counting revolutions.

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Table 2.1. Part Ordering Guide

Part Number	Description
Si7201	Low voltage switches
Si7202	Low voltage latches
Si7203	Low voltage switch with tamper and/or disable pins
Si7204	Low voltage latches with tamper and/or disable pins
Si7205	High voltage switches
Si7206	High voltage latches

The output pin (push pull or open collector) can go high or low when the magnetic field crosses a threshold. The output pin configuration is determined by the type of part ordered.

The parts are preconfigured for the magnetic field measurement range, magnetic field operate and release points, sleep time, temperature compensation, tamper threshold and digital filtering and will wake into this mode when first powered. The specific configuration output type (open collector or push pull) are determined by the part number. See Magnetic Sensors Selector Guide for details.

Examples:

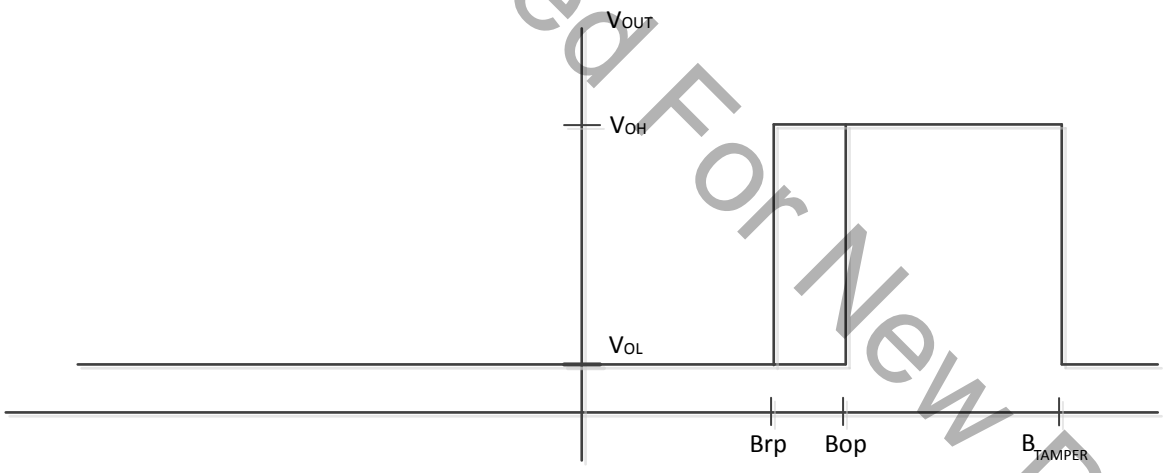


Figure 2.1. Unipolar Switch with Tamper

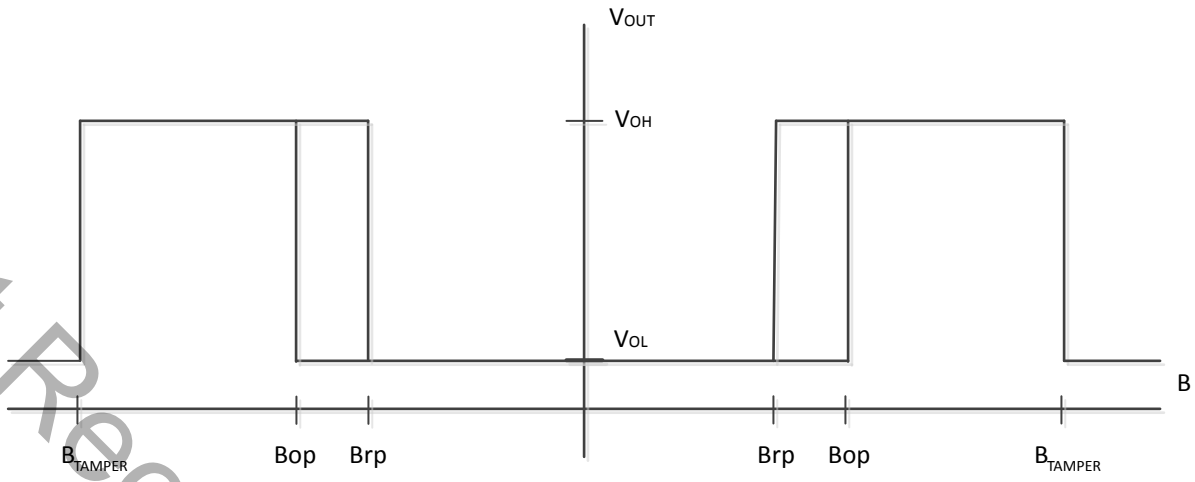


Figure 2.2. Omnipolar Swith with Tamper

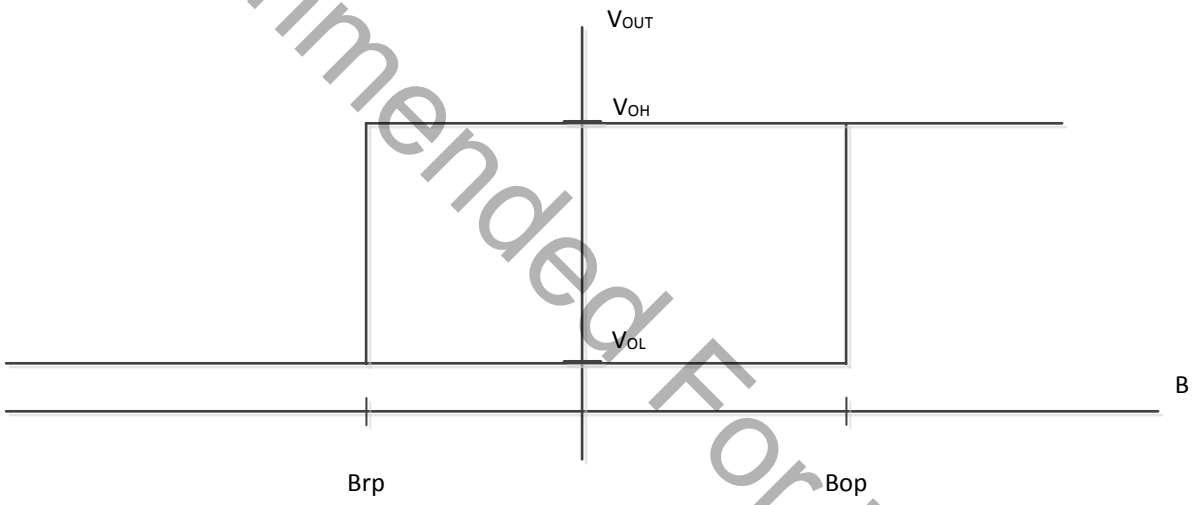


Figure 2.3. Latch

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3. DISABLE Pin Timing

For a part that has a DISABLE pin, DISABLE high will put the part in complete sleep mode with I_{DD} typical of 50 nA. When DISABLE goes low, the part will wake and initiate a measurement. For a single measurement, this takes 11 µsec typically. Additional measurements in a burst take 8.8 µsec. Once the measurement (burst) is complete, the output pin status is updated and the part enters idle mode. The part will make a new measurement or measurement burst at the time-interval determined by the idle timer (typically 1 msec). The idle timer is reset when DISABLE transitions from high to low, so the time from the first measurement until the next measurement will always be the programmed idle time.

Disable low pulses can be as short as 1 µsec. For pulses shorter than a conversion burst, the part will make one burst and then go back to sleep.

When disable returns high, a measurement in progress (if any) will complete and the part will enter sleep mode.

As the idle time is typically long (i.e. 1 msec) compared to the measurement time (i.e. 11 µsec), it is possible to keep the DISABLE pin low duration short (i.e. 15 µsec) and have a long period in the sleep state. This is an effective way to control the sample rate and power.

For example, if the part is programmed to make a single measurement at a time and is programmed with an idle time of 1 msec and DISABLE is pulsed low for 15 µsec every 50 msec, then the average I_{DD} will be:

- 11 µsec to wake and make a measurement at I_{DD} typical of 5.0 mA (3.3V)/(50.015 msec cycle time) = 1.0 µA
- 4 µsec in idle mode at typical current of 600 µA/(50.015 msec cycle time) = 0.05 µA
- 50 msec in sleep mode at 50 nA/(50.015 msec cycle time) = 0.05uA
- Or 1.1 µA total

As the programmed idle time is shorter than the DISABLE low time in the example, the value of the programmed idle time does not make a difference.

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4. Pin Description

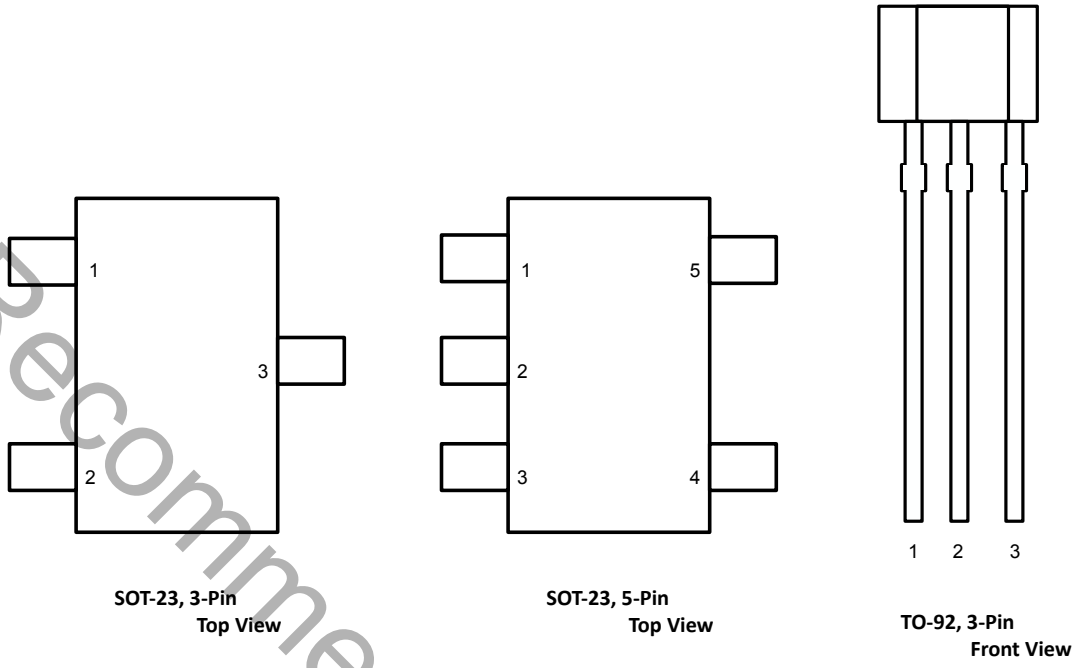


Figure 4.1. Si720xxx Pin Assignments

Note:

The 3-pin option includes part numbers: Si7201/2/5/6.

The SOT-23 5 pin option include part numbers: Si7203/4.

Table 4.1. Si7201/2/5/6 (SOT23 3-pin Package)

Pin Name	Pin Number	Description
VDD	1	Power 1.71 to 5.5 V or 3.3 to 26.5 V
OUT1	2	Switch/latch output
GND	3	Ground

Table 4.2. Si7203/4/5 (SOT23 5-pin Package Excluding Si7203-B-01-IV(R))

Pin Name	Pin Number	Description
OUT2/TAMPERb	1	OUT2/TAMPERb (tamper/high field indicator)
GND	2	Ground
DIS	3	Disables part (puts into sleep mode) when high. Measurement cycle will resume when pin goes low
VDD	4	Power 1.71 to 5.5 V
OUT1	5	Switch/latch output

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Table 4.3. Si7203-B-01-IV(R) (SOT23 5-pin Package)

Pin Name	Pin Number	Description
TAMPER	1	TAMPER (tamper)
GND	2	Ground
FLOAT	3	Must be left floating for correct operation of the device
VDD	4	Power 1.71 to 5.5 V
OUT1	5	Switch output

Table 4.4. Si7201/2/5/6 (TO-92 Package)

Pin Name	Pin Number	Description
VDD	1	Power
GND	2	Ground
OUT1	3	Output

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5. Ordering Guide

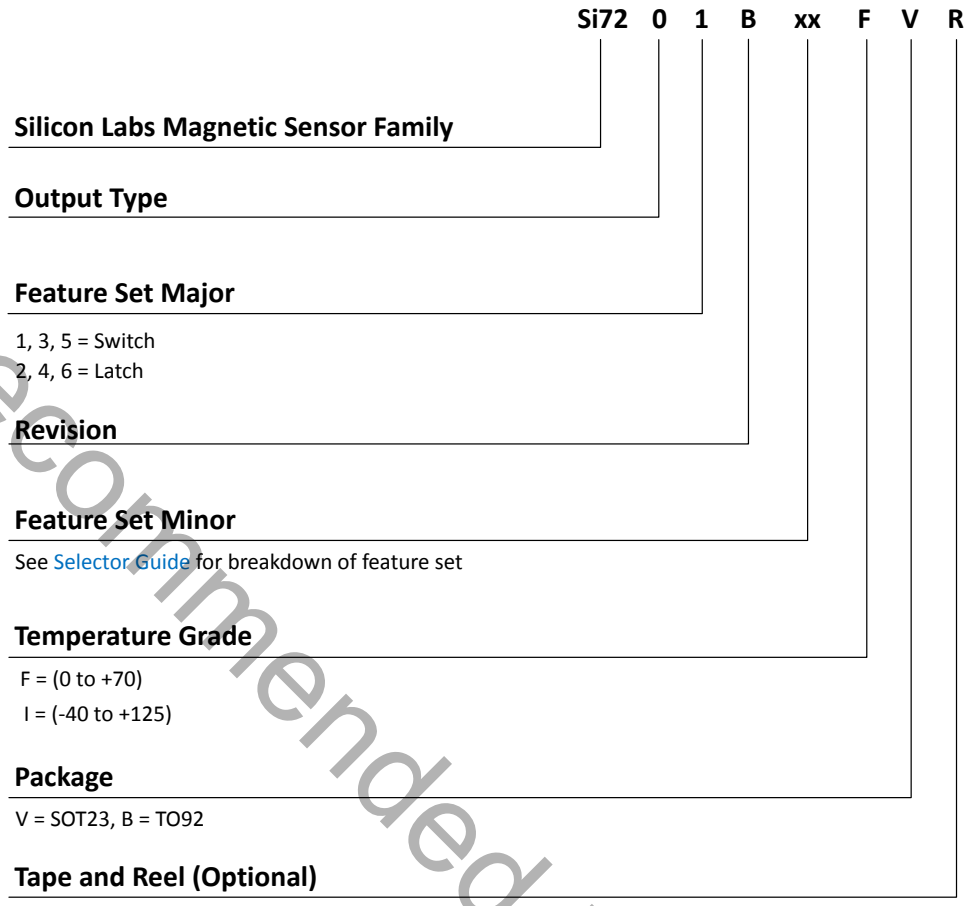


Figure 5.1. Si720x Part Numbering

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Table 5.1. Switch Product Selection Guide

OPN	Bop max (mT)	Brp min (mT)	Bop Typ (mT)	Brp Typ (mT)	Hyst (mT)	Type	Output type	Full Scale (mT)	Sample frequency (Hz)	Typical Idd (uA)	Vdd Range (V)	Temperature (°C)	Package	Tamper detection (mT)	Temperature compensation (% per °C)	Digital filtering
Si7201-B-00-FV	1.1	0.2	0.8	0.4	0.4	Omnipolar switch	Low (Push-Pull)	20	5	0.4	1.7-3.6	0 - 70°	SOT23-3	—	—	—
Si7201-B-01-FV*	1.1	0.2	0.8	0.4	0.4	Omnipolar switch	Low (Push-Pull)	20	5	0.4	1.7-3.6	0 - 70°	SOT23-3	19.8	—	—
Si7201-B-02-FV	0.9	0.2	0.6	0.4	0.2	Omnipolar switch	High (Push-Pull)	20	5	1.1	1.7-3.6	0 - 70°	SOT23-3	19.8	0.12%	4 sample FIR
Si7201-B-03-IV	2.8	1.1	2.2	1.6	0.6	Omnipolar switch	High (Push-Pull)	20	1000	56.7	1.7-5.5	-40 - 125°	SOT23-3	—	—	—
Si7201-B-04-IV	1.4	0.2	1.0	0.6	0.4	Omnipolar switch	Low (Push-Pull)	20	5	0.4	1.7-5.5	-40 - 125°	SOT23-3	—	—	—
Si7201-B-05-IV	2.0	0.6	1.6	1.0	0.6	Omnipolar switch	Low (Push-Pull)	20	5	0.4	1.7-5.5	-40 - 125°	SOT23-3	19.8	—	—
Si7201-B-06-IV	2.0	0.6	1.6	1.0	0.6	Omnipolar switch	Low (Open Drain)	20	5	0.4	1.7-5.5	-40 - 125°	SOT23-3	—	—	—
Si7201-B-07-IV*	2.0	0.6	1.6	1.0	0.6	Omnipolar switch	Low (Open Drain)	20	5	0.4	1.7-5.5	-40 - 125°	SOT23-3	19.8	—	—
Si7201-B-08-IV*	3.4	1.6	2.7	2.1	0.6	Omnipolar switch	Low (Open-Drain)	20	1000	56.7	1.7-5.5	-40 - 125°	SOT23-3	—	—	—

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OPN	Bop max (mT)	Brp min (mT)	Bop Typ (mT)	Brp Typ (mT)	Hyst (mT)	Type	Output type	Full Scale (mT)	Sample frequency (Hz)	Typical Idd (uA)	Vdd Range (V)	Temperature (°C)	Package	Tamper detection (mT)	Temperature compensation (% per °C)	Digital filtering
Si7201-B-09-IB*	2.3	0.8	1.6	1.2	0.4	Omnipolar switch	Low (push-pull)	20	20	1.2	1.7-5.5	-40 - 125°	TO92	—	—	—
SI7201-B-10-IV*	3.7	1.5	3.0	2.0	1.0	Omnipolar switch	Low (Open Drain)	20	5	0.4	1.7-5.5	-40 - 125°	SOT23-3	—	—	—
Si7201-B-11-IB*	2.8	1.1	2.2	1.6	0.6	Omnipolar switch	High (push-pull)	20	8000	420.7	1.7-5.5	-40 - 125°	TO92	—	—	—
SI7201-B-12-IV*	3.7	1.5	3.0	2.0	1.0	Omnipolar switch	Low (Open Drain)	20	20	1.2	1.7-5.5	-40 - 125°	SOT23-3	—	—	—
SI7201-B-20-IV	4.9	2.3	4.0	3.0	1.0	Omnipolar switch	Low (Open Drain)	20	5	0.4	1.7-5.5	-40 - 125°	SOT23-3	—	—	—
SI7201-B-21-IV*	4.9	2.3	4.0	3.0	1.0	Omnipolar switch	Low (Open Drain)	20	13.3	0.9	1.7-5.5	-40 - 125°	SOT23-3	—	—	—
SI7201-B-22-IV*	4.9	2.3	4.0	3.0	1.0	Omnipolar switch	Low (Open Drain)	20	20	1.2	1.7-5.5	-40 - 125°	SOT23-3	—	—	—
SI7201-B-30-IV	7.0	4.1	6.0	5.0	1.0	Omnipolar switch	Low (Open Drain)	20	5	0.4	1.7-5.5	-40 - 125°	SOT23-3	—	—	—
SI7201-B-31-IV*	7.0	4.1	6.0	5.0	1.0	Omnipolar switch	Low (Open Drain)	20	13.3	0.9	1.7-5.5	-40 - 125°	SOT23-3	—	—	—
SI7201-B-32-IV	7.0	4.1	6.0	5.0	1.0	Omnipolar switch	Low (Open Drain)	20	20	1.2	1.7-5.5	-40 - 125°	SOT23-3	—	—	—

Not Recommended For New Designs

OPN	Bop max (mT)	Brp min (mT)	Bop Typ (mT)	Brp Typ (mT)	Hyst (mT)	Type	Output type	Full Scale (mT)	Sample frequency (Hz)	Typical Idd (uA)	Vdd Range (V)	Temperature (°C)	Package	Tamper detection (mT)	Temperature compensation (% per °C)	Digital filtering
SI7201-B-40-IV	15.0	9.6	13.2	11.2	2.0	Omnipolar switch	Low (Open Drain)	20	5	0.4	1.7-5.5	-40 - 125°	SOT23-3	—	—	—
SI7201-B-41-IV*	15.0	9.6	13.2	11.2	2.0	Omnipolar switch	Low (Open Drain)	20	13.3	0.9	1.7-5.5	-40 - 125°	SOT23-3	—	—	—
Si7201-B-80-FV	3.4	1.7	3.0	2.0	1.0	Omnipolar switch	Low (Push-Pull)	20	5	0.4	1.7-3.6	0 - 70°	SOT23-3	—	—	—
Si7201-B-81-FV*	3.4	1.7	3.0	2.0	1.0	Omnipolar switch	Low (Push-Pull)	20	5	0.4	1.7-3.6	0 - 70°	SOT23-3	19.84	—	—
Si7201-B-82-FV*	3.4	1.7	3.0	2.0	1.0	Omnipolar switch	High (Push-Pull)	20	5	1.1	1.7-3.6	0 - 70°	SOT23-3	19.84	0.12%	4 sample FIR
Si7201-B-83-IV*	3.7	1.4	3.0	2.0	1.0	Omnipolar switch	High (Push-Pull)	20	1000	56.7	1.7-5.5	-40 - 125°	SOT23-3	—	—	—
Si7201-B-84-IV	3.7	1.4	3.0	2.0	1.0	Omnipolar switch	Low (Push-Pull)	20	5	0.4	1.7-5.5	-40 - 125°	SOT23-3	—	—	—
Si7201-B-85-IV*	3.7	1.4	3.0	2.0	1.0	Omnipolar switch	Low (Push-Pull)	20	5	0.4	1.7-5.5	-40 - 125°	SOT23-3	19.84	—	—
Si7201-B-86-IV	3.7	1.4	3.0	2.0	1.0	Omnipolar switch	Low (Open-drain)	20	5	0.4	1.7-5.5	-40 - 125°	SOT23-3	—	—	—
Si7201-B-87-IV*	3.7	1.4	3.0	2.0	1.0	Omnipolar switch	Low (Open-drain)	20	5	0.4	1.7-5.5	-40 - 125°	SOT23-3	19.84	—	—

Not Recommended For New Designs

OPN	Bop max (mT)	Brp min (mT)	Bop Typ (mT)	Brp Typ (mT)	Hyst (mT)	Type	Output type	Full Scale (mT)	Sample frequency (Hz)	Typical Idd (uA)	Vdd Range (V)	Temperature (°C)	Package	Tamper detection (mT)	Temperature compensation (% per °C)	Digital filtering
Si7203-B-00-FV*	1.1	0.2	0.8	0.4	0.4	Omnipolar switch	High (Open Drain)	20	1000	412	1.7-3.6	0 - 70°	SOT23-5	19.8	—	—
Si7205-B-00-IV*	3.0	0.8	2.2	1.6	0.6	Omnipolar switch	Low (Open Drain)	20	1000	950	3.3-26.5	-40 - 125°	SOT23-3	—	—	—
***Note:** End of life.																

Not Recommended For New Designs

Table 5.2. 3-pin Latch Product Selection Guide

OPN	Brp Typ [mT]	Bop Typ [mT]	Brp min [mT]	Brp max [mT]	Bop min [mT]	Bop max [mT]	Hyst (mT)	Type	Output Type	Output (+ field)	Sam-ples Freq (Hz)	Idd Typ	Vdd min	Vdd max	Temp Range	Pack-age
Si7202-B-00-FV*	-0.4	0.4	-0.7	-0.1	0.1	0.7	0.8	Latch	Push Pull	High	5	0.4	1.7	3.6	0 - 70°	SOT23-3
Si7202-B-01-IB*	-1.0	1.0	-1.5	-0.5	0.5	1.5	1.9	Latch	Push Pull	Low	5	0.4	1.7	5.5	-40 - 125°	TO92
Si7202-B-01-IV	-1.0	1.0	-1.5	-0.5	0.5	1.5	1.9	Latch	Push Pull	Low	5	0.4	1.7	5.5	-40 - 125°	SOT23-3
Si7202-B-02-IV*	-5.1	5.1	-6.1	-4.3	4.3	6.1	10.2	Latch	Push Pull	High	5	0.4	1.7	5.5	-40 - 125°	SOT23-3
Si7202-B-04-IB*	-1.0	1.0	-1.5	-0.5	0.5	1.5	1.9	Latch	Push Pull	Low	5	0.4	1.7	5.5	-40 - 125°	TO92
Si7206-B-00-IV*	-1.0	1.0	-1.5	-0.5	0.5	1.5	1.9	Latch	Open Drain	Low	1000	950	3.3	26.5	-40 - 125°	SOT23-3
***Note:** End of life.																

Not Recommended For New Designs

Table 5.3. 5-pin Latch Product Selection Guide

OPN	Brp Typ [mT]	Bop Typ [mT]	Brp min [mT]	Brp max [mT]	Bop min [mT]	Bop max [mT]	Hyst (mT)	Pin 1	Pin 3	Idle/ Sleep Mode	Type	Output (+ field)	Sam-ples Freq (Hz)	Idd Typ	Vdd min	Vdd max	Temp Range	Pack-age
Si7204 - B-00-FV*	-0.9	0.9	-1.2	-0.6	0.6	1.2	1.8	No Con-nect	Disable	Idle	Latch	High	1000	-	1.7	3.6	0 - 70°	SOT23 -5
***Note:** End of life.																		

Not Recommended For New Designs

Additional Information

For information on the below specifications of each OPN please refer to the Magnetic Sensors Selector Guide:

- Current Consumption
- Amount of digital filtering applied to the samples
- Time between measurements
- Temperature compensation

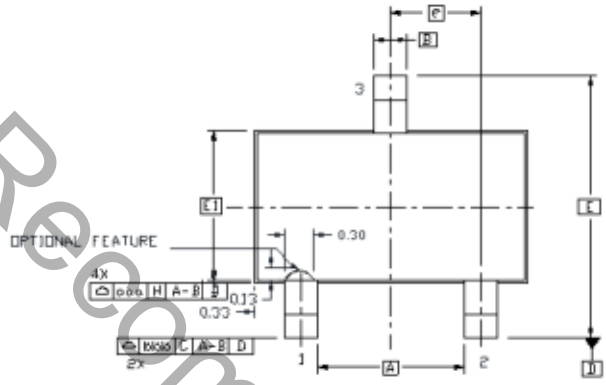
A temperature compensation can be applied to the field data to adjust for the variation in field with temperature for common magnet types.

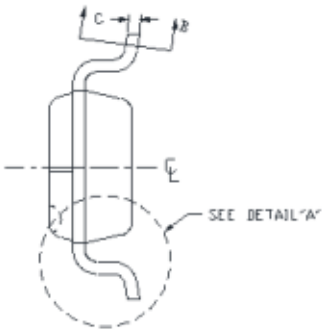
Note: North pole of a magnet at the bottom of a SOT23 package or front of a TO92 package is defined as positive field.

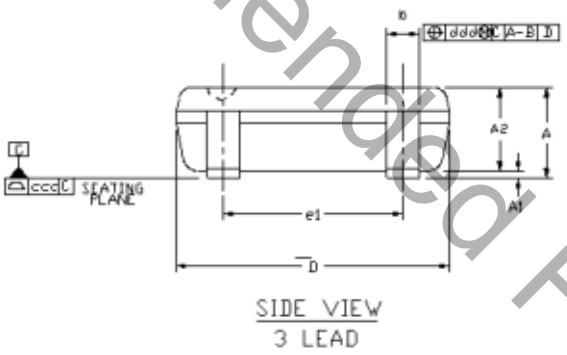
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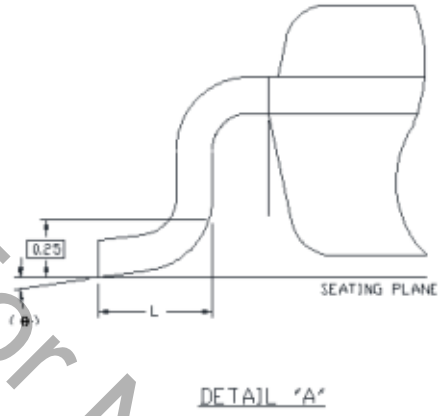
6. Package Outline

6.1 SOT23 3-Pin Package









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Table 6.1. SOT23 3-Pin Package Dimensions

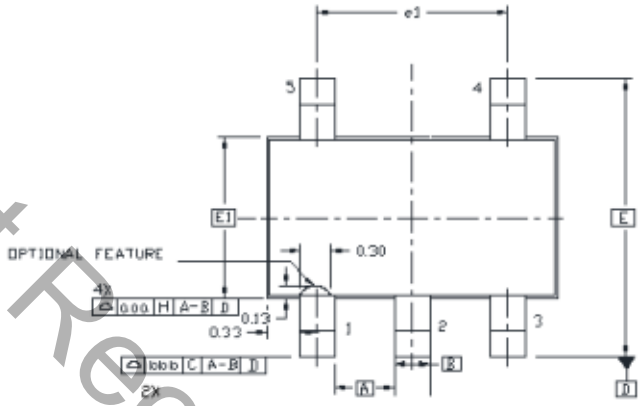
Dimension	Min	Max
A	--	1.25
A1	0.00	0.10
A2	0.85	1.15
b	0.30	0.50
c	0.10	0.20
D	2.90 BSC	
E	2.75 BSC	
E1	1.60 BSC	
e	0.95 BSC	
e1	1.90 BSC	
L	0.30	0.60
θ	0°	8°
aaa	0.15	
bbb	0.20	
ccc	0.10	
ddd	0.20	

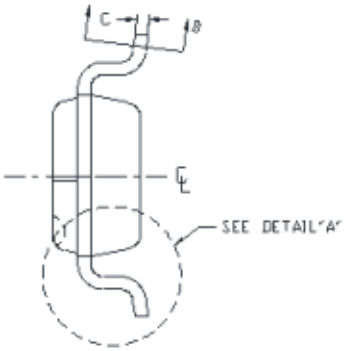
Note:

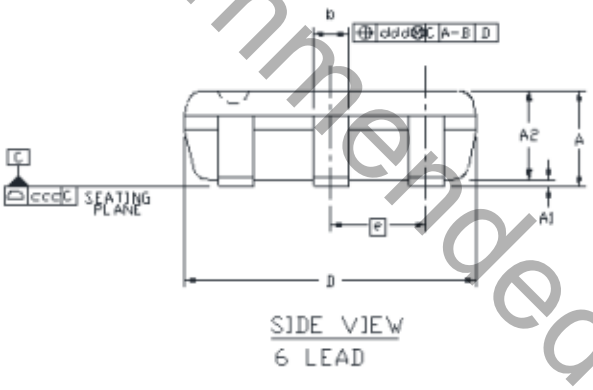
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-193, Variation AB.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020D specification for Small Body Components.

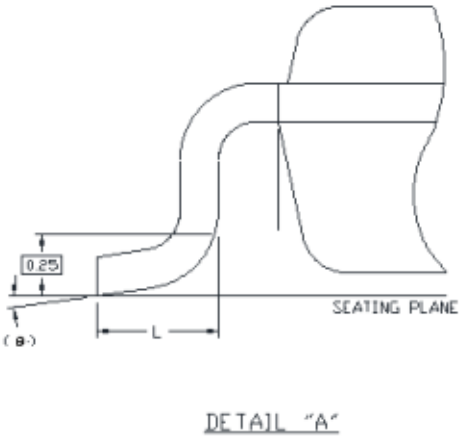
Not Recommended For New Designs

6.2 SOT23-5 5-Pin Package









Not Recommended For New Designs

Table 6.2. SOT23-5 5-Pin Package Dimensions

Dimension	Min	Max
A	--	1.25
A1	0.00	0.10
A2	0.85	1.15
b	0.30	0.50
c	0.10	0.20
D	2.90 BSC	
E	2.75 BSC	
E1	1.60 BSC	
e	0.95 BSC	
e1	1.90 BSC	
L	0.30	0.60
L2	0.25 BSC	
θ	0°	8°
aaa	0.15	
bbb	0.20	
ccc	0.10	
ddd	0.20	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-193, Variation AB.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020D specification for Small Body Components.

Not Recommended For New Designs

6.3 TO92S 3-Pin Package

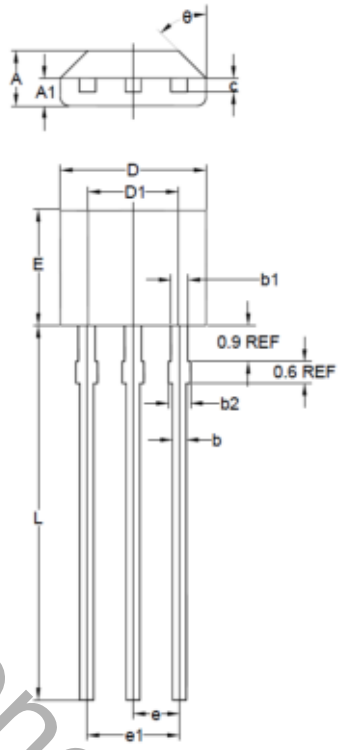


Table 6.3. TO92S 3-Pin Package Dimensions

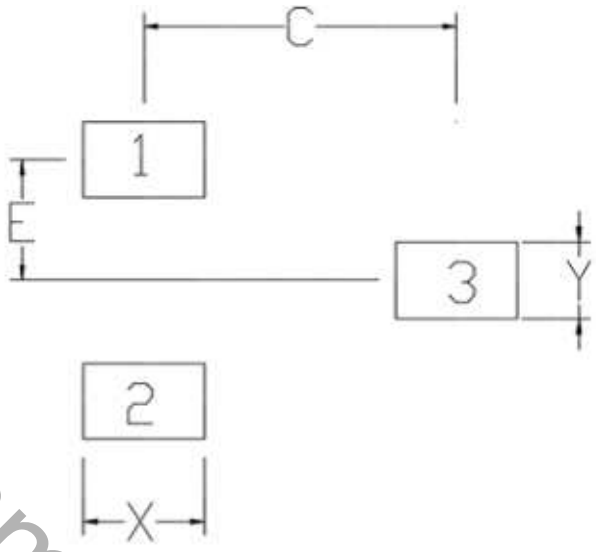
Dimension	Min	Max
A	1.42	1.62
A1	0.66	0.86
b	0.33	0.48
b1	0.40	0.51
b2	0	0.76
c	0.33	0.51
D	3.90	4.10
D1	2.28	2.68
E	3.05	3.25
e	1.27 TYP	
e1	2.44	2.46
L	15.10	15.50
θ	45° TYP	

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

Not Recommended For New Designs

7. Land Patterns

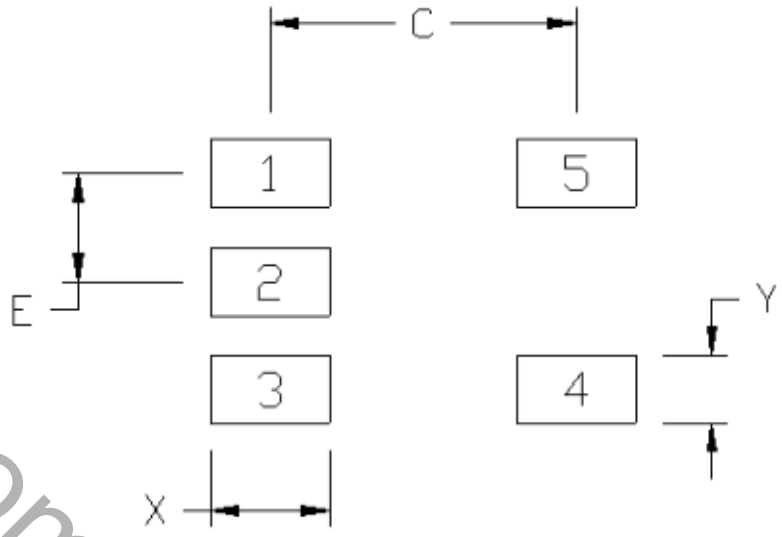
7.1 SOT23 3-Pin PCB Land Pattern



Dimension	(mm)
C	2.70
E	0.95
X	1.05
Y	0.60

Not Recommended For New Designs

7.2 SOT23-5 5-Pin PCB Land Pattern



Dimension	(mm)
C	2.70
E	0.95
X	1.05
Y	0.60

Note:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

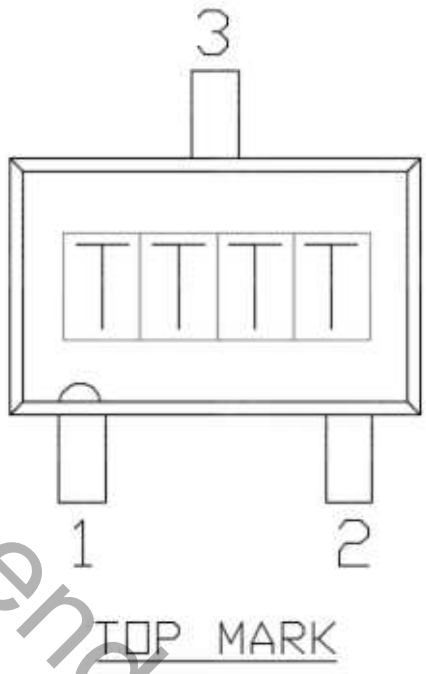
Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020D specification for Small Body Components.

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8. Top Marking

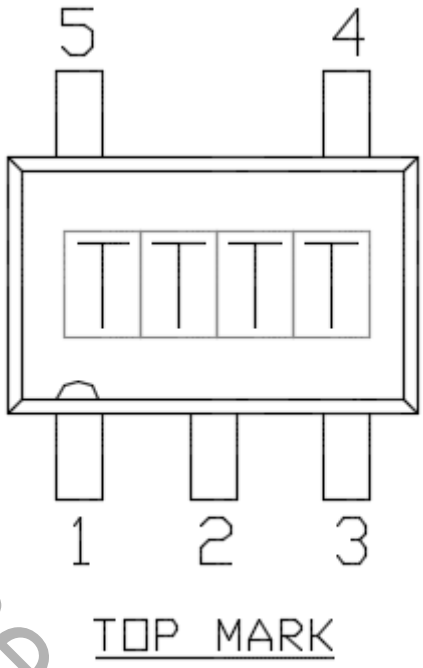
8.1 SOT23 3-Pin Top Marking



Note: TTTT is a manufacturing code.

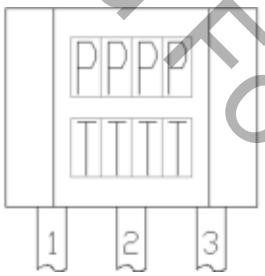
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8.2 SOT23-5 5-Pin Top Marking



Note: TTTT is a manufacturing code.

8.3 TO92 Top Marking



Note: TTTT is a manufacturing code. PPPP is OPN Top Mark as shown below.

OPN	PPPP Top Mark
Si7201-B-09-IB	7201
Si7201-B-11-IB	7201
Si7202-B-01-IB	Si72
Si7202-B-04-IB	7202

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9. Revision History

Revision 1.7

May, 2025
- Added EOL note for specific Si7201/02/03/04 OPNs in the Ordering Guide.

Revision 1.6

May, 2024
- Added table to 8.3 TO92 Top Marking.

Revision 1.5

August, 2023
- Corrected top mark for the TO92 package.
- Removed erroneous mention of DFN8 pacakge.
- Added EOL note for specific Si7201/02 OPNs in the Ordering Guide.

Revision 1.4

May, 2020
- Added EOL note for Si7205/06 in the Ordering Guide (200324717 End of Life Notification for High Voltage Si72xx Devices).

Revision 1.3

October, 2019
- Updated Chapter 5. Ordering Guide with newly released part numbers.
  - Si7203-B-01-IV
- Added specific pinout for newly release Si7203-B-01-IV

Revision 1.2

July, 2019
- Updated Chapter 5. Ordering Guide with newly released part numbers.
  - Si7201-B-1x
  - Si7201-B-2x
  - Si7201-B-3x
  - Si7201-B-4x
  - Si7201-B-8x
  - Si7201-B-9x
- Updated wording on frontpage to clarify package types and switch vs latch

Revision 1.1

March, 2019
- Removed all mention of AEC-Q100 qualification in product description and feature list.

Revision 1.0

July 2018
- Updated power numbers to be consistent with production test limits.
- Added more detailed part characteristics to the ordering guide.
- Updated detailed description to be clearer and more accurate.

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Revision 0.92

October 4, 2017

- Added new part number to Chapter 5. Ordering Guide (Si7202-B-01-IV(R).

Revision 0.91

August 7, 2017

- Added new part number to Chapter 5. Ordering Guide (Si7201-B-08-IV(R).

Revision 0.9

June 30, 2017

- Updated Chapter 1. Electrical Specifications .
- Updated Chapter 5. Ordering Guide.
- Minor typo corrections.

Revision 0.1

February 1, 2016

- Initial release.

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