Si8239x Data Sheet

4.0 A ISODrivers with 2.5 V VDDI and Safety Features

The Si8239x combines two isolated drivers with either an independent input control or a single input into a single package for high power applications. All drivers operate with a 2.5 V input VDD and a maximum drive supply voltage of 24 V.

The Si8239x isolators are ideal for driving power MOSFETs and IGBTs used in a wide variety of switched power and motor control applications. These drivers utilize Skyworks Solutions' proprietary silicon isolation technology, supporting up to 5 kVRMS withstand voltage. This technology enables high CMTI (100 kV/µs), lower prop delays and skew, reduced variation with temperature and age and tighter part-to-part matching.

It also offers some unique features such as an output UVLO fault detection and feedback, and automatic shutdown for both drivers, an EN (active high) pin, a safe delayed start-up time of 1 ms, fail-safe drivers with default low in case of VDDI power-down, and dead time programmability. The Si8239x family offers longer service life and dramatically higher reliability compared to opto-coupled gate drivers.

Automotive Grade is available for certain part numbers. These products are built using automotive-specific flows at all steps in the manufacturing process to ensure the robustness and low defectivity required for automotive applications.

Industrial Applications

- Power Delivery Systems
- Motor Control Systems
- Isolated DC-DC Power Supplies
- Lighting Control Systems
- Solar and Industrial Inverters

Safety Approvals (Pending)

- UL 1577 recognized
  - Up to 5000 Vrms for 1 minute
- CSA approval
  - IEC60950-1, 62368-1 (reinforced insulation)
- VDE certification conformity
  - VDE 0884-10 (basic insulation)
  - EN60950-1, 62368-1 (reinforced insulation)
- CQC certification approval
  - GB4943.1-2011 (reinforced insulation)

Automotive Applications

- On-board chargers
- Battery management systems
- Charging stations
- Traction inverters
- Hybrid Electric Vehicles
- Battery Electric Vehicles

KEY FEATURES

- Two isolated drivers in one package
  - Up to 5 kVRMS isolation
  - Up to 1500 VDC peak driver-to-driver differential voltage
- Enhanced output UVLO safety
  - Status feedback to controller
  - Both outputs drive low on UVLO
- EN pin for enhanced safety
- Extended VDDI: 2.5 V – 5.5 V
- PWM and dual driver versions
- 4.0 A peak output
- High electromagnetic immunity
- Extended start-up time (1ms) for safe initialization sequence
- 30 ns propagation delay
- Transient immunity: 100 kV/µs
- Programmable dead time
  - 10–200 ns
  - 40–600 ns
- Deglitch option for filtering noise
- Wide operating range
  - –40 to +125 °C
- RoHS-compliant packages
  - SOIC-14/-16 wide body
  - SOIC-16 narrow body
- AEC-Q100 qualified
- Automotive-grade OPNs available
  - AIAG compliant PPAP documentation support
  - IMDS and CAMDS listing support

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1. Ordering Guide

Industrial and Automotive Grade OPNs

Industrial-grade devices (part numbers having an “-I” in their suffix) are built using well-controlled, high-quality manufacturing flows to ensure robustness and reliability. Qualifications are compliant with JEDEC, and defect reduction methodologies are used throughout definition, design, evaluation, qualification, and mass production steps.

Automotive-grade devices (part numbers having an “-A” in their suffix) are built using automotive-specific flows at all steps in the manufacturing process to ensure robustness and low defectivity. These devices are supported with AIAG-compliant Production Part Approval Process (PPAP) documentation, and feature International Material Data System (IMDS) and China Automotive Material Data System (CAMDS) listing. Qualifications are compliant with AEC-Q100, and a zero-defect methodology is maintained throughout definition, design, evaluation, qualification, and mass production steps.

Table 1.1. Si8239x Ordering Guide

Ordering Part Number (OPN)	Automotive Grade OPN	Output UVLO	Enhanced UVLO	UVLO Status Pin	Delayed Startup Time	Dead-Time Setting	Deglitch	Package Type
Independent dual drivers with separate VIA, VIB inputs								
Si82390AB-IS1	Si82390AB-AS1	6 V	Yes	Yes	Yes	N/A	No	SOIC-16 NB
Si82390BB-IS1	Si82390BB-AS1	8 V	Yes	Yes	Yes	N/A	No	SOIC-16 NB
Si82390CB-IS1	Si82390CB-AS1	12 V	Yes	Yes	Yes	N/A	No	SOIC-16 NB
Si82391AB-IS1	Si82391AB-AS1	6 V	Yes	Yes	No	N/A	No	SOIC-16 NB
Si82391BB-IS1	Si82391BB-AS1	8 V	Yes	Yes	No	N/A	No	SOIC-16 NB
Si82391CB-IS1	Si82391CB-AS1	12 V	Yes	Yes	No	N/A	No	SOIC-16 NB
Si82395AB-IS1	Si82395AB-AS1	6 V	No	Yes	Yes	N/A	No	SOIC-16 NB
Si82395BB-IS1	Si82395BB-AS1	8 V	No	Yes	Yes	N/A	No	SOIC-16 NB
Si82395CB-IS1	Si82395CB-AS1	12 V	No	Yes	Yes	N/A	No	SOIC-16 NB
Si82396AB-IS1	Si82396AB-AS1	6 V	No	Yes	No	N/A	No	SOIC-16 NB
Si82396BB-IS1	Si82396BB-AS1	8 V	No	Yes	No	N/A	No	SOIC-16 NB
Si82396CB-IS1	Si82396CB-AS1	12 V	No	Yes	No	N/A	No	SOIC-16 NB
Si82390AD-IS	Si82390AD-AS	6 V	Yes	Yes	Yes	N/A	No	SOIC-16 WB
Si82390BD-IS	Si82390BD-AS	8 V	Yes	Yes	Yes	N/A	No	SOIC-16 WB
Si82390CD-IS	Si82390CD-AS	12 V	Yes	Yes	Yes	N/A	No	SOIC-16 WB
Si82391AD-IS	Si82391AD-AS	6 V	Yes	Yes	No	N/A	No	SOIC-16 WB
Si82391BD-IS	Si82391BD-AS	8 V	Yes	Yes	No	N/A	No	SOIC-16 WB
Si82391CD-IS	Si82391CD-AS	12 V	Yes	Yes	No	N/A	No	SOIC-16 WB
Si82395AD-IS	Si82395AD-AS	6 V	No	Yes	Yes	N/A	No	SOIC-16 WB
Si82395BD-IS	Si82395BD-AS	8 V	No	Yes	Yes	N/A	No	SOIC-16 WB
Si82395CD-IS	Si82395CD-AS	12 V	No	Yes	Yes	N/A	No	SOIC-16 WB
Si82396AD-IS	Si82396AD-AS	6 V	No	Yes	No	N/A	No	SOIC-16 WB
Si82396BD-IS	Si82396BD-AS	8 V	No	Yes	No	N/A	No	SOIC-16 WB
Si82396CD-IS	Si82396CD-AS	12 V	No	Yes	No	N/A	No	SOIC-16 WB

Ordering Part Number (OPN)	Automotive Grade OPN	Output UVLO	Enhanced UVLO	UVLO Status Pin	Delayed Startup Time	Dead-Time Setting	Deglitch	Package Type
Si82397AD-IS	Si82397AD-AS	6 V	No	No	Yes	N/A	No	SOIC-16 WB
Si82397BD-IS	Si82397BD-AS	8 V	No	No	Yes	N/A	No	SOIC-16 WB
Si82397CD-IS	Si82397CD-AS	12 V	No	No	Yes	N/A	No	SOIC-16 WB
Si82390AD-IS3	Si82390AD-AS3	6 V	Yes	Yes	Yes	N/A	No	SOIC-14 WB
Si82390BD-IS3	Si82390BD-AS3	8 V	Yes	Yes	Yes	N/A	No	SOIC-14 WB
Si82390CD-IS3	Si82390CD-AS3	12 V	Yes	Yes	Yes	N/A	No	SOIC-14 WB
Si82391AD-IS3	Si82391AD-AS3	6 V	Yes	Yes	No	N/A	No	SOIC-14 WB
Si82391BD-IS3	Si82391BD-AS3	8 V	Yes	Yes	No	N/A	No	SOIC-14 WB
Si82391CD-IS3	Si82391CD-AS3	12 V	Yes	Yes	No	N/A	No	SOIC-14 WB
Si82395AD-IS3	Si82395AD-AS3	6 V	No	Yes	Yes	N/A	No	SOIC-14 WB
Si82395BD-IS3	Si82395BD-AS3	8 V	No	Yes	Yes	N/A	No	SOIC-14 WB
Si82395CD-IS3	Si82395CD-AS3	12 V	No	Yes	Yes	N/A	No	SOIC-14 WB
Si82396AD-IS3	Si82396AD-AS3	6 V	No	Yes	No	N/A	No	SOIC-14 WB
Si82396BD-IS3	Si82396BD-AS3	8 V	No	Yes	No	N/A	No	SOIC-14 WB
Si82396CD-IS3	Si82396CD-AS3	12 V	No	Yes	No	N/A	No	SOIC-14 WB
Si82397AD-IS3	Si82397AD-AS3	6 V	No	No	Yes	N/A	No	SOIC-14 WB
Si82397BD-IS3	Si82397BD-AS3	8 V	No	No	Yes	N/A	No	SOIC-14 WB
Si82397CD-IS3	Si82397CD-AS3	12 V	No	No	Yes	N/A	No	SOIC-14 WB
High-side/low-side drivers with separate VIA, VIB inputs								
Si82392BB-IS1	Si82392BB-AS1	8 V	No	Yes	No	N/A	No	SOIC-16 NB
Si82393CD-IS	Si82393CD-AS	12 V	Yes	Yes	No	N/A	Yes	SOIC-16 WB
Si82393CD-IS3	Si82393CD-AS3	12 V	Yes	Yes	No	N/A	Yes	SOIC-14 WB
High-side/low-side drivers with single PWM input								
Si82394AB4-IS1	Si82394AB4-AS1	6 V	No	Yes	Yes	40–600 ns	Yes	SOIC-16 NB
Si82394BB4-IS1	Si82394BB4-AS1	8 V	No	Yes	Yes	40–600 ns	Yes	SOIC-16 NB
Si82394CB4-IS1	Si82394CB4-AS1	12 V	No	Yes	Yes	40–600 ns	Yes	SOIC-16 NB
Si82398AB4-IS1	Si82398AB4-AS1	6 V	No	Yes	No	40–600 ns	Yes	SOIC-16 NB
Si82398BB4-IS1	Si82398BB4-AS1	8 V	No	Yes	No	40–600 ns	Yes	SOIC-16 NB
Si82398CB4-IS1	Si82398CB4-AS1	12 V	No	Yes	No	40–600 ns	Yes	SOIC-16 NB
Si82394AD4-IS	Si82394AD4-AS	6 V	No	Yes	Yes	40–600 ns	Yes	SOIC-16 WB
Si82394AD-IS	Si82394AD-AS	6 V	No	Yes	Yes	10–200 ns	No	SOIC-16 WB
Si82394BD4-IS	Si82394BD4-AS	8 V	No	Yes	Yes	40–600 ns	Yes	SOIC-16 WB
Si82394BD-IS	Si82394BD-AS	8 V	No	Yes	Yes	10–200 ns	No	SOIC-16 WB
Si82394CD4-IS	Si82394CD4-AS	12 V	No	Yes	Yes	40–600 ns	Yes	SOIC-16 WB
Si82394CD-IS	Si82394CD-AS	12 V	No	Yes	Yes	10–200 ns	No	SOIC-16 WB

Ordering Part Number (OPN)	Automotive Grade OPN	Output UVLO	Enhanced UVLO	UVLO Status Pin	Delayed Startup Time	Dead-Time Setting	Deglitch	Package Type
Si82398AD4-IS	Si82398AD4-AS	6 V	No	Yes	No	40–600 ns	Yes	SOIC-16 WB
Si82398AD-IS	Si82398AD-AS	6 V	No	Yes	No	10–200 ns	No	SOIC-16 WB
Si82398BD4-IS	Si82398BD4-AS	8 V	No	Yes	No	40–600 ns	Yes	SOIC-16 WB
Si82398BD-IS	Si82398BD-AS	8 V	No	Yes	No	10–200 ns	No	SOIC-16 WB
Si82398CD4-IS	Si82398CD4-AS	12 V	No	Yes	No	40–600 ns	Yes	SOIC-16 WB
Si82398CD-IS	Si82398CD-AS	12 V	No	Yes	No	10–200 ns	No	SOIC-16 WB
Si82394AD4-IS3	Si82394AD4-AS3	6 V	No	Yes	Yes	40–600 ns	Yes	SOIC-14 WB
Si82394AD-IS3	Si82394AD-AS3	6 V	No	Yes	Yes	10–200 ns	No	SOIC-14 WB
Si82394BD4-IS3	Si82394BD4-AS3	8 V	No	Yes	Yes	40–600 ns	Yes	SOIC-14 WB
Si82394BD-IS3	Si82394BD-AS3	8 V	No	Yes	Yes	10–200 ns	No	SOIC-14 WB
Si82394CD4-IS3	Si82394CD4-AS3	12 V	No	Yes	Yes	40–600 ns	Yes	SOIC-14 WB
Si82394CD-IS3	Si82394CD-AS3	12 V	No	Yes	Yes	10–200 ns	No	SOIC-14 WB
Si82398AD4-IS3	Si82398AD4-AS3	6 V	No	Yes	No	40–600 ns	Yes	SOIC-14 WB
Si82398AD-IS3	Si82398AD-AS3	6 V	No	Yes	No	10–200 ns	No	SOIC-14 WB
Si82398BD4-IS3	Si82398BD4-AS3	8 V	No	Yes	No	40–600 ns	Yes	SOIC-14 WB
Si82398BD-IS3	Si82398BD-AS3	8 V	No	Yes	No	10–200 ns	No	SOIC-14 WB
Si82398CD4-IS3	Si82398CD4-AS3	12 V	No	Yes	No	40–600 ns	Yes	SOIC-14 WB
Si82398CD-IS3	Si82398CD-AS3	12 V	No	Yes	No	10–200 ns	No	SOIC-14 WB

Note:

1. All products are rated at 4 A output drive current max, VDDI = 2.5 V – 5.5 V, EN (active high).
2. All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.
3. “Si” and “SI” are used interchangeably.
4. An "R" at the end of the part number denotes tape and reel packaging option.
5. Automotive-Grade devices (with an "–A" suffix) are identical in construction materials, topside marking, and electrical parameters to their Industrial-Grade (with a "–I" suffix) version counterparts. Automotive-Grade products are produced utilizing full automotive process flows and additional statistical process controls throughout the manufacturing flow. The Automotive-Grade part number is included on shipping labels.
6. Referring to 13. Top Markings , the Manufacturing Code represented by either “RTTTTT” or “TTTTTT” contains as its first character a letter in the range N through Z to indicate Automotive-Grade.

2. System Overview

The operation of an Si8239x channel is analogous to that of an optocoupler and gate driver, except an RF carrier is modulated instead of light. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up. A simplified block diagram for a single Si8239x channel is shown in the following figure.

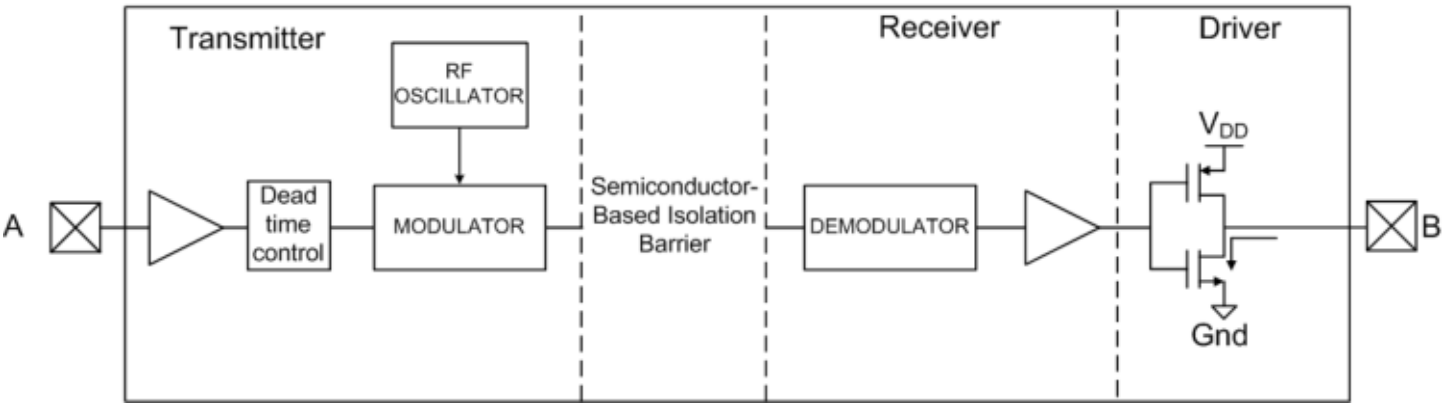


Figure 2.1. Simplified Channel Diagram

A channel consists of an RF Transmitter and RF Receiver separated by a semiconductor-based isolation barrier. Referring to the Transmitter, input A modulates the carrier provided by an RF oscillator using on/off keying. The Receiver contains a demodulator that decodes the input state according to its RF energy content and applies the result to output B via the output driver. This RF on/off keying scheme is superior to pulse code schemes as it provides best-in-class noise immunity, low power consumption, and better immunity to magnetic fields. See the following figure for more details.

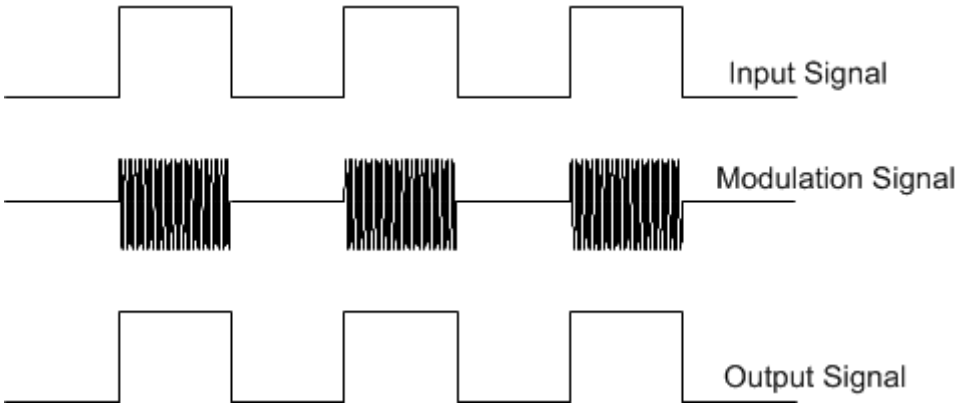


Figure 2.2. Modulation Scheme

2.1 Typical Performance Characteristics

The typical performance characteristics depicted in the following figures are for information purposes only. Refer to the Electrical Characteristics table for actual specification limits.

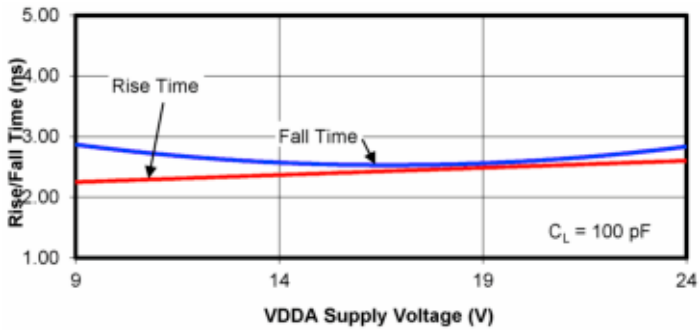


Figure 2.3. Rise/Fall Time vs. Supply Voltage

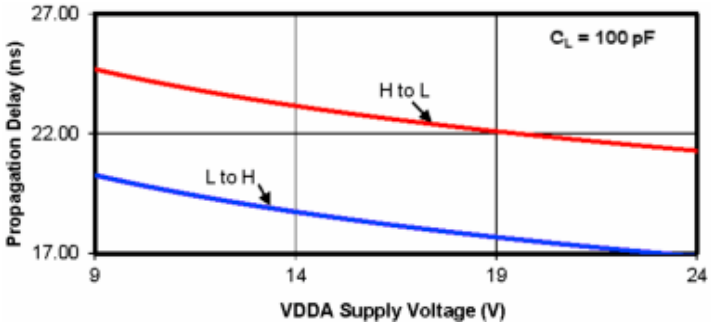


Figure 2.4. Propagation Delay vs. Supply Voltage

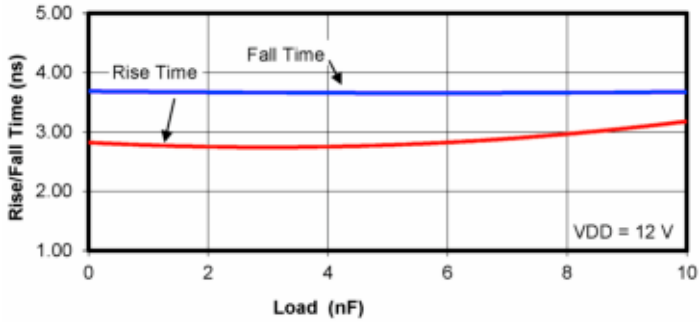


Figure 2.5. Rise/Fall Time vs. Load

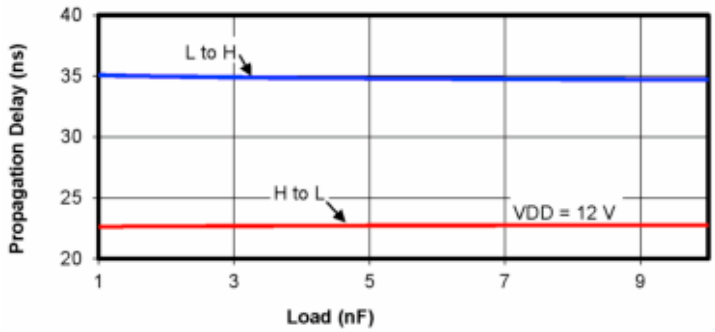


Figure 2.6. Propagation Delay vs. Load

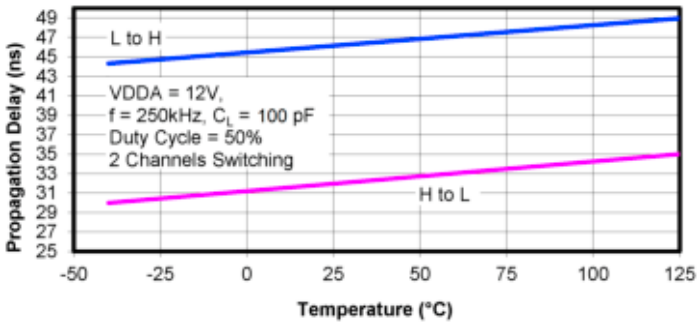


Figure 2.7. Propagation Delay vs. Temperature

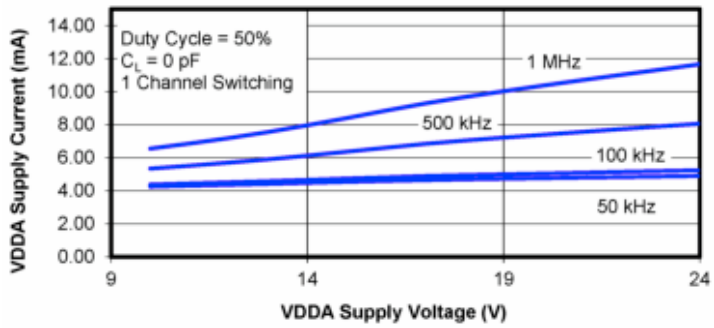


Figure 2.8. Supply Current vs. Supply Voltage

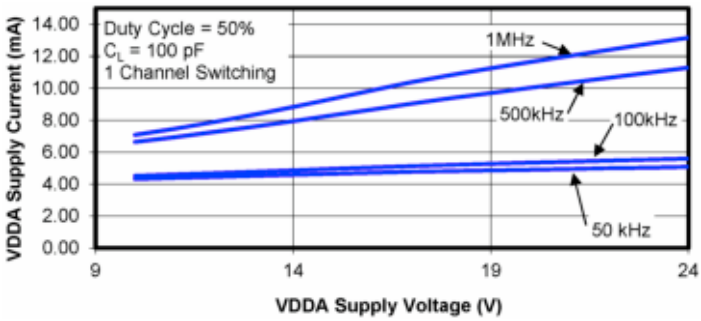


Figure 2.9. Supply Current vs. Supply Voltage

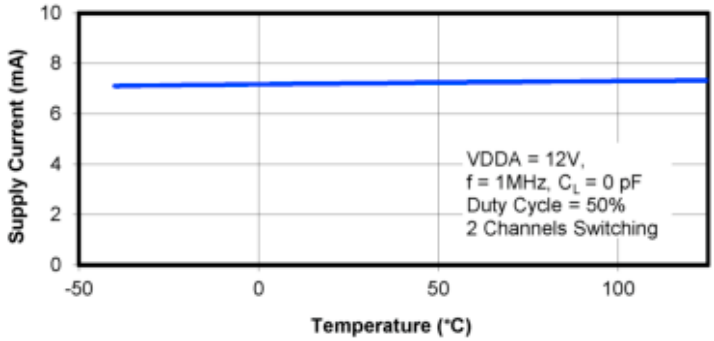


Figure 2.10. Supply Current vs. Temperature

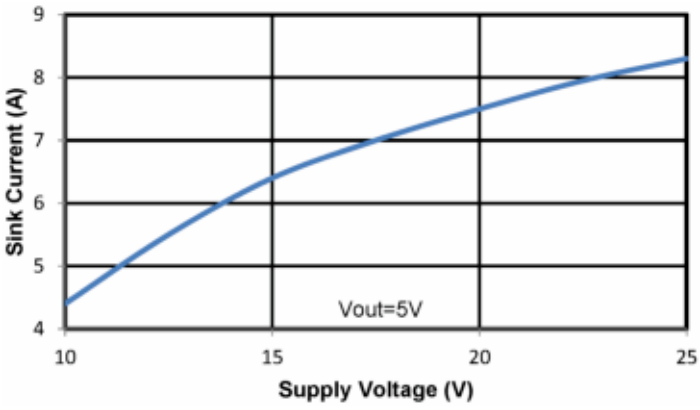


Figure 2.11. Output Sink Current vs. Supply Voltage

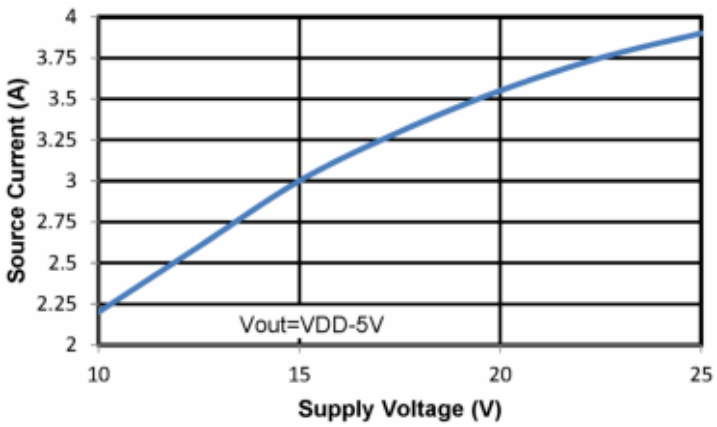


Figure 2.12. Output Source Current vs. Supply Voltage

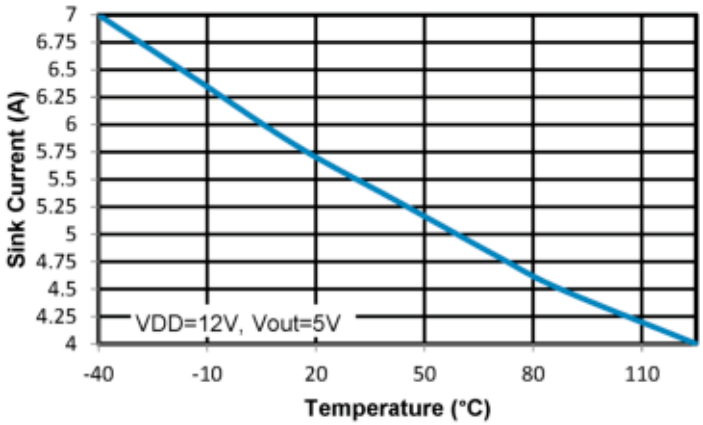


Figure 2.13. Output Sink Current vs. Temperature

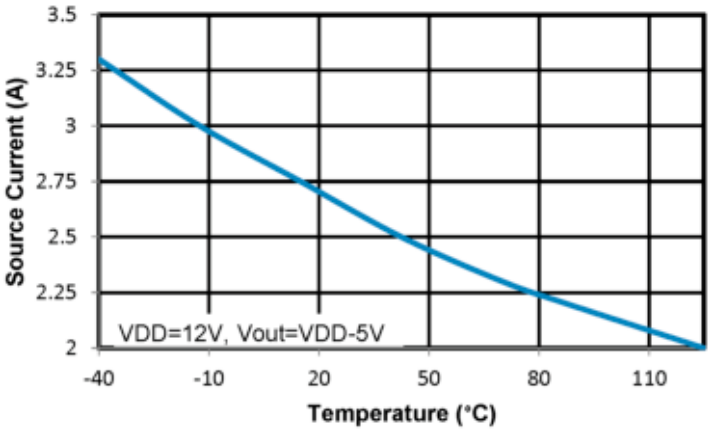


Figure 2.14. Output Source Current vs. Temperature

2.2 Family Overview and Logic Operation During Startup

The Si8239x family of isolated drivers consists of high-side/low-side and dual driver configurations.

2.2.1 Device Behavior

The following are truth tables for the Si8239x families.

Table 2.1. Si82390/1/3 Drivers Enhanced UVLO and Status

VIA	VIB	EN[1]	VDDI	VDDA	VDDB	VOA	VOB	RDY	Notes
H	L	H	P[2]	P	P	H	L	H	
L	H	H	P	P	P	L	H	H	
H	H	H	P	P	P	H / L[4]	H / L[4]	H	
L	L	H	P	P	P	L	L	H	
X	X	L/NC	P	P	P	L	L	H	Device disabled
X	X	X	UP[2]	P	P	L	L	UD[3]	Fail-safe output when VDDI unpowered
X	X	H	P	P	UP	L	UD	L	VOA, VOB are actively driven low if either VDDA or VDDB is UP
X	X	H	P	UP	P	UD	L	L	

Note:

1. The EN pin needs to be pulled down with a 100 kΩ resistor externally to GND.
2. The chip can be powered through the VIA,VIB input ESD diodes even if VDDI is unpowered. It is recommended that inputs be left unpowered when VDDI is unpowered. The EN pin has a special ESD circuit that prevents the IC from powering up through the EN pin.
3. UD = undetermined if same side power is UP.
4. VOA = VOB = L for Si82393 only

Table 2.2. Si82392/5/6 Drivers with UVLO Status

VIA	VIB	EN[1]	VDDI	VDDA	VDDB	VOA	VOB	RDY	Notes
H	L	H	P	P	P	H	L	H	
L	H	H	P	P	P	L	H	H	
H	H	H	P	P	P	H / L[4]	H / L[4]	H	
L	L	H	P	P	P	L	L	H	
X	X	L/NC	P	P	P	L	L	H	Device disabled
X	X	X	UP[2]	P	P	L	L	UD[3]	Fail-safe output when VDDI unpowered
H	X	H	P	P	UP	H	UD	L	VOA depends on VDDA state
L	X	H	P	P	UP	L	UD	L	
X	H	H	P	UP	P	UD	H	L	VOB depends on VDDB state
X	L	H	P	UP	P	UD	L	L	

VIA	VIB	EN[1]	VDDI	VDDA	VDDB	VOA	VOB	RDY	Notes

Note:

1. The EN pin needs to be pulled down with a 100 kΩ resistor externally to GND.
2. The chip can be powered through the VIA,VIB input ESD diodes even if VDDI is unpowered. It is recommended that inputs be left unpowered when VDDI is unpowered. The EN pin has a special ESD circuit that prevents the IC from powering up through the EN pin.
3. UD = undetermined if same side power is UP.
4. VOA = VOB = L for Si82392 only

Table 2.3. Si82397 Dual Drivers with No UVLO Status

VIA	VIB	EN[1]	VDDI	VDDA	VDDB	VOA	VOB	Notes
H	L	H	P	P	P	H	L	
L	H	H	P	P	P	L	H	
H	H	H	P	P	P	H	H	
L	L	H	P	P	P	L	L	
X	X	L/NC	P	P	P	L	L	Device disabled
X	X	X	UP[2]	P	P	L	L	Fail-safe output when VDDI is unpowered
H	X	H	P	P	UP	H	UD[3]	VOA depends on VDDA state
L	X	H	P	P	UP	L	UD	
X	H	H	P	UP	P	UD	H	VOB depends on VDDB state
X	L	H	P	UP	P	UD	L	

Note:

1. The EN pin needs to be pulled down with a 100 kΩ resistor externally to GND.
2. The chip can be powered through the VIA,VIB input ESD diodes even if VDDI is unpowered. It is recommended that inputs be left unpowered when VDDI is unpowered. The EN pin has a special ESD circuit that prevents the IC from powering up through the EN pin.
3. UD = undetermined if same side power is UP.

Table 2.4. Si82394/8 PWM Input HS/LS Drivers with UVLO Status

PWM	EN[1]	VDDI	VDDA	VDDB	VOA	VOB	RDY	Notes
H	H	P	P	P	H	L	H	See Dead-time note and Figure 2.18 Dead Time Waveforms for High-Side/Low-Side Drivers on page 17 for timing
L	H	P	P	P	L	H	H	
X	L/NC	P	P	P	L	L	H	Device disabled
X	X	UP[2]	P	P	L	L	UD[3]	Fail-safe output when VDDI unpowered
H	H	P	P	UP	H	UD	L	VOA depends on VDDA state
L	H	P	P	UP	L	UD	L	

PWM	EN[1]	VDDI	VDDA	VDDB	VOA	VOB	RDY	Notes
H	H	P	UP	P	UD	L	L	VOB depends on VDDB state
L	H	P	UP	P	UD	H	L	

Note:

1. The EN pin needs to be pulled down with a 100 kΩ resistor externally to GND.
2. The chip can be powered through the PWM input ESD diodes even if VDDI is unpowered. It is recommended that inputs be left unpowered when VDDI is unpowered. The EN pin has a special ESD circuit that prevents the IC from powering up through the EN pin.
3. UD = undetermined if same side power is UP.

2.3 Power Supply Connections

Isolation requirements mandate separating VDDI from the driver supplies. The decoupling caps for these supplies must be placed as close to the VDD and GND pins of the Si8239x as possible. The optimum values for these capacitors are 1 µF and 0.1 µF for VDDI and 10 µF and 0.1 µF for each driver supply. Low effective series resistance (ESR) capacitors, such as Tantalum, are recommended.

2.4 Power Dissipation Considerations

Proper system design must assure that the Si8239x operates within safe thermal limits across the entire load range.The Si8239x total power dissipation is the sum of the power dissipated by bias supply current, internal parasitic switching losses, and power dissipated by the series gate resistor and load. Equation 1 shows total Si8239x power dissipation.

$$P_D = (V_{DDI})(I_{DDI}) + 2(I_{DD2})(V_{DD2}) + \left(f\right)\left(Q_G\right)\left(V_{DD2}\right)\left[\frac{R_P}{R_P + R_G}\right] + \left(f\right)\left(Q_G\right)\left(V_{DD2}\right)\left[\frac{R_N}{R_N + R_G}\right] + 2(f)(Cint)(V_{DD2})^2$$

where:

P_D is the total Si8239x device power dissipation (W)

I_{DDI} is the input-side maximum bias current (from table 4.1, 3.8 mA)

I_{DD2} is the driver die maximum bias current (from table 4.1, 6.5 mA)

C_{int} is the internal parasitic capacitance (370 pF)

V_{DDI} is the input-side VDD supply voltage (2.7 to 5.5 V)

V_{DD2} is the driver-side supply voltage (10 to 24 V)

f is the switching frequency (Hz)

Q_G is the total gate charge of the FET being driven (C)

R_G is the external gate resistor (Ω)

R_P is the $R_{DS(ON)}$ of the driver pull-up switch: (2.7 Ω)

R_N is the $R_{DS(ON)}$ of the driver pull-down switch: (1 Ω)

Example calculation (using IDDX values from Table 4.1 for Si82397)

V_{DDI} = 5.0 V

V_{DD2} = 12 V

f = 350 kHz

R_G = 22 Ω

Q_G = 24 nC

$$P_D = (5.0)(.0021) + 2(.0025)(12) + \left(350000\right)\left(.000000024\right)(12)\left[\frac{2.7}{2.7 + 22}\right] + \left(350000\right)\left(.000000024\right)(12)\left[\frac{1}{1+22}\right] + 2(350000)(370)(12)^2$$

$$P_D = 0.123 \text{ W}$$

123 mW is the total dissipated power by the Si8239x package.

From this, the driver junction temperature is calculated using Equation 2.

$$\begin{aligned} T_j &= P_d \times \Theta_{ja} + T_A \\ &= 0.123 \times 59 + 25 = 32.3°C \end{aligned}$$

Where:

T_j is the junction temperature (°C)

T_A is the ambient temperature (°C)

P_d is the power dissipated in the package (W)

θ_{ja} is the thermal resistance from junction to air (59 °C/W from table 4.7)

The maximum power dissipation allowable for the Si8239x is a function of the package thermal resistance, ambient temperature, and maximum allowable junction temperature, as shown in Equation 2:

$$P_{Dmax} \leq \frac{T_{jmax} - T_A}{\Theta ja} = 2.12 \quad W$$

Where:

P_{Dmax} is the maximum allowed power dissipation (W)

T_{jmax} is the maximum allowed junction temperature (150 °C from table 4.8)

T_A is the ambient temperature (25 °C in this example)

Θ_{ja} is the junction-to-air thermal resistance of the package (59°C/W from table 4.7)

Substituting values used in this example back into Equation 1, establishes a relationship between the maximum capacitive load and switching frequency.

The following figure shows the relationship between the capacitive load and the switching frequency for four different driver supply voltages. In the figure, the points along the load line represent the package dissipation-limited value of CL as a function of switching frequency.

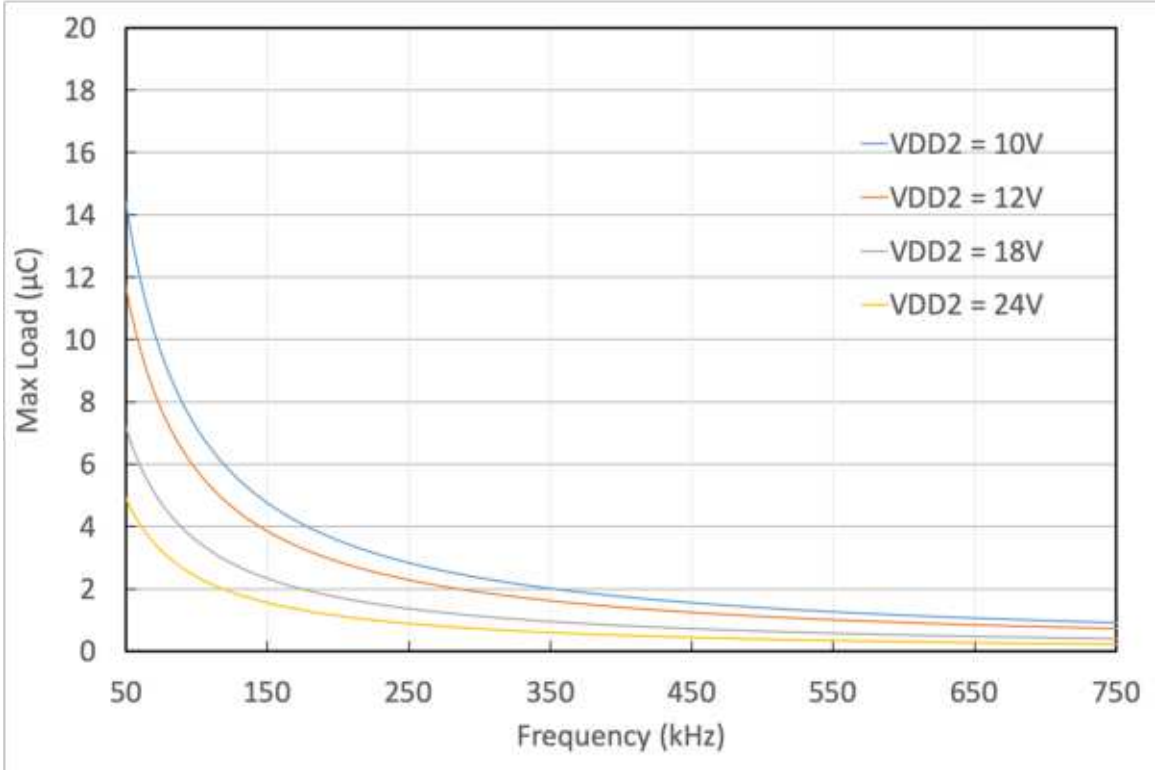


Figure 2.15. Max Load vs. Switching Frequency

2.5 Layout Considerations

It is most important to minimize ringing in the drive path and noise on the Si8239x VDD lines. Care must be taken to minimize parasitic inductance in these paths by locating the Si8239x as close to the device it is driving as possible. In addition, the VDD supply and ground trace paths must be kept short. For this reason, the use of power and ground planes is highly recommended. A split ground plane system having separate ground and VDD planes for power devices and small signal components provides the best overall noise performance.

2.6 Undervoltage Lockout Operation

Device behavior during start-up, normal operation and shutdown is shown in Figure 2.16 Si82391/2/3/6/8 Device Behavior during Normal Operation and Shutdown on page 15, where UVLO+ and UVLO- are the positive-going and negative-going thresholds respectively. Note that outputs VOA and VOB default low when input side power supply (VDDI) is not present.

2.6.1 Device Startup

Outputs VOA and VOB are held low during power-up until VDD is above the UVLO threshold for time period tSTART. Following this, the outputs follow the states of inputs VIA and VIB.

2.6.2 Undervoltage Lockout

Undervoltage Lockout (UVLO) is provided to prevent erroneous operation during device startup and shutdown or when VDD is below its specified operating circuits range. The input (control) side, Driver A and Driver B, each have their own undervoltage lockout monitors.

The Si8239x input side enters UVLO when VDDI < VDDIUV–, and exits UVLO when VDDI > VDDIUV+. The driver outputs, VOA and VOB, remain low when the input side of the Si8239x is in UVLO and their respective VDD supply (VDDA, VDDB) is within tolerance. Each driver output can enter or exit UVLO independently for the Si82394/5/6/7/8 products. For example, VOA unconditionally enters UVLO when VDDA falls below VDDAUV– and exits UVLO when VDDA rises above VDDAUV+. For the Si82390/1/3 products, when either VDDA or VDDB falls under VDDxUV–, this information is fed back through the isolation barrier to the input side logic which forces VOB or VOA to be driven low respectively under these conditions. If the application is driving a transformer for an isolated power converter, for example, this behavior is useful to prevent flux imbalances in the transformer. Please note that this feature implies that it can only be implemented when the VDDA and VDDB power supplies are independent from each other. If a bootstrap circuit is used for Si82390/1/3, it will prevent the IC from powering up. Do not use the Si82390/1/3 in conjunction with a bootstrap circuit for driver power.

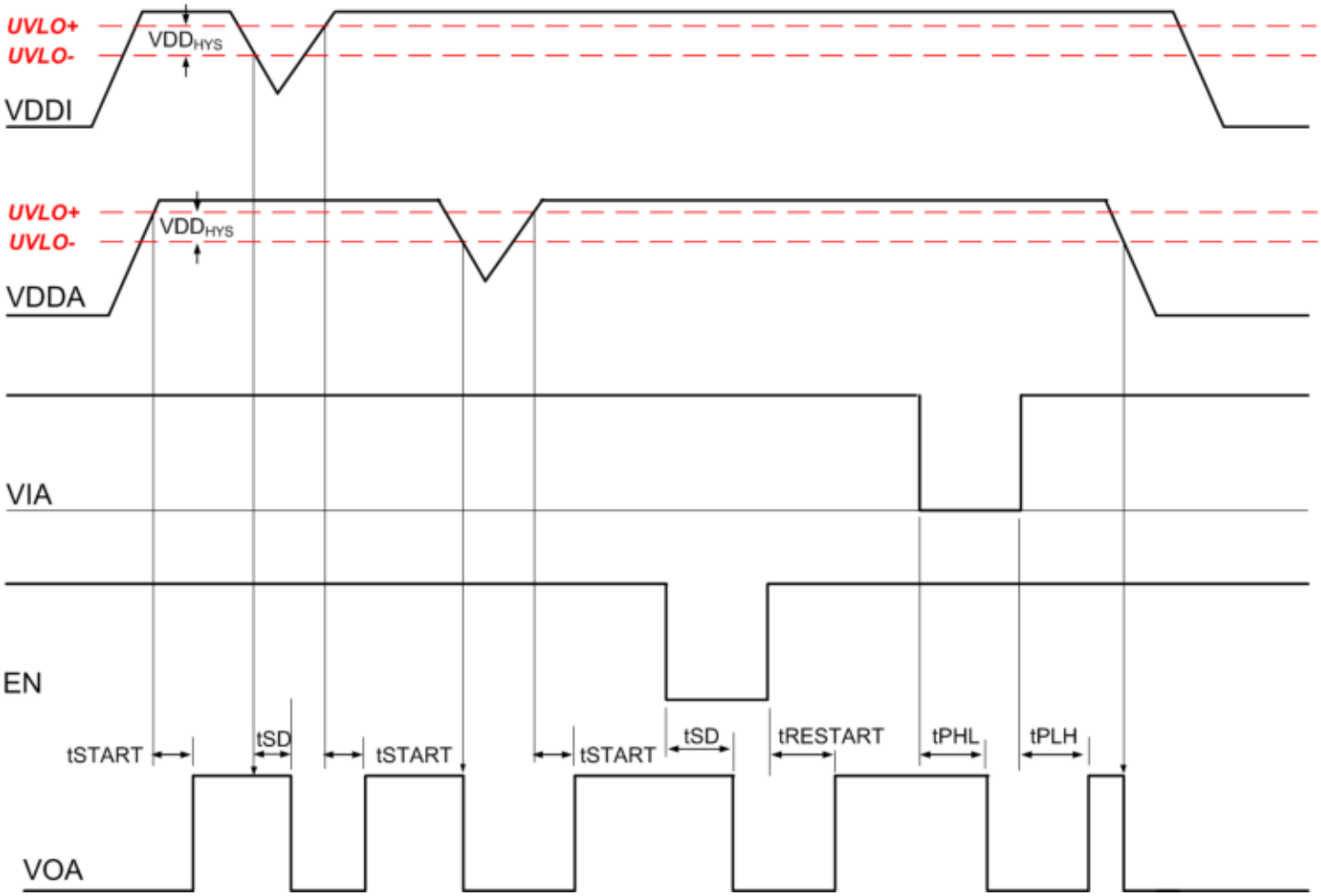


Figure 2.16. Si82391/2/3/6/8 Device Behavior during Normal Operation and Shutdown

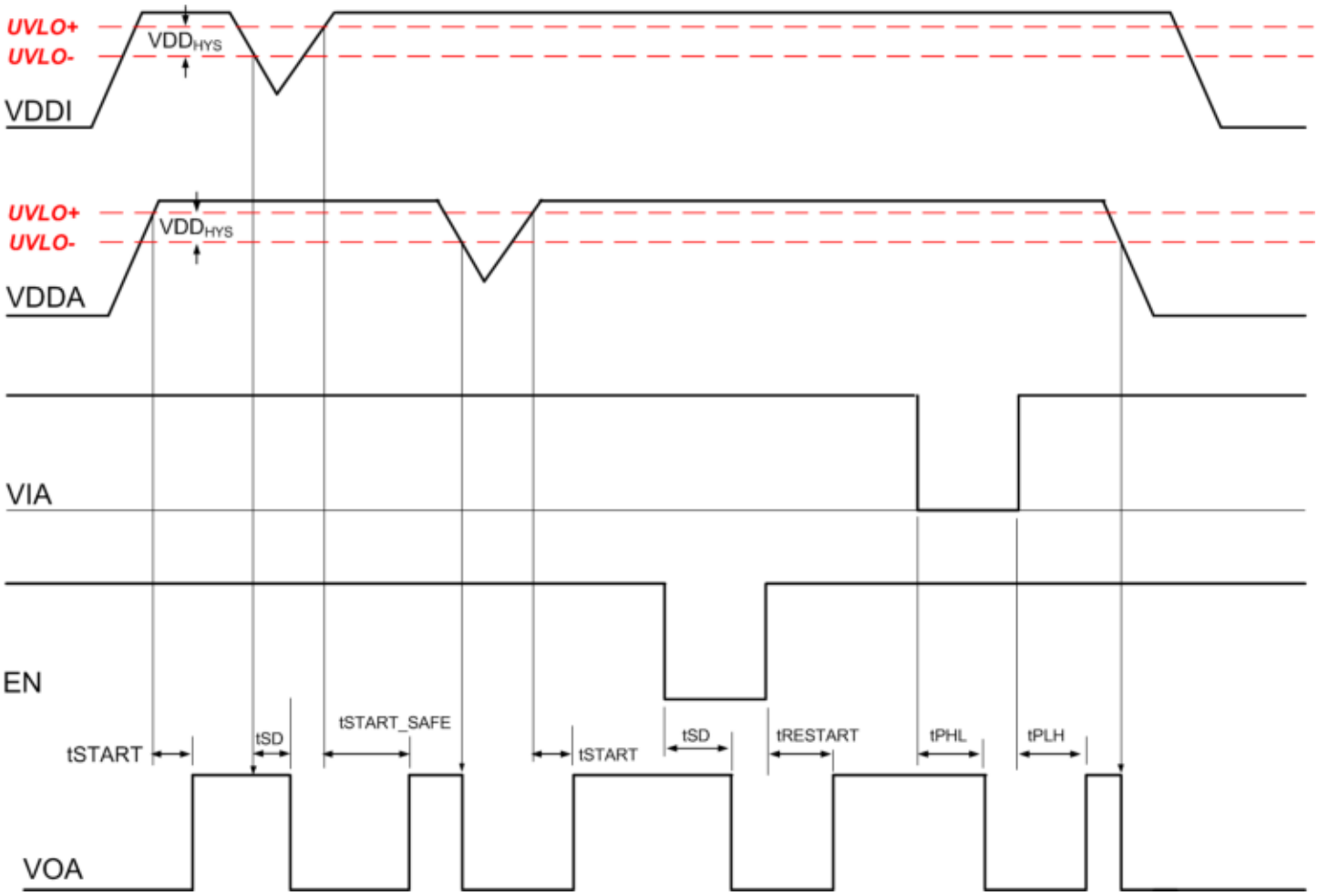


Figure 2.17. Si82390/4/5/7 Device Behavior during Normal Operation and Shutdown

2.6.3 Control Inputs

VIA, VIB, and PWM inputs are high-true, TTL level-compatible logic inputs. A logic high signal on VIA or VIB causes the corresponding output to go high. For PWM input versions (Si82394/8), VOA is high and VOB is low when the PWM input is high, and VOA is low and VOB is high when the PWM input is low.

2.6.4 Enable Input

When brought low, the EN input unconditionally drives VOA and VOB low regardless of the states of VIA and VIB. Device operation terminates within tSD after EN = VIL and resumes within tRESTART after EN = VIH. The EN input has no effect if VDDI is below its UVLO level (i.e., VOA, VOB remain low). The EN pin should be connected to GNDI through a 100 kΩ pull-down resistor.

2.6.5 Delayed Startup Time

Product options Si82390/4/5/7 have a safe startup time (tSTARTUP_SAFE) of 1ms typical from input power valid to output showing valid data. This feature allows users to proceed through a safe initialization sequence with a monotonic output behavior.

2.6.6 RDY Pin

This is a digital output pin available on all options except the Si82397. The RDY pin is “H” if all the UVLO circuits monitoring VDDI, VDDA, and VDDB are above UVLO threshold. It indicates that device is ready for operation. An “L” status indicates that one of the power supplies (VDDI, VDDA, or VDDB) is in an unpowered state.

2.7 Overlap Protection and Programmable Dead Time

Overlap protection prevents the two driver outputs from both going high at the same time. Programmable dead time control sets the amount of time between one output going low and the other output going high.

All drivers configured as high-side/low-side pairs with separate inputs (Si82392/3) have overlap protection. Drivers controlled with a single input have inherit overlap protection by virtue of one driver being active high and the other being active low with respect to the PWM input.

All high-side/low-side drivers with a single PWM input (Si82394/8) include programmable dead time, which adds a user-programmable delay between transitions of VOA and VOB. When enabled, dead time is present on all transitions. The amount of dead time delay (DT) is programmed by a single resistor (RDT) connected from the DT input to ground per the equation below. Note that the dead time pin should be connected to GND1 through a resistor between the values of 6 kΩ and 100 kΩ and a filter capacitor of 100 pF in parallel as shown in Figure 3.2 Si82394/8 Application Diagram on page 18. It is highly recommended it not be tied to VDDI. See Figure 2.18 Dead Time Waveforms for High-Side/Low-Side Drivers on page 17 below.

$$DT(typical) = 1.97 \times RDT + 2.75$$

where:

DT is the dead time (ns)

RDT is the dead time programming resistor (kΩ, 6 kΩ to 100 kΩ)

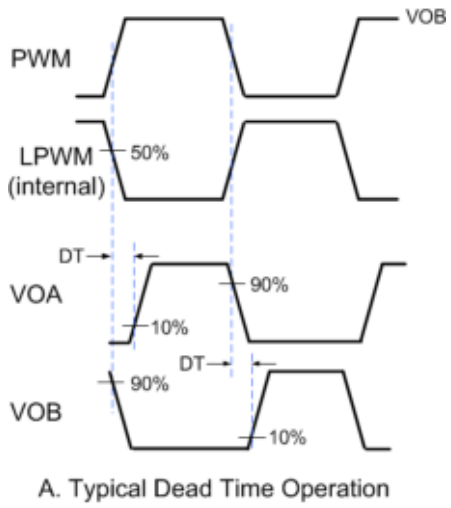


Figure 2.18. Dead Time Waveforms for High-Side/Low-Side Drivers

2.8 De-glitch Feature

A de-glitch feature is provided on some options, as defined in the Ordering Guide. The de-glitch basically provides an internal time delay during which any noise is ignored and will not pass through the IC. It is about 30 ns; so, for these product options, the prop delay will be extended by 30 ns.

3. Applications

The following examples illustrate typical circuit configurations using the Si8239x.

3.1 High-Side/Low-Side Driver

The Si82392 and Si82393 devices are high-side/low-side type drivers controlled by separate driver signals, VIA and VIB.

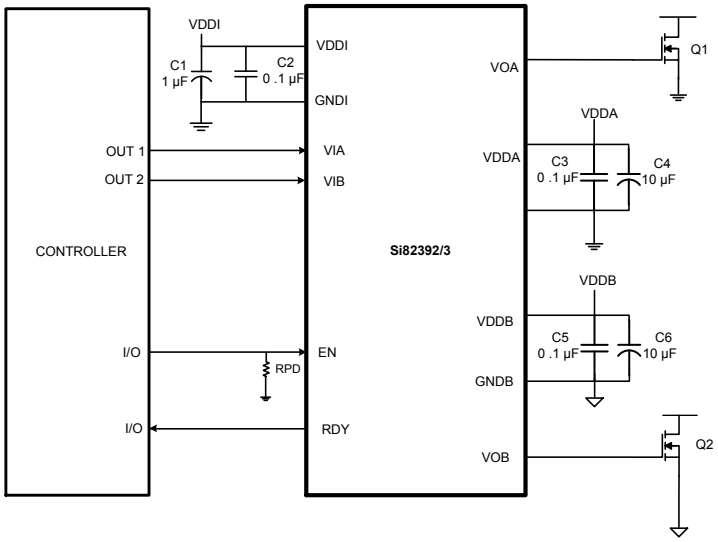


Figure 3.1. Si82392/3 Application Diagram

The following figure shows the Si82394/8 controlled by a single PWM signal.

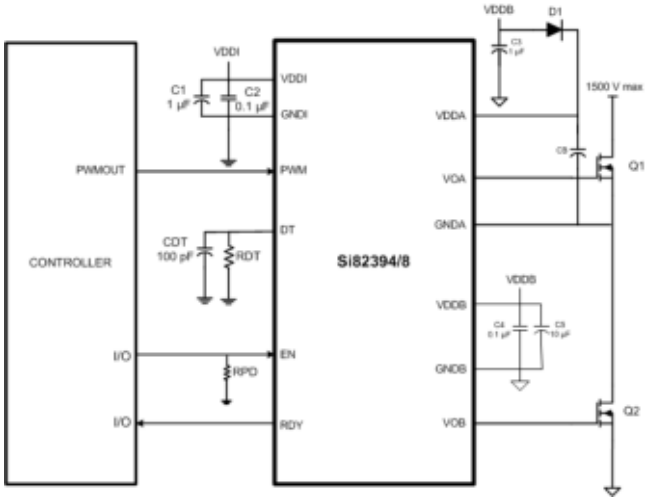


Figure 3.2. Si82394/8 Application Diagram

In the above figure, D1 and CB form a conventional bootstrap circuit that allows VOA to operate as a high-side driver for Q1, which has a maximum drain voltage of 1500 V. VOB is connected as a conventional low-side driver. Note that the input side of the Si8239x requires VDDI in the range of 2.5 to 5.5 V, while the VDDA and VDDB output side supplies must be between 6.5 and 24 V with respect to their respective grounds. The bootstrap start up time will depend on the CB cap chosen. Also note that the bypass capacitors on the Si8239x should be located as close to the chip as possible.

3.2 Dual Driver

The following figure shows the Si82390/1/5/6/7 configured as a dual driver. Note that the drain voltages of Q1 and Q2 can be referenced to a common ground or to different grounds with as much as 1500 Vdc between them.

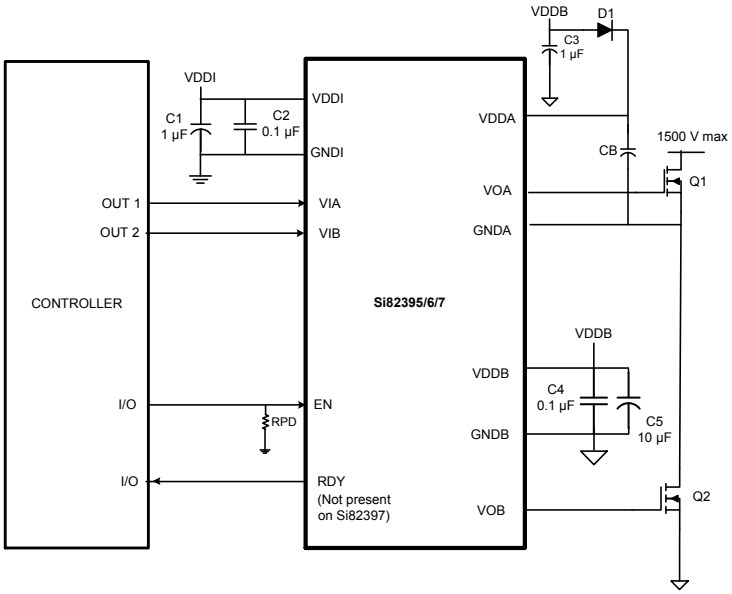


Figure 3.3. Si82395/6/7 Application Diagram

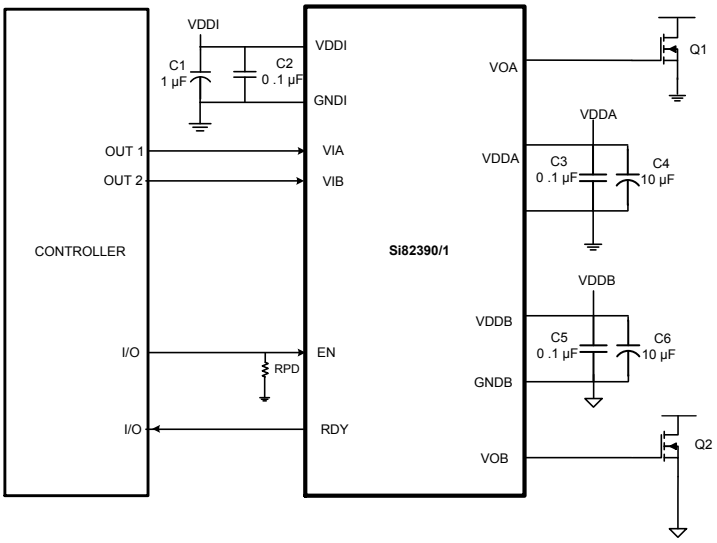


Figure 3.4. Si82390/1 with Enhanced UVLO Feature Application Diagram

Because each output driver resides on its own die, the relative voltage polarities of VOA and VOB can reverse without damaging the driver. A dual driver can operate as a dual low-side or dual high-side driver and is unaffected by static or dynamic voltage polarity changes.

3.3 Enhanced UVLO

The Si82390/1/3 come equipped with an enhanced UVLO feature as described in 2.6.2 Undervoltage Lockout. This feature is intended for systems which provide VDDA and VDDB as independent isolated power supplies. Si82390/1/3 are not recommended for use with bootstrap configuration for driver supply since the driver output will not be asserted unless both VDDA and VDDB are above the UVLO threshold.

4. Electrical Characteristics

Table 4.1. Electrical Characteristics[1,2]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC Specifications						
Input-side Power Supply Voltage	VDDI		2.5	3.3	5.5	V
Driver Supply Voltage	VDDA, VDDB	Voltage between VDDA and GNDA, and VDDB and GNDB	6.5	—	24	V
Input Supply Quiescent Current EN = 0	IDDI(Q)	Si82390/1/2/3/4/5/6/8	—	2.8	3.8	mA
		Si82397	—	1.5	2.1	mA
Output Supply Quiescent Current, per channel EN = 0	IDDA(Q), IDDB(Q)	Si82390/1/2/3/4/5/6/8	—	4.2	6.5	mA
		Si82397	—	1.5	2.5	mA
Input Supply Active Current	IDDI	Si82390/1/2/3/5/6 VIA, VIB freq = 1 MHz	—	5.0	7.2	mA
		Si82394/8: PWM freq = 1 MHz	—	5.2	7.3	
		Si82397: VIA, VIB freq = 1 MHz	—	3.7	5.6	
Output Supply Active Current, per channel	IDDA/B	Si82390/1/2/3/4/5/6/8: Input freq = 1 MHz, no load	—	7.1	16.0	mA
		Si82397: Input freq = 1 MHz, no load	—	4.4	12.4	
Digital Parameters						
Input Pin Leakage Current, VIA, VIB, PWM	IVIA, IVIB, IPWM		–10	—	+10	µA
Input Pin Leakage Current, EN	IENABLE		–10	—	+10	µA
Logic High Input Threshold	VIH	TTL Levels	2.0	—	—	V
Logic Low Input Threshold	VIL	TTL Levels	—	—	0.8	V
Input Hysteresis	VI_{HYST}		400	450	—	mV
High Level Output Voltage (RDY pin only)	VOH	IOH = –4 mA	VDDI - 0.4	4.8	—	V
Low Level Output Voltage (RDY pin only)	VOL	IOL = 4 mA	—	0.2	0.4	V
Drive Parameters						
Logic High Output Voltage	VOAH, VOBH	IOA, IOB = –1 mA	VDDA, VDDB – 0.04	—	—	V
Logic Low Output Voltage	VOAL, VOBL	IOA, IOB = 1 mA	—	—	0.04	V
Output Short-Circuit Pulsed Source Current	IOA(SCL), IOB(SCL)	See Figure 4.1 IOL Sink Current Test on page 23	—	4.0	—	A
Output Short-Circuit Pulsed Source Current	IOA(SCH), IOB(SCH)	See Figure 4.2 IOH Source Current Test on page 23	—	2.0	—	A

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Sink Resistance	$R_{ON(SINK)}$		—	1.0	—	Ω
Output Source Resistance	$R_{ON(SOURCE)}$		—	2.7	—	Ω
VDDI Undervoltage Threshold	$VDDI_{UV+}$	VDDI rising	2.15	2.3	2.5	V
VDDI Undervoltage Threshold	$VDDI_{UV-}$	VDDI falling	2.1	2.2	2.4	V
VDDI Lockout Hysteresis	$VDDI_{HYS}$		80	100	—	mV
VDDA, VDDB Undervoltage Threshold	$VDDA_{UV+}$, $VDDB_{UV+}$	VDDA, VDDB rising				V
6 V			5.0	6.0	7.0	
8 V			7.2	8.6	10.0	
12 V			9.2	11.1	12.8	
VDDA, VDDB Undervoltage Threshold	$VDDA_{UV-}$, $VDDB_{UV-}$	VDDA, VDDB falling				V
6 V			4.7	5.8	6.7	
8 V			6.6	8.0	9.3	
12 V			8.7	10.1	11.6	
VDDA, VDDB Lockout Hysteresis	$VDDA_{HYS}$, $VDDB_{HYS}$	UVLO = 6 V	200	280	—	mV
		UVLO = 8 V	450	600	—	
		UVLO = 12 V	600	1000	—	
AC Specifications						
UVLO Fault Shutdown Time Enhanced Mode Si82390/1/3 only		$VDDA_{UV-}$ to VOB low $VDDB_{UV-}$ to VOA low	—	120	—	ns
UVLO Fault Shutdown Time		$VDDA_{UV-}$ to VOA low $VDDB_{UV-}$ to VOB low	—	10	—	ns
UVLO fault to RDY	t_FLT		—	92	—	ns
Minimum Pulse Width			—	30	—	ns
Propagation Delay	t_{pHL}, t_{pLH}	Si82390/1/2/3/5/6/7 (with no de-glitch)	20	30	40	ns
VDDA/B = 12 V	t_{pHL}	Si82394/8 (with no de-glitch)	20	30	40	ns
C_L = 0 pF	t_{pLH}	Si82394/8 (with no de-glitch; measured with 6 kΩ RDT resistor; includes minimum dead time)	35	45	55	ns
	t_{pHL}	Si82394xx4/8xx4 (have de-glitch)	60	77	95	ns
	t_{pLH}	Si82394xx4/8xx4 (have de-glitch and measured with 6 kΩ RDT resistor; includes minimum dead time and de-glitch delay)	99	116	135	ns

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Pulse Width Distortion $\|t_{PLH} – t_{PHL}\|$	PWD	VDDA/B = 12 V C_L = 0 pF	—	2.7	5.60	ns
Programmed Dead Time for product options with 40–600 ns dead time setting range	DT	RDT = 6 kΩ RDT = 15 kΩ RDT = 100 kΩ	27 70 450	38 90 590	57 130 750	ns
Output Rise and Fall Time	t_R,t_F	C_L = 200 pF	—	—	12	ns
Shutdown Time from Enable False	t_{SD}	All options with no de-glitch	—	—	60	ns
		All options with de-glitch	—	—	113	
Restart Time from Enable True	$t_{RESTART}$	All options with no de-glitch	—	—	60	ns
		All options with de-glitch	—	—	95	
Device Start-up Time Input Si82390/4/5/7 Si82391/2/3/6/8	 t_{START_SAFE} t_{START}	Time from VDDI_ = VDDI_UV+ to VOA, VOB = VIA, VIB	—	 1 40	—	 ms µs
Device Start-up Time Output	t_{START_OUT}	Time from VDDA/B = VDDA/B_UV+ to VOA, VOB = VIA, VIB	—	60	—	µs
Common Mode Transient Immunity	CMTI	VIA, VIB, PWM = VDDI or 0 V V_{CM} = 1500 V	35	100	—	kV/µs

Note:

1. 2.5 V < VDDI < 5.5 V; 6.5 V < VDDA, VDDB < 24 V; T_A = –40 to +125 °C.
2. Typical specs at 25 °C, VDDA = VDDB = 12 V for 5 V and 8 V UVLO devices, otherwise 15 V.

The following figures depict sink current, source current, and common-mode transient immunity test circuits, respectively.

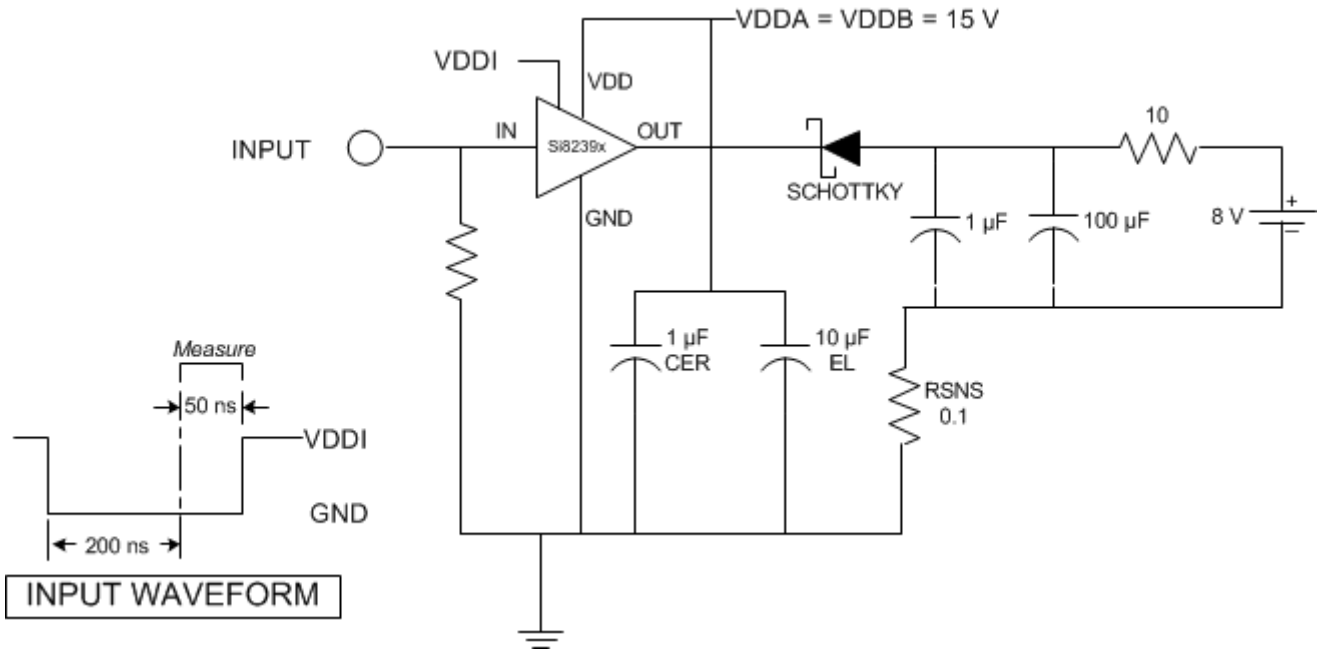


Figure 4.1. IOL Sink Current Test

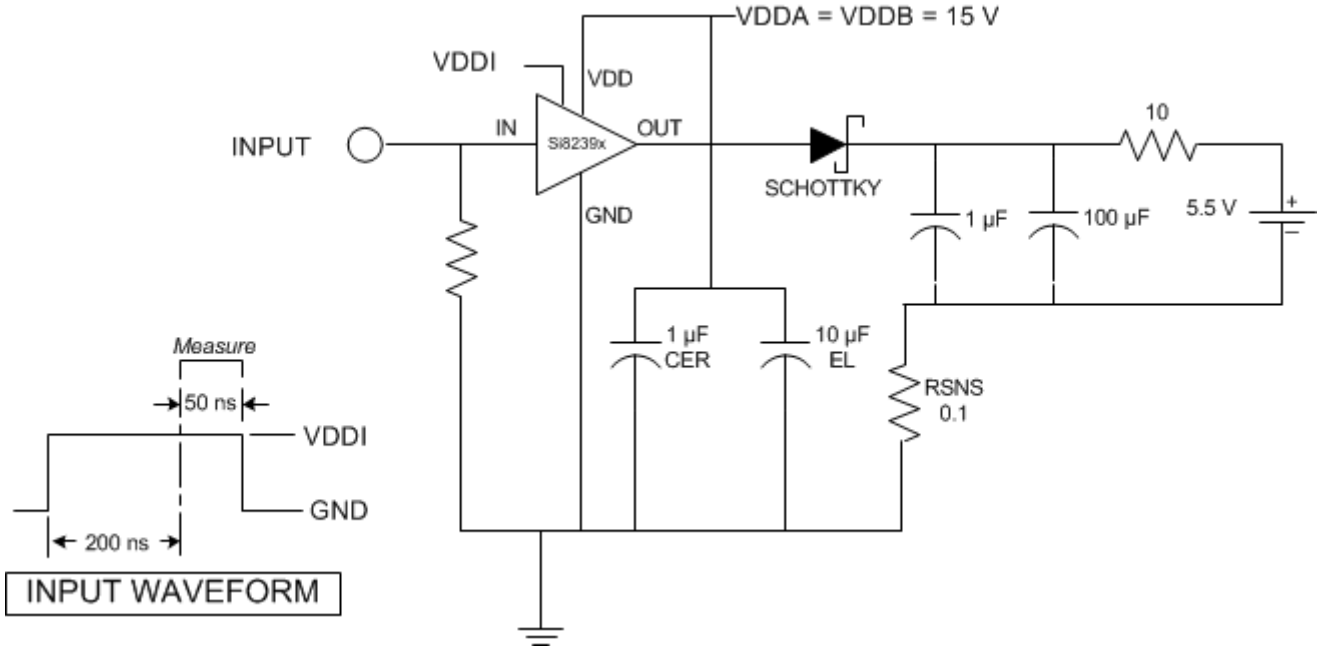


Figure 4.2. IOH Source Current Test

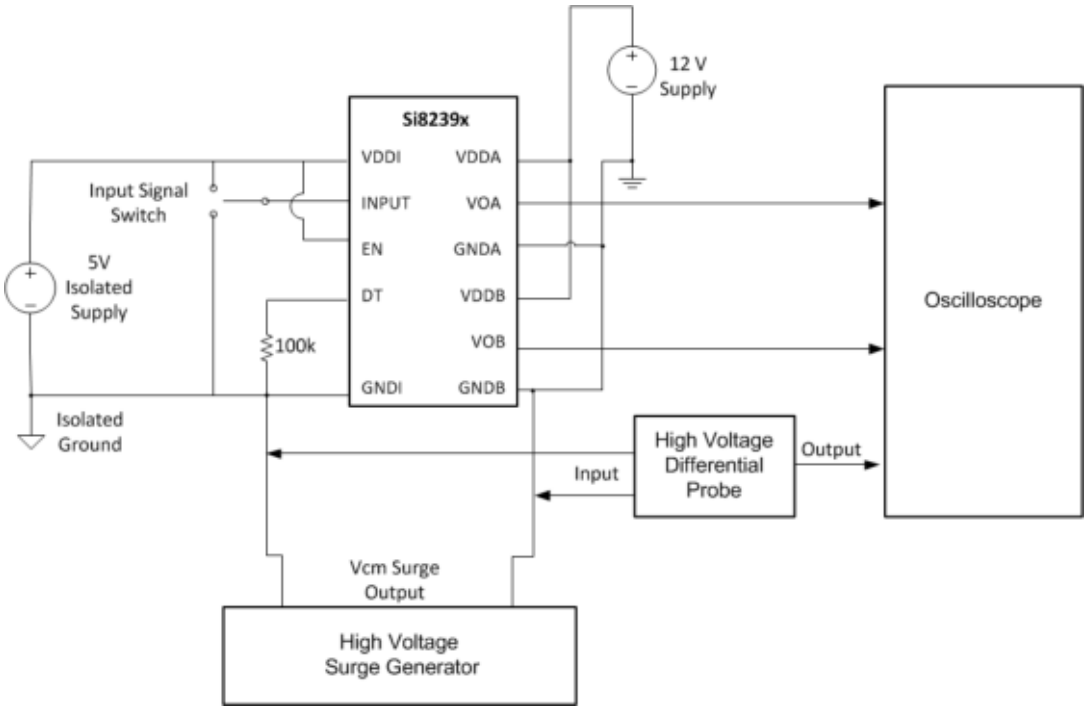


Figure 4.3. CMTI Test Circuit

Table 4.2. Regulatory Information[1,2,3]

CSA
The Si8239x is certified under CSA. For more details, see Master Contract File 232873.
60950-1, 62368-1: Up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
VDE
The Si8239x is certified according to VDE 0884-10. For more details, see File 5006301-4880-0001.
VDE 0884-10: Up to 891 V_{peak} for basic insulation working voltage.
60950-1, 62368-1: Up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
UL
The Si8239x is certified under UL1577 component recognition program. For more details, see File E257455.
Rated up to 5000 V_{RMS} isolation voltage for basic protection.
CQC
The Si8239x is certified under GB4943.1-2011.
Rated up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
Note: 1. Regulatory Certifications apply to 2.5 kV_{RMS} rated devices which are production tested to 3.0 kV_{RMS} for 1 sec. 2. Regulatory Certifications apply to 5.0 kV_{RMS} rated devices which are production tested to 6.0 kV_{RMS} for 1 sec. 3. For more information, see Ordering Guide.

Table 4.3. Insulation and Safety-Related Specifications

Parameter	Symbol	Test Condition	Value		Unit
			WB SOIC-14/16	NB SOIC-16	
Nominal External Air Gap (Clearance)[1]	CLR		8.0	4.01	mm
Nominal External Tracking (Creepage)	CPG		8.0	4.01	mm
Minimum Internal Gap (Internal Clearance)	DTI		0.014	0.014	mm
Tracking Resistance	PTI or CTI	IEC60112	600	600	V
Erosion Depth	ED		0.019	0.019	mm
Resistance (Input-Output)[2]	R_{IO}		10^{12}	10^{12}	Ω
Capacitance (Input-Output)[2]	C_{IO}	f = 1 MHz	1.4	1.4	pF
Input Capacitance[3]	C_I		4.0	4.0	pF

Note:

1. The values in this table correspond to the nominal creepage and clearance values as detailed in 9. Package Outline: 16-Pin Wide Body SOIC, 7. Package Outline: 14-Pin Wide Body SOIC, and 11. Package Outline: 16-Pin Narrow Body SOIC. VDE certifies the clearance and creepage limits as 4.7 mm minimum for the NB SOIC-16 and 8.5 mm minimum for the WB SOIC-16 and WB SOIC-14 packages. UL does not impose a clearance and creepage minimum for component level certifications. CSA certifies the clearance and creepage limits as 3.9 mm minimum for the NB SOIC16 and 7.6 mm minimum for the WB SOIC-16 and WB SOIC-14 packages.
2. To determine resistance and capacitance, the Si8239x is converted into a 2-terminal device. All pins on one side are shorted together to form the first terminal, and all pins on the other side are shorted together to form the second terminal. The parameters are then measured between these two terminals.
3. Measured from input pin to ground.

Table 4.4. IEC 60664-1 Ratings

Parameter	Test Condition	Specification	
		WB SOIC-14/16	NB SOIC-16
Basic Isolation Group	Material Group	I	I
Installation Classification	Rated Mains Voltages < 150 V_{RMS}	I-IV	I-IV
	Rated Mains Voltages < 300 V_{RMS}	I-IV	I-III
	Rated Mains Voltages < 400 V_{RMS}	I-III	I-II
	Rated Mains Voltages < 600 V_{RMS}	I-III	I-II

Table 4.5. VDE0884-10 Insulation Characteristics

Parameter	Symbol	Test Condition	Characteristic		Unit
			WB SOIC-14/16	NB SOIC-16	
Maximum Working Insulation Voltage	V_{IORM}		891	560	V peak
Input to Output Test Voltage	V_{PR}	Method b1 (V_{IORM} x 1.875 = V_{PR}, 100% Production Test, t_m = 1 sec, Partial Discharge < 5 pC)	1671	1050	V peak
Transient Overvoltage	V_{IOTM}	t = 60 sec	6000	4000	V peak
Surge Voltage	V_{IOSM}	Tested per IEC 60065 with surge voltage of 1.2 µs/50µs Si8239xxB/D tested with 4000 V	3077	3077	V peak
Pollution Degree (DIN VDE 0110, See Table 4.1 Electrical Characteristics[1,2] on page 20)			2	2	
Insulation Resistance at T_S, V_{IO} = 500 V	R_S		$>10^9$	$>10^9$	Ω

Note:
1. Maintenance of the safety data is ensured by protective circuits. The Si8239x provides a climate classification of 40/125/21.

Table 4.6. IEC Safety Limiting Values[1]

Parameter	Symbol	Test Condition	WB SOIC-14/16	NB SOIC-16	Unit
Safety Temperature	T_S		150	150	°C
Safety Input Current	I_S	θ_{JA} = 59 °C/W (WB SOIC-14/16), 63 °C/W (NB SOIC-16) V_{DDI} = 5.5 V, V_{DDA} = V_{DDB} = 24 V, T_J = 150 °C, T_A = 25 °C	88	83	mA
Device Power Dissipation[2]	P_D		2.1	2.0	W

Parameter	Symbol	Test Condition	WB SOIC-14/16	NB SOIC-16	Unit

Note:

1. Maximum value allowed in the event of a failure. Refer to the thermal derating curves in Figure 4.4 WB SOIC-14/16 Thermal Derating Curve, Dependence of Safety Limiting Values on page 28 and Figure 4.5 NB SOIC-16 Thermal Derating Curve, Dependence of Safety Limiting Values on page 28.
2. The Si8239x is tested with VDDI = 5.5 V, VDDA = VDDB = 24 V, TJ = 150 ºC, CL = 100 pF, input 2 MHz 50% duty cycle square wave.

Table 4.7. Thermal Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
IC Junction-to-Air Thermal Resistance (WB SOIC-14/16)	θ_{JA}	---	59	---	°C/W
IC Junction-to-Air Thermal Resistance (NB SOIC-16)	θ_{JA}	---	63	---	°C/W
Junction Temperature	T_J	---	---	150	°C

Table 4.8. Absolute Maximum Ratings[1]

Parameter	Symbol	Min	Max	Unit
Ambient Temperature under Bias	T_A	–40	+125	°C
Storage Temperature	T_{STG}	–65	+150	°C
Junction Temperature	T_J	—	+150	°C
Input-side Supply Voltage	VDDI	–0.6	6.0	V
Output Current Drive (RDY pin)	I_o	—	10	mA
Driver-side Supply Voltage	VDDA, VDDB	–0.6	30	V
Voltage on any Pin with respect to Ground	V_{IO}	–0.5	VDD + 0.5	V
Peak Output Current (t_{PW} = 10 µs, duty cycle = 0.2%)	I_{OPK}	—	4.0	A
Lead Solder Temperature (10 s)		—	260	°C
ESD per AEC-Q100	HBM	—	4	kV
	CDM	—	2	kV
Maximum Isolation (Input to Output) (1 s) WB SOIC		—	6500	V_{RMS}
Maximum Isolation (Output to Output) (1 s) WB SOIC-16		—	2500	V_{RMS}
Maximum Isolation (Output to Output) (1 s) WB SOIC-14		—	3250	V_{RMS}

Parameter	Symbol	Min	Max	Unit
Maximum Isolation (Input to Output) (1 s) NB SOIC		—	4500	V_{RMS}
Maximum Isolation (Output to Output) (1 s) NB SOIC		—	2500	V_{RMS}

Note:

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

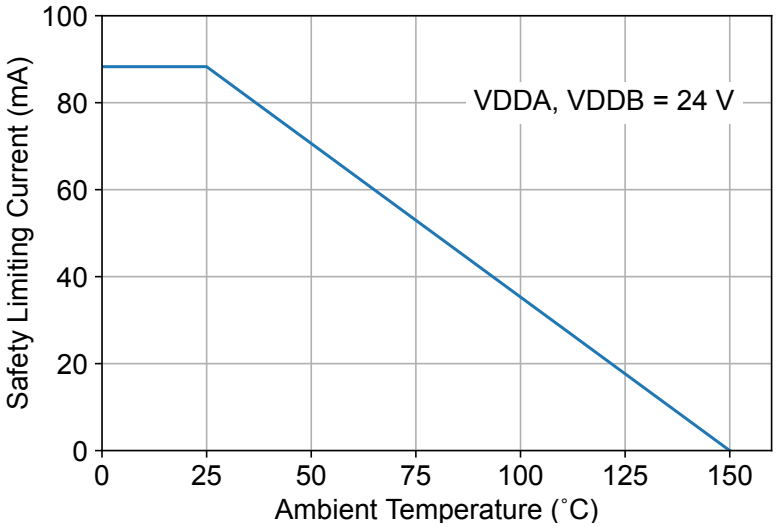


Figure 4.4. WB SOIC-14/16 Thermal Derating Curve, Dependence of Safety Limiting Values

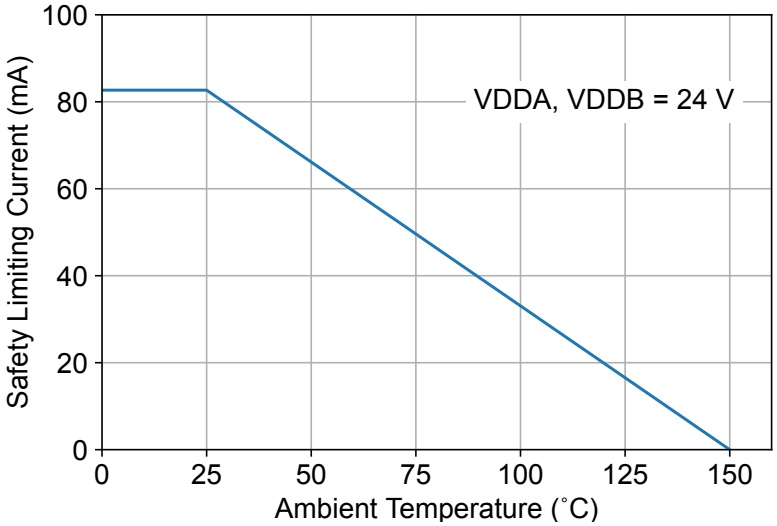


Figure 4.5. NB SOIC-16 Thermal Derating Curve, Dependence of Safety Limiting Values

5. Top-Level Block Diagrams

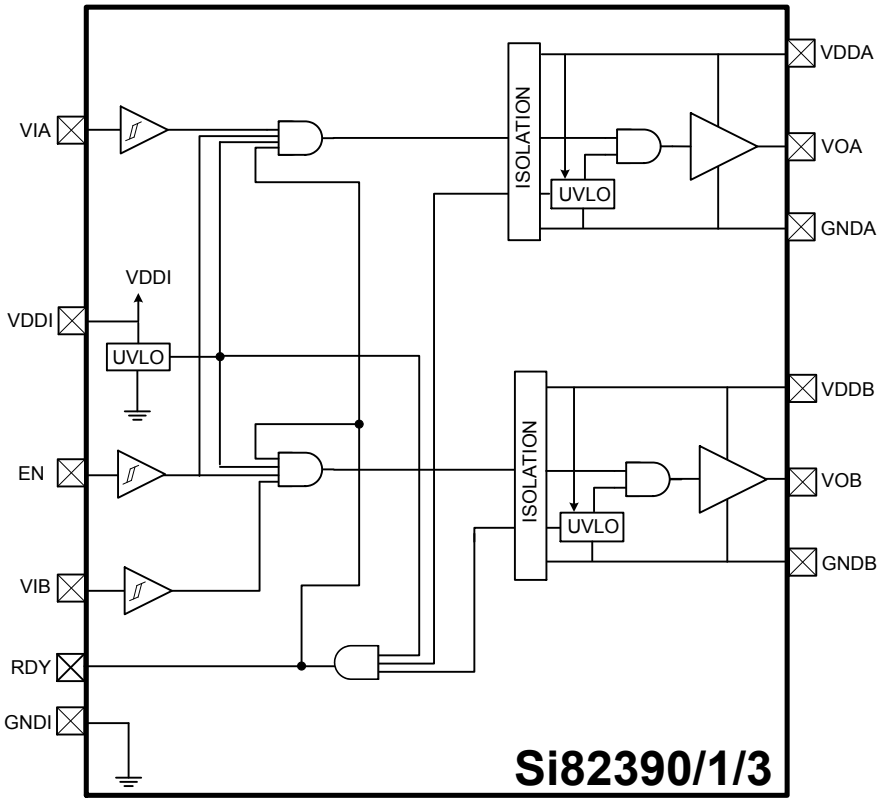


Figure 5.1. Si82390/1/3 Dual Isolated Drivers with Enhanced UVLO Safety

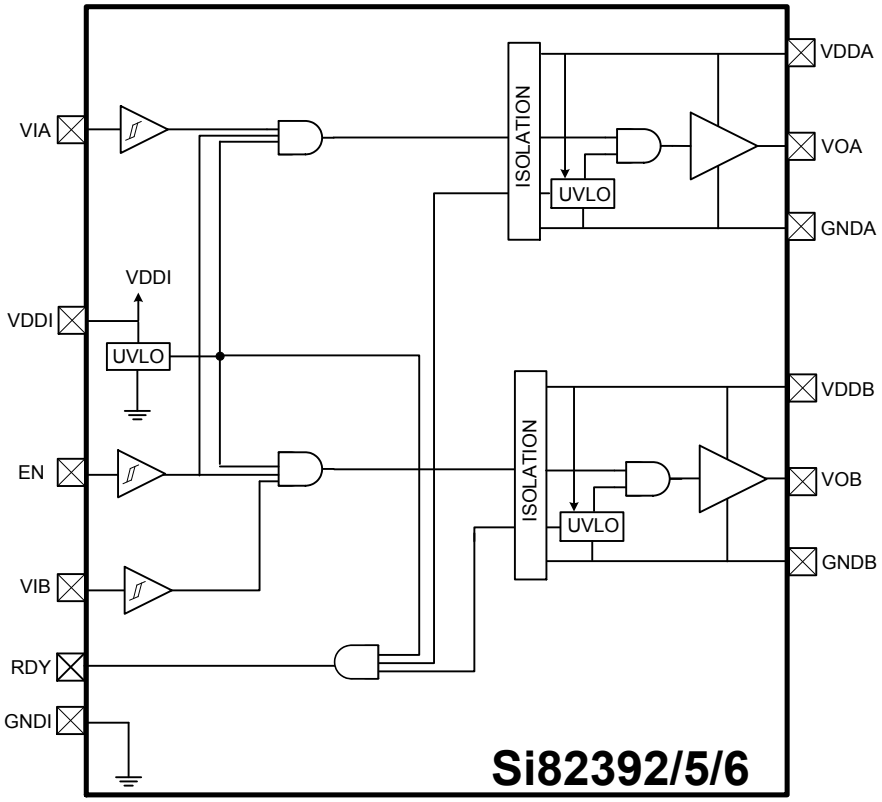


Figure 5.2. Si82392/5/6 Dual Isolated Drivers with RDY Pin

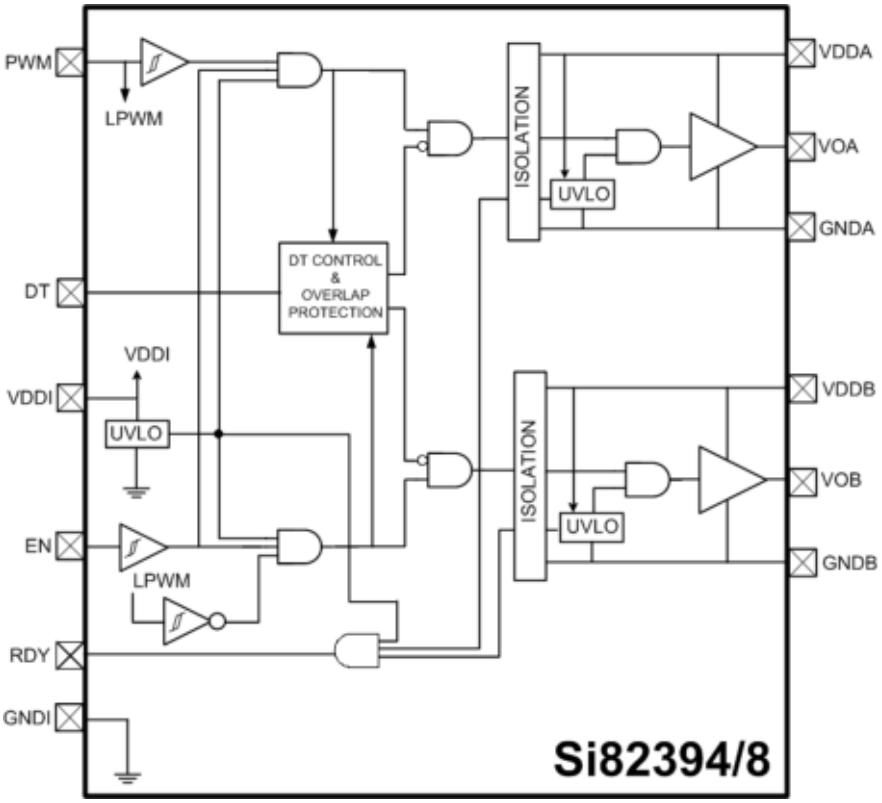


Figure 5.3. Si82394/98 Single-Input High-Side/Low-Side Isolated Drivers

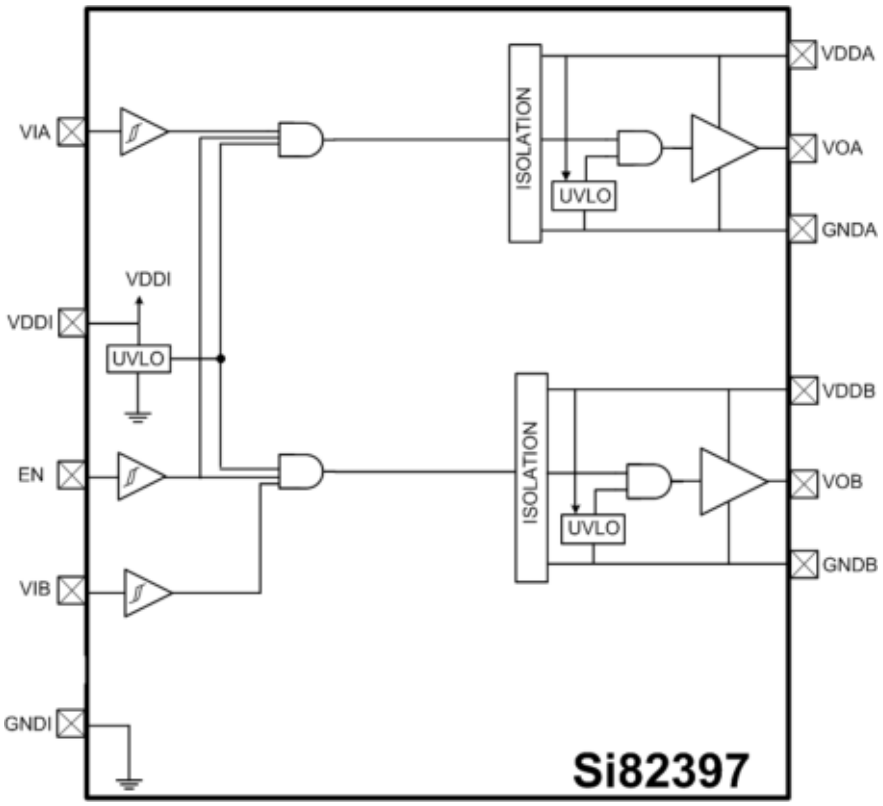


Figure 5.4. Si82397 Dual Isolated Drivers

6. Pin Descriptions

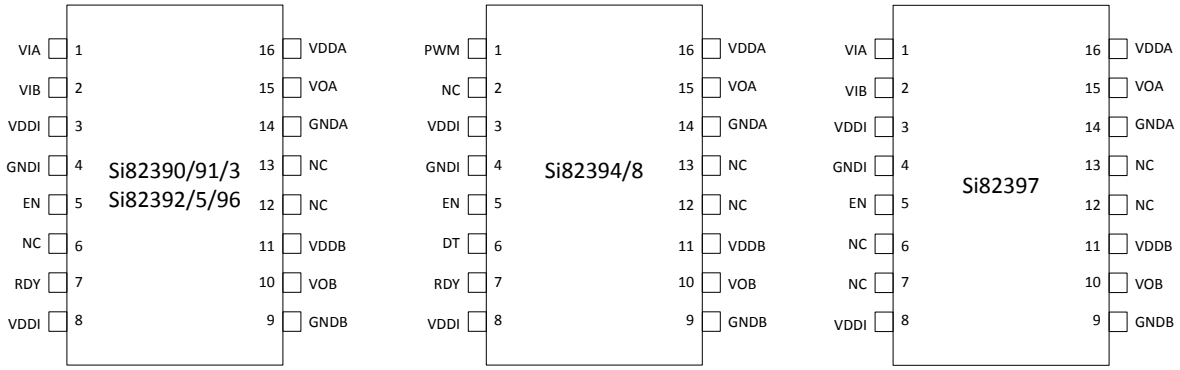


Figure 6.1. Si8239x SOIC-16[1]

Note:

1. WB SOIC-14 with IS3 package designation has pins 12 & 13 missing.

Table 6.1. Pin Descriptions

Pin Name	Description
GNDI	Input-side ground terminal.
PWM	PWM input
VIA	Non-inverting logic input terminal for Driver A.
VIB	Non-inverting logic input terminal for Driver B.
VDDI	Input-side power supply terminal; connect to a source of 2.5 to 5.5 V.
EN	Device ENABLE. When low or NC, this input unconditionally drives outputs VOA, VOB LOW. When high, device is enabled to perform in normal operating mode. It is strongly recommended that this input be connected to external logic level to avoid erroneous operation due to capacitive noise coupling.
DT	Dead time programming input. The value of the resistor connected from DT to ground sets the dead time between output transitions of VOA and VOB.
NC	No connection.
GNDB	Ground terminal for Driver B.
VOB	Driver B output (low-side driver).
VDDB	Driver B power supply voltage terminal; connect to a source of 6.5 to 24 V.
GNDA	Ground terminal for Driver A.
VOA	Driver A output (high-side driver).
VDDA	Driver A power supply voltage terminal; connect to a source of 6.5 to 24 V.
RDY	Power ready on secondary side for Driver A and Driver B (both UVLO thresholds for VDDA and VDDB need to be crossed). High state indicates UVLO thresholds crossed, low state indicates UVLO low condition. No reset is necessary.

7. Package Outline: 14-Pin Wide Body SOIC

Figure 7.1 Si8239x 14-pin WB SOIC Outline on page 33 illustrates the package details for the Si8239x in a 14-Pin Wide Body SOIC. Table 7.1 Package Diagram Dimensions on page 33 lists the values for the dimensions shown in the illustration.

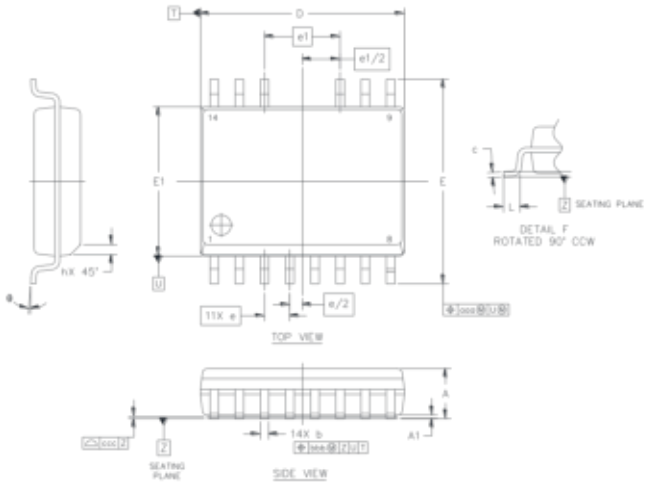


Figure 7.1. Si8239x 14-pin WB SOIC Outline

Table 7.1. Package Diagram Dimensions

Dimension	MIN	MAX
A	—	2.65
A1	0.10	0.30
A2	2.05	—
b	0.35	0.49
c	0.23	0.32
D	10.15	10.45
E	10.05	10.55
E1	7.40	7.60
e	1.27 BSC	
e1	3.81 BSC	
L	0.40	1.27
h	0.25	0.75
Θ	0°	8°
aaa	—	0.25
bbb	—	0.25
ccc	—	0.10

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended reflow profile per JEDEC J-STD-020 specification for small body, lead-free components.

8. Land Pattern: 14-Pin Wide Body SOIC

Figure 8.1 14-Pin WB SOIC Land Pattern on page 34 illustrates the recommended land pattern details for the Si8239x in a 14-pin Wide Body SOIC. Table 8.1 14-Pin WB SOIC Land Pattern Dimensions on page 34 lists the values for the dimensions shown in the illustration.

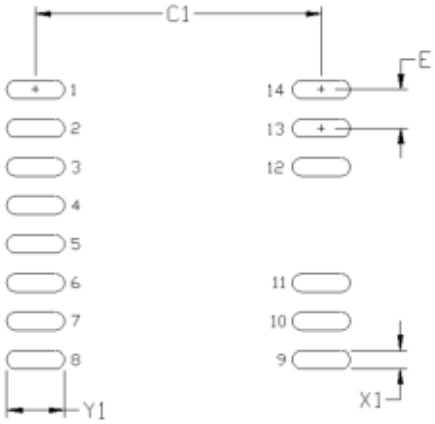


Figure 8.1. 14-Pin WB SOIC Land Pattern

Table 8.1. 14-Pin WB SOIC Land Pattern Dimensions

Dimension	Feature	(mm)
C1	Pad Column Spacing	9.70
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.60

Notes:

1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P1032X265-16AN for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

9. Package Outline: 16-Pin Wide Body SOIC

The following figure illustrates the package details for the Si8239x in a 16-Pin Wide Body SOIC. The table lists the values for the dimensions shown in the illustration.

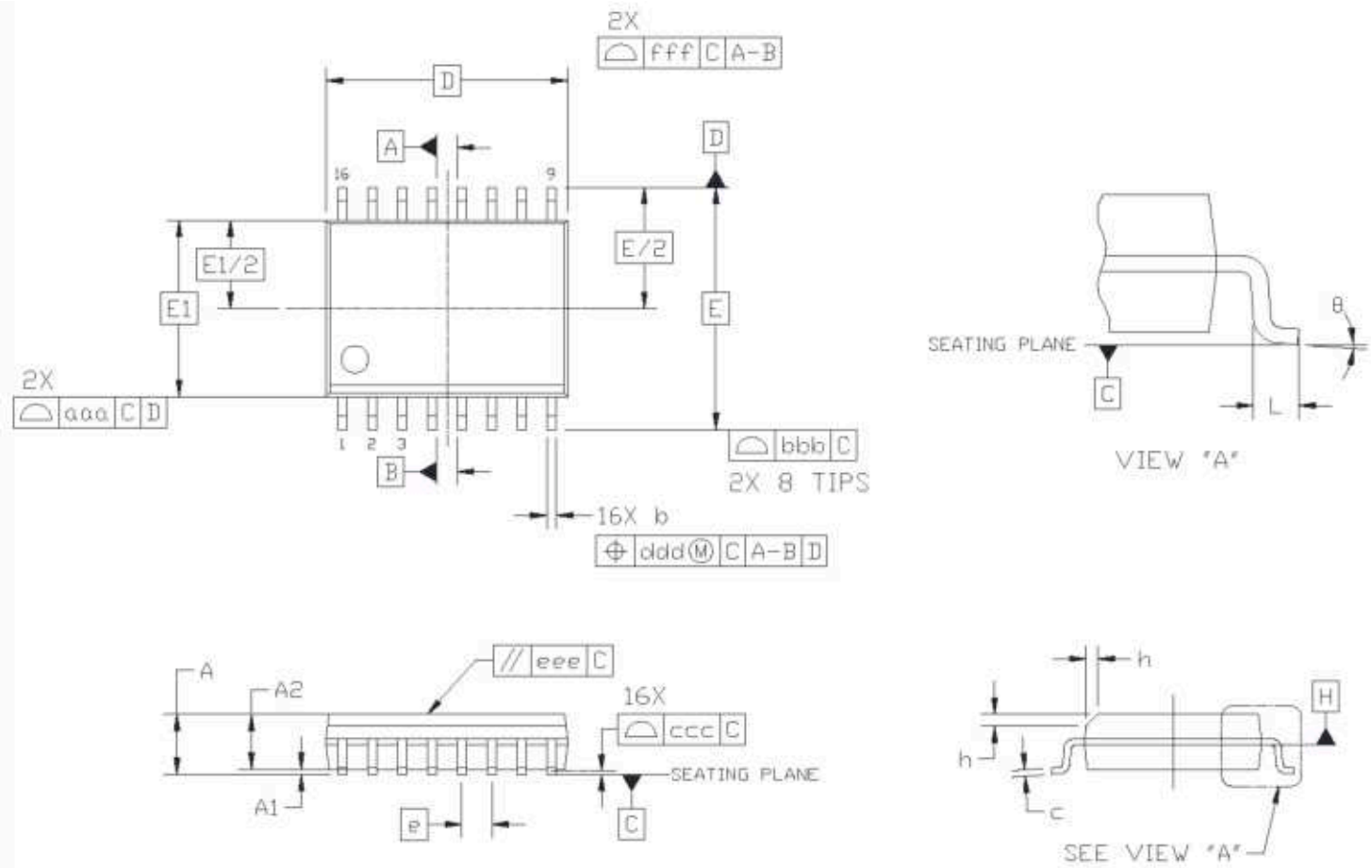


Figure 9.1. 16-Pin Wide Body SOIC

Table 9.1. Package Diagram Dimensions

Symbol	Millimeters	
	Min	Max
A	—	2.65
A1	0.10	0.30
A2	2.05	—
b	0.31	0.51
c	0.20	0.33
D	10.30 BSC	
E	10.30 BSC	
E1	7.50 BSC	
e	1.27 BSC	
L	0.40	1.27
h	0.25	0.75

Symbol	Millimeters	
	Min	Max
θ	0°	8°
aaa	—	0.10
bbb	—	0.33
ccc	—	0.10
ddd	—	0.25
eee	—	0.10
fff	—	0.20

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Outline MS-013, Variation AA.
4. Recommended reflow profile per JEDEC J-STD-020 specification for small body, lead-free components.

10. Land Pattern: 16-Pin Wide Body SOIC

The following figure illustrates the recommended land pattern details for the Si8239x in a 16-Pin Wide-Body SOIC. The table lists the values for the dimensions shown in the illustration.

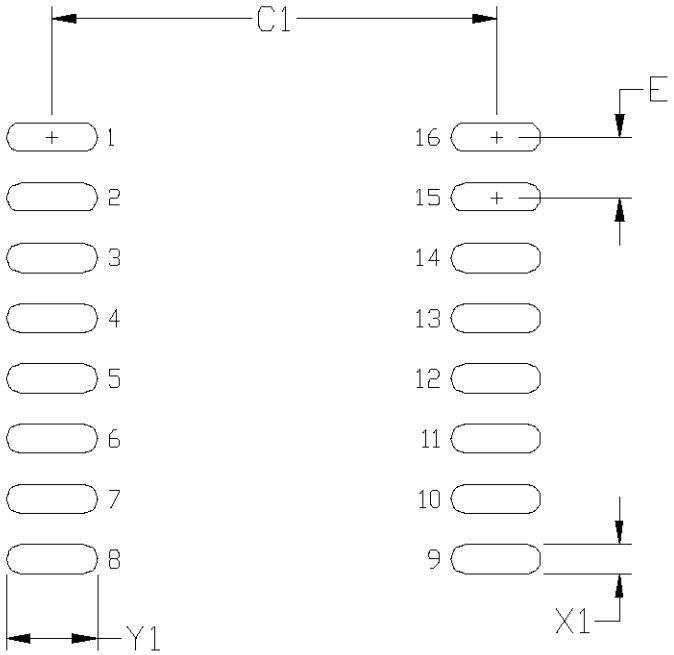


Figure 10.1. 16-Pin Wide Body SOIC PCB Land Pattern

Table 10.1. 16-Pin Wide Body SOIC Land Pattern Dimensions

Dimension	Feature	(mm)
C1	Pad Column Spacing	9.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.90

Note:

1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P1032X265-16AN for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

11. Package Outline: 16-Pin Narrow Body SOIC

The following figure illustrates the package details for the Si8239x in a 16-Pin Narrow-Body SOIC. The table lists the values for the dimensions shown in the illustration.

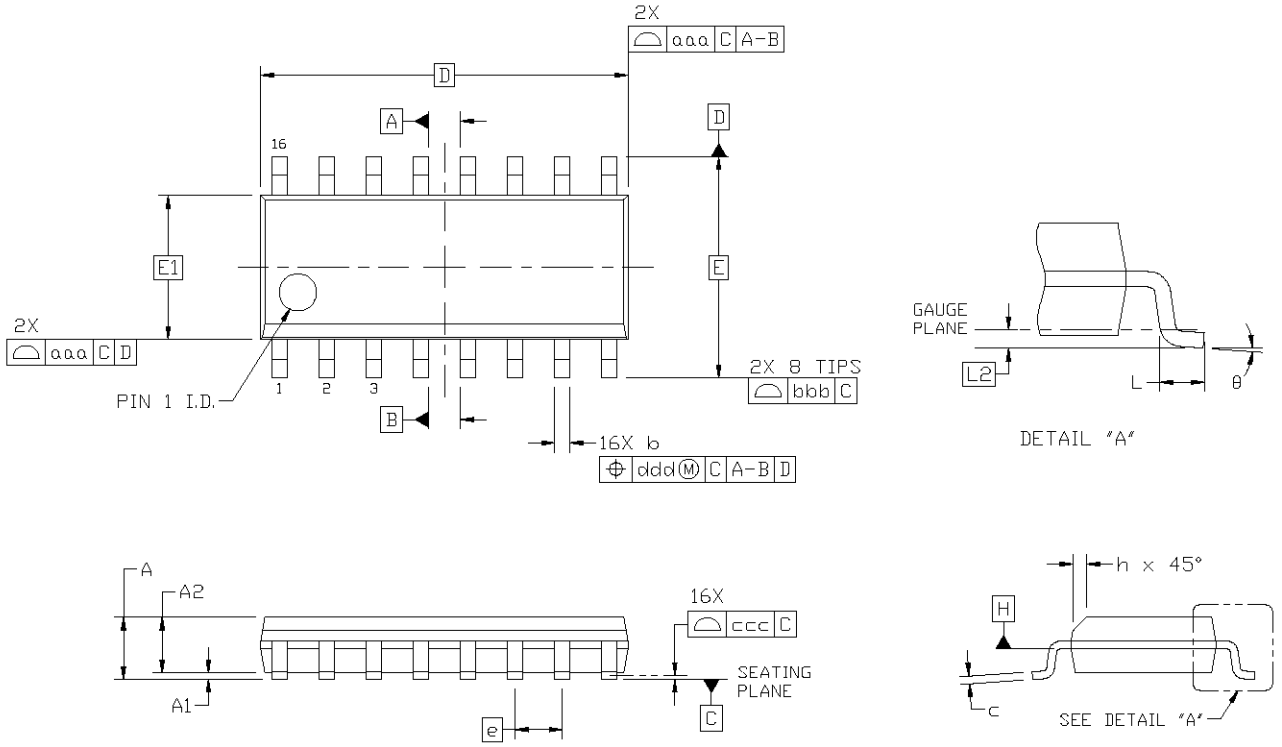


Figure 11.1. 16-Pin Narrow Body SOIC

Table 11.1. Package Diagram Dimensions

Dimension	Min	Max		Dimension	Min	Max
A	—	1.75		L	0.40	1.27
A1	0.10	0.25		L2	0.25 BSC	
A2	1.25	—		h	0.25	0.50
b	0.31	0.51		θ	0°	8°
c	0.17	0.25		aaa	0.10	
D	9.90 BSC			bbb	0.20	
E	6.00 BSC			ccc	0.10	
E1	3.90 BSC			ddd	0.25	
e	1.27 BSC					

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MS-012, Variation AC.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

12. Land Pattern: 16-Pin Narrow Body SOIC

The following figure illustrates the recommended land pattern details for the Si8239x in a 16-Pin Narrow-Body SOIC. The table lists the values for the dimensions shown in the illustration.

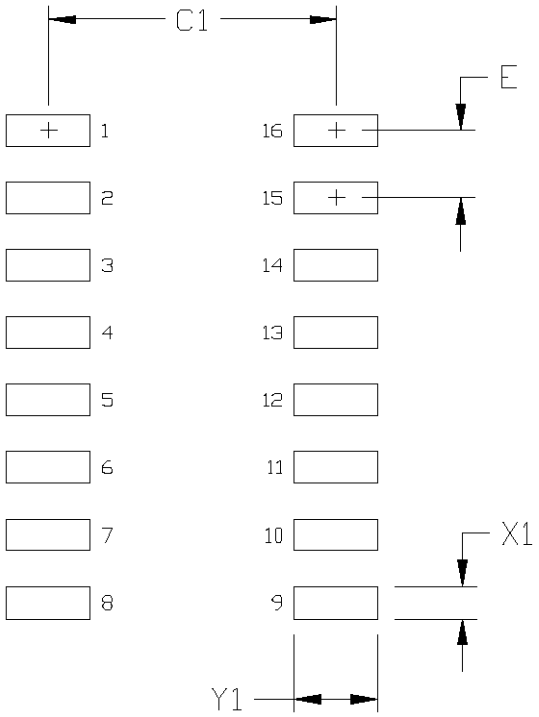


Figure 12.1. 16-Pin Narrow Body SOIC PCB Land Pattern

Table 12.1. 16-Pin Narrow Body SOIC Land Pattern Dimensions

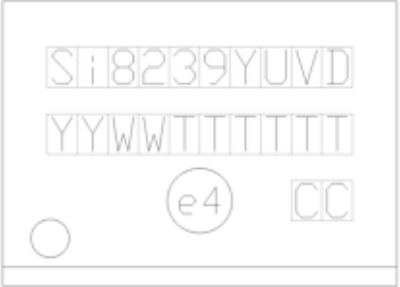
Dimension	Feature	(mm)
C1	Pad Column Spacing	5.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.55

Note:

1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X165-16N for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

13. Top Markings

13.1 Si8239x Top Marking (14-/16-Pin Wide Body SOIC)



13.2 Top Marking Explanation (16-Pin Wide Body SOIC)

Line 1 Marking:	Base Part Number Ordering Options See Ordering Guide for more information.	Si8239 = ISOdriver product series Y = Output configuration: 0, 1, 3, 4, 5, 6, 7, 8 0, 1, 5, 6, 7 = Dual drivers 3 = Dual input (VIA, VIB) High Side/Low Side drivers 4, 8 = PWM input High side/Low side drivers U = UVLO level: A, B, C A = 6 V; B = 8 V; C = 12 V V = Isolation rating: B, D B = 2.5 kV; D = 5.0 kV D = Dead time setting range: none, 4 none = 10–200 ns; 4 = 40–600 ns
Line 2 Marking:	YY = Year WW = Workweek	Assigned by the Assembly House. Corresponds to the year and workweek of the mold date.
	TTTTTT = Mfg Code	Manufacturing Code from Assembly Purchase Order form.
Line 3 Marking:	Circle = 1.5 mm Diameter (Center Justified)	“e4” Pb-Free Symbol
	Country of Origin ISO Code Abbreviation	TW = Taiwan

13.3 Si8239x Top Marking (16-Pin Narrow Body SOIC)

13.4 Top Marking Explanation (16-Pin Narrow Body SOIC)

Line 1 Marking:	Base Part Number Ordering Options See Ordering Guide for more information.	Si8239 = ISOdriver product series Y = Output configuration: 0, 1, 2, 4, 5, 6, 7, 8 0, 1, 5, 6, 7 = Dual drivers 2 = Dual input (VIA, VIB) High side/Low side drivers 4, 8 = PWM input High side/Low side drivers U = UVLO level: A, B, C A = 6 V; B = 8 V; C = 12 V V = Isolation rating: B, D B = 2.5 kV; D = 5.0 kV D = Dead time setting range: none, 4 none = 10–200; 4 = 40–600
Line 2 Marking:	YY = Year WW = Workweek	Assigned by the Assembly House. Corresponds to the year and workweek of the mold date.
	TTTTTT = Mfg Code	Manufacturing Code from Assembly Purchase Order form.

14. Revision History

Revision A

September, 2023

- Updated decimal-based revision number to alphanumeric code.

Revision 1.02

August, 2020

- Added new package
- Corresponding -A OPNs are added for all existing -I OPNs
- Safety and certification tables were brought up-to-date
- Power calculation section updated
- Application diagrams updated to clarify devices represented
- Enhanced UVLO description taken to separate section
- Output threshold specs added for digital output pin

Revision 1.01

July 2018

- Added Automotive-grade information including features, applications, and Ordering Guide table.