DATA SHEET

Si8931 and Si8932 Isolated Analog Amplifiers

Applications

- Industrial, hybrid electric vehicle (HEV), and renewable energy inverters
- AC, brushless, and dc motor controls and drives
- Variable-speed motor control in white goods
- Isolated switch mode and uninterruptible power supplies (UPS)
- General industrial data acquisition and sensor interface
- Automotive onboard chargers, battery management systems, and charging stations

Features

- 0 to 2.5 V nominal input voltage
- Low signal delay: 1 µs
- Typical input offset: 0.16 mV
- Typical gain error: ±0.06%
- Excellent drift specifications
- 0.75 µV/°C offset drift
- 6 ppm/°C typical gain drift
- Typical nonlinearity: 0.01%
- Typical SNR: 76 dB
- High common-mode transient immunity: 75 kV/µs
- Automotive-grade OPNs available
  - AEC-Q100 qualification
  - AIAG-compliant PPAP documentation support
  - IMDS and CAMDS listing support
- Compact packages
  - 8-pin, wide-body stretched SOIC
  - 8-pin, narrow-body SOIC
- –40 to 125 °C
- For RoHS and other product compliance information, see the Skyworks Certificate of Conformance.

Safety Regulatory Approvals

- UL recognized
  - 1577 (up to 5000 V_{RMS} for one minute)
- CSA certification conformity
  - 62368-1 (reinforced insulation)
  - 60601-1 (2 MOPP)
- VDE certification conformity
  - 60747-17 (reinforced insulation)
- CQC certification approval
  - GB4943.1 (reinforced insulation)

Description

The Si8931 and Si8932 galvanically isolated analog amplifiers feature 2.5 V input range and are optimized for isolated voltage-sensing applications. The outputs consist of either a differential analog signal (Si8931) or a single-ended signal (Si8932) proportional to the input voltage.

The Si8931/32 provide excellent linearity with low offset and gain drift to maintain accuracy over the entire operating temperature range.
Exceptionally high common-mode transient immunity ensures the Si8931/32 deliver accurate measurements, even in high-power switching environments found in motor drive systems and inverters.

The Si8931/32 isolated voltage-sensing amplifiers utilize Skyworks proprietary isolation technology, which supports up to 5.0 kV_{RMS} withstand voltage per UL1577. This technology enables high performance, reduced variation with temperature and age, tighter part-to-part matching, and longer lifetimes compared to other isolation technologies.

Automotive Grade is available for certain part numbers. These products are built using automotive-specific flows at all steps in the manufacturing process to ensure the robustness and low defectivity required for automotive applications.

1. Functional Block Diagrams

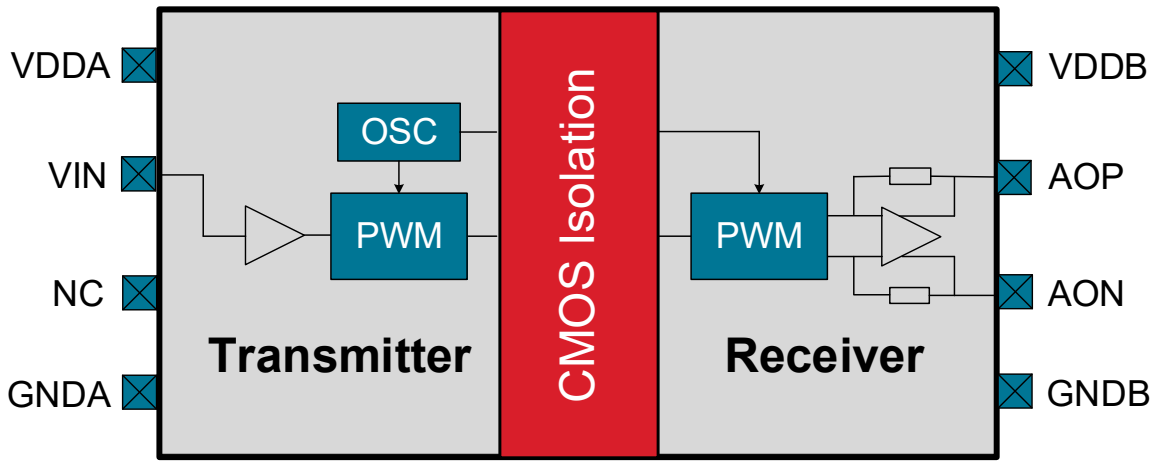


Figure 1. Si8931 Functional Block Diagram

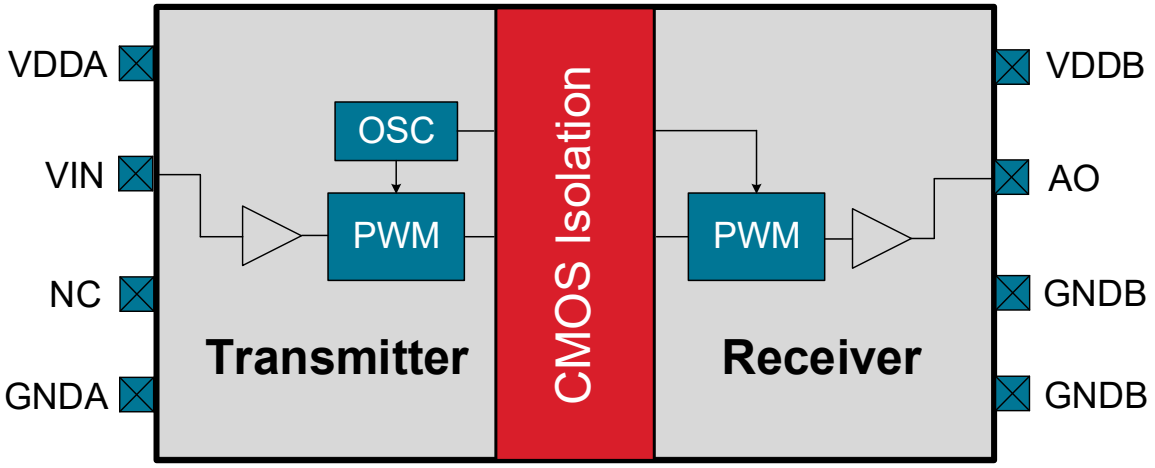


Figure 2. Si8932 Functional Block Diagram

2. Pin Descriptions

2.1. Si8931

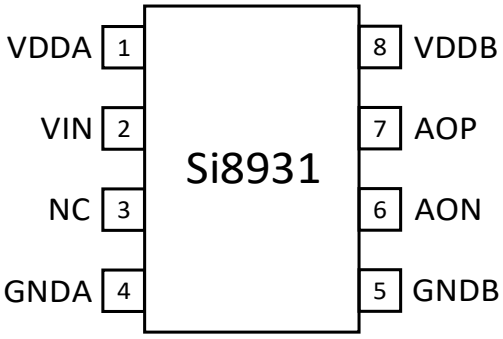


Figure 3. Si8931 Pinout (Top View)

Table 1. Si8931 Pin Descriptions

Name	Pin Number	Description
VDDA	1	Input side power supply
VIN	2	Voltage input
NC[1]	3	No connect
GNDA	4	Input side ground
GNDB	5	Output side ground
AON	6	Analog output low
AOP	7	Analog output high
VDDB	8	Output side power supply

1. No connect. These pins are not internally connected. To maximize CMTI performance, these pins should be connected to the ground plane.

2.2. Si8932

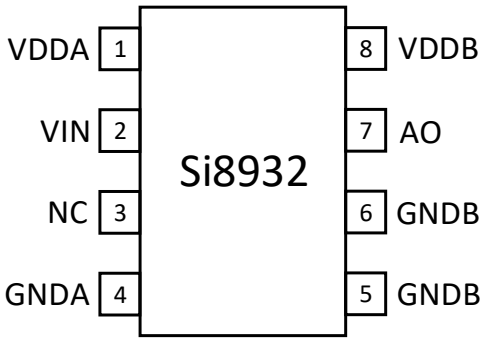


Figure 4. Si8932 Pinout (Top View)

Table 2. Si8932 Pin Descriptions

Name	Pin Number	Description
VDDA	1	Input side power supply
VIN	2	Voltage input
NC[1]	3	No connect
GNDA	4	Input side ground
GNDB[2]	5	Output side ground
GNDB[2]	6	Output side ground
AO	7	Analog output
VDDB	8	Output side power supply

1. No connect. These pins are not internally connected. To maximize CMTI performance, these pins should be connected to the ground plane.
2. Both Pin 5 and Pin 6 must be connected to ground.

3. Functional Description

The Si8931/32 are designed for 0 to 2.5 V nominal input.

The Si8931/32 modulates the analog signal in a unique way for transmission across the semiconductor-based isolation barrier. The input signal is first converted to a pulse-width modulated digital signal. On the other side of the isolation barrier, the signal is demodulated to faithfully reproduce the analog signal. This solution provides exceptional signal bandwidth and accuracy. The Si8931 provides a differential voltage output while the Si8932 provides a single-ended voltage output.

3.1. Fail-Safe and Low-Power Modes

The Si8931/32 implements a fail-safe output when the high-side supply voltage VDDA goes away. This is important for safe operation in systems with high safety requirements. The fail-safe output is nominally 2.8 V (Si8932) or –2.8 V (Si8931), which can be differentiated from the maximum clipping output voltage of 2.6 V to simplify diagnostics on the system level.

Table 3. Si8931 and Si8932 Output Voltages

Device	Output Voltage (VDDA Normal)	Output Voltage (VDDA Removed)
Si8931	~ ±2.6 V	~ –2.8 V
Si8932	0 to ~2.6 V	~ +2.8 V

In addition to the fail-safe output, when a loss of VDDA supply occurs, the part automatically moves into a lower-power mode that reduces IDDB current to approximately 1 mA. The controller side continues to monitor high-side communications to determine when VDDA supply returns. When the supply voltage is returned, normal operation begins in approximately 250 µs.

3.2. Voltage Sense Application

A typical, isolated voltage-sensing application circuit is shown in Figure 5 on page 6. In this example, a high voltage is divided down to produce a voltage (VIN) within the optimum input signal range of the Si8931/32. Numerous alternative inputs configurations are possible with the flexibility of a high impedance input isolator.

The Si8931 senses the single-ended input voltage and reproduces it as a differential (or single-ended with the Si8932) output voltage across the galvanic isolation barrier. The Si8931 differential outputs (AOP, AON) can be routed directly to a differential analog-to-digital converter (ADC) as shown below.

The Si8932 senses the single-ended input voltage and reproduces it as a single-ended output voltage across the galvanic isolation barrier. The single-ended output can be routed directly to a standard ADC (not shown). If the voltage sensed is >2.5 V, a simple voltage divider consisting of R1 and R2 can be used to scale down any voltage to fit the input range of the Si8931/32. R2 < 10 kΩ is recommended for best performance.

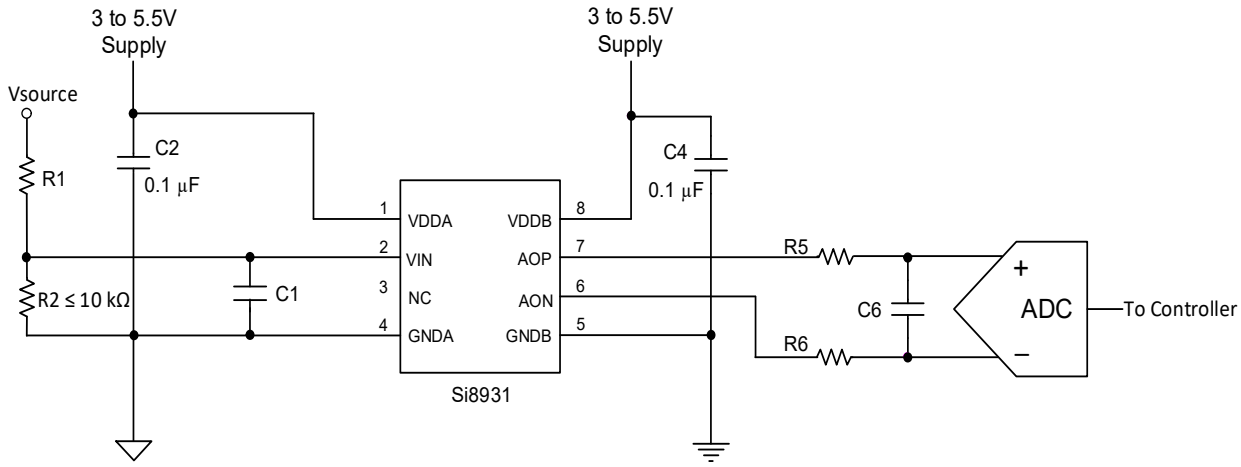


Figure 5. Voltage Sense Application

The amplifier bandwidth of the Si8931/32 is approximately 600 kHz. For applications where input filtering is required, a passive, differential RC low-pass filter can be placed at the input pin. Consider the source resistance of the signal measured (or the parallel combination of R1 and R2 if using a voltage divider) as it should be included in the filter calculation. Capacitor C1 should be sized to make a band limiting filter at the desired frequency.

The local bypass capacitor, C4, for the B-side of Si8931/32, should be placed closed to VDDB supply pin with its return close to GNDB. The output signal at AOP and AON is differential with unity gain and common mode of 1.4 V. The outputs are sampled by a differential input ADC. Depending on the sample rate of the ADC, an anti-aliasing filter may be required. A simple anti-aliasing filter can be made from the passive components, R5, C6, and R6. The characteristics of this filter are dictated by the input topology and sampling frequency of the ADC.

However, to ensure the Si8931/32 outputs are not overloaded, R5 = R6 > 5 kΩ and C6 can be calculated using Equation 1:

$$C6 = \frac{1}{2 \times \pi \times (R5 + R6) \times f_{3dB}}$$

Equation 1.

4. Electrical Specifications

Table 4. Absolute Maximum Ratings[1]

Parameter	Symbol	Min	Max	Unit
Storage temperature	T_{STG}	–65	150	°C
Ambient temperature under bias	T_A	–40	125	°C
Junction temperature	T_J	—	150	°C
Supply voltage	VDDA, VDDB	–0.5	6.0	V
Input voltage respect to GNDA	VAIP, VAIN	–0.5	VDDA + 0.5	V
Output sink or source current	$\lvert I_O \rvert$	—	5	mA
Total power dissipation	P_T	—	212	mW
Lead solder temperature (10 s)		—	260	°C
Human body model ESD rating	HBM	—	6000	V
Charged device model ESD rating	CDM	—	2000	V

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

***ESD Handling**: Industry-standard ESD handling precautions must be adhered to at all times to avoid damage to this device.*

Table 5. Electrical Specifications[1]

T_A = –40 to +125 °C; typical specs at 25 °C with VDDA = VDDB = 5 V unless specified differently under test condition.

Parameter		Symbol	Test Condition	Min	Typ	Max	Unit
Input side supply voltage		VDDA		3.0	—	5.5	V
Input supply current	Si8931/32	IDDA	VDDA = 3.3 V	—	4.7	5.7	mA
Output side supply voltage		VDDB		3.0	—	5.5	V
Output supply current	Si8931	IDDB	VDDB = 3.3 V	—	3.5	4.5	mA
	Si8932	IDDB	VDDB = 3.3 V	—	4.3	5	mA
Amplifier bandwidth				—	600	—	kHz
Amplifier Input							
Specified linear input range		VIN		0.25	—	2.25	V
Maximum input voltage before clipping		VIN		—	2.5	—	V
Input referred offset		VOS	T_A = 25 °C, VIN = 0.25 V	–1	±0.16	1	mV
Input offset drift		VOST		–25	±0.75	25	µV/°C
Input impedance		RIN		—	500	—	MΩ
Amplifier Output							
Full-scale output				—	2.5	—	Vpk
Gain				—	1	—	
Gain error			T_A = 25 °C	–0.25	±0.06	0.25	%
Gain error drift	Si8931			–40	6	20	ppm/°C
	Si8932			–30	–5	30	ppm/°C
Output common-mode voltage	Si8931	(VAOP + VAON)/2		1.34	1.39	1.44	V
Nonlinearity	Si8931		T_A = 25 °C	–0.04	0.01	0.04	%
	Si8932		T_A = 25 °C	–0.05	0.01	0.05	%
Nonlinearity drift			T_A = 25 °C	–5	—	5	ppm/°C
Signal-to-noise ratio	Si8931	SNR	100 kHz bandwidth	73	77	—	dB
	Si8932	SNR	100 kHz bandwidth	72	76	—	dB
Total harmonic distortion	Si8931	THD	FIN = 1 kHz	—	–80	–60	dB
	Si8932	THD	FIN = 1 kHz	—	–80	–60	dB

Table 5. Electrical Specifications[1] (Continued)

T_A = –40 to +125 °C; typical specs at 25 °C with VDDA = VDDB = 5 V unless specified differently under test condition.

Parameter		Symbol	Test Condition	Min	Typ	Max	Unit
Power supply rejection ratio		PSRR	VDDA at dc	—	–100	—	dB
Power supply rejection ratio		PSRR	VDDA at 100 mV and 10 kHz ripple	—	–100	—	dB
			VDDB at dc	—	–100	—	dB
			VDDB at 100 mV and 10 kHz ripple	—	–100	—	dB
Output resistive load	Si8931	R_{LOAD}	Between AON and AOP	5	—	—	kΩ
	Si8932		Between AO and GND	5	—	—	kΩ
Output capacitive load		C_{LOAD}	Each pin to ground	—	—	100	pF
Timing							
Signal delay		t_{PD}	50% to 50%	—	1	—	µs
Rise time		t_R	10% to 90%	—	1.6	—	µs
Common-mode transient immunity[2]		CMTI	VIN = GNDA, VCM = 1500 V	50	75	—	kV/µs

1. Performance is assured only under the conditions listed in this table and is not invariant over the full operating or storage temperature ranges. Operation at elevated temperatures may reduce reliability of the device.
2. An analog CMTI failure is defined as an output error of more than 100 mV persisting for at least 1 µs.

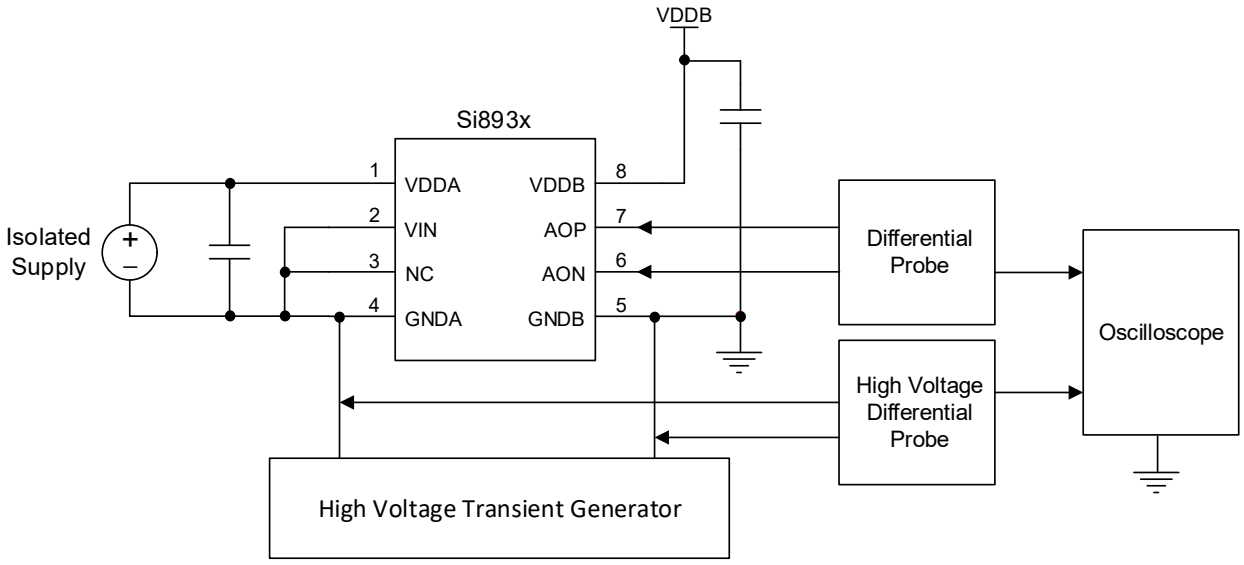


Figure 6. Common-Mode Transient Immunity Characterization Circuit

4.1. Typical Performance Characteristics

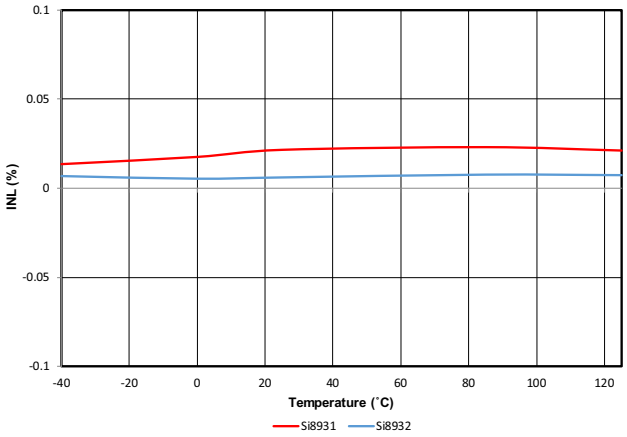


Figure 7. Nonlinearity (%) vs. Temperature (°C)

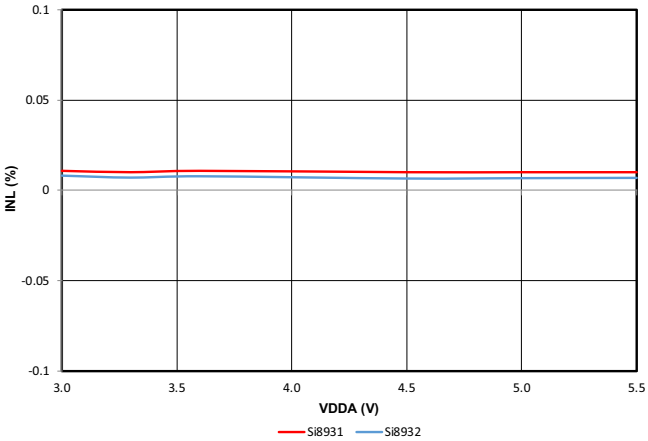


Figure 8. Nonlinearity (%) vs. VDDA Supply (V)

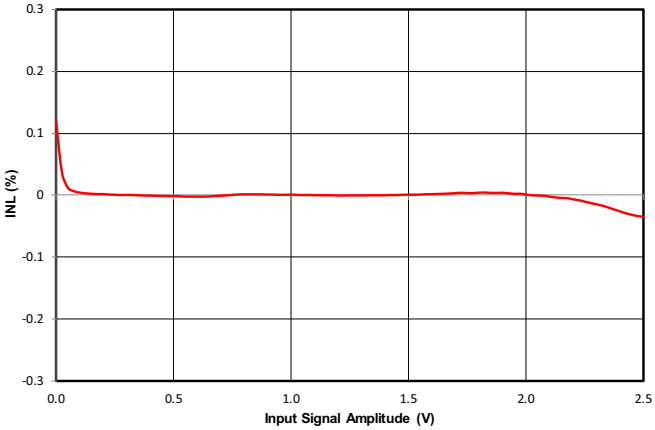


Figure 9. Si8931 Nonlinearity (%) vs. Input Signal Amplitude (mV)

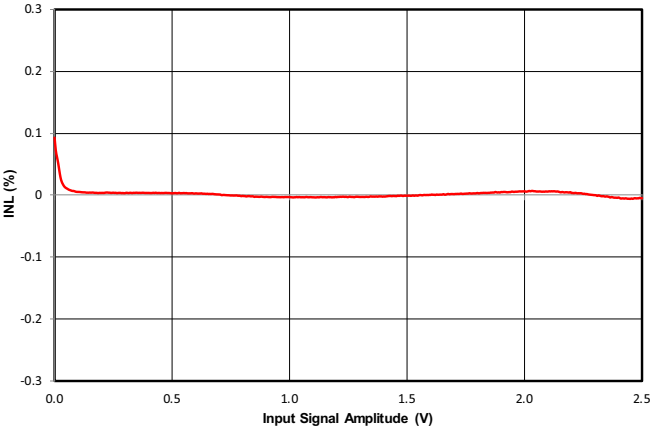


Figure 10. Si8932 Nonlinearity (%) vs. Input Signal Amplitude (mV)

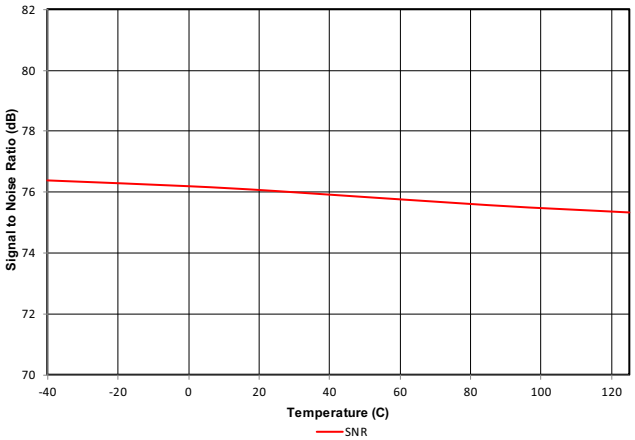


Figure 11. Signal-to-Noise Ratio (dB) vs. Temperature (°C)

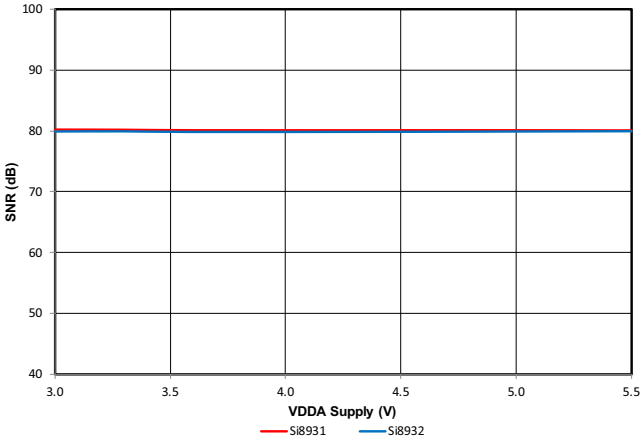


Figure 12. Signal-to-Noise Ratio (dB) vs. VDDA Supply (V)

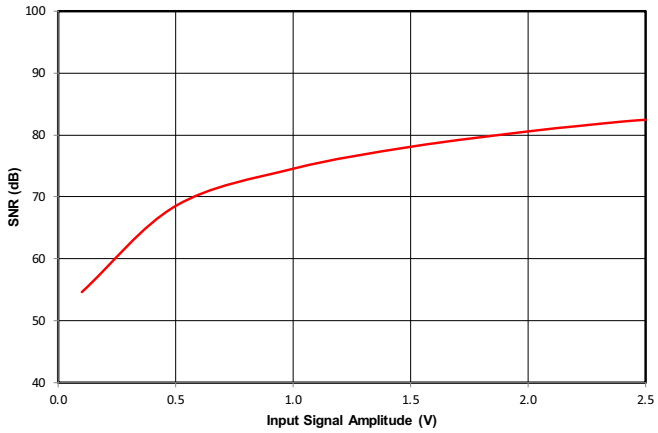


Figure 13. Si8931 Signal-to-Noise Ratio (dB) vs. Input Signal Amplitude (V)

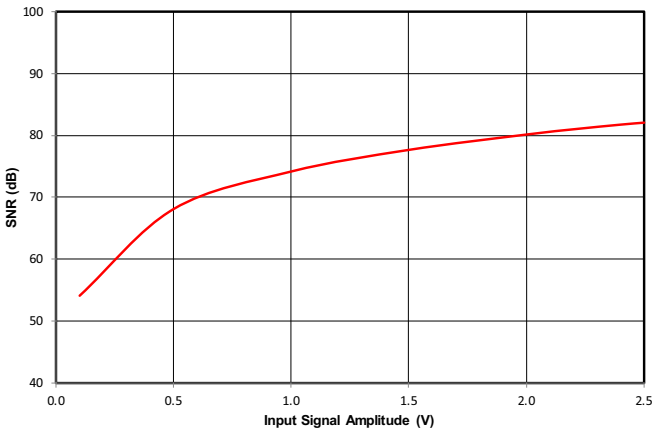


Figure 14. Si8932 Signal-to-Noise Ratio (dB) vs. Input Signal Amplitude (V)

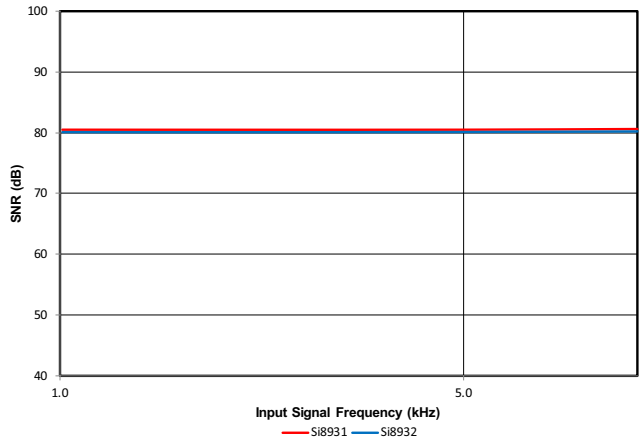


Figure 15. Signal-to-Noise Ratio (dB) vs. Input Signal Frequency (kHz)

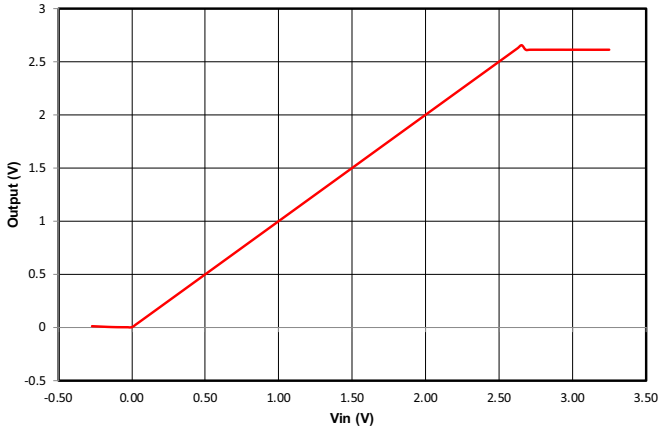


Figure 16. Output Voltage (V) vs. Input Voltage (V)

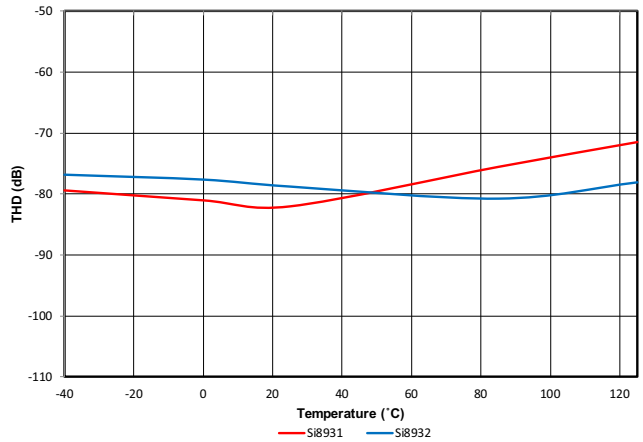


Figure 17. Total Harmonic Distortion (dB) vs. Temperature (°C)

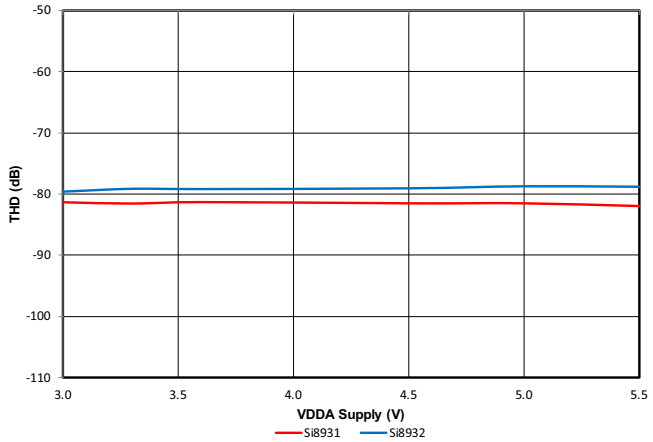


Figure 18. Total Harmonic Distortion (dB) vs. VDDA Supply (V)

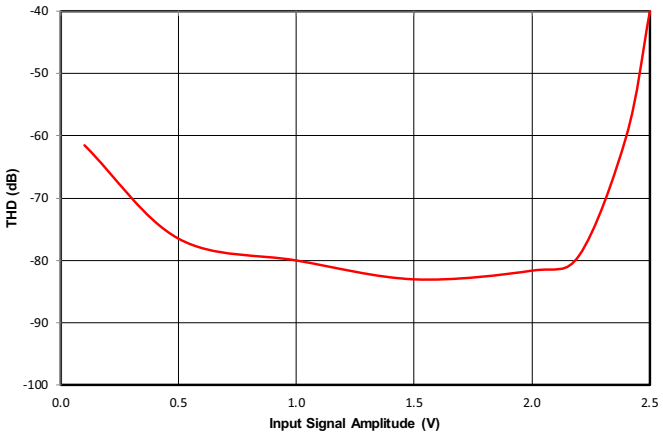


Figure 19. Si8931 Total Harmonic Distortion (dB) vs. Input Signal Amplitude (V)

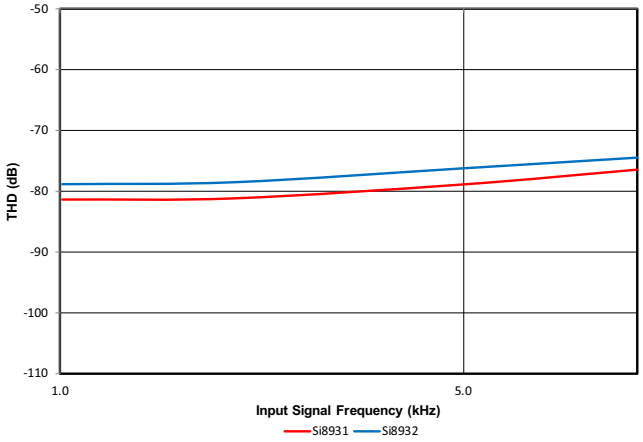


Figure 20. Total Harmonic Distortion (dB) vs. Input Signal Frequency (kHz)

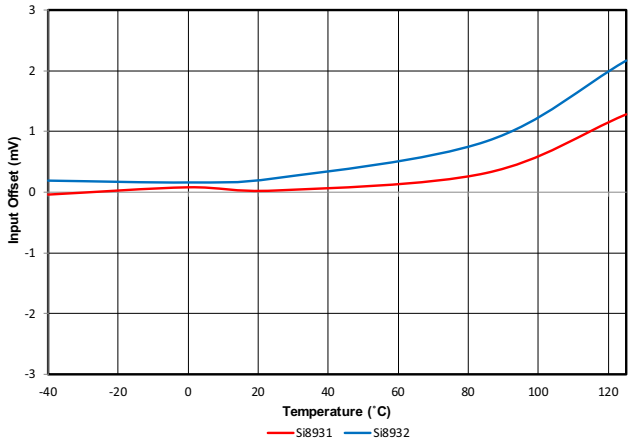


Figure 21. Input Offset (mV) vs. Temperature (°C)

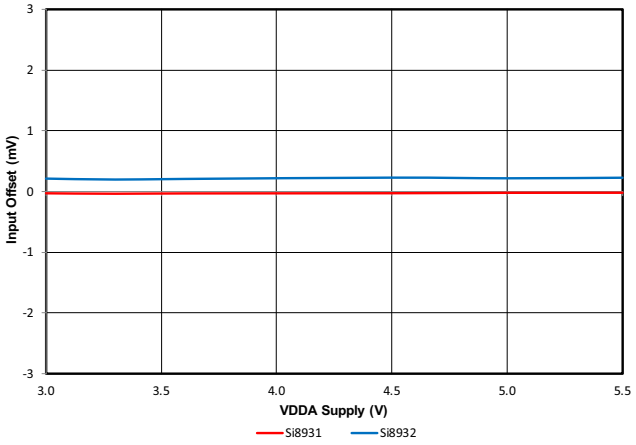


Figure 22. Input Offset (mV) vs. VDDA Supply (V)

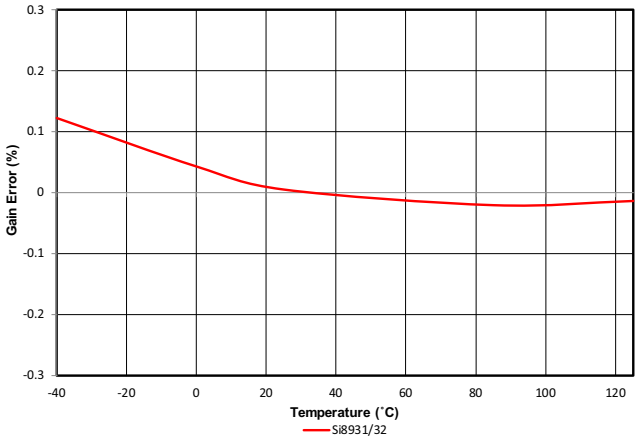


Figure 23. Gain Error (%) vs. Temperature (°C)

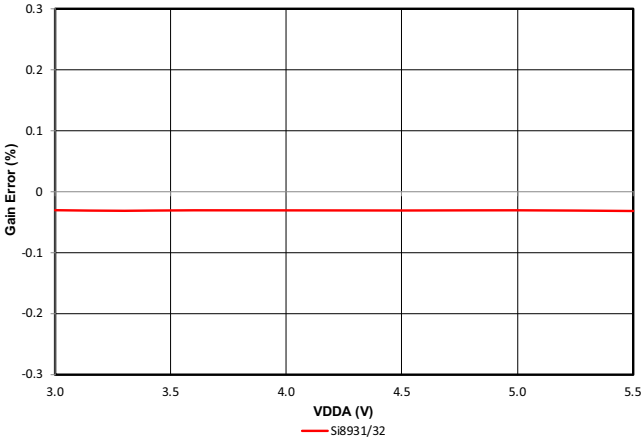


Figure 24. Gain Error (%) vs. VDDA Supply (V)

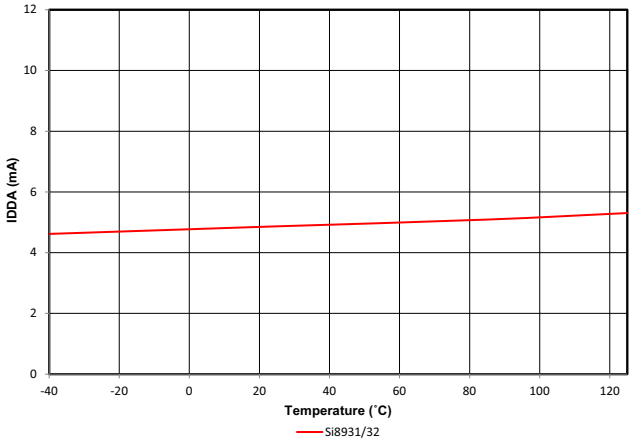


Figure 25. IDDA (mA) vs. Temperature (°C)

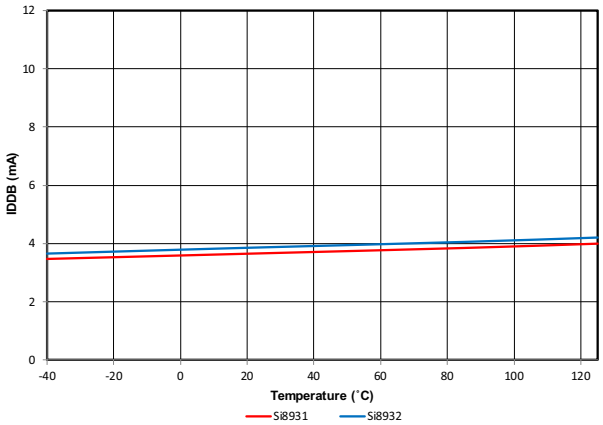


Figure 26. IDDB (mA) vs. Temperature (°C)

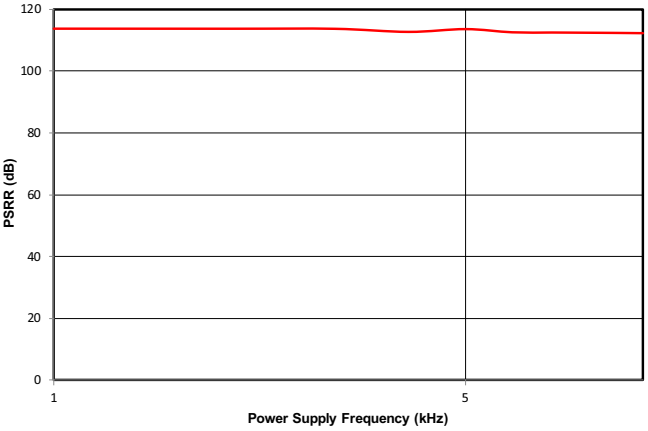


Figure 27. PSRR (dB) vs. Power Supply Frequency (kHz)

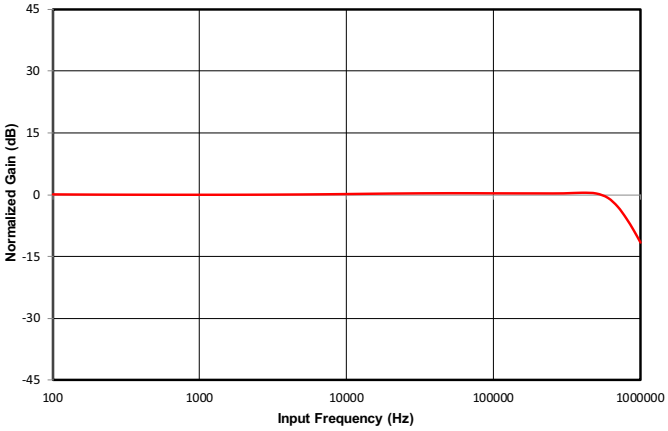


Figure 28. Amplifier Bandwidth

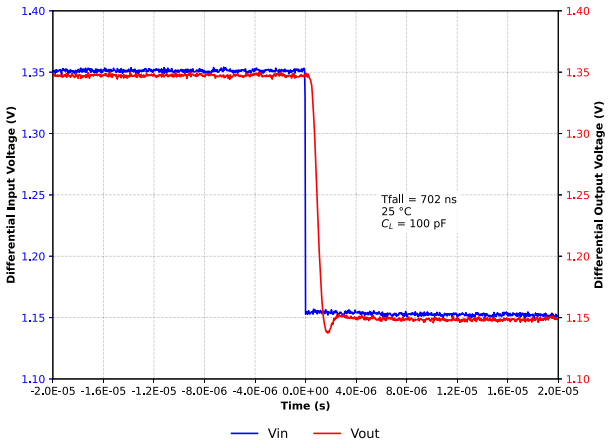


Figure 29. Si8931 High-to-Low Step Response

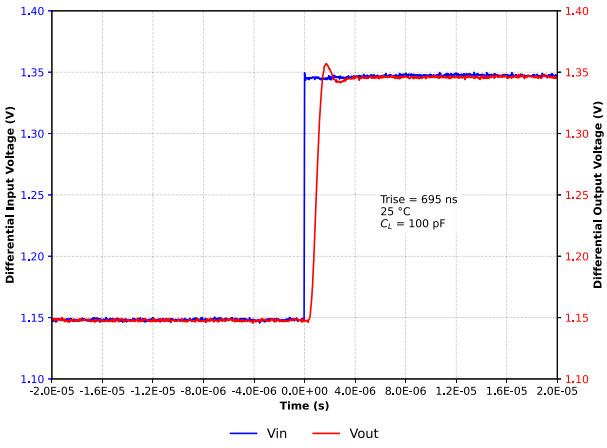


Figure 30. Si8931 Low-to-High Step Response

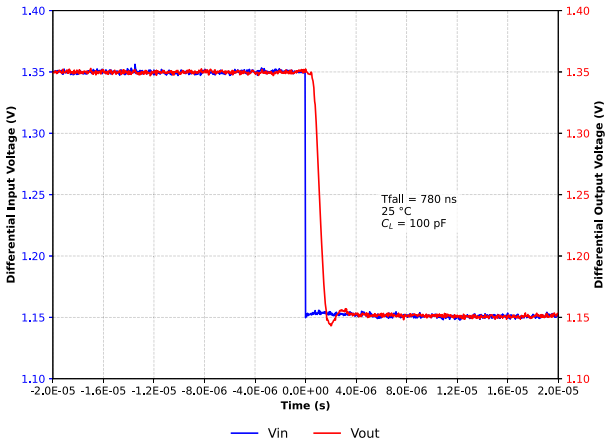


Figure 31. Si8932 High-to-Low Step Response

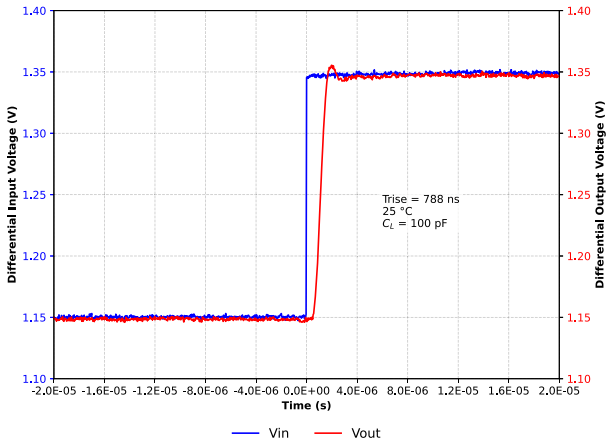


Figure 32. Si8932 Low-to-High Step Response

4.2. Thermal Characteristics

Table 6. Thermal Characteristics

Parameter	Symbol	WB Stretched SOIC-8	NB SOIC-8	Unit
IC junction-to-ambient thermal resistance	θ_{JA}	90	112	°C/W

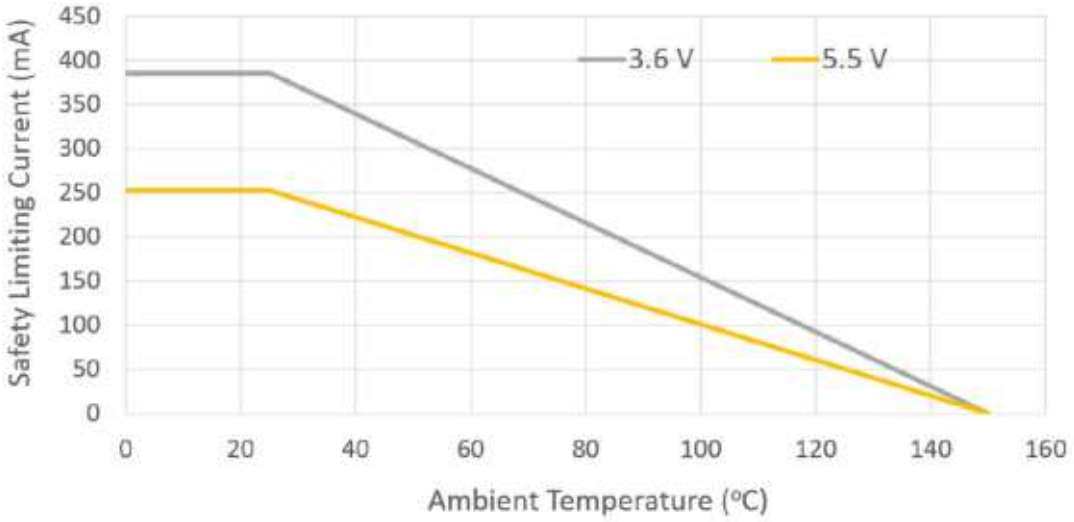


Figure 33. WB Stretched SOIC-8 Safety Current vs. Ambient Temperature Derating Curve

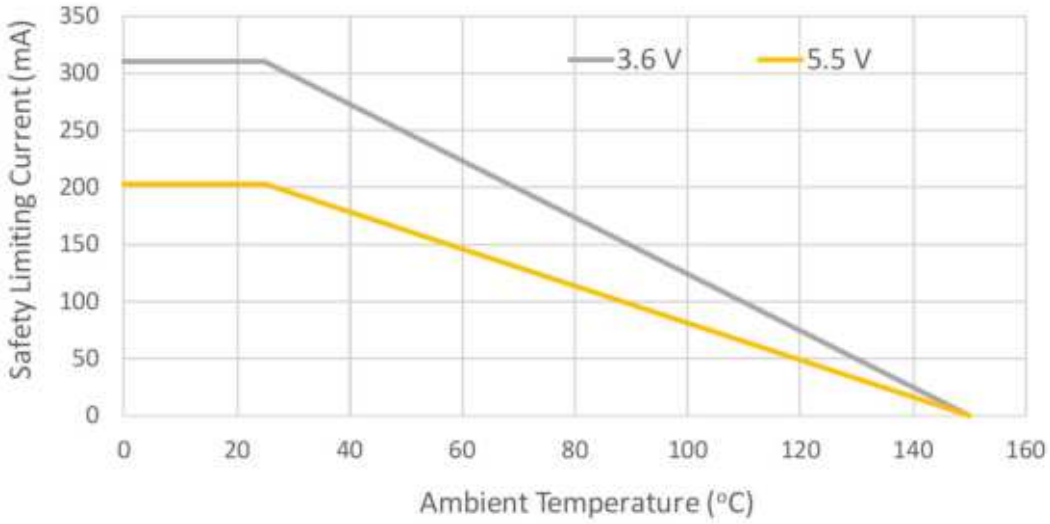


Figure 34. NB SOIC-8 Safety Current vs. Ambient Temperature Derating Curve

4.3. Safety Certifications and Specifications

Table 7. Regulatory Information[1]

CSA
The Si89xx is certified under CSA. For more details, see Master Contract File 232873.
62368-1: Rated up to 600 V_{RMS} reinforced insulation working voltage; rated up to 1000 V_{RMS} basic insulation working voltage.
60601-1: Rated up to 250 V_{RMS} working voltage and two means of patient protection (MOPP).
VDE
The Si89xx is certified under VDE. For more details, see File 5028467.
60747-17: Rated up to 2121 V_{peak} for reinforced insulation working voltage.
UL
The Si89xx is certified under UL1577 component recognition program. For more details, see File E257455.
Rated up to 5000 V_{RMS} V_{ISO} isolation voltage for basic protection.
CQC
The Si89xx is certified under GB4943.1.
Rated up to 250 V_{RMS} reinforced insulation working voltage at 5000 meters tropical climate.

1. For more information, see 6. "Ordering Information" on page 30.

Table 8. Insulation and Safety-Related Specifications

Parameter	Symbol	Test Condition	Value		Unit
			WB Stretched SOIC-8	NB SOIC-8	
Nominal external air gap (clearance)[1,2,3]	CLR		8.5	4.0	mm
Nominal external tracking (creepage)[1,2,3]	CRP		8.5	4.0	mm
Minimum internal gap (internal clearance)	DTI		0.036	0.036	mm
Tracking resistance	CTI or PTI	IEC60112	Up to 600	Up to 600	V_{RMS}

1. CSA certifies the clearance and creepage limits listed in this table.
2. UL does not impose a clearance and creepage minimum for component-level certifications.
3. VDE certifies the clearance and creepage limits as: NB SOIC-8 $\geq$ 4.0 mm, WB Stretched SOIC-8 $\geq$ 8.5 mm.

Table 9. IEC 60664-1 Ratings

Parameter	Test Conditions	Specification	
		WB Stretched SOIC-8	NB SOIC-8
Material group		I/II	I/II
Overvoltage category	Rated mains voltage ≤150 V_{RMS}	I-IV	I-IV
	Rated mains voltage ≤300 V_{RMS}	I-IV	I-III
	Rated mains voltage ≤600 V_{RMS}	I-IV	I-II
	Rated mains voltage ≤1000 V_{RMS}	I-III	I

Table 10. IEC 60747-17 Insulation Characteristics[1]

Parameter	Symbol	Test Condition	Characteristic		Unit
			WB Stretched SOIC-8	NB SOIC-8	
Maximum working isolation voltage	V_{IOWM}	According to Time-Dependent Dielectric Breakdown (TDDB) Test	1500	445	V_{RMS}
Maximum repetitive isolation voltage	V_{IORM}	According to Time-Dependent Dielectric Breakdown (TDDB) Test	2121	630	V_{peak}
Apparent charge	q_{pd}	Method b: At routine test (100% production) and preconditioning (type test); V_{ini} = 1.2 x V_{IOTM}, t_{ini} = 1 s; $V_{pd(m)}$ = 1.875 x V_{IORM}, t_m = 1 s (method b1) or $V_{pd(m)}$ = V_{ini}, t_m = t_{ini} (method b2)	≤5	≤5	pC
Maximum transient isolation voltage	V_{IOTM}	V_{TEST} = V_{IOTM}, t = 60 s (qualification); V_{TEST} = 1.2 x V_{IOTM}, t = 1 s (100% production)	7070	3535	V_{peak}
Maximum surge isolation voltage	V_{IOSM}	Tested in oil with ≥1.3 x V_{IMP}, 10 kV minimum, and 1.2 µs/50 µs profile (qualification)	10400	10400	V_{peak}
Maximum impulse voltage	V_{IMP}	Tested in air with 1.2 µs/50 µs profile	8000	5000	V_{peak}
Capacitance (input-output)[2]	C_{IO}	f = 1 MHz	1	1	pF
Isolation resistance[2]	R_{IO}	T_A = 25 °C, V_{IO} = 500 V	$>10^{12}$	$>10^{12}$	Ω
		T_A = 125 °C, V_{IO} = 500 V	$>10^{11}$	$>10^{11}$	Ω
	R_{IO_S}	T_A = T_S, V_{IO} = 500 V	$>10^9$	$>10^9$	Ω
Pollution degree			2	2	
Climatic category			40/125/21	40/125/21	

1. This coupler is suitable for “reinforced insulation” only within the safety limiting values. Compliance with the safety limiting values shall be ensured by means of suitable protective circuits.
2. To determine resistance and capacitance, the device is converted into a two-terminal device. Pins on Side A are shorted together to form the first terminal, and pins on Side B are shorted together to form the second terminal. The parameters are then measured between these two terminals.

Table 11. IEC 60747-17 Safety Limiting Values[1]

Parameter	Symbol	Test Condition	Characteristic	Unit
Safety temperature	T_S		150	°C
Safety input, output or supply current (WB stretched SOIC-8)	I_S	θ_{JA} = 90 °C/W VDD = 5.5 V T_J = 150 °C T_A = 25 °C	253	mA
		θ_{JA} = 90 °C/W VDD = 3.6 V T_J = 150 °C T_A = 25 °C	386	mA
Safety input, output or supply current (NB SOIC-8)	I_S	θ_{JA} = 112 °C/W VDD = 5.5 V T_J = 150 °C T_A = 25 °C	203	mA
		θ_{JA} = 112 °C/W VDD = 3.6 V T_J = 150 °C T_A = 25 °C	310	mA
Safety input, output or total power (WB stretched SOIC-8)	P_S	θ_{JA} = 90 °C/W T_J = 150 °C T_A = 25 °C	1389	mW
Safety input, output or total power (NB SOIC-8)	P_S	θ_{JA} = 112 °C/W T_J = 150 °C T_A = 25 °C	1116	mW

1. Maximum value allowed in the event of a failure. Refer to the derating curves Figure 33. "WB Stretched SOIC-8 Safety Current vs. Ambient Temperature Derating Curve" and Figure 34, "NB SOIC-8 Safety Current vs. Ambient Temperature Derating Curve," on page 15.

Table 12. UL 1577 Insulation Characteristics

Parameter	Symbol	Test Condition	Characteristic		Unit
			WB Stretched SOIC-8	NB SOIC-8	
Maximum withstanding isolation voltage	V_{ISO}	$V_{TEST} = V_{ISO}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production)	5000	2500	V_{RMS}
Primary-side current rating		VDD = 5.5 V, T_A = 25 °C (qualification)	6.9	6.9	mA
Primary-side power rating			49.5	49.5	mW
Secondary-side current rating			10.75	10.75	mA
Secondary-side power rating			59	59	mW

5. Package and Handling Information

Since the device package is sensitive to moisture absorption, it is baked and vacuum packed before shipping. Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The Si8931D-IS4, Si8931D-AS4, Si8932D-IS4, and Si8932D-AS4 are rated to Moisture Sensitivity Level 2A (MSL2A) at 260 °C, while the Si8931B-IS, Si8931B-AS, Si8932B-IS, and Si8932B-AS are rated to MSL2 at 260 °C.

They can be used for lead or lead-free soldering. For additional information, refer to Skyworks Application Note, “PCB Design and SMT Assembly/Rework Guidelines,” Document Number 101752.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Refer to Standard SMT Reflow Profiles: JEDEC Standard J-STD-020.

5.1. 8-Pin Wide Body Stretched SOIC Top Marking

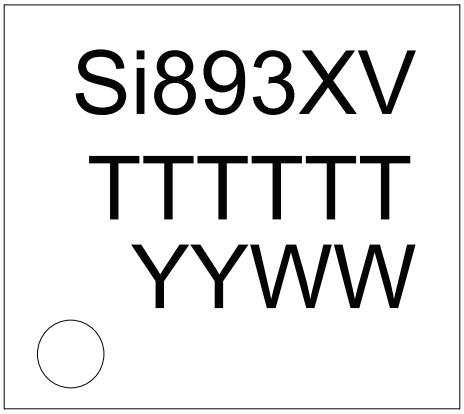


Figure 35. Si8931/32 Typical Package Marking, 8-Pin Wide Body Stretched SOIC

Table 13: 8-Pin Wide Body Stretched SOIC Marking Explanation

Line 1	Part Number	Si893x X = Base part number 1 = Differential output 2 = Single-ended output V = Insulation rating: D = 5.0 kV_{RMS}
Line 2	TTTTTT	Manufacturing Code
Line 3	YY = Year WW = Work Week Circle = 43 mils diameter left justified	Year and work week

5.2. 8-Pin Narrow Body SOIC Top Marking

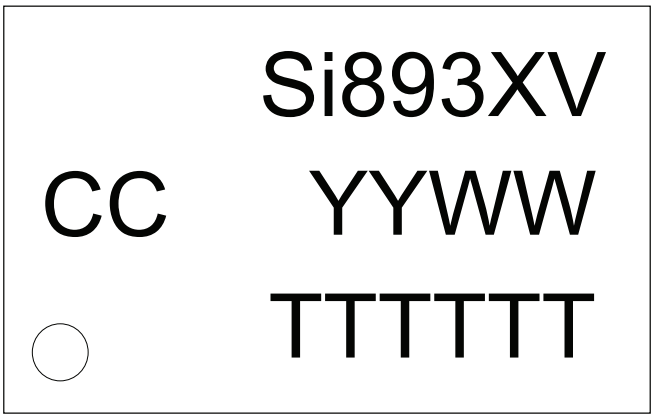


Figure 36. Si8931/32 Typical Package Marking, 8-Pin Narrow Body SOIC

Table 14. 8-Pin Narrow Body SOIC Marking Explanation

Line 1	Part Number	Si893x X = Base part number 1 = Differential output 2 = Single-ended output V = Insulation rating B = 2.5 kV_{RMS}
Line 2	CC = Country of origin ISO code abbreviation	
	YY = Year WW = Work Week	Year and work week
Line 3	Circle = 19.7 mils diameter left justified	Manufacturing code

5.3. 8-Pin, Wide-Body Stretched SOIC Package

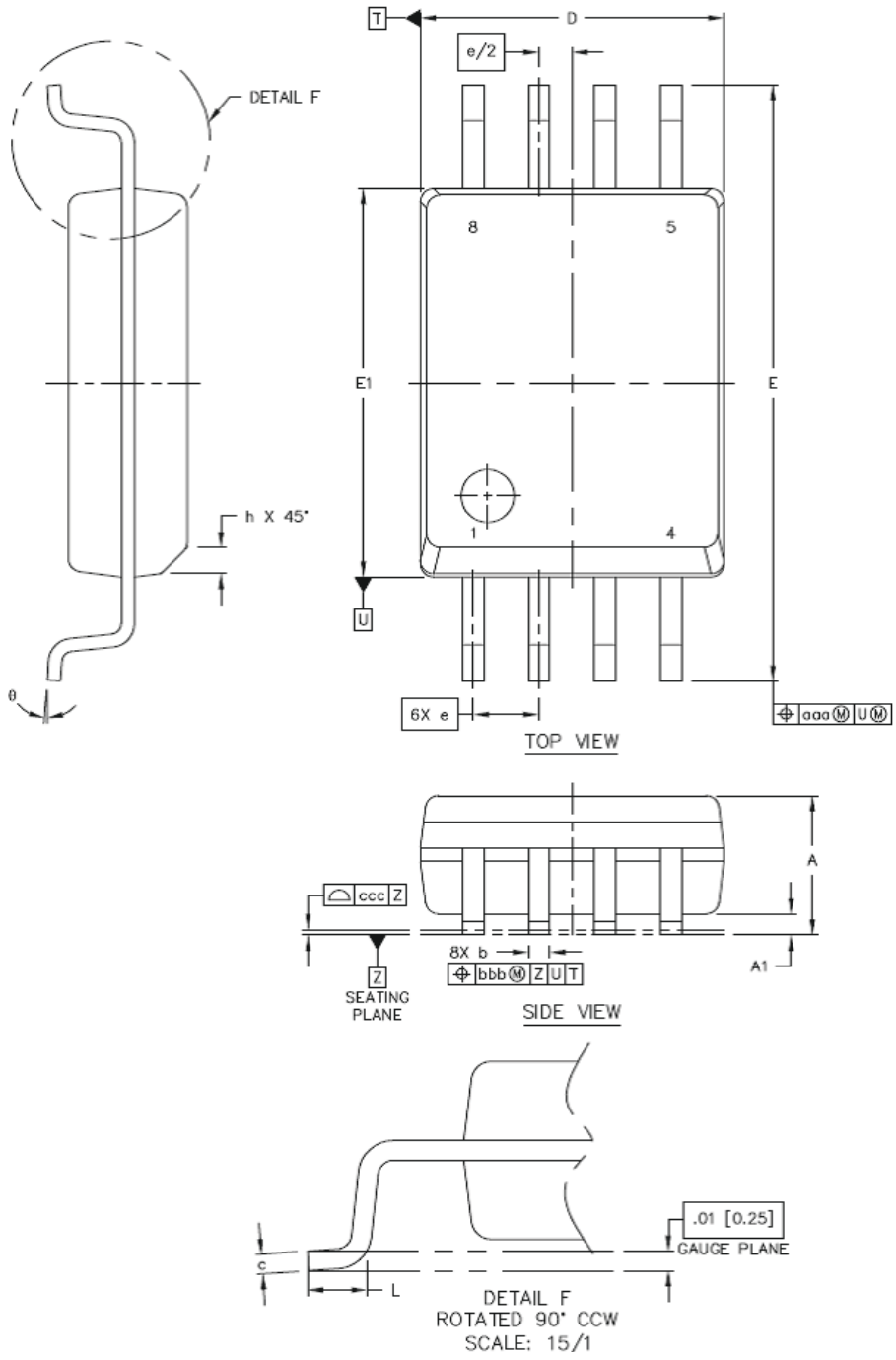


Figure 37. 8-Pin Wide Body Stretched SOIC Package

Table 15. 8-Pin Wide Body Stretched SOIC Package Dimensions[1,2,3]

Dimension	Millimeters	
	Min	Max
A	2.49	2.79
A1	0.36	0.46
b	0.30	0.51
c	0.20	0.33
D	5.74	5.94
E	11.25	11.76
E1	7.39	7.59
e	1.27 BSC	
L	0.51	1.02
h	0.25	0.76
θ	0°	8°
aaa		0.25
bbb		0.25
ccc		0.10

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. Recommended reflow profile per JEDEC J-STD-020C specification for small body, lead-free components.

5.4. 8-Pin, Narrow-Body SOIC Package

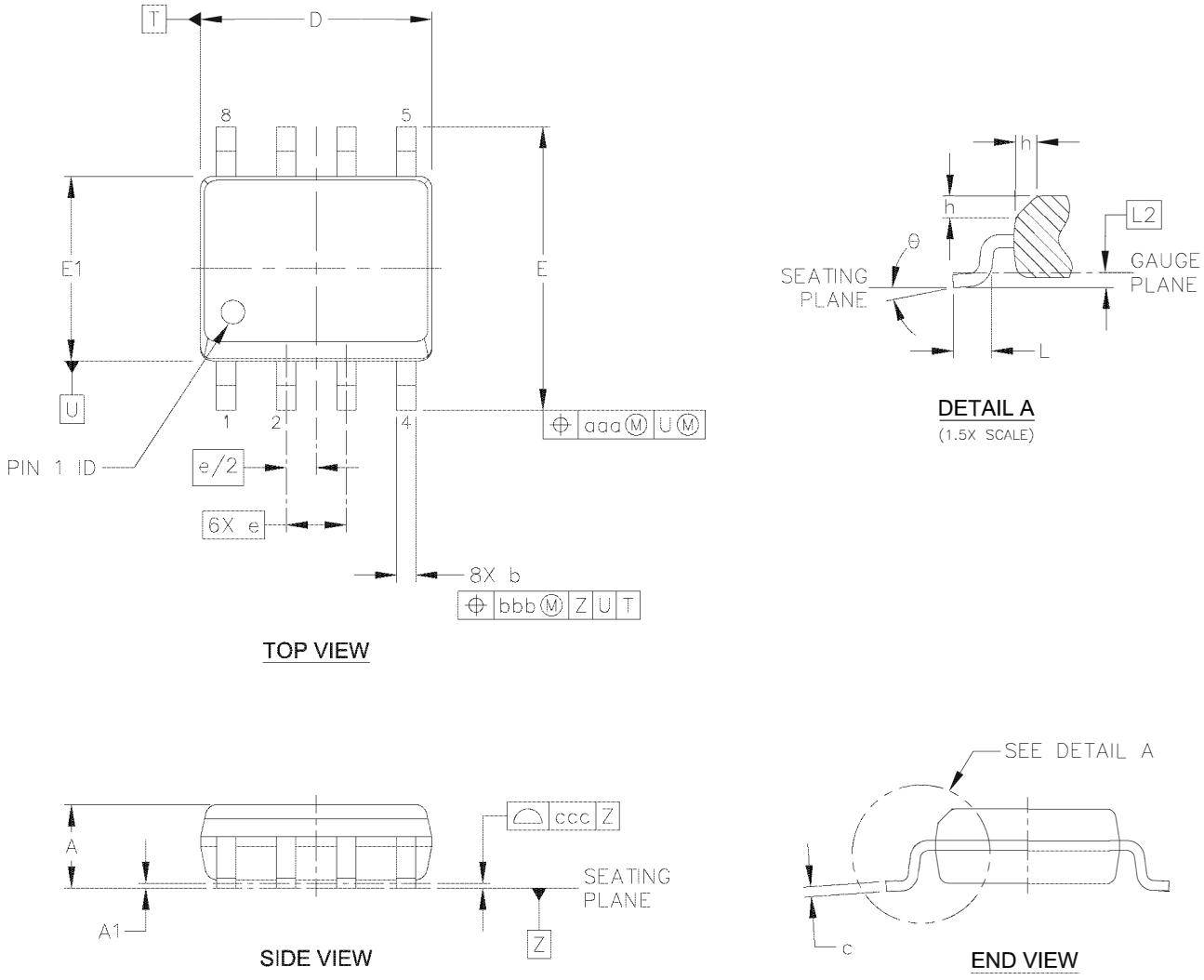


Figure 38. 8-Pin Narrow Body SOIC Package

Table 16. 8-Pin Narrow Body SOIC Package Dimensions[1,2,3,4,5]

Dimension	Symbol	Min	Max
Overall height	A	—	1.75
Stand off	A1	0.10	0.25
Lead width	b	0.33	0.51
L/F thickness	c	0.19	0.25
Body size	D	4.80	5.00
	E	5.80	6.20
	E1	3.80	4.00
Lead pitch	e	1.27 BSC	
Lead length	L	0.40	1.27
Gauge plane	L2	0.25 BSC	
Corner chamfer	h	0.25	0.50
Foot angle	θ	0°	8°
Lead edge tolerance	aaa	0.10	
Lead offset	bbb	0.20	
Coplanarity	ccc	0.10	

1. All linear dimensions are in millimeters.
2. Dimensioning and tolerancing per ANSI Y14.5M.
   BSC: Basic dimension. Theoretically exact shown without tolerance.
   REF: Reference dimension. Usually without tolerance; for information purposes only.
3. Dimension D does not include mold flash, protrusions, or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. This drawing conforms to the JEDEC Solid State Outline MS-137, Variation AB.
5. Recommended reflow profile per JEDEC J_STD_020 specification for small body, lead-free components.

5.5. 8-Pin, Wide Body Stretched SOIC Land Pattern

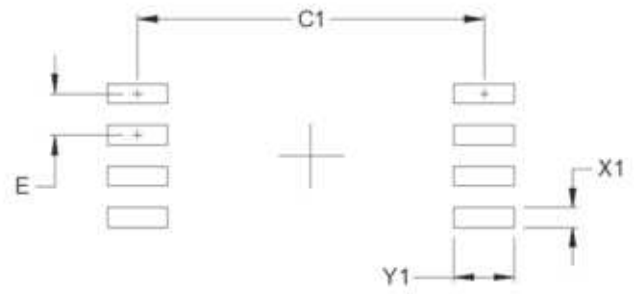
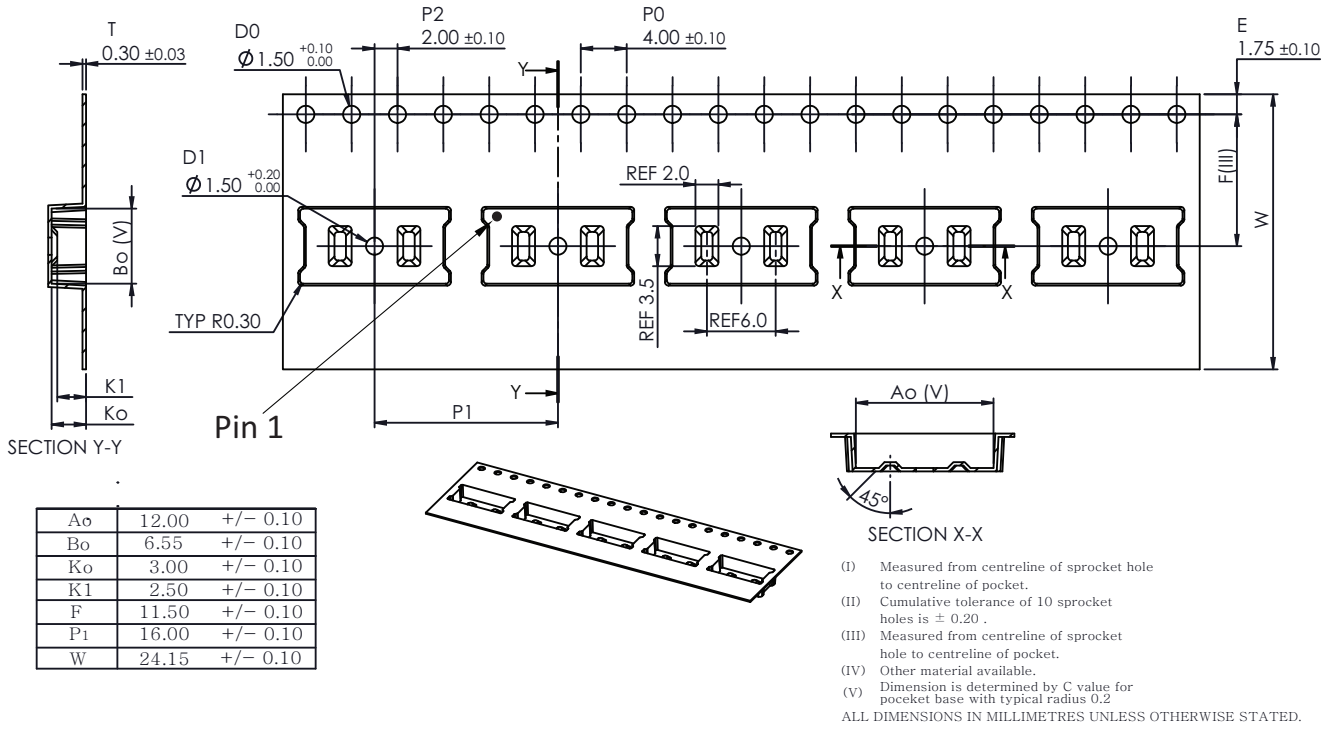


Figure 39. 8-Pin Wide Body Stretched SOIC Land Pattern

Table 17. 8-Pin Wide Body Stretched SOIC Land Pattern Dimensions

Dimension	mm	Notes
C1	10.60	**General** 1. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a fabrication allowance of 0.05 mm. 2. This land pattern design is based on the IPC-7351 guidelines. **Solder Mask Design** 1. All metal pads are to be non-solder-mask-defined (NSMD). 2. Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad. **Stencil Design** 1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release. 2. The stencil thickness should be 0.125 mm (5 mils). 3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads. **Card Assembly** 1. A No-Clean, Type-3 solder paste is recommended. 2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for small body components.
E	1.27	
X1	0.60	
Y1	1.85	

5.6. 8-Pin Wide Body Stretched SOIC Tape and Reel Information

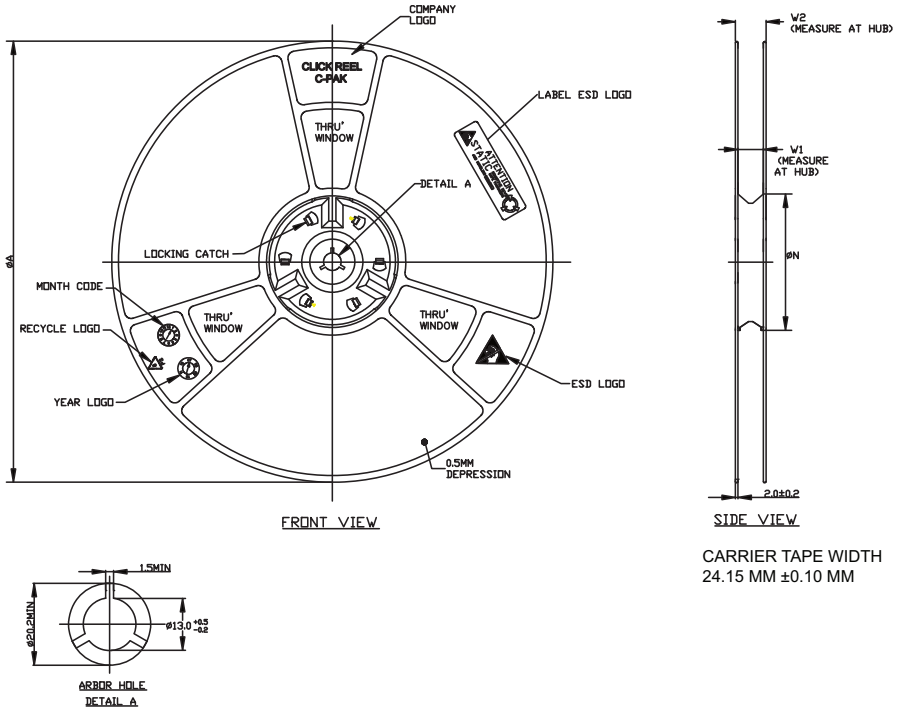


Ao	12.00	+/− 0.10
Bo	6.55	+/− 0.10
Ko	3.00	+/− 0.10
K1	2.50	+/− 0.10
F	11.50	+/− 0.10
P1	16.00	+/− 0.10
W	24.15	+/− 0.10

(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.
(V) Dimension is determined by C value for poceket base with typical radius 0.2

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED.

Figure 40. Wide Body Carrier Tape Information



CARRIER TAPE WIDTH
24.15 MM ±0.10 MM

Figure 41. Wide Body Reel Information

5.7. 8-Pin Narrow Body SOIC Land Pattern

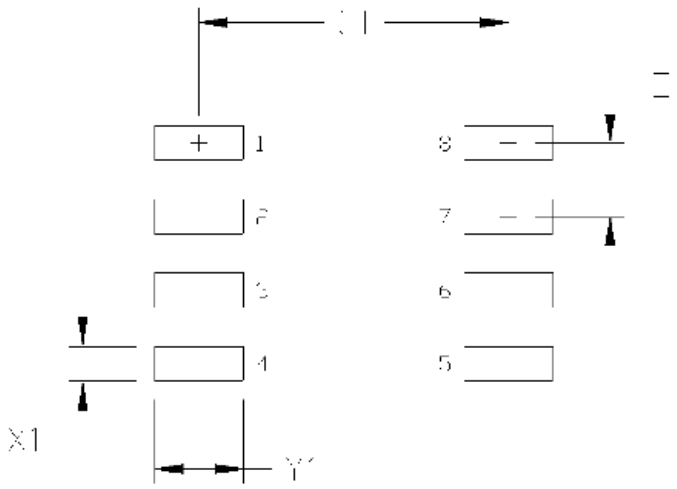


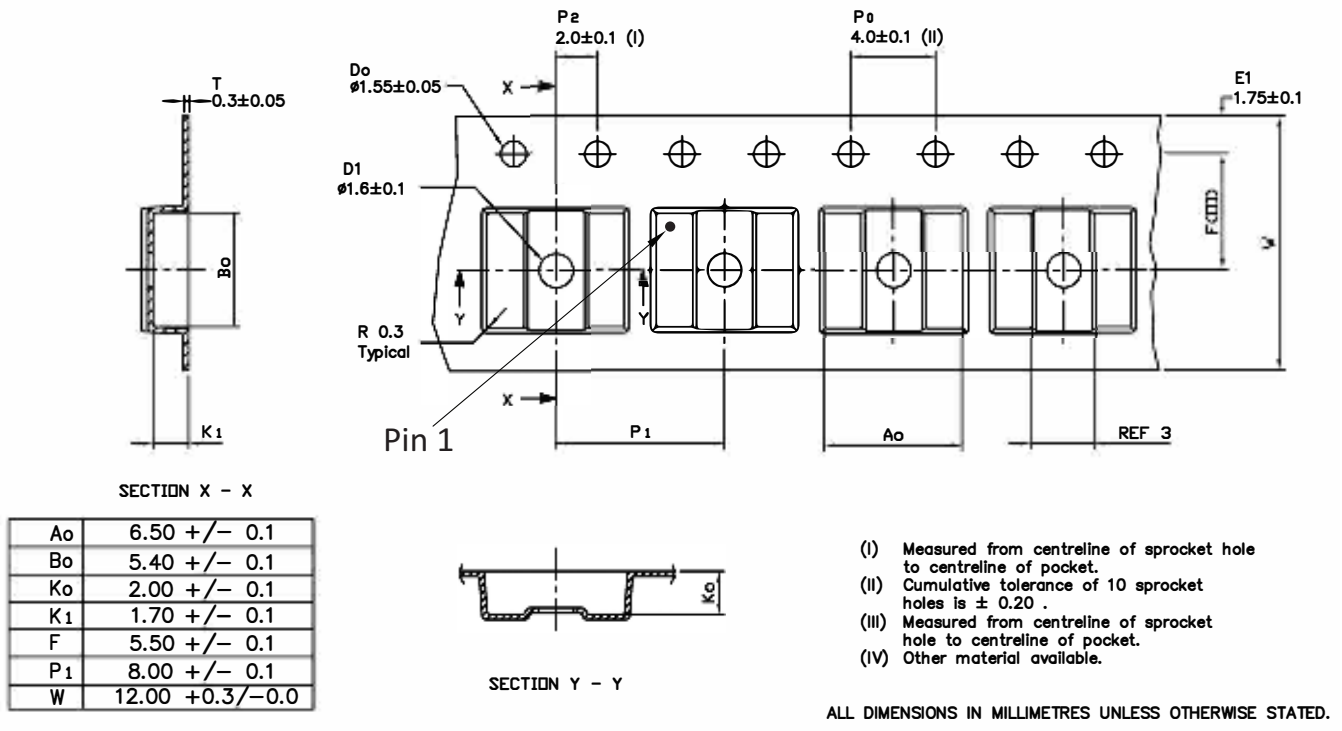
Figure 42. 8-Pin Narrow Body SOIC Land Pattern

Table 18. 8-Pin Narrow Body SOIC Land Pattern Dimensions[1,2]

Dimension	mm
C1	5.40
E	1.27
X1	0.60
Y1	1.55

1. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.
2. This land pattern design is based on IPC-7351 pattern SOIC127P600X173-8N for Density Level B (Median Land Protrusion).

5.8. 8-Pin Narrow Body SOIC Tape and Reel Information



Ao	6.50 +/– 0.1
Bo	5.40 +/– 0.1
Ko	2.00 +/– 0.1
K1	1.70 +/– 0.1
F	5.50 +/– 0.1
P1	8.00 +/– 0.1
W	12.00 +0.3/–0.0

Figure 43. Narrow Body Carrier Tape Information

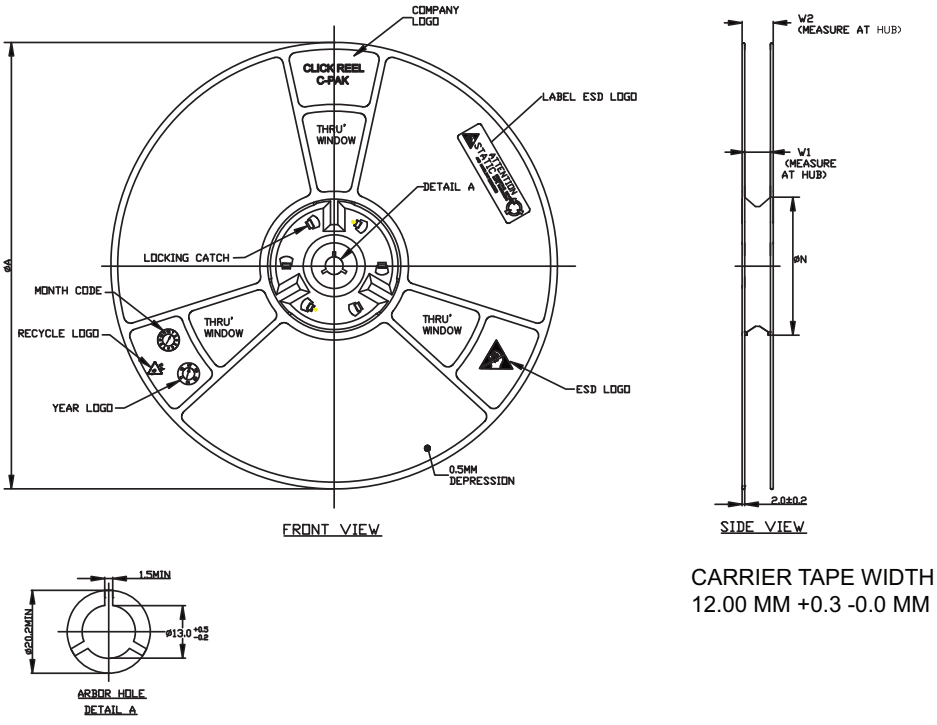


Figure 44. Narrow Body Reel Information

6. Ordering Information

6.1. Industrial and Automotive Grade Ordering Part Numbers (OPNs)

Industrial-grade devices (part numbers with an “-I” in their suffix) are built using well-controlled, high-quality manufacturing flows to ensure robustness and reliability. Qualifications are compliant with JEDEC, and defect reduction methodologies are used throughout definition, design, evaluation, qualification, and mass production steps.

Automotive-grade devices (part numbers with an “-A” in their suffix) are built using automotive-specific flows at all steps in the manufacturing process to ensure robustness and low defectivity. These devices are supported with AIAG-compliant Production Part Approval Process (PPAP) documentation, and feature International Material Data System (IMDS) and China Automotive Material Data System (CAMDS) listings. Qualifications are compliant with AEC-Q100, and a zero-defect methodology is maintained throughout definition, design, evaluation, qualification, and mass production steps.

Table 19. Si8931/32 Ordering Information

Ordering Part Number[1, 2, 3]	Automotive Ordering Part Number[1, 2, 3, 4, 5]	Ordering Options			
		Input Range	Isolation Rating	Output	Package Type
Si8931D-IS4	Si8931D-AS4	0 to 2.5 V nominal	5.0 kV_{RMS}	Differential	WB stretched SOIC-8
Si8931B-IS	Si8931B-AS	0 to 2.5 V nominal	2.5 kV_{RMS}	Differential	NB SOIC-8
Si8932D-IS4	Si8932D-AS4	0 to 2.5 V nominal	5.0 kV_{RMS}	Single-ended	WB stretched SOIC-8
Si8932B-IS	Si8932B-AS	0 to 2.5 V nominal	2.5 kV_{RMS}	Single-ended	NB SOIC-8

1. All packages are RoHS-compliant.
2. “Si” and “SI” are used interchangeably.
3. An “R” at the end of the part number denotes tape and reel packaging option.
4. Automotive-grade devices (“-A” suffix) are identical in construction materials, topside marking, and electrical parameters to their Industrial Grade (“-I suffix”) version counterparts. Automotive-Grade products are produced utilizing full automotive process flows and additional statistical process controls throughout the manufacturing flow. The Automotive-Grade part number is included on shipping labels.
5. In the top markings of each device, the Manufacturing Code represented by “TTTTTT” contains as its first character a letter in the range N through Z to indicate Automotive Grade.

7. Revision History

Revision	Date	Description

E	June, 2026	• Updated formatting.
		• Updated 3.1. "Fail-Safe and Low-Power Modes".
		  - Removed reference to low-power mode when VDDB supply is lost.
		• Removed “pending” and updated tables in 4.3. "Safety Certifications and Specifications" to reflect content required by certification bodies.
		  - Updated Table 7. "Regulatory Information".
		  - Updated Table 8. "Insulation and Safety-Related Specifications".
		  - Updated Table 9. "IEC 60664-1 Ratings".
		  - Updated Table 10. "IEC 60747-17 Insulation Characteristics".
		  - Updated Table 11. "IEC 60747-17 Safety Limiting Values".
		• Updated Table 12. "UL 1577 Insulation Characteristics".
		• Added tape and reel information.

D	October, 2023	• Updated regulatory information. • Updated Note 1 of absolute maximum table, removed not needed minimum IDD specification. • Added back in timing specifications that were inadvertently removed on previous revision.
C	May, 2023	• Updated block diagrams on page 1, Si8932 pin description, and regulatory information.
B	February, 2023	• Updated formatting. • Added new text for automotive grade products, AEC-Q100 qualification. • Added tape and reel information. • Added MSL ratings. • Updated THD specifications.
A	December, 2022	• Updated document number.
0.9	September, 2022	• Updated safety approvals on front page. • Updated minimum supply currents in 4. Electrical Specifications. • Updated 4.1. Regulatory Information.
0.8	May, 2021	• Added Automotive OPNs to ordering guide. • Updated Figure 3.1. Voltage Sense Application on page 6. • Updated Table 4.4. Absolute Maximum Ratings 1 on page 11. • Added surge voltage parameter to Table 4.8 IEC 60747-17 Insulation Characteristics on page 13. • Changed “60 mm” to “60 µm” in Solder Mask Design note in Table 6.3. 8-Pin Wide Body Stretched SOIC Land Pattern Dimensions on page 25.
0.7	December, 2019	• Updated applications and key features on front page. • Updated electrical specifications after full characterization. • Added section for automotive grade OPNs. • Updated Table 4.6. Insulation and Safety-Related Specifications on page 12. • Updated 6.6. Top Marking: 8-Pin Narrow Body SOIC. • Changed Si8932 Pin 6 from NC to GND. • Numerous clarifications throughout.
0.5	March, 2019	• Updated specifications. • Added narrow body SOIC-8 package.
0.2	May, 2018	• Corrections and clarifications.
0.1	January, 2018	Initial release.

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