DATA SHEET

Si8935/36/37 Delta-Sigma Modulator for Voltage Measurement

Applications

- Industrial, HEV and renewable energy inverters
- AC, brushless, and DC motor controls and drives
- Variable speed motor control in consumer white goods
- Isolated switch mode and UPS power supplies
- General industrial data acquisition and sensor interface
- Automotive on-board chargers, battery management systems, and charging stations

Features

- 0 to 2.5 V nominal input voltage
- Modulator clock options
  - External clock up to 25 MHz (Si8935)
  - 10 MHz internal clock (Si8936)
  - 20 MHz internal clock (Si8937)
- Typical input offset: ±0.4 mV
- Typical gain error: ±0.05%
- Excellent drift specifications
  - ±0.5 µV/°C typical offset drift
  - 9 ppm/°C typical gain drift
- Typical nonlinearity: 0.003%
- Typical SNR: 86 dB
- High common-mode transient immunity: 75 kV/µs
- Automotive-grade OPNs available
  - AEC-Q100 qualification
  - AIAG-compliant PPAP documentation support
  - IMDS and CAMDS listing support
- Compact packages
  - 8-pin wide body stretched SOIC
  - 8-pin narrow body SOIC
- –40 to 125 °C

Safety Approvals

- UL 1577 recognized
  - Up to 5000 V_{RMS} for 1 minute
- CSA certification conformity
  - 62368-1 (reinforced insulation)
- VDE certification conformity (pending)
  - 60747-17 (reinforced insulation)
- CQC certification approval
  - GB4943.1

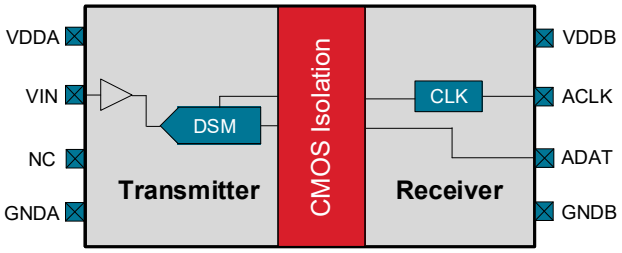


Figure 1. Si8935/36/37 Block Diagram

Description

The Si8935/36/37 are galvanically isolated delta-sigma modulators optimized for voltage sensing. Its 2.5 V input range is ideal for isolated voltage sensing applications. The Si8935/36/37 provides excellent linearity with low offset and gain drift to ensure that accuracy is maintained over the entire operating temperature range. Exceptionally high common-mode transient immunity means that the Si8935/36/37 delivers accurate measurements even in the presence of high-power switching found in motor drive systems and inverters.

The output of the Si8935/36/37 comes from a second-order, delta-sigma modulator. The modulator can be clocked either from an on-board oscillator (Si8936/37) or from an external clock (Si8935). The output is typically digitally filtered by a MCU or FPGA in the system.

The Si8935/36/37 isolated delta-sigma modulators utilize Skyworks proprietary isolation technology. It supports up to 5.0 kV_{RMS} withstand voltage per UL1577. This technology enables higher performance, reduced variation with temperature and age, tighter part-to-part matching, and longer lifetimes compared to other isolation technologies.

Automotive Grade is available for certain part numbers. These products are built using automotive-specific flows at all steps in the manufacturing process to ensure the robustness and low defectivity required for automotive applications.

Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green™*, document number SQ04–0074.

1. Pin Descriptions

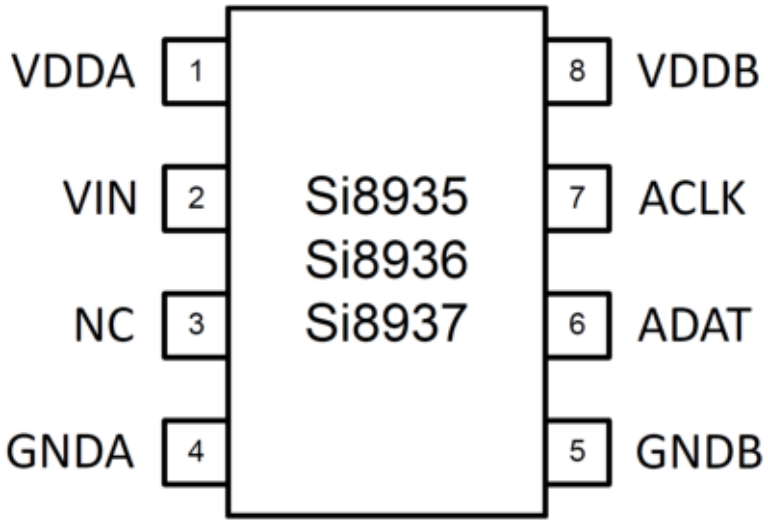


Figure 2. Si8935/36/37 Pinout (Top View)

Table 1. Si8935/36/37 Pin Descriptions

Name	Pin Number	Description
VDDA	1	Input side power supply
VIN	2	Voltage input
NC[1]	3	No connect
GNDA	4	Input side ground
GNDB	5	Output side ground
ADAT	6	Delta-sigma modulator data output
ACLK	7	Delta-sigma modulator clock (input on Si8935, output on Si8936/37)
VDDB	8	Output side power supply

1. No Connect. These pins are not internally connected. To maximize CMTI performance, these pins should be connected to the ground plane.

2. Technical Description

The input to the Si8935/36/37 is designed for 0 to 2.5 V nominal.

The analog input stage of the Si8935/36/37 is a single-ended amplifier feeding the input of a second-order, delta-sigma modulator that digitizes the input signal into a 1-bit output stream. The isolated data output ADAT pin of the converter provides a stream of digital ones and zeros that is synchronous to the ACLK pin. The Si8936/37 clock is generated internally while the Si8935 clock is provided externally. The time average of this serial bit-stream output is proportional to the analog input voltage.

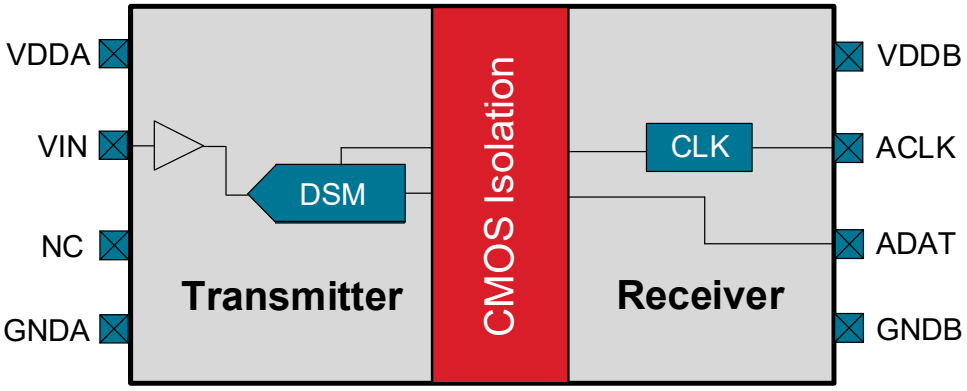


Figure 3. Si8935/36/37 Functional Block Diagram

3. Fail-Safe and Low-Power Modes

The Si8935/36/37implements a fail-safe output when the high voltage-side supply (VDDA) goes away. The fail-safe output is steady state logic 0 on ADAT for the externally clocked Si8935. The fail-safe output is a steady state logic 1 on ADAT for the internally clocked Si8936/37. The clock output ACLK of the Si8935/36/37 will stop after 256 cycles with a steady state logic 1. When the supply comes back, the clock will be turned back on and normal DSM data stream will be output in approximately 200 µs. To differentiate from the fail-safe output, a maximum nominal input signal will generate a single one every 128 bits at ADAT.

In addition to the fail-safe output, when a loss of VDDA supply occurs, the part will automatically move into a lower power mode that reduces IDDB current to approximately 1 mA. Similarly, a loss of VDDB supply will reduce IDDA current to approximately 1 mA. When the supply voltage is returned, normal operation begins in approximately 250 µs.

4. Modulator

The output of the Si8935/36/37 comes from a second-order, delta-sigma modulator like that shown in the figure below. The modulator provides 1-bit data stream whose average represents the input analog voltage. Zero volts across the inputs is represented at the output by a pulse train that has 50% ones density. Specified linear full-scale at the input (e.g., +2.25 V) produces an output data stream that has 92.87% ones density.

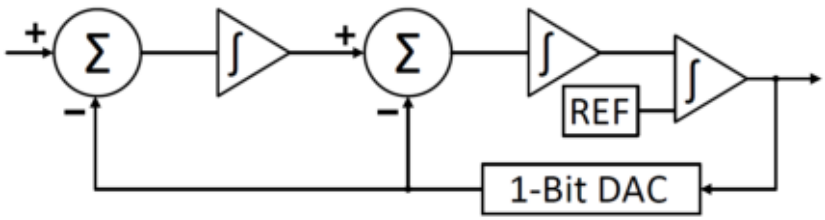


Figure 4. Typical 2nd Order Delta-Sigma Modulator Block Diagram

Table 2. Modulator Output

Single-Ended Input (V)	Bit Stream % Ones
2.25	92.87
1.125	71.44
0	50

5. Voltage Sense Application

A typical isolated voltage sensing application circuit is shown below. In this example, a high voltage is divided down to produce a voltage (VIN) within the optimum input signal range of the Si8935/36/37. Numerous alternative inputs configurations are possible with the flexibility of a high impedance input isolator. The Si8935/36/37 senses the single-ended input voltage where it is oversampled and converted into a 1-bit bitstream, then transmitted across the isolation barrier to be processed by the system controller/FPGA. If the voltage sensed is > 2.5 V, a simple voltage divider consisting of R1 and R2 can be used to scale down any voltage to fit the input range of the Si8935/36/37. R2 < 10 kΩ is recommended for best performance.

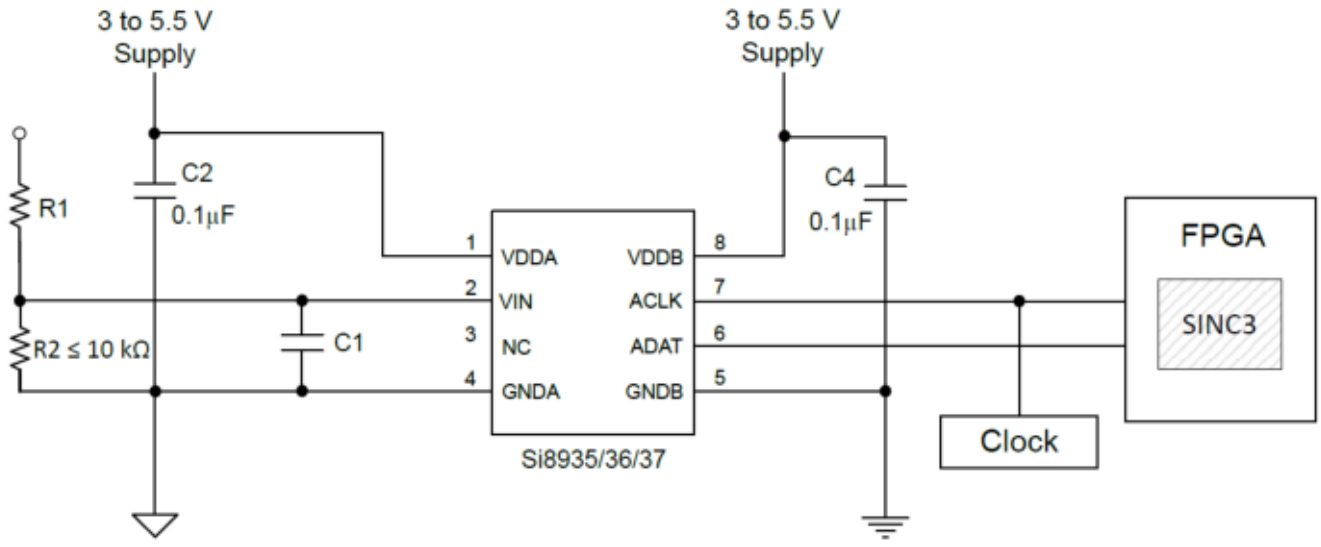


Figure 5. Voltage Sense Application

The Si8935/36/37 has intrinsic low-pass filtering at approximately 800 kHz. For applications where input filtering is required, a passive RC low-pass filter can be placed at the input pin. Consider the source resistance of the signal measured (or the parallel combination of R1 and R2 if using a voltage divider) as it should be included in the filter calculation. Capacitor C1 should be sized to make a band limiting filter at the desired frequency.

C4, the local bypass capacitor for the B-side of the Si8935/36/37, should be placed close to the VDDB supply pin with its return close to GNDB. The output signal typically goes directly to a digital filter for additional processing. The digital filter may be implemented by a dedicated FPGA in the system or may be a peripheral in the main system controller. The Si8935 expects an external clock to provide the clock signal for the modulator. That external clock can be provided by the same device that implements the digital filtering or another device that syncs both the modulator and the digital filter. The Si8936/37 generates an internal clock to the digital filter.

6. Electrical and Mechanical Specifications

The absolute maximum ratings of the Si8935/36/37 are provided below, followed by electrical specifications, performance graphs, and mechanical specifications.

Table 3. Si8935/36/37 Absolute Maximum Ratings[1]

Parameter	Symbol	Min	Max	Unit
Storage temperature	T_{STG}	–65	150	°C
Ambient temperature under bias	T_A	–40	125	°C
Junction temperature	T_J		150	°C
Supply voltage	VDDA, VDDB	–0.5	6.0	V
Input voltage respect to GNDA	VIN	–0.5	VDDA + 0.5	V
Output sink or source current	|Io|		5	mA
Total power dissipation	P_T		212	mW
Lead solder temperature (10 s)			260	°C
Human Body Model ESD rating		6000		V
Charged Device Model ESD rating		2000		V

1. Note:Exposure to maximum rating conditions for extended periods may reduce device reliability. Exceeding any of the limits listed here may result in permanent damage to the device.

ESD Handling: Industry-standard ESD handling precautions must be adhered to at all times to avoid damage to this device.

Table 4. Si8935/36/37 Electrical Specifications[1]

TA = -40 to +125 °C, SINC3 filter with 256 oversampling ratio and 20 MHz clock; typical specs at 25 °C and VDDA = VDDB = 5V unless specified otherwise

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Input side supply voltage	VDDA		3.0		5.5	V
Input supply current	IDDA	VDDA = 3.3 V		7	8.7	mA
Output side supply voltage	VDDB		3.0		5.5	V
Output supply current (si8935)	IDDB	VDDB = 3.3 V		1.8	2.7	mA
Output supply current (si8936)	IDDB	VDDB = 3.3 V		4.4	7.2	mA
Output supply current (si8937)	IDDB	VDDB = 3.3 V		6.1	11	mA
Amplifier input						
Specified linear in- put range	VIN		0.25		2.25	V
Maximum input voltage before clipping	VIN			2.5		V
Input referred offset	VOS	T_A = 25 °C, VIN = 0.25 V	–3	±0.4	3	mV
Input offset drift	VOS_T		–40	±0.5	25	µV/°C
Input impedance	RIN			500		MΩ
Dynamic Characteristics						
Gain				1		
Gain error		T_A = 25 °C	–0.15	±0.05	0.15	%
Gain error drift			–7	9	20	ppm/°C
Nonlinearity		T_A = 25 °C	–0.016	0.003	0.016	%
Nonlinearity drift			–1		1	ppm/°C
Signal-to-noise ratio	SNR	F_{IN} = 5 kHz BW = 40 kHz (Si8935/37) BW = 20 kHz (Si8936)	73	86		dB
Total harmonic distortion	THD	F_{IN} = 5 kHz BW = 40 kHz (Si8935/37) BW = 20 kHz (Si8936)		–83	–60	dB
Common-mode transient immunity	CMTI	VIN = GNDA, VCM = 1500 V	50	75		kV/µs
Power-supply rejection ratio	PSRR	VDDA at DC		–100		dB
		VDDA at 100 mV and 10 kHz ripple		–100		dB
		VDDB at DC		–100		dB
		VDDB at 100 mV and 10 kHz ripple		–100		dB
Digital						
Logic high input threshold (Si8935)	VIH		85% of VDDB			V
Logic low input threshold (Si8935)	VIL				15% of VDDB	V
Input hysteresis	VIHYST			120		mV
Output load capacitance	C_{LOAD}			15		pF
External Clock (Si8935)						
Clock frequency	FCLKIN		5		25	MHz
Duty cycle	FDUTY		45	50	55	%
Delay to data valid	TDELAY				23	ns

Table 4. Si8935/36/37 Electrical Specifications[1] (Continued)

TA = -40 to +125 °C, SINC3 filter with 256 oversampling ratio and 20 MHz clock; typical specs at 25 °C and VDDA = VDDB = 5V unless specified otherwise

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Data hold time	THOLD		6			ns
Internal Clock (si8936)						
Clock frequency	FCLKOUT	T_A = 25 ℃	9.9	10	10.1	MHz
		T_A = –40 °C to 125 °C	9.8	10	10.2	MHz
Duty cycle	FDUTY		45	50	55	%
Delay to data valid	TDELAY				60	ns
Data hold time	THOLD		40			ns
Internal Clock (Si8937)						
Clock frequency	FCLKOUT	T_A = 25 ℃	19.8	20	20.2	MHz
		T_A = –40 °C to 125 °C	19.6	20	20.4	MHz
Duty cycle	FDUTY		45	50	55	%
Delay to data valid	TDELAY				30	ns
Data hold time	THOLD		20			ns

1. Performance is guaranteed only under the conditions listed in this Table and is not guaranteed over the full operating or storage temperature ranges. Operation at elevated temperatures may reduce reliability of the device.

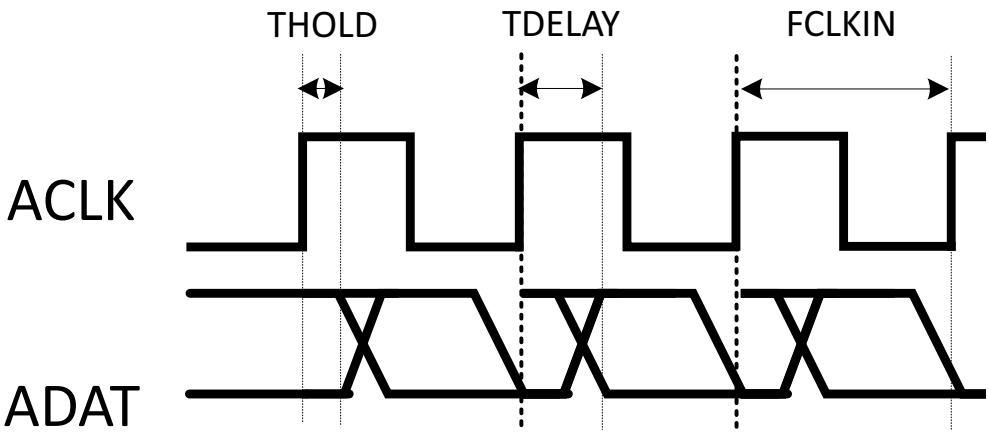


Figure 6. Si8935 Clock Input

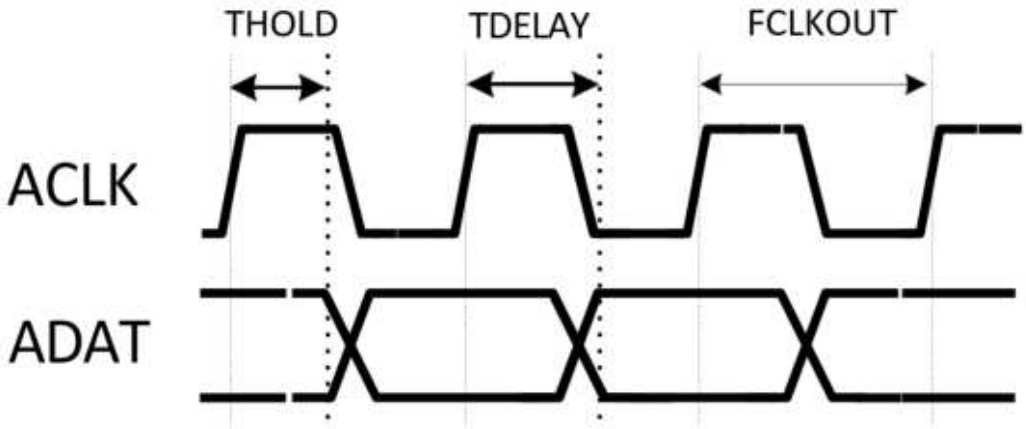


Figure 7. Si8936/37 Clock Output

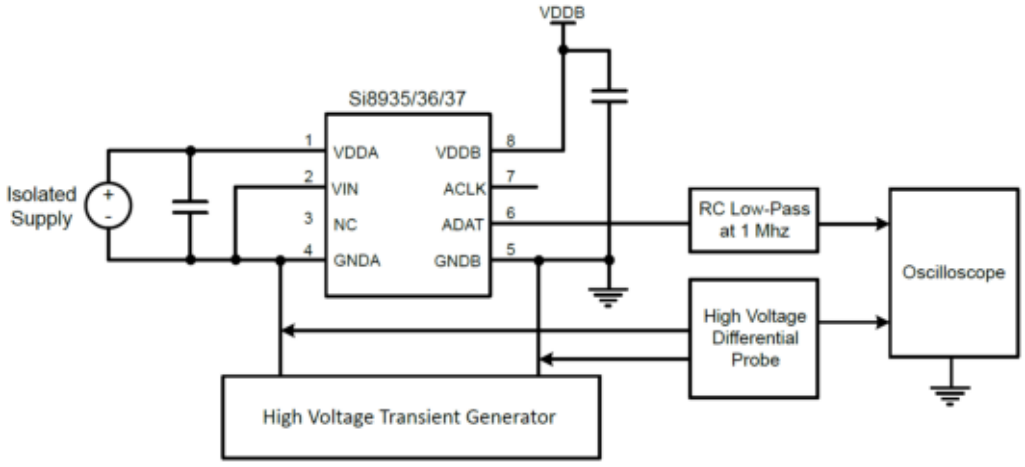


Figure 8. Common-Mode Transient Immunity Characterization Circuit

7. Typical Performance Characteristics

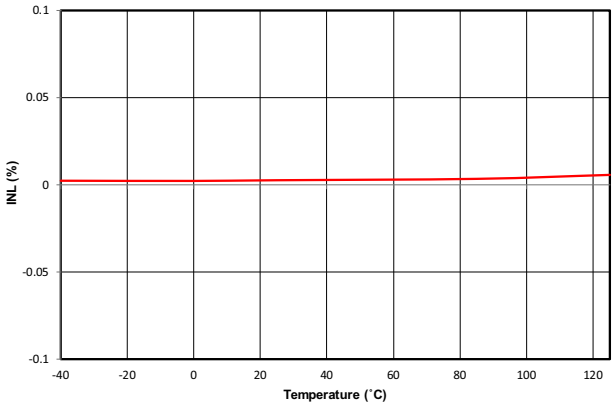


Figure 9. Si8935 Nonlinearity (%) vs. Temperature (°C)

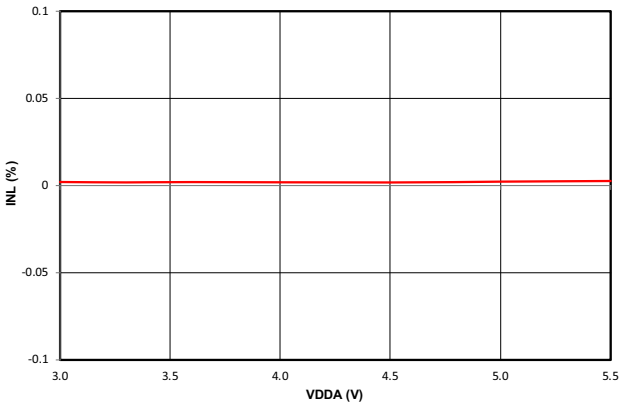


Figure 10. Si8935 Nonlinearity (%) vs. VDDA Supply (V)

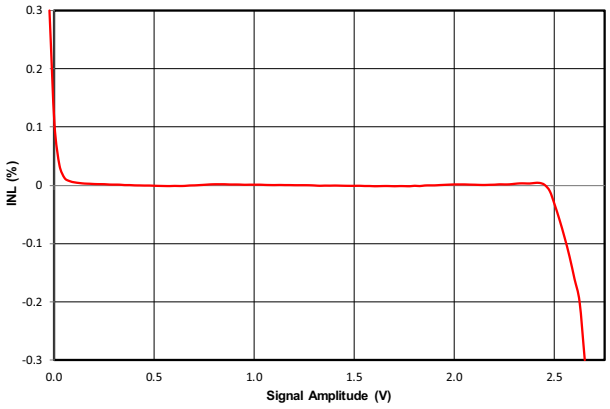


Figure 11. Si8935 Nonlinearity (%) vs. Input Signal Amplitude (mV)

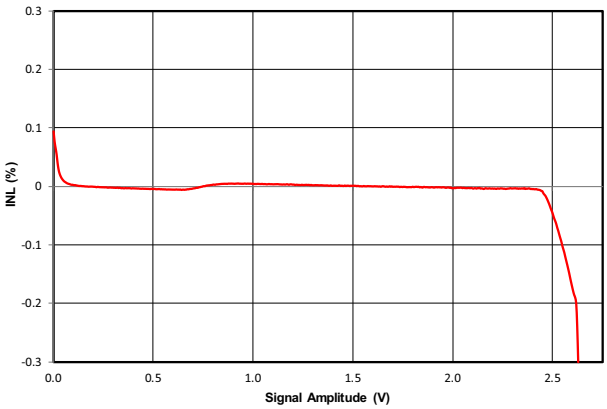


Figure 12. Si8936 Nonlinearity (%) vs. Input Signal Amplitude (mV)

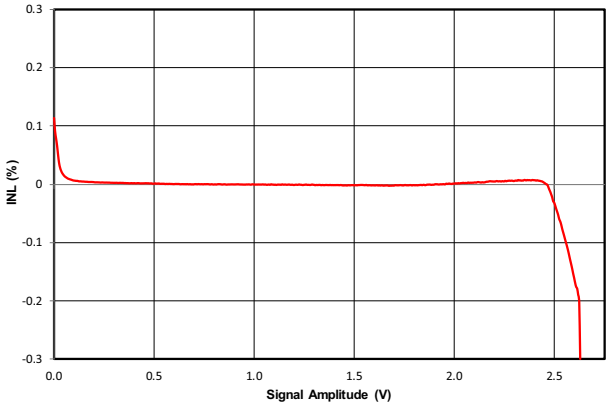


Figure 13. Si8937 Nonlinearity (%) vs. Input Signal Amplitude (mV)

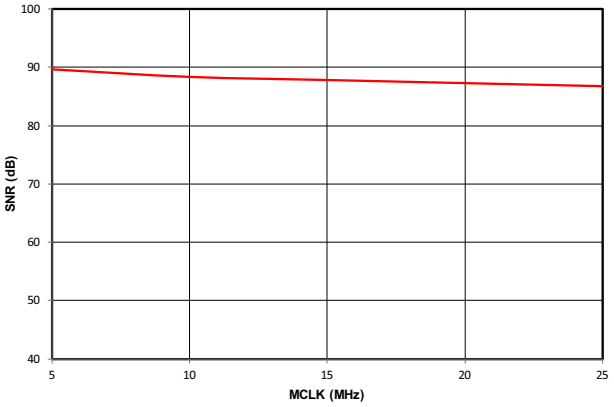


Figure 14. Si8935 Signal-to-Noise Ratio (dB) vs. MCLK (MHz)

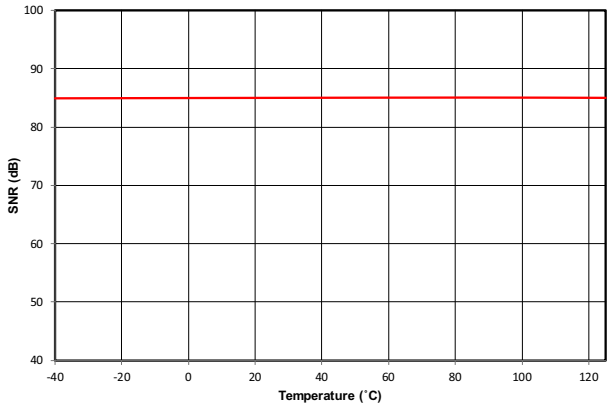


Figure 15. Si8935 Signal-to-Noise Ratio (dB) vs. Temperature (°C)

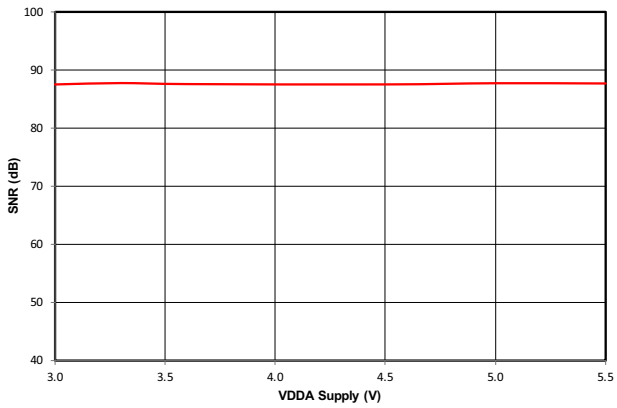


Figure 16. Si8935 Signal-to-Noise Ratio (dB) vs. VDDA Supply (V)

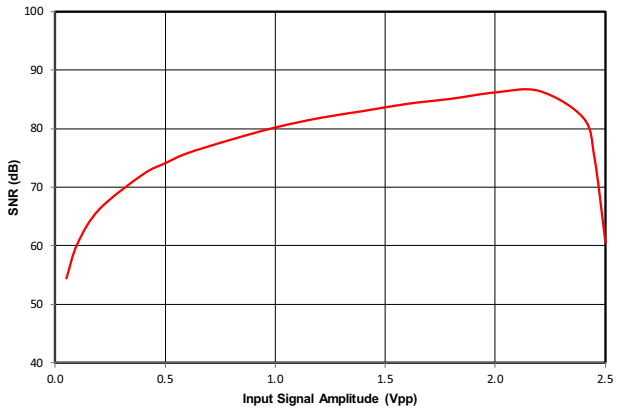


Figure 17. Si8935 Signal-to-Noise Ratio (dB) vs. Input Signal Amplitude (mV)

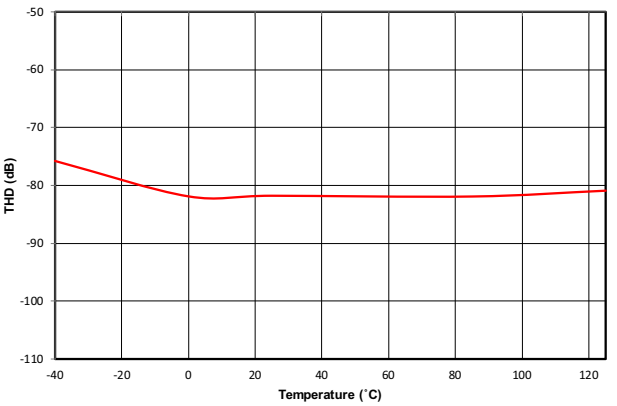


Figure 18. Si8935 Toal Harmonic Distortion (dB) vs. Temperature (°C)

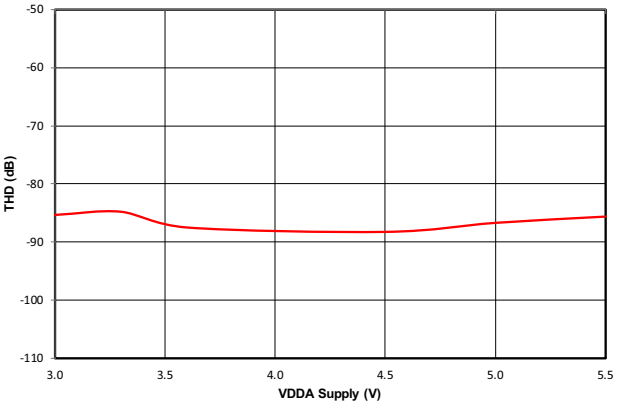


Figure 19. Si8935 Total Harmonic Distortion (dB) vs. VDDA Supply (V)

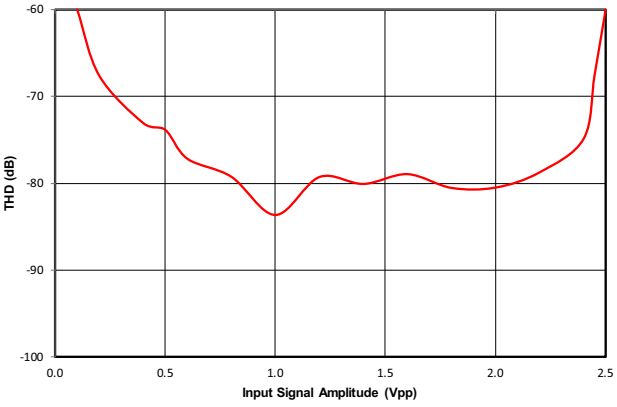


Figure 20. Si8935 Total Harmonic Distortion (dB) vs. Input Signal Amplitude (mV)

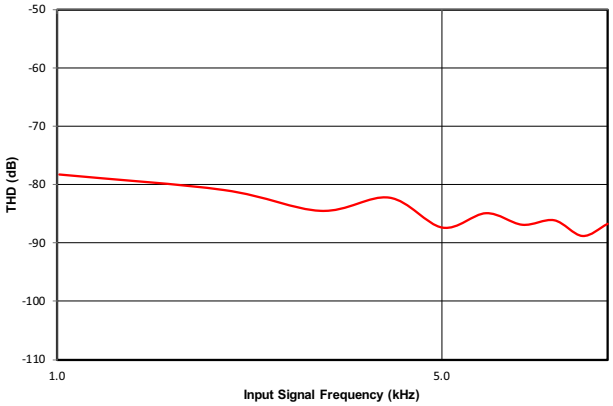


Figure 21. Si8935 Total Harmonic Distortion (dB) vs. Input Signal Frequency (kHz)

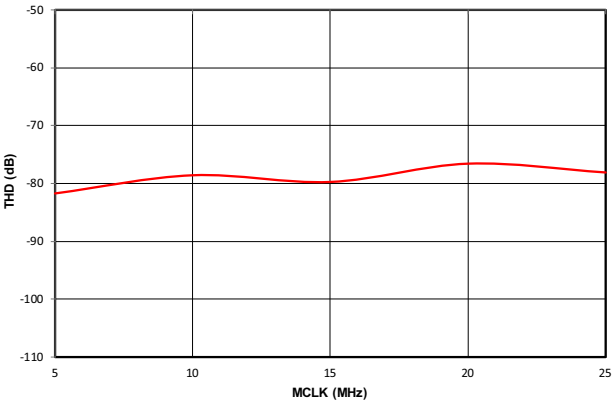


Figure 22. Si8935 Total Harmonic Distortion (dB) vs. MCLK (MHz)

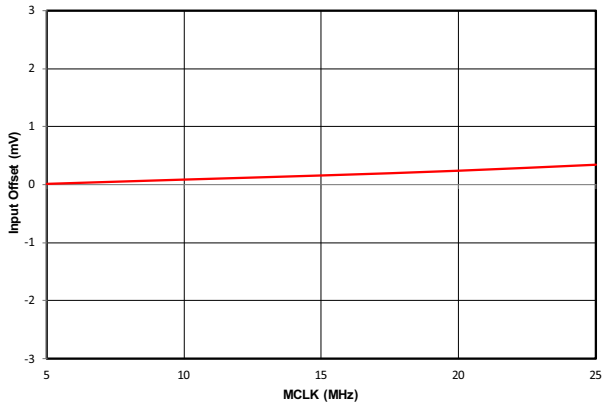


Figure 23. Si8935 Input Offset (mV) vs. MCLK (MHz)

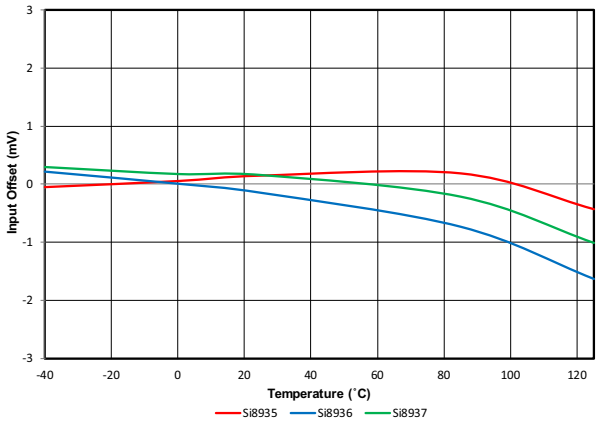


Figure 24. Input Offset (mV) vs. Temperature (°C)

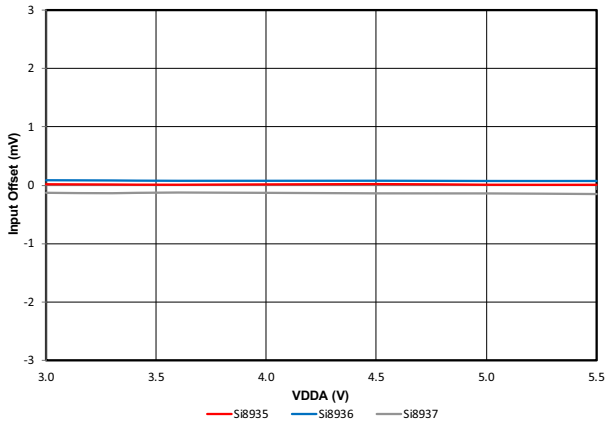


Figure 25. Input Offset (mV) vs. VDD Supply (V)

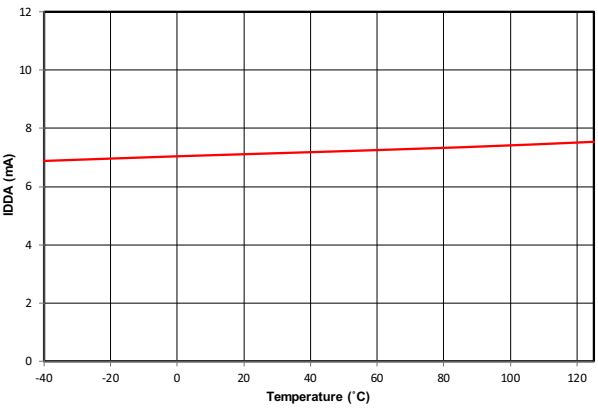


Figure 26. Si8935/36/37 IDDA (mA) vs. Temperature (°C)

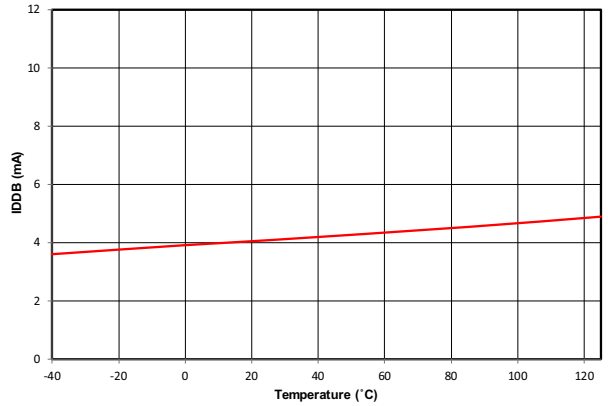


Figure 27. Si8935 IDDB (mA) vs. Temperature (°C)

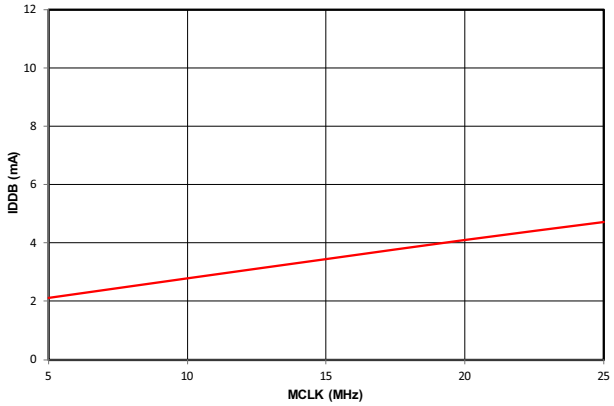


Figure 28. Si8935 IDDB (mA) vs. MCKL (MHz)

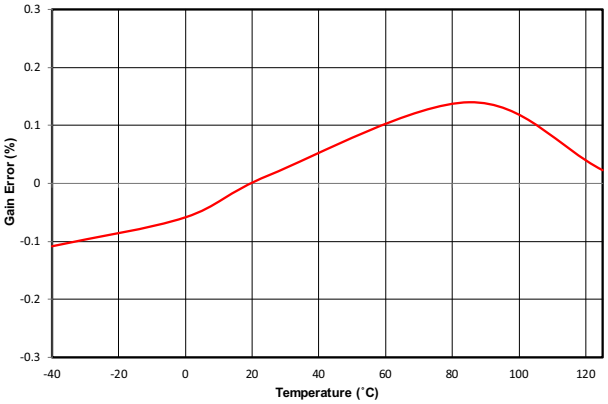


Figure 29. Si8935 Gain Error (%) vs. Temperature (°C)

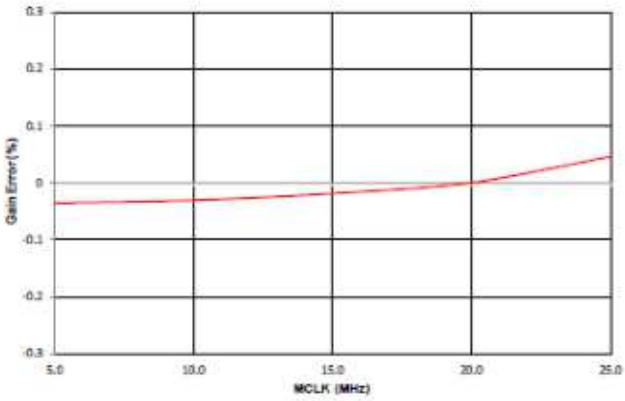


Figure 30. Si8935 Gain Error (%) vs. MCLK (MHz)

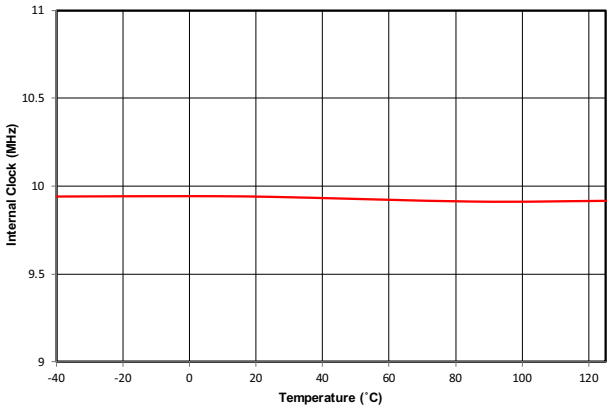


Figure 31. Si8936 Internal Clock Frequency (MHz) vs. Temperature (°C)

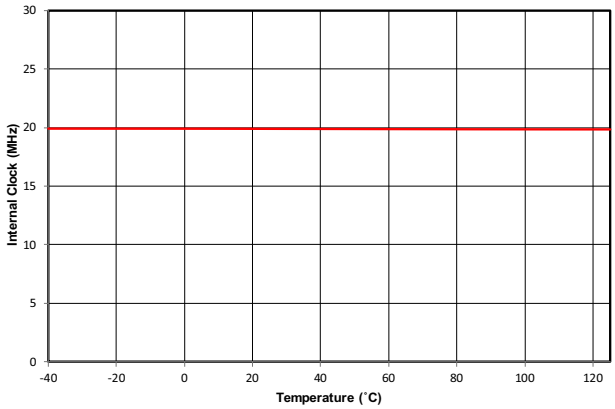


Figure 32. Si8937 Internal Clock Frequency (MHz) vs. Temperature (°C)

Figure 33. Si8932 High-to-Low Step Response

8. Safety Certifications and Specifications

Table 5. Regulatory Information[1]

CSA
The Si8935/36/37 is certified under CSA. For more details, see Master Contract File 232873.
62368-1: Up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
VDE
The Si8935/36/37 is certified under VDE. For more details, see File 5028467.
60747-17: Up to 2121 V_{peak} for reinforced insulation working voltage.
UL
The Si8935/36/37 is certified under UL1577 component recognition program. For more details, see File E257455.
Rated up to 5000 V_{RMS} V_{ISO} isolation voltage for basic protection.
CQC
The Si8935/36/37 is certified under GB4943.1.
Rated up to 250 V_{RMS} reinforced insulation working voltage at 5000 meters tropical climate.

1. For more information, see Section 10. Ordering Information

Table 6. Insulation and Safety-Related Specifications

Parameter	Symbol	Test Condition	Value		Unit
			WB Stretched SOIC-8	NB SOIC-8	
Nominal external air gap (clearance)	CLR		8.0	4.0	mm
Nominal external tracking (creepage)	CRP		8.0	4.0	mm
Minimum internal gap (internal clearance)	DTI		0.036	0.036	mm
Tracking resistance	PTI or CTI	IEC60112	600	600	V_{RMS}
Erosion depth	ED		0.04	0.04	mm
Resistance (input-output)[1]	R_{IO}	Test voltage = 500 V, 25 °C	10^{12}	10^{12}	Ω
Capacitance (input-output)[1]	C_{IO}	f = 1 MHz	1	1	pF

1. To determine resistance and capacitance, the Si8935/36/37 is converted into a two-terminal device. Pins 1 to 4 are shorted together to form the first terminal, and pins 5 to 8 are shorted together to form the second terminal. The parameters are then measured between these two terminals.

Table 7. IEC 60664-1 Ratings

Parameter	Test Conditions	Specification	
		WB Stretched SOIC-8	NB SOIC-8
Material group		I	I
Overvoltage category	Rated mains voltage ≤150 V_{RMS}	I-IV	I-IV
	Rated mains voltage ≤300 V_{RMS}	I-IV	I-III
	Rated mains voltage ≤600 V_{RMS}	I-IV	I-II
	Rated mains voltage ≤1000 V_{RMS}	I-III	I

Table 8. IEC 60747-17 Insulation Characteristics[1]

Parameter	Symbol	Test Condition	Characteristic		Unit
			WB Stretched SOIC-8	NB SOIC-8	
Maximum working isolation voltage	V_{IOWM}	According to Time-Dependent Dielectric Breakdown (TDDB) Test	1500	445	V_{RMS}
Maximum repetitive isolation voltage	V_{IORM}	According to Time-Dependent Dielectric Breakdown (TDDB) Test	2121	630	V_{peak}
Apparent charge	q_{pd}	Method b: At routine test (100% production) and preconditioning (type test); V_{ini} = 1.2 x V_{IOTM}, t_{ini} = 1 s; $V_{pd(m)}$ = 1.875 x V_{IORM}, t_m = 1 s (method b1) or $V_{pd(m)}$ = V_{ini}, t_m = t_{ini} (method b2)	≤5	≤5	pC
Maximum transient isolation voltage	V_{IOTM}	V_{TEST} = V_{IOTM}, t = 60 s (qualification); V_{TEST} = 1.2 x V_{IOTM}, t = 1 s (100% production)	7070	3535	V_{peak}
Maximum surge isolation voltage	V_{IOSM}	Tested in oil with 1.3 x V_{IMP} or 10 kV minimum and 1.2 µs/50 µs profile	10400	10400	V_{peak}
Maximum impulse voltage	V_{IMP}	Tested in air with 1.2 µs/50 µs profile	8000	5000	V_{peak}
Isolation resistance	R_{IO_S}	T_{AMB} = T_S, V_{IO} = 500 V	$>10^9$	$>10^9$	Ω
Pollution degree			2	2	
Climatic category			40/125/21	40/125/21	

1. This coupler is suitable for “safe electrical insulation” only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

Table 9. UL 1577 Insulation Characteristics

Parameter	Symbol	Test Condition	Characteristic		Unit
			WB Stretched SOIC-8	NB SOIC-8	
Maximum withstanding isolation voltage	V_{ISO}	V_{TEST} = V_{ISO}, t = 60 s (qualification); V_{TEST} = 1.2 x V_{ISO}, t = 1 s (100% production)	5000	2500	V_{RMS}

Table 10. IEC 60747-17 Safety Limiting Values[1]

Parameter	Symbol	Test Condition	Characteristic	Unit
Safety temperature	T_S		150	°C
Safety input, output or supply current (WB stretched SOIC-8)	I_S	θ_{JA} = 90 °C/W V_{DD} = 5.5 V T_J = 150 °C T_A = 25 °C	253	mA
		θ_{JA} = 90 °C/W V_{DD} = 3.6 V T_J = 150 °C T_A = 25 °C	386	mA
Safety input, output or supply current (NB SOIC-8)	I_S	θ_{JA} = 112 °C/W V_{DD} = 5.5 V T_J = 150 °C T_A = 25 °C	203	mA
		θ_{JA} = 112 °C/W V_{DD} = 3.6 V T_J = 150 °C T_A = 25 °C	310	mA
Safety input, output or total power (WB stretched SOIC-8)	P_S	θ_{JA} = 90 °C/W T_J = 150 °C T_A = 25 °C	1389	mW
Safety input, output or total power (NB SOIC-8)	P_S	θ_{JA} = 112 °C/W T_J = 150 °C T_A = 25 °C	1116	mW

1. Maximum value allowed in the event of a failure. Refer to the derating curves Figure 34, "WB Stretched SOIC-8 Thermal Derating Curve (Dependence of Safety Limiting Current)," on page 16 and Figure 35, "NB SOIC-8 Thermal Derating Curve (Dependence of Safety Limiting Current)," on page 16.

Table 11. Thermal Characteristics

Parameter	Symbol	WB Stretched SOIC-8	NB SOIC-8	Unit
IC Junction-to-air thermal resistance	θ_{JA}	90	112	°C/W

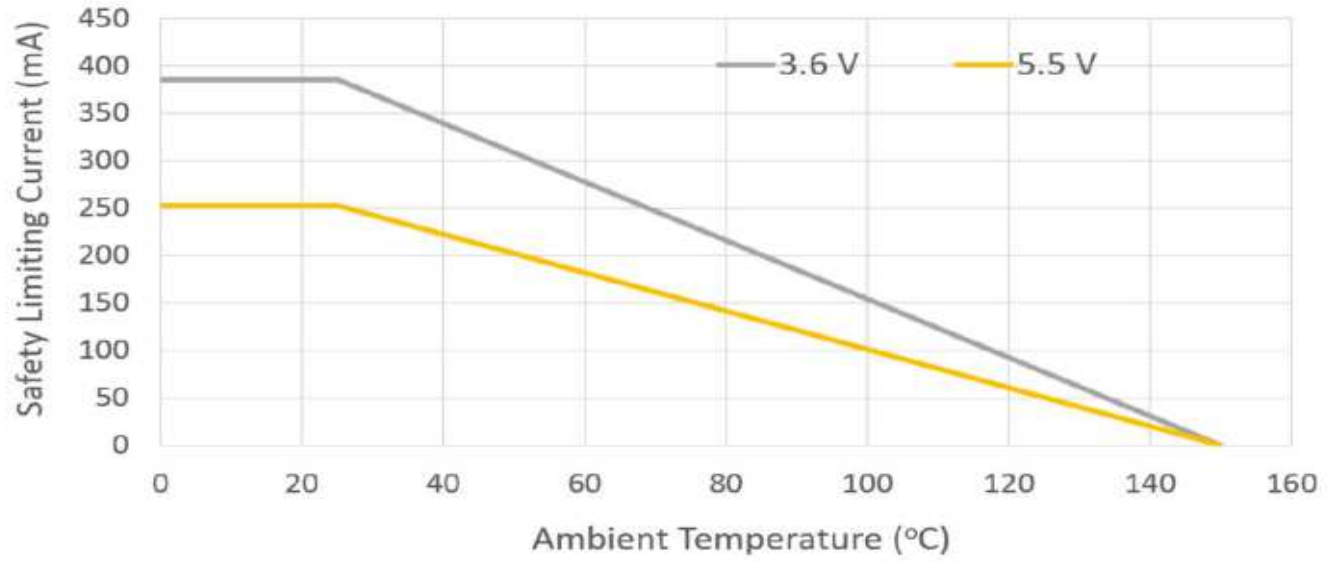


Figure 34. WB Stretched SOIC-8 Thermal Derating Curve (Dependence of Safety Limiting Current)

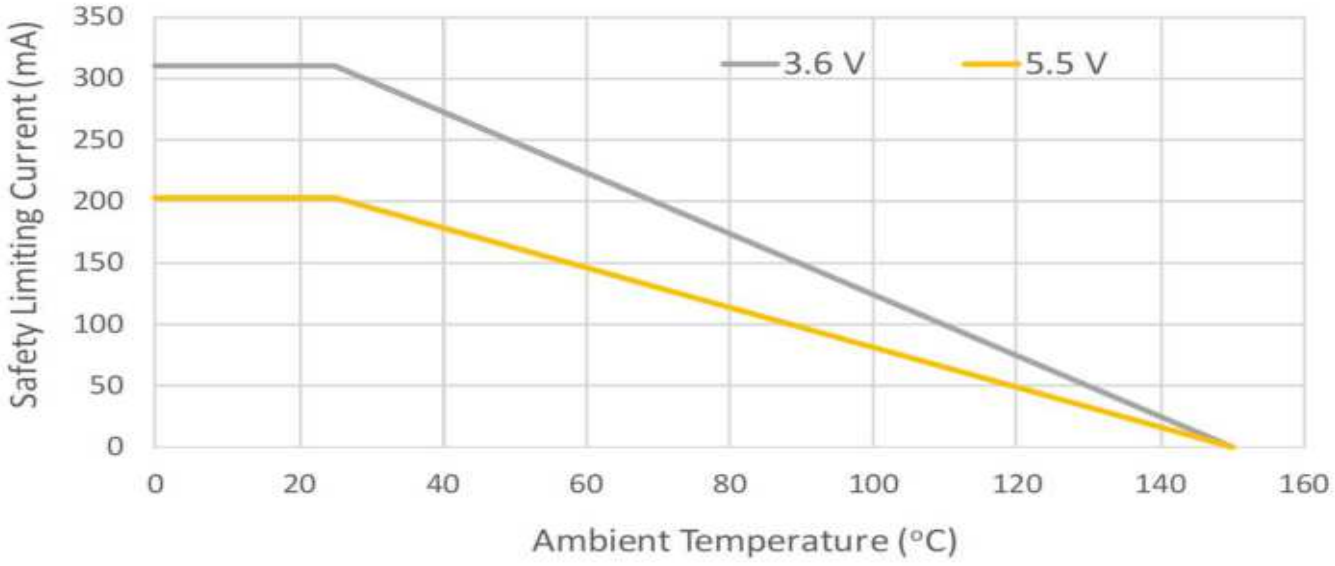


Figure 35. NB SOIC-8 Thermal Derating Curve (Dependence of Safety Limiting Current)

9. Package and Handling Information

Since the device package is sensitive to moisture absorption, it is baked and vacuum packed before shipping. Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The Si8935D-IS4, Si8936D-IS4, Si8937D-IS4, Si8935D-AS4, Si8936D-AS4, and Si8937D-AS4 are rated to Moisture Sensitivity Level 2A (MSL2A) at 260°C, while the Si8935B-IS, Si8936B-IS, Si8937B-IS, Si8935B-AS, Si8936B-AS, and Si8937B-AS are rated to MSL2 at 260°C.

They can be used for lead or lead-free soldering. For additional information, refer to Skyworks Application Note, “PCB Design and SMT Assembly/Rework Guidelines,” Document Number 101752.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Refer to Standard SMT Reflow Profiles: JEDEC Standard J-STD-020.

9.1. Package Outline: 8-Pin Wide Body Stretched SOIC

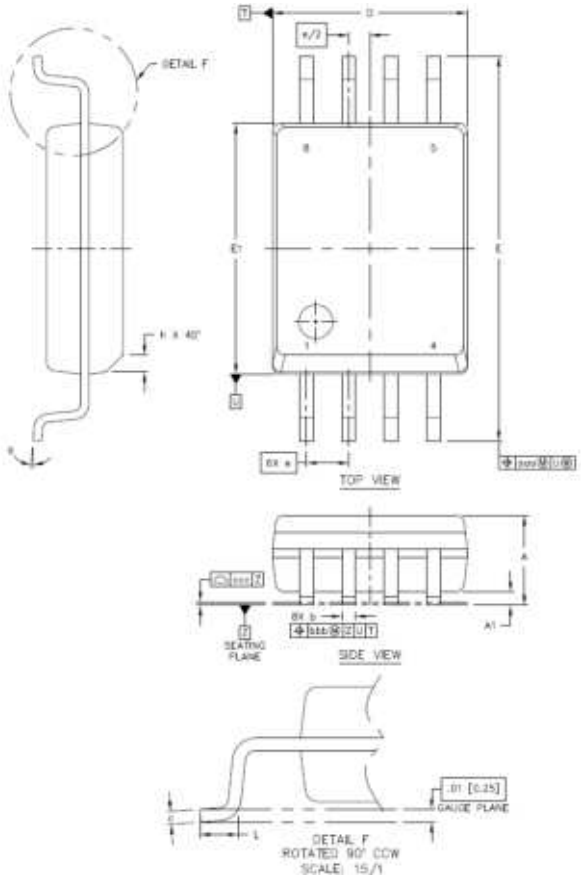


Figure 36. 8-Pin Wide Body Stretched SOIC Package

Table 12. 8-Pin Wide Body Stretched SOIC Package Dimensions

Dimension	Millimeters		Notes
	Min	Max	
A	2.49	2.79	All dimensions shown are in millimeters (mm) unless otherwise noted. Dimensioning and tolerancing per ANSI Y14.5M-1994. Recommended reflow profile per JEDEC J-STD-020C specification for small body, lead-free components.
A1	0.36	0.46	
b	0.30	0.51	
c	0.20	0.33	
D	5.74	5.94	
E	11.25	11.76	
E1	7.39	7.59	
e	1.27 BSC		
L	0.51	1.02	
h	0.25	0.76	
θ	0°	8°	
aaa		0.25	
bbb		0.25	
ccc		0.10	

9.2. Land Pattern: 8-Pin Wide Body Stretched SOIC

9.2.1. General Guidelines

1. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a fabrication allowance of 0.05 mm.
2. This land pattern design is based on the IPC-7351 guidelines.

9.2.2. Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD).
2. Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

9.2.3. Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pins.

9.2.4. Card Assembly

1. A No-clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

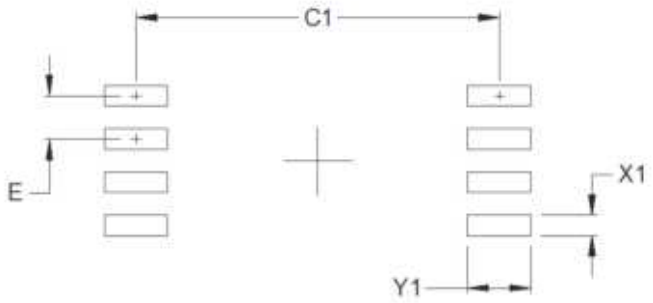


Figure 37. 8-Pin Wide Body Stretched SOIC Land Pattern

Table 13. 8-Pin Wide Body Stretched SOIC Land Pattern Dimensions[1]

Dimension	(mm)
C1	10.60
E	1.27
X1	0.60
Y1	1.85

1. See General Guidelines

9.3. Top Marking: 8-Pin Wide Body Stretched SOIC

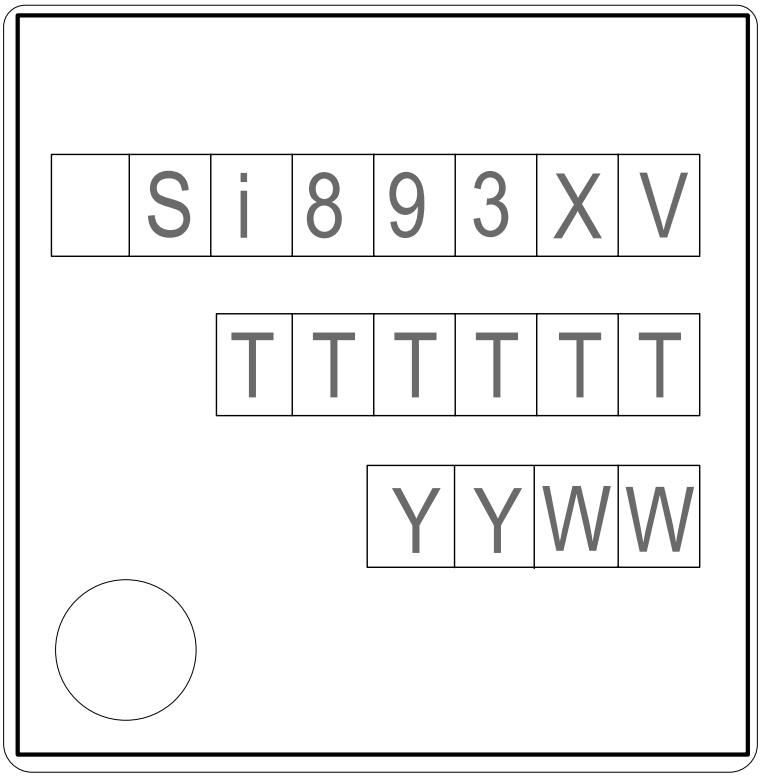
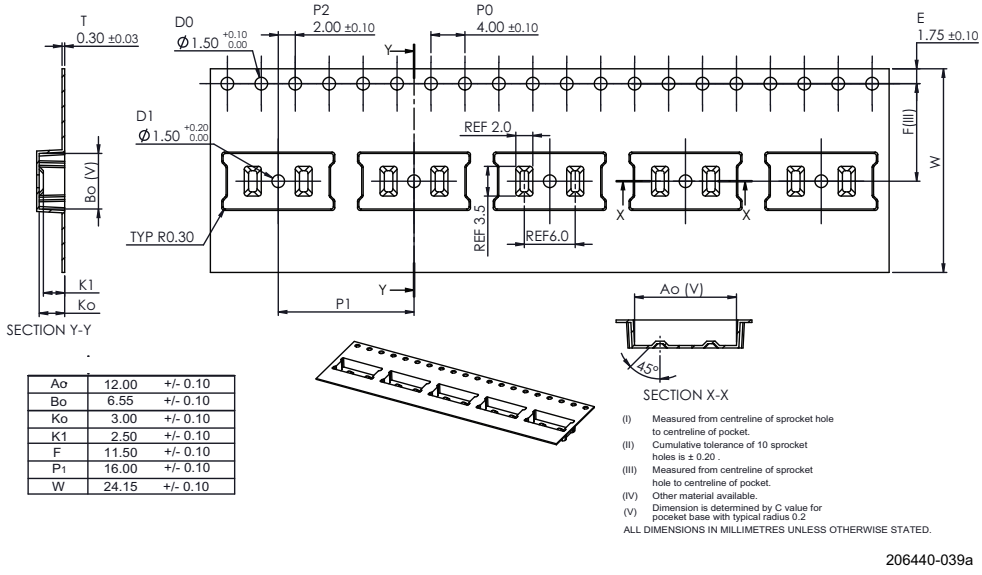


Figure 38. Si8935/36/37 Typical Package Marking, 8-Pin Wide Body Stretched SOIC

Table 14: 8-Pin Wide Body Stretched SOIC Top Marking Explanation

Line 1	Part Number	Si893x X = Base part number 5 = External clock 6 = Internal 10 MHz clock 7 = Internal 20 MHz clock V = Insulation rating: D = 5.0 kV_{RMS}
Line 2	TTTTTT	Manufacturing Code
Line 3	YY = Year WW = Work Week Circle = 43 mils diameter left justified	Year and work week

9.4. Tape and Reel Information: 8-Pin Wide Body Stretched SOIC



Ao	12.00	+/- 0.10
Bo	6.55	+/- 0.10
Ko	3.00	+/- 0.10
K1	2.50	+/- 0.10
F	11.50	+/- 0.10
P1	16.00	+/- 0.10
W	24.15	+/- 0.10

Figure 39. Wide Body Carrier Tape Information

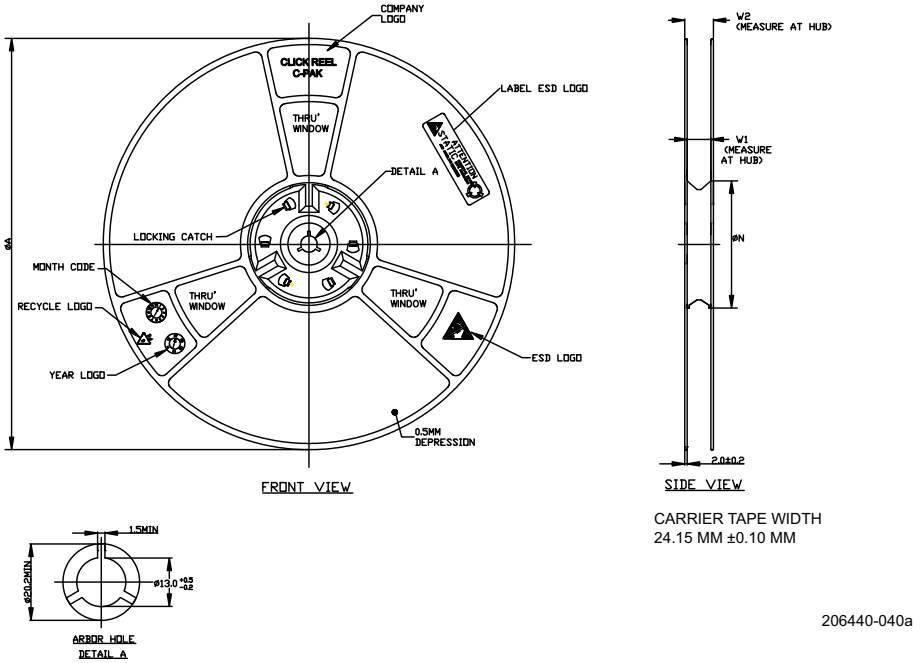


Figure 40. Wide Body Reel Information

9.5. Package Outline: 8-Pin Narrow Body SOIC

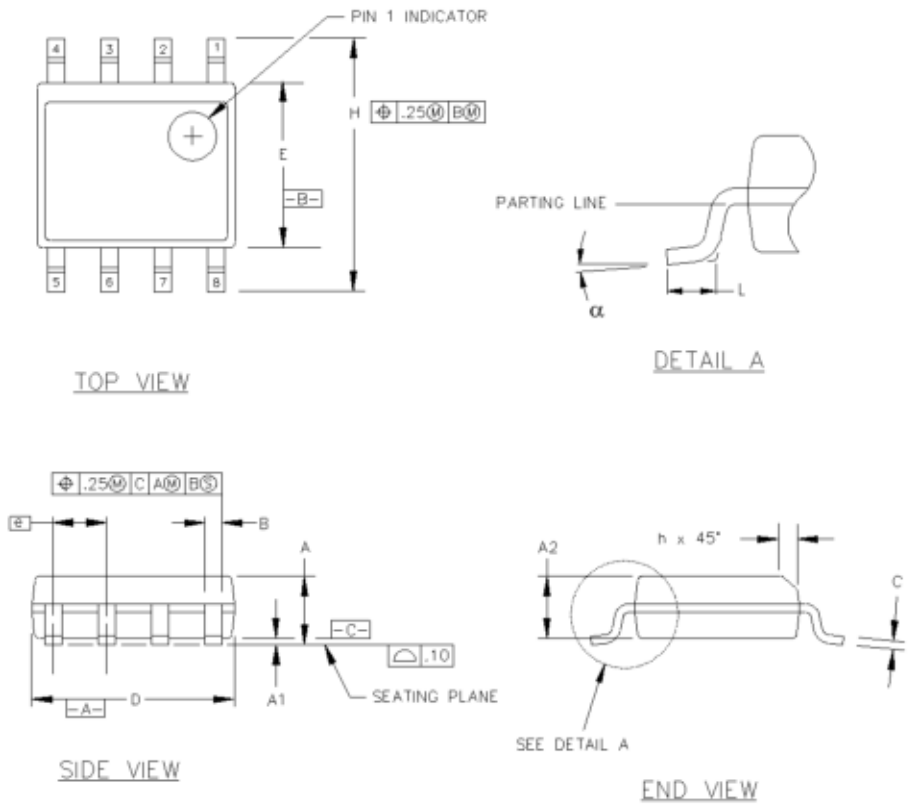


Figure 41. 8-Pin Narrow Body SOIC Package

Table 15. 8-Pin Narrow Body SOIC Package Dimensions

Dimension	Millimeters		Notes
	Min	Max	
A	1.35	1.75	All dimensions shown are in millimeters (mm) unless otherwise noted. Dimensioning and tolerancing per ANSI Y14.5M-1982. This drawing conforms to JEDEC Outline MS-012. Recommended card reflow profile is per the JEDEC/IPC J-STD-020B specification for small body components.
A1	0.10	0.25	
A2	1.40 REF	1.55 REF	
B	0.33	0.51	
C	0.19	0.25	
D	4.80	5.00	
E	3.80	4.00	
e	1.27 BSC		
H	5.80	6.20	
h	0.25	0.50	
L	0.40	1.27	
α	0°	8°	

9.6. Land Pattern: 8-Pin Narrow Body SOIC

9.6.1. General Guidelines

1. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.
2. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X173-8N for Density Level B (Median Land Protrusion).

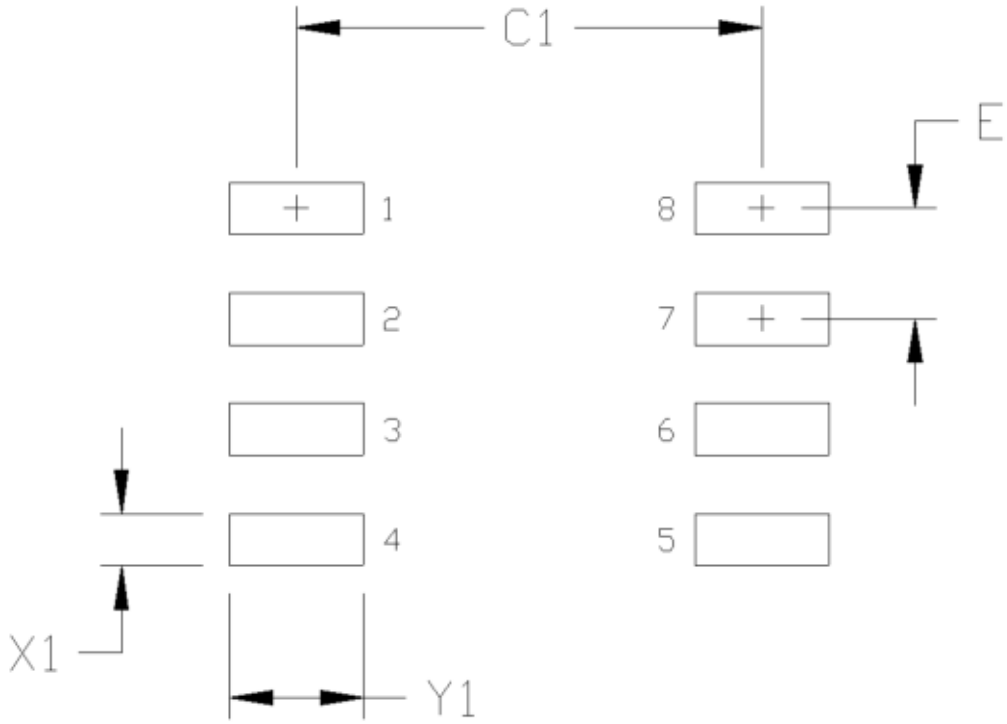


Figure 42. 8-Pin Narrow Body SOIC Land Pattern

Table 16. 8-Pin Narrow Body SOIC Land Pattern Dimensions[1]

Dimension	mm
C1	5.40
E	1.27
X1	0.60
Y1	1.55

1. See General Guidelines

9.7. Top Marking: 8-Pin Narrow Body SOIC

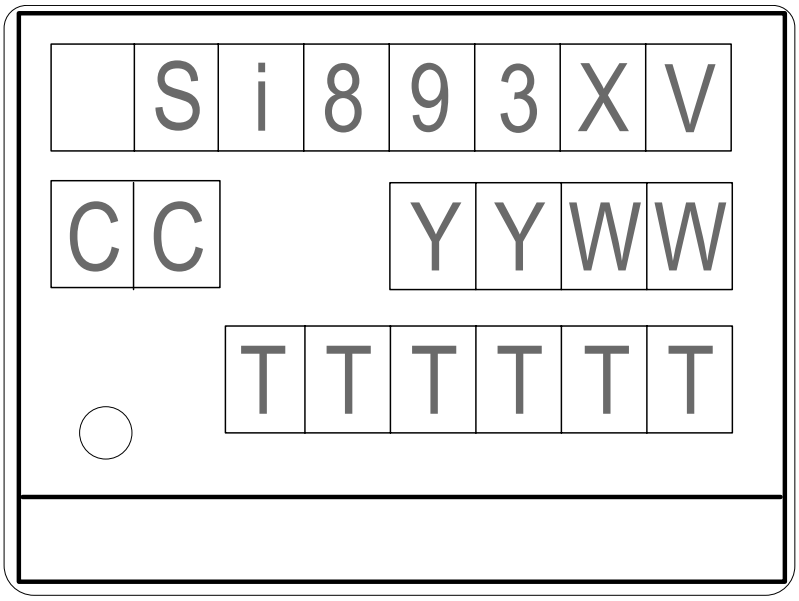
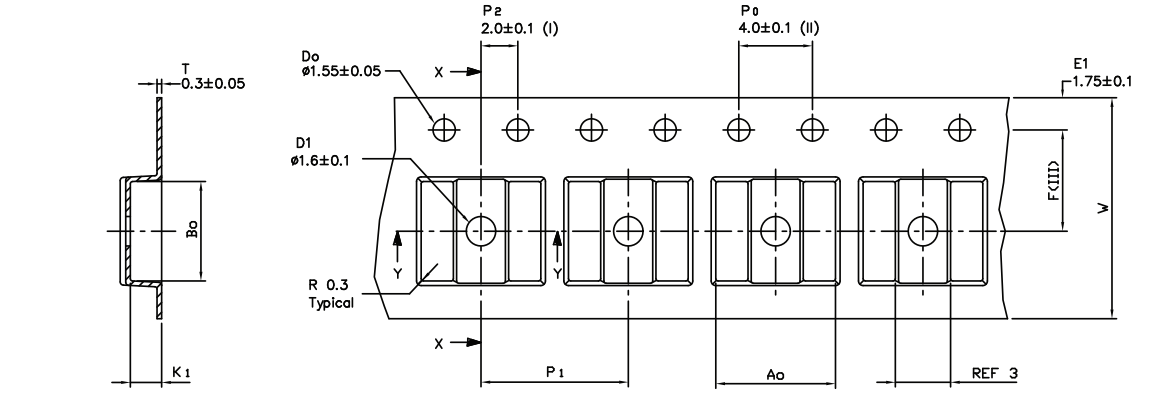


Figure 43. Si8935/36/37 Typical Package Marking, 8-Pin Narrow Body SOIC

Table 17. 8-Pin Narrow Body SOIC Top Marking Explanation

Line 1	Part Number	Si893x X = Base part number 5 = External clock 6 = Internal 10 MHz clock 7 = Internal 20 MHz clock V = Insulation rating B = 2.5 kV_{RMS}
Line 2	CC = Country of origin ISO code abbreviation	
	YY = Year WW = Work Week	Year and work week
Line 3	TTTTTT = Manufacturing code Circle = 19.7 mils diameter left justified	Manufacturing code

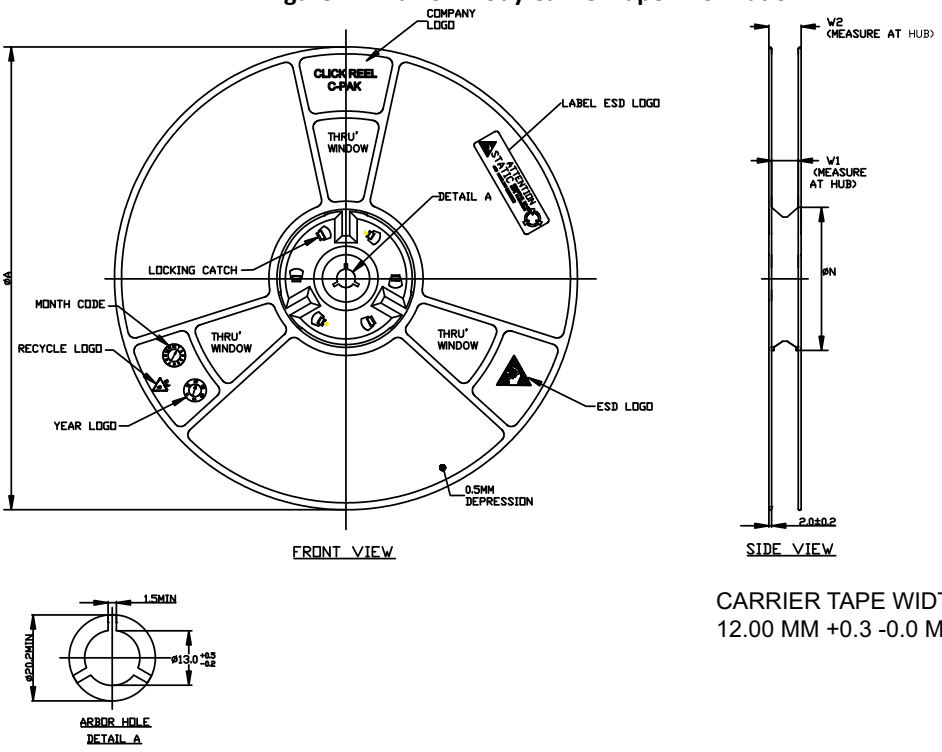
9.8. Tape and Reel Information: Narrow Body



Ao	6.50 +/– 0.1
Bo	5.40 +/– 0.1
Ko	2.00 +/– 0.1
K1	1.70 +/– 0.1
F	5.50 +/– 0.1
P1	8.00 +/– 0.1
W	12.00 +0.3/–0.0

206440-044a

Figure 44. Narrow Body Carrier Tape Information



206440-045

Figure 45. Narrow Body Reel Information

10. Ordering Information

10.1. Industrial and Automotive Grade Ordering Part Numbers (OPNs)

Industrial-grade devices (part numbers with an "-I" in their suffix) are built using well-controlled, high-quality manufacturing flows to ensure robustness and reliability. Qualifications are compliant with JEDEC, and defect reduction methodologies are used throughout definition, design, evaluation, qualification, and mass production steps.

Automotive-grade devices (part numbers with an "-A" in their suffix) are built using automotive-specific flows at all steps in the manufacturing process to ensure robustness and low defectivity. These devices are supported with AIAG-compliant Production Part Approval Process (PPAP) documentation, and feature International Material Data System (IMDS) and China Automotive Material Data System (CAMDS) listings. Qualifications are compliant with AEC-Q100, and a zero-defect methodology is maintained throughout definition, design, evaluation, qualification, and mass production steps.

Table 18. Si8935-36-37 Ordering Guide[1, 2, 3, 4]

Ordering Part Number (OPN)	Automotive OPN[5]	Ordering Options		
		Isolation Rating	Clock	Package Type
Si8935D-IS4	Si8935D-AS4	5.0 kVrms	Input	WB Stretched SOIC-8
Si8935B-IS	Si8935B-AS	2.5 kVrms	Input	NB SOIC-8
Si8936D-IS4	Si8936D-AS4	5.0 kVrms	10 MHz output	WB Stretched SOIC-8
Si8936B-IS	Si8936B-AS	2.5 kVrms	10 MHz output	NB SOIC-8
Si8937D-IS4	Si8937D-AS4	5.0 kVrms	20 MHz output	WB Stretched SOIC-8
Si8937B-IS	Si8937B-AS	2.5 kVrms	20 MHz output	NB SOIC-8

1. All packages are RoHS-compliant.
2. "Si" and "SI" are used interchangeably.
3. An "R" at the end of the part number denotes tape and reel packaging option.
4. In the top markings of each device, the Manufacturing Code represented by "TTTTTT" contains as its first character a letter in the range N through Z to indicate Automotive Grade.
5. Automotive-Grade devices ("-A") suffix) are identical in construction materials, topside marking, and electrical parameters to their Industrial-Grade ("-I" suffix) version counterparts. Automotive-Grade products are produced utilizing full automotive process flows and additional statistical process controls throughout the manufacturing flow. The Automotive-Grade part number is included on shipping labels.

Revision History

Revision C

October 2, 2023

Updated regulatory information, updated absolute maximum note 1, and removed unneeded minimum

IDD specifications.

Revision B

May, 2023

Re-formatted to new standards. Added new text for Automotive Grade products, AEC-Q100 qualification, updated regulatory information, added tape and reel information, and added MSL ratings.

Revision 206440A

December, 2022

Updated decimal-based revision number to alphanumeric code.

Revision 0.8

September, 2022

Updated Safety Approvals, minimum supply currents in Electrical Specifications, and Regulatory Information.

Revision 0.7

April, 2021

Updated Applications and Key Features, added Automotive OPNs to Ordering Guide, updated Insulation and Safety-Related Specifications, Electrical Specifications after full characterization, updated narrow body top marking, and numerous clarifications throughout.

Revision 0.1

March, 2019

Initial release.

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