

Low-Power, Highly-Integrated, Programmable 16-Bit, 26-KSPS, Dual-Channel CODEC

FEATURES

- Stereo 16-Bit Oversampling Sigma-Delta A/D Converter
- Stereo 16-Bit Oversampling Sigma-Delta D/A Converter
- Support Maximum Master Clock of 100 MHz to Allow DSPs Output Clock to be Used as a Master Clock
- Selectable FIR/IIR Filter With Bypassing Option
- Programmable Sampling Rate up to:
  - Max 26 Ksps With On-Chip IIR/FIR Filter
  - Max 104 Ksps With IIR/FIR Bypassed
- On-Chip FIR Produced 84-dB SNR for ADC and 92-dB SNR for DAC over 13-Khz BW
- Smart Time Division Multiplexed (SMARTDM®) Serial Port
  - Glueless 4-Wire Interface to DSP
  - Automatic Cascade Detection (ACD) Self-Generates Master/Slave Device Addresses
  - Programming Mode to Allow On-The-Fly Reconfiguration
  - Continuous Data Transfer Mode to Minimize Bit Clock Speed
  - Support Different Sampling Rate for Each Device
  - Turbo Mode to Maximize Bit Clock For Faster Data Transfer and Allow Multiple Serial Devices to Share the Same Bus
  - Allows up to Eight Devices to be Connected to a Single Serial Port
- Host port
  - 2-Wire Interface
  - Selectable I^2C or S^2C
- Differential and Single-Ended Analog Input/Output
- Built-In Analog Functions:
  - Analog and Digital Sidetone
  - Antialiasing Filter (AAF)
  - Programmable Input and Output Gain Control (PGA)
  - Microphone/Handset/Headset Amplifiers
  - AIC20/21/20K Have a Built-In 8-Ω Speaker Driver
  - Power Management With Hardware/Software Power-Down Modes 30 µW
- Separate Software Control for ADC and DAC Power Down
- Fully Compatible With Common TMS320® DSP Family and Microcontroller Power Supplies
  - 1.65-V - 1.95-V Digital Core Power
  - 1.1-V - 3.6-V Digital I/O
  - 2.7-V - 3.6-V Analog
- Internal Reference Voltage (V_{ref})
- 2s Complement Data Format
- Test Mode Which Includes Digital Loopback and Analog Loopback

APPLICATIONS

- Wireless Accessories
- Hands-Free Car Kits
- VOIP
- Cable Modem
- Speech Processing



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION

The TLV320AIC2x is a low-cost, low-power, highly-integrated, high-performance, dual-voice codec. It features two 16-bit analog-to-digital (A/D) channels and two 16-bit digital-to-analog (D/A) channels, which can be connected to a handset, headset, speaker, microphone, or a subscriber line via a programmable analog crosspoint.

The TLV320AIC2x provides high resolution signal conversion from digital-to-analog (D/A) and from analog-to-digital (A/D) using oversampling sigma-delta technology with programmable sampling rate.

The TLV320AIC2x implements the smart time division multiplexed serial port (SMARTDM™) . The SMARTDM port is a synchronous 4-wire serial port in TDM format for glue-free interface to TI DSPs (i.e., TMS320C5000®, TMS320C6000® DSP platforms) and microcontrollers. The SMARTDM™ supports both continuous data transfer mode and on-the-fly reconfiguration programming mode. The TLV320AIC2x can be gluelessly cascaded to any SMARTDM-based device to form a multichannel codec, and up to eight TLV320AIC2x codecs can be cascaded to a single serial port.

The TLV320AIC2x provides a flexible host port. The host port interface is a two-wire serial interface that can be programmed to be either an industrial standard I^2C or a simple S^2C (start-stop communication protocol).

The TLV320AIC2x integrates all of the critical functions needed for most voice-band applications including MIC preamplifier, handset amplifier headset amplifier, 8-Ω speaker driver, sidetone control, antialiasing filter (AAF), input/output programmable gain amplifier (PGA), and selectable low-pass IIR/FIR filters.

The TLV320AIC2x implements an extensive power management; including device power-down, independent software control for turning off ADC, DAC, operational-amplifiers, and IIR/FIR filter (bypassable) to maximize system power conservation. The TLV320AIC2x consumes only 14.9 mW per channel at 3 V.

The TLV320AIC2x low power operation from 2.7-V to 3.6-V power supplies along with extensive power management make it ideal for portable applications including wireless accessories, hands-free car kits, VOIP, cable modem, and speech processing. Its low group delay characteristic makes it suitable for single or multichannel active control applications.

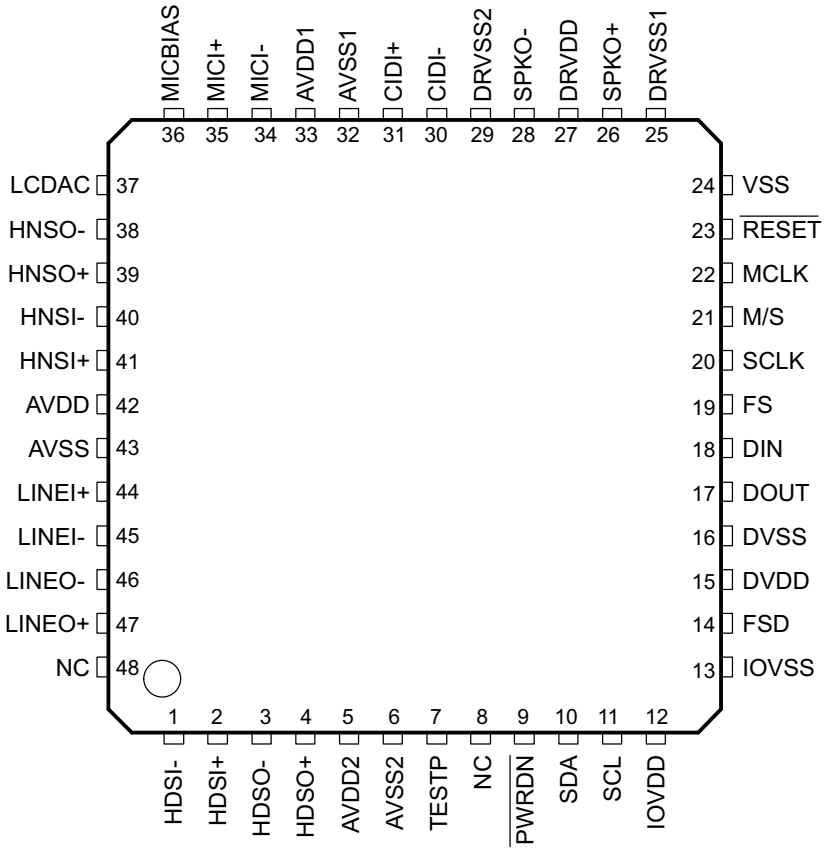
The TLV320AIC2x is characterized for commercial operation from 0°C to 70°C, and industrial operation from -40°C to 85°C. The TLV320AIC2xk is characterized for industrial operation from -40°C to 85°C.

ORDERING INFORMATION

T_A	48-TQFP PFB PACKAGE(1)
0°C to 70°C	TLV320AIC2xC
-40°C to 85°C	TLV320AIC2xI

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

PFB
TOP VIEW



Terminal Functions

TERMINAL			
NAME	NO.	I/O	DESCRIPTION
HDSI- HDSI+	1 2	I	Head-set input. The Head-set input can be treated similar to the Line-input pins
HDSO- HDSO+	3 4	O	150-Ω output
AVDD2	5	I	Analog power supply
AVSS2	6	I	Analog ground
TESTP	7	I	Test pin. Should be connected to digital ground.
NC	8, 48		Not connected
$\overline{\text{PWRDN}}$	9	I	Power down
SDA	10	I/O	I^2C/S^2C data
SCL	11	I	I^2C/S^2C clock
IOVDD	12	I	I/O power supply
IOVSS	13	I	I/O ground
FSD	14	O	Frame sync delayed
DVDD	15	I	Digital supply (1.8 V)
DVSS	16	I	Digital ground
DOUT	17	O	Data OUT
DIN	18	I	Data IN
FS	19	I/O	Frame sync
SCLK	20	I/O	Serial clock

Terminal Functions (continued)

TERMINAL			
NAME	NO.	I/O	DESCRIPTION
M/S	21	I	Master slave select applied to CODEC1 only. CODEC2 is always a slave.
MCLK	22	I	Master clock
$\overline{\text{RESET}}$	23	I	Reset
VSS	24	I	Device ground. Typically this should be connected to the Analog Ground.
DRVSS1	25	I	Driver ground
SPKO+ SPKO-	26 28	O	8-Ω output
DRVDD	27	I	Driver supply
DRVSS2	29	I	Driver ground
CIDI- CIDI+	30 31	I	Caller-ID input. The Caller-ID input can be treated similar to the Line-input pins
AVDD1	33	I	Analog supply
AVSS1	32	I	Analog ground
MICI-	34	I	Microphone input
MICI+	35	I	Microphone input
MICBIAS	36	I	Microphone bias
LCDAC	37	O	6-Bit DAC output may be used to drive LCDAC
HNSO- HNSO+	38 39	O	150-Ω output
HNSI- HNSI+	40 41	I	Hand-set input. The Hand-set input can be treated similar to the Line-input pins
AVDD	42	I	Analog supply
AVSS	43	I	Analog ground
LINEI+ LINEI-	44 45	I	Line input
LINEO- LINEO+	46 47	O	600-Ω output

Electrical Characteristics

All specifications are common across the AIC20, AIC21, AIC24, AIC25, AIC20K, and AIC24K except where explicitly stated.

AIC20/21/24/25: Over Recommended Operating Free-Air Temperature Range, AVDD = 3.3 V, DVDD = 1.8 V, IOVDD = 3.3 V (Unless Otherwise Noted)

AIC20K/24K: Over Recommended Operating Free-Air Temperature Range, AVDD = 3.3 V, DVDD = 1.8 V, IOVDD = 3.3 V (Unless Otherwise Noted)

Absolute Maximum Ratings(1)

over Operating Free-Air Temperature Range (Unless Otherwise Noted)

			TLV320AIC2x
V_{CC}	Supply voltage range:	DVDD(2)	-0.3 V to 2.25 V
		AVDD, IOVDD, DRVDD(2)	-0.3 V to 4 V
V_O	Output voltage range, all digital output signals		-0.3 V to IOVDD + 0.3 V
V_I	Input voltage range, all digital input signals		-0.3 V to IOVDD + 0.3 V
T_A	Operating free-air temperature range		-40°C to 85°C
T_{stg}	Storage temperature range		-65°C to 150°C
	Case temperature for 10 seconds: package		260°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to V_{SS}.

Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	Analog, AVDD	2.7	3.3	3.6	V
		Analog output driver, DRVDD(1)	2.7	3.3	3.6	V
		Digital core, DVDD	1.65	1.8	1.95	V
		Digital I/O, IOVDD	1.1	3.3	3.6	V
	Analog single-ended peak-to-peak input voltage, $V_{I(analog)}$				2	V
R_L	Output load resistance,	Between LINEO+ and LINEO- (differential)		600		Ω
		Between HDSO+ and HDSO- (differential)		150		
		Between HNSO+ and HDSO- (differential)		150		
		Between SPKO+ and SPKO- (differential)		8		
C_L	Analog output load capacitance				20	pF
	Digital output capacitance				20	pF
	Master clock				100	MHz
	ADC or DAC conversion rate				26	kHz
T_A	Operating free-air temperature,		-40		85	°C

(1) DRVDD should be kept at the same voltage as AVDD.

Digital Inputs and Outputs

FS = 8 KHz, outputs not loaded

PARAMETER		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage, DOUT	0.8 IOVDD			V
V_{OL}	Low-level output voltage, DOUT			0.1 IOVDD	V
I_{IH}	High-level input current, any digital input		5		µA
I_{IL}	Low-level input current, any digital input		5		µA
C_i	Input capacitance		3		pF
C_o	Output capacitance		5		pF

ADC PATH FILTER

FS = 8 KHz (1)(2)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
PATH FILTER			**FIR FILTER**			**IIR FILTER**		
Filter gain relative to gain at 1020 Hz	0 Hz to 60 Hz			-27 / 0.07			-27 / 0.15	dB
	60 Hz to 200 Hz			-1 / 0.07			-0.75 / 0.15	
	200 Hz to 300 Hz			-0.03 / 0.05			0. 11 / 0.15	
	300 Hz to 2.4 KHz	-0.1		0.15	-0.1		0.25	
	2.4 kHz to 3 kHz	-0.05		0.15	-0.5		0.2	
	3 kHz to 3.4 KHz	-0.5		0.1	-0.5		0.2	
	3.4 kHz to 3.6 KHz			-0.4			0.15	
	4 KHz			-26			-42	
	4.5 KHz to 72 kHz			-52			-52	

(1) The filter gain outside of the passband is measured with respect to the gain at 1020 Hz. The analog input test signal is a sine wave with 0 dB = 4 $V_{I(PP)}$ as the reference level for the analog input signal. The pass band is 0 to 3600 Hz for an 8-KHz sample rate. This pass band scales linearly with the sample rate.

(2) The filter characteristics are specified by design and are not tested in production. In places where more than one value is specified, the first value is with the High Pass Filter on and the second value is with the HPF off

ADC DYNAMIC PERFORMANCE

With FIR Filter, FS = 8 KHz (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Line In Driver				**AIC20/21/24/25**			**AIC20k/24k**		
SNR	Signal-to-noise ratio	V_I = -3 dB	81	84		70	84		dB
		V_I = -9 dB	73	76			76		
THD	Total harmonic distortion	V_I = -3 dB	83	90		70	90		
		V_I = -9 dB	81	88			88		
THD+N	Signal-to-harmonic distortion + noise	V_I = -3 dB	80	83			83		
		V_I = -9 dB	73	76			76		

(1) The test condition is a differential 1020-Hz input signal with an 8-KHz conversion rate. Input and output common mode is 1.35 V.

ADC DYNAMIC PERFORMANCE

With IIR Filter, FS = 8 KHz

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
				AIC20/21/24/25			AIC20k/24k		
SNR	Signal-to-noise ratio	V_I = -3 dB		82			82		dB
		V_I = -9 dB		76			76		
THD	Total harmonic distortion	V_I = -3 dB		83			83		
		V_I = -9 dB		77			77		
THD+N	Signal-to-harmonic distortion + noise	V_I = -3 dB		78			78		
		V_I = -9 dB		70			70		

ADC CHANNEL CHARACTERISTICS

PARAMETER		TEST CONDITIONS	AIC20/21/24/25/20k/24k			
			MIN	TYP	MAX	UNIT
$V_{I(pp)}$	Differential-ended input level	PGA gain = 0 dB			4	V
V_{IO}	Input offset voltage			±5		mV
I_B	Input bias current			125		µA
	Common mode voltage			1.35		V
	Dynamic range	V_I = -3 dB		87		dB
	Mute attenuation	PGA = MUTE		Zero Digital Code		dB
	Intrachannel isolation			87		dB
E_G	Gain error	V_I = -3 dB at 1020 Hz		-0.45		dB
$E_{O(ADC)}$	ADC converter offset error			±15		mV
CMRR	Common-mode rejection ratio at INMx and INPx	V_I = -100 mV at 1020 Hz		50		dB
	Idle channel noise	$V_{(INP,INM,MICIN)}$ = 0 V		70		µVrms
R_i	Input resistance	T_A = 25°C		10		kΩ
C_i	Input capacitance	T_A = 25°C		2		pF
Channel delay		IIR		$5/f_s$		S
		FIR		$17/f_s$		S

DAC PATH FILTER

FS = 8 KHz (1)(2)

PARAMETER	TEST CONDITIONS	FIR FILTER			IIR FILTER			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
PATH FILTER, FS = 8 KHz								
Filter gain relative to gain at 1020 Hz	0 Hz to 200 Hz			0.1			0.05	dB
	200 Hz to 300 Hz			-0.05			0.05	
	300 Hz to 2.4 KHz	-0.25		0.15	-0.1		0.1	
	2.4 kHz to 3 kHz	-0.3		0.1	-0.2		0.1	
	3 kHz to 3.4 KHz	-0.55		0.05	-0.25		0.05	
	3.4 kHz to 3.6 KHz			-30			0	
	4 KHz			-28			-34	
	4.5 KHz to 72 KHZ			-70			-70	

(1) The filter gain outside of the passband is measured with respect to the gain at 1020 Hz. The input signal is the digital equivalent of a sine wave (digital full scale = 0 dB). The nominal differential DAC channel output with this input condition is 4 $V_{I(PP)}$. The pass band is 0 to 3600 Hz for an 8-kHz sample rate. This pass band scales linearly with the conversion rate.
(2) The filter characteristics are specified by design and are not tested in production.

DAC DYNAMIC PERFORMANCE

PARAMETER		TEST CONDITIONS	AIC20/21/24/25			AIC20k/24k			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
DAC Line Output (LINEO-, LINEO+) Using FIR Filter		The test condition is the digital equivalent of a 1020-Hz input signal with an 8-kHz conversion rate. The test is measured at output of the application schematic low-pass filter. The test is conducted in 16-bit mode.							
SNR	Signal-to-noise ratio	V_I = 0 dB	88	92		80	92		dB
		V_I = -9 dB	81	83			83		
THD	Total Harmonic Distortion	V_I = 0 dB	84	90		70	90		
		V_I = -9 dB	77	84			84		
THD+N	Signal-to-total Harmonic Distortion + noise	V_I = 0 dB	82	88			88		
		V_I = -9 dB	76	80			80		
DAC Line Output (LINEO-, LINEO+) Using IIR Filter		The test condition is the digital equivalent of a 1020-Hz input signal with an 8-kHz conversion rate. The test is measured at output of the application schematic low-pass filter. The test is conducted in 16-bit mode.							
SNR	Signal-to-noise ratio	V_I = 0 dB		83			83		dB
		V_I = -9 dB		74			74		
THD	Total Harmonic Distortion	V_I = 0 dB		85			85		
		V_I = -9 dB		80			80		
THD+N	Signal-to-total Harmonic Distortion + noise	V_I = 0 dB		80			80		
		V_I = -9 dB		73			73		
DAC Headphone Output (HDSO-, HDSO+), (HNSO-, HNSO+)(1)		The test condition is the digital equivalent of a 1020-Hz input signal with an 8-kHz conversion rate. The test is measured at output of the application schematic low-pass filter. The test is conducted in 16-bit mode.							
SNR	Signal-to-noise ratio	V_I = 0 dB		92			92		dB
		V_I = -9 dB		83			83		
THD	Total Harmonic Distortion	V_I = 0 dB		90			90		
		V_I = -9 dB		89			89		
THD+N	Signal-to-total Harmonic Distortion + noise	V_I = 0 dB		88			88		
		V_I = -9 dB		82			82		
DAC Speaker Output (SPKO-, SPKO+)(1)(2)		The test condition is the digital equivalent of a 1020-Hz input signal with an 8-kHz conversion rate. The test is measured at output of the application schematic low-pass filter. The test is conducted in 16-bit mode.							
SNR	Signal-to-noise ratio	V_I = 0 dB		91			91		dB
		V_I = -9 dB		83			83		
THD	Total Harmonic Distortion	V_I = 0 dB		91			91		
		V_I = -9 dB		91			91		
THD+N	Signal-to-total Harmonic Distortion + noise	V_I = 0 dB		88			88		
		V_I = -9 dB		82			82		

(1) The conversion rate is 8 kHz.
(2) The speaker driver is valid only for the AIC20/21/20K.

DAC CHANNEL CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Dynamic range	V_I = 0 dB at 1020 Hz		92		dB
	Interchannel isolation			90		dB
E_G	Gain error, 0 dB	V_O = 0 dB at 1020 Hz		-0.7		dB
	Mute attenuation	PGA = Mute		90		dB
	Common-mode voltage			1.35		V
	Idle channel narrow band noise	0 - 4 kHz (1)		40		V rms
V_{OO}	Output offset voltage at OUTP1_150 (differential)	DIN = All zeros		±8		V
V_O	Analog output voltage, (3.3 V)	HDSO+	0.35		2.35	V
	Channel delay	IIR		$5/f_s$		s
		FIR		$18/f_s$		s

(1) The conversion rate is 8 kHz.

OUTPUT AMPLIFIER CHARACTERISTICS

PARAMETER	TEST CONDITIONS	AIC20/21/24/25/20k/24k			
		MIN	TYP	MAX	UNIT
SPEAKER INTERFACE (1)					
Speaker output power	V_{CC} = 3.3 V, fully differential, 8-Ω load		250		mW
Maximum output current			250		mA
HANDSET AND HEADSET INTERFACE					
Speaker output power	V_{CC} = 3.3 V, fully differential, 150-Ω load		13		mW
Maximum output current			13		mA
LINE INTERFACE					
Speaker output power	V_{CC} = 3.3 V, fully differential, 600-Ω load		3.5		mW
Maximum output current			3.5		mA

(1) The speaker driver is valid only for the AIC20/21/20k.

BIAS AMPLIFIER CHARACTERISTICS

PARAMETER		TEST CONDITIONS	AIC20/21/24/25/20k/24k			
			MIN	TYP	MAX	UNIT
V_O	Output voltage			1.35/2.35		V
	Integrated noise	300 Hz – 13 KHz		20		µV
V_S	Offset voltage			10		mV
	Current drive			5		mA
	Unity gain bandwith			1		MHz
	DC gain			90		dB
	PSRR			70		dB

POWER-SUPPLY REJECTION(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AV_{DD}	Supply-voltage rejection ratio, analog supply (fj = 0 to $f_s/2$)	Differential		75		

(1) Power supply rejection measurements are made with both the ADC and the DAC channels idle and a 200 mV peak-to-peak signal applied to the appropriate supply.

POWER-CONSUMPTION

PARAMETER	TEST CONDITIONS	AIC20/21/24/25/20k/24k			
		MIN	TYP	MAX	UNIT
ADC (single channel)			5.7		mW
DAC (single channel)	Without drivers		3.5		
Speaker driver (1)	No signal		9.3		
Handset driver	No signal		2		
Headset driver	No signal		2		
Lineout driver	No signal		2		
Reference			2.3		
Digital	PLL off		3.4		
PLL	Analog		4.6		
	Digital		1.8		
Total Analog with all sections on	No signal, PLL off		35.8		
POWER DOWN CURRENT					
Hardware power-down (no clock)			1		µA
Software power-down	Analog, PLL off		2		
	Digital		650		

(1) The speaker driver is valid only for the AIC20/21/20k.

LCD DAC

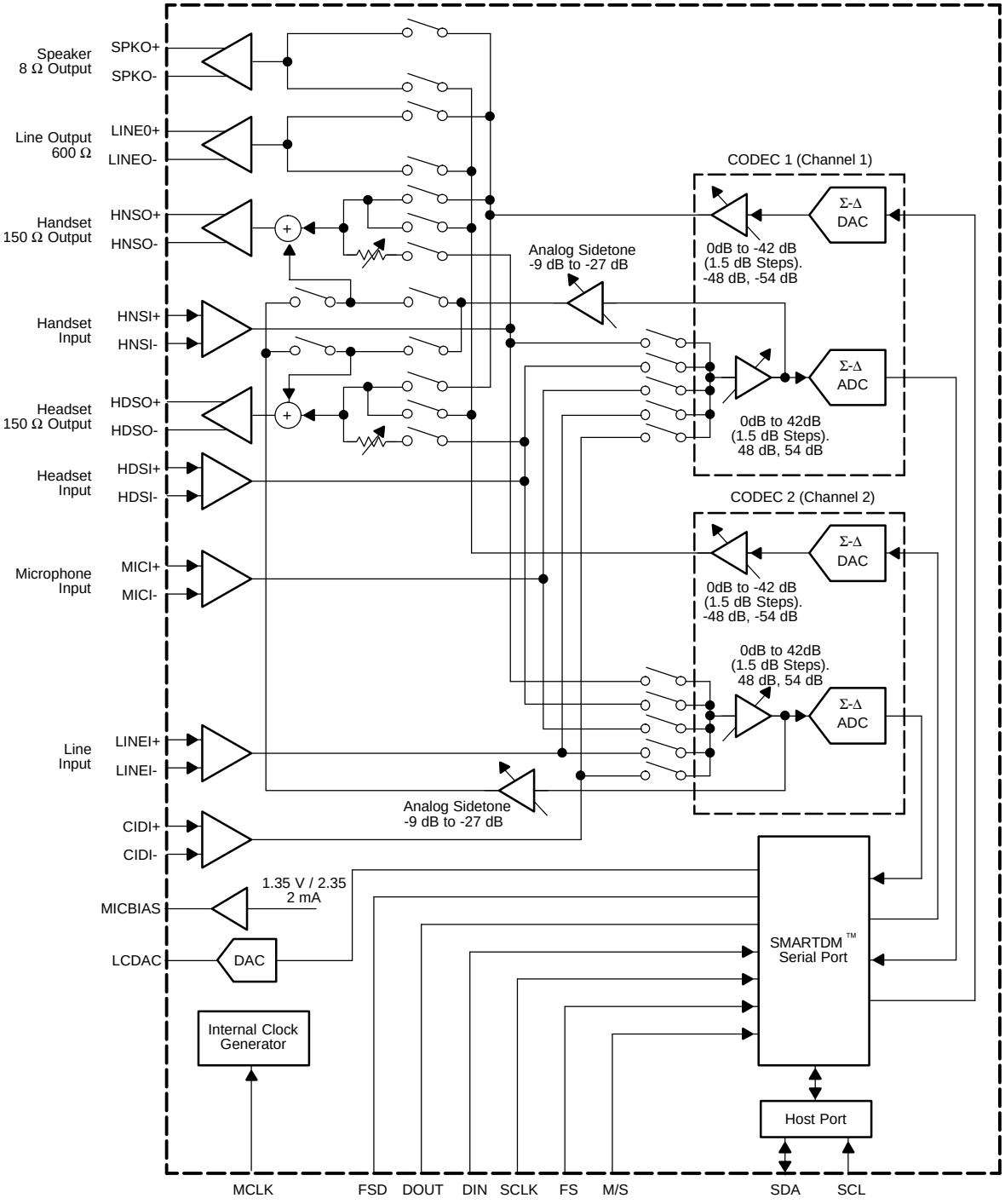
PARAMETER		AIC20/21/20k			
		MIN	TYP	MAX	UNIT
V_O	Output range	0.35		2.35	V
	Sampling rate			104	kHz
	INL		±0.5		LSB
	DNL		±0.25		LSB
V_S	Offset voltage		±25		mV
E_G	Gain error		±0.02		dB

Typical ADC performance With PGA Gain Setting Using FIR(1)

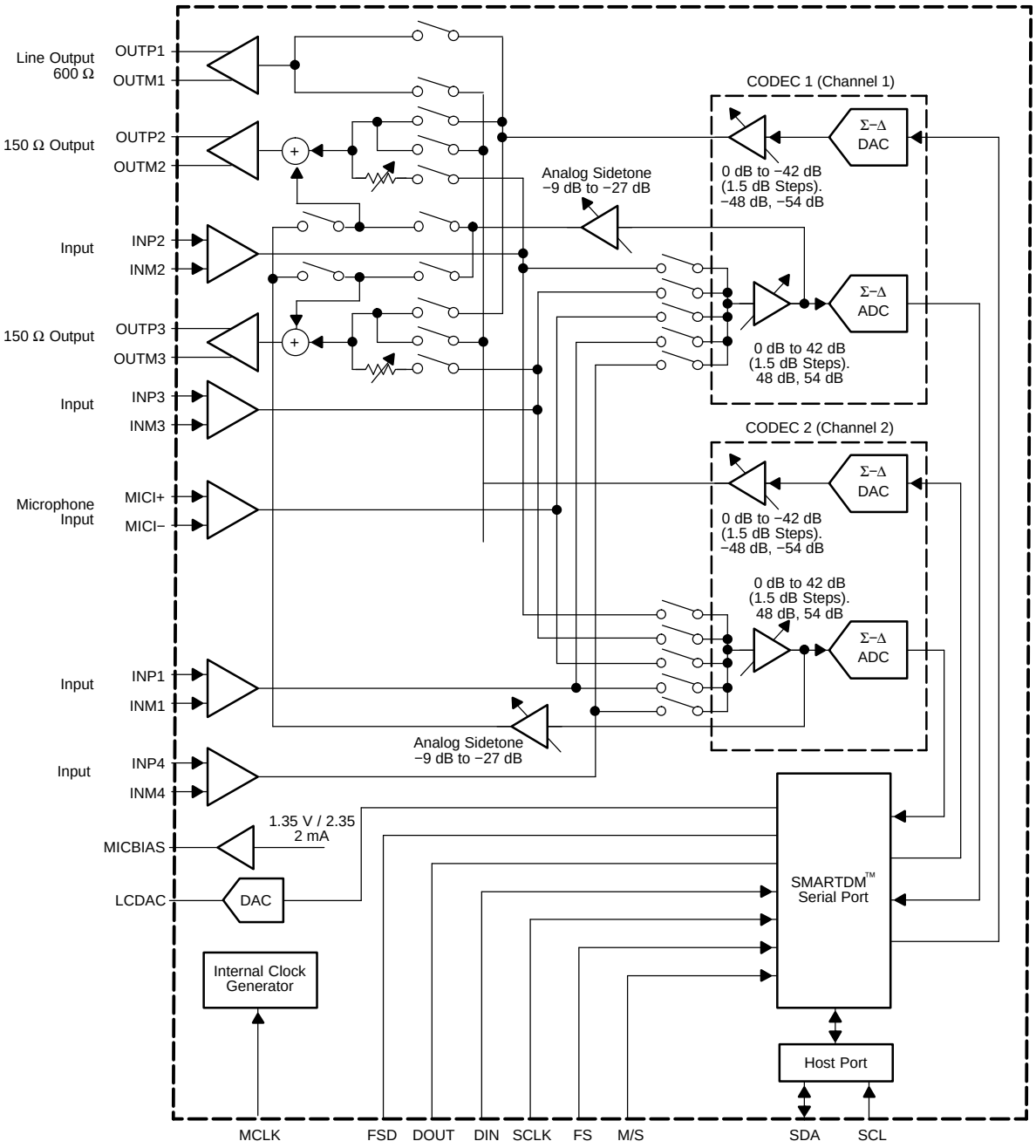
PGA GAIN SETTING	SNR	THD	SINAD	UNIT
9 dB	83	90	81	dB
18 dB	83	97	83	
24 dB	78	95	77	
36 dB	72	95	72	

(1) Test condition is a 1020-Hz input differential signal with an 8-kHz conversion rate. Input amplitude is given such that output of PGA is at -3 dB level.

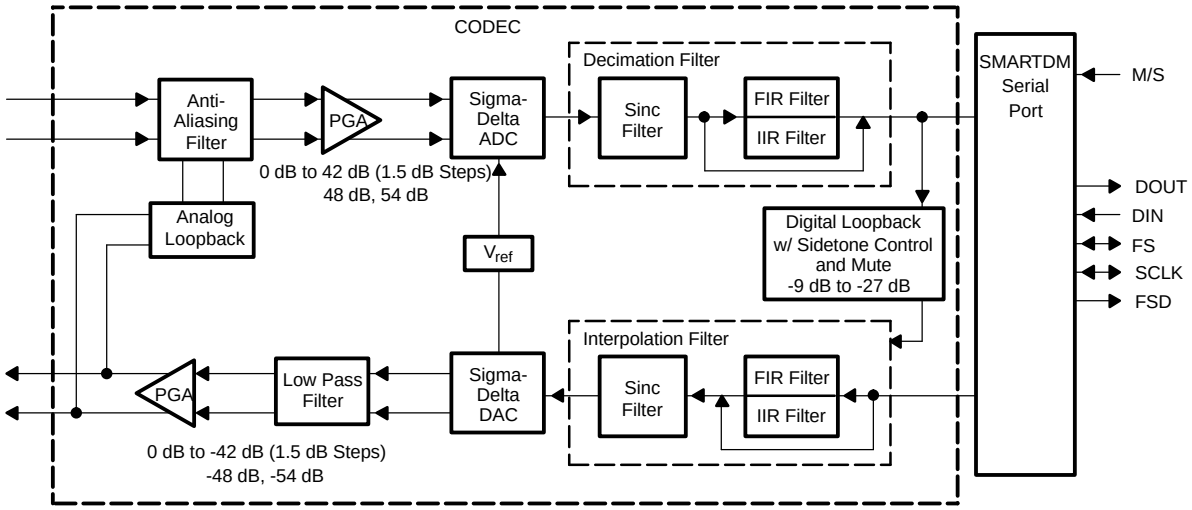
Functional Block Diagram - AIC20/21/20K



Functional Block Diagram - AIC24/25/24K



Functional Block Diagram (One of Two Channels Shown)



Definitions and Terminology

Data Transfer Interval	**The time during which data is transferred from DOUT and to DIN. The interval is 16 shift clocks, and the data transfer is initiated by the falling edge of the FS signal.**
Signal Data	This refers to the input signal and all of the converted representations through the ADC channel and the signal through the DAC channel to the analog output. This is contrasted with the purely digital software control data.
Frame Sync	Frame sync refers only to the falling edge of the signal FS that initiates the data transfer interval
Frame Sync and Sampling Period	Frame sync and sampling period is the time between falling edges of successive FS signals.
f_s	The sampling frequency
ADC Channel	ADC channel refers to all signal processing circuits between the analog input and the digital conversion result at DOUT.
DAC channel	DAC channel refers to all signal processing circuits between the digital data word applied to DIN and the differential output analog signal available at OUTP and OUTM.
Dxx	Bit position in the primary data word (xx is the bit number)
DSxx	Bit position in the secondary data word (xx is the bit number)
d	The alpha character d represents valid programmed or default data in the control register format (see Section 3.2, Secondary Serial Communication) when discussing other data bit portions of the register.
PGA	Programmable gain amplifier
IIR	Infinite impulse response
FIR	Finite impulse response

TIMING REQUIREMENTS

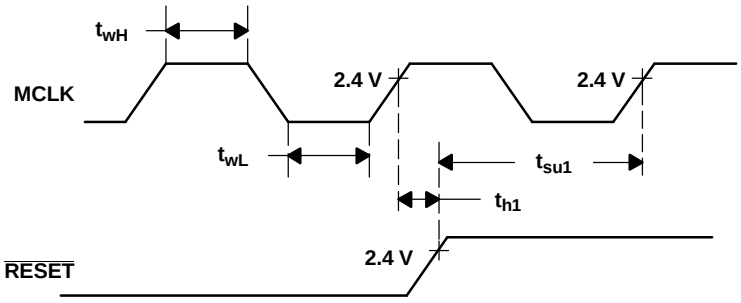


Figure 1. Hardware Reset Timing

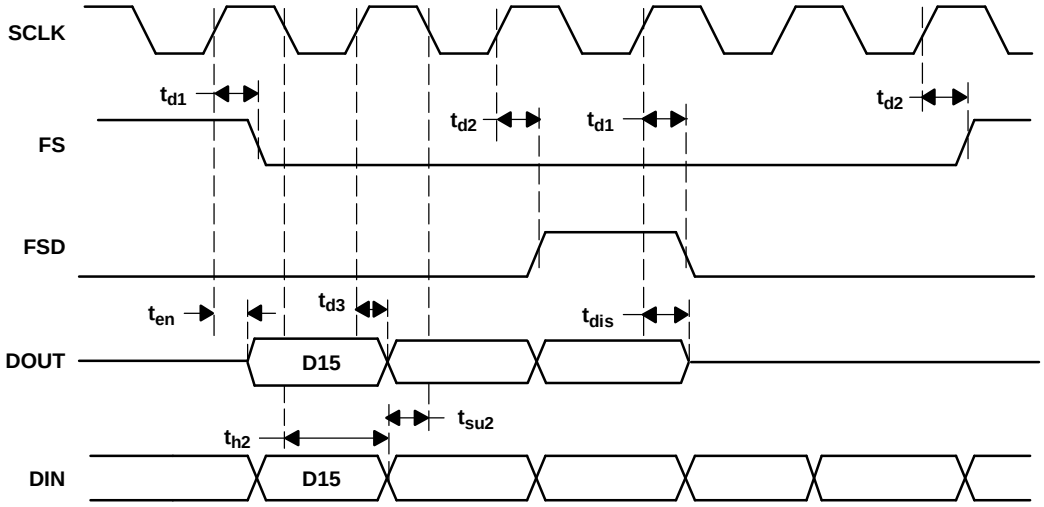


Figure 2. Serial Communication Timing

		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{wH}	Pulse duration, MCLK high		5			
t_{wL}	Pulse duration, MCLK low		5			
t_{su1}	Setup time, $\overline{\text{RESET}}$, before MCLK high (see Figure 1)		3			
t_{h1}	Hold time, $\overline{\text{RESET}}$, after MCLK high (see Figure 1)		2			
t_{d1}	Delay time, SCLK↑ to FS/FSD↓	C_L = 20 pF			5	ns
t_{d2}	Delay time, SCLK↑ to FS/FSD↑				5	
t_{d3}	Delay time, SCLK↑ to DOUT				15	
t_{en}	Enable time, SCLK↑ to DOUT				15	
t_{dis}	Disable time, SCLK↑ to DOUT				15	
t_{su2}	Setup time, DIN, before SCLK↓		10			
t_{h2}	Hold time, DIN, after SCLK↓		10			

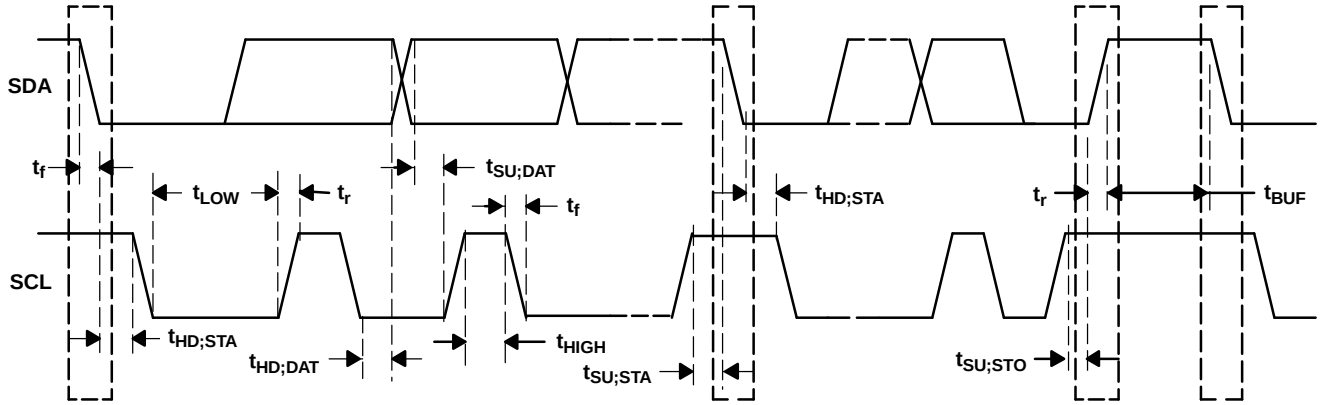


Figure 3. I^2C / S^2C Timing Diagram

PARAMETER	SYMBOL	MIN	MAX	UNIT
SCL clock frequency	t_{SCL}	0	900	kHz
Hold time (repeated START condition. After this period, the first clock pulse is generated.	$t_{HD;STA}$	100		ns
Low period of the SCL clock	t_{LOW}	560		
High period of the SCL clock	t_{HIGH}	560		
Set-up time for a repeated START condition	$t_{SU;STA}$	100		
Data hold time	$t_{HD;DAT}$	50		
Data set-up time	$t_{SU;DAT}$	50		
Rise time of both SDA and SCL signals	t_r		300	
Fall time of both SDA and SCL signals	t_f		100	
Set-up time for STOP condition	$t_{SU;STO}$	100		
Bus free time between a STOP and START condition	t_{BUF}	500		

PARAMETER MEASUREMENT INFORMATION

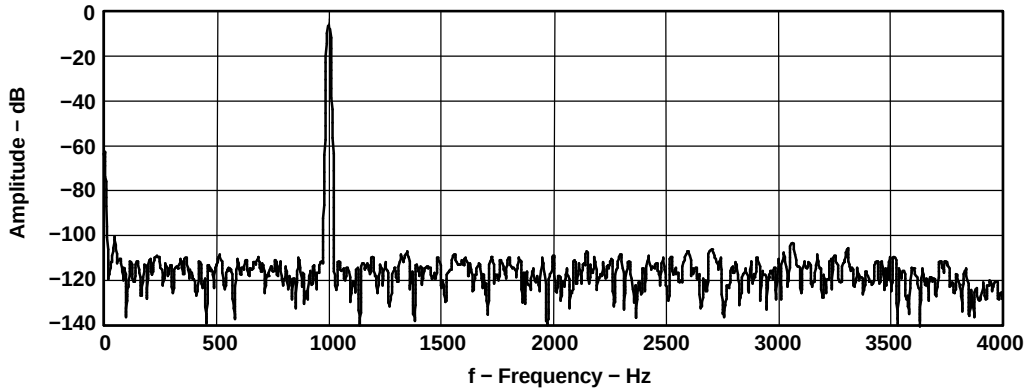


Figure 4. FFT—ADC Channel (-3 dB input)

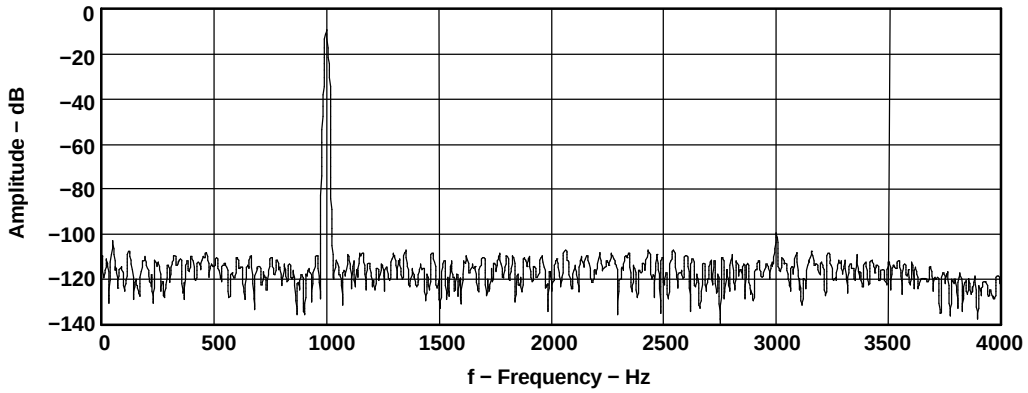


Figure 5. FFT—ADC Channel (-9 dB input)

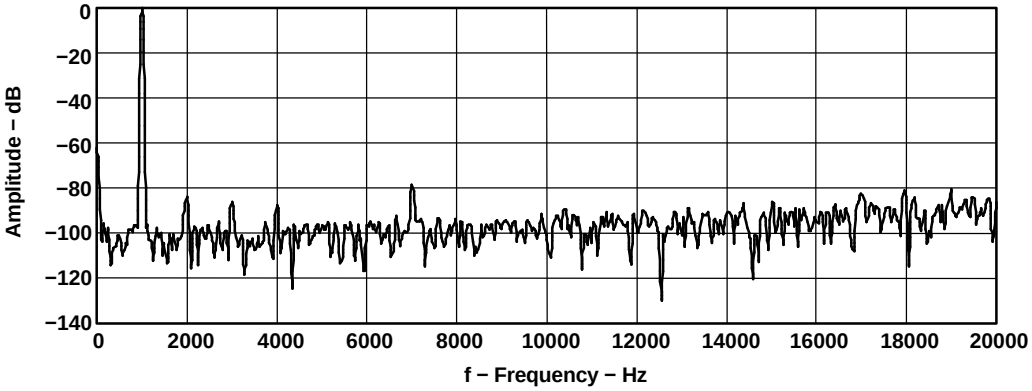


Figure 6. FFT—DAC Channel (0 dB input)

PARAMETER MEASUREMENT INFORMATION (continued)

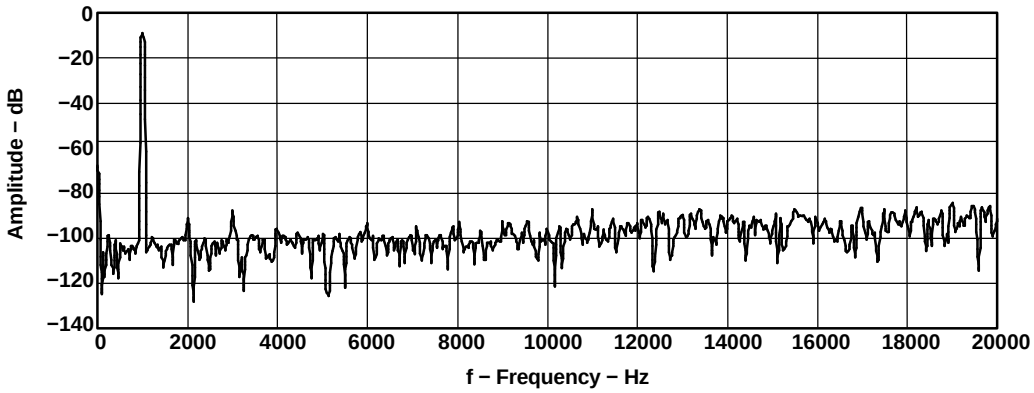


Figure 7. FFT—DAC Channel (-9 dB input)

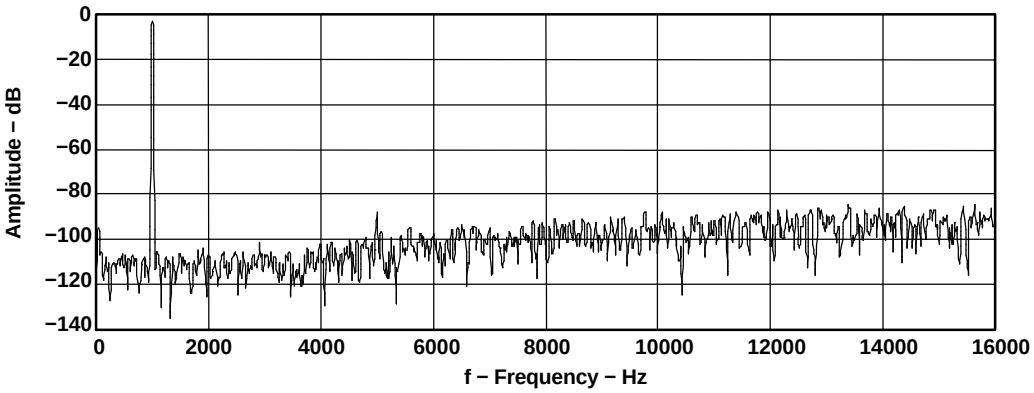


Figure 8. FFT—ADC Channel in FIR/IIR Bypass Mode (-3 dB input)

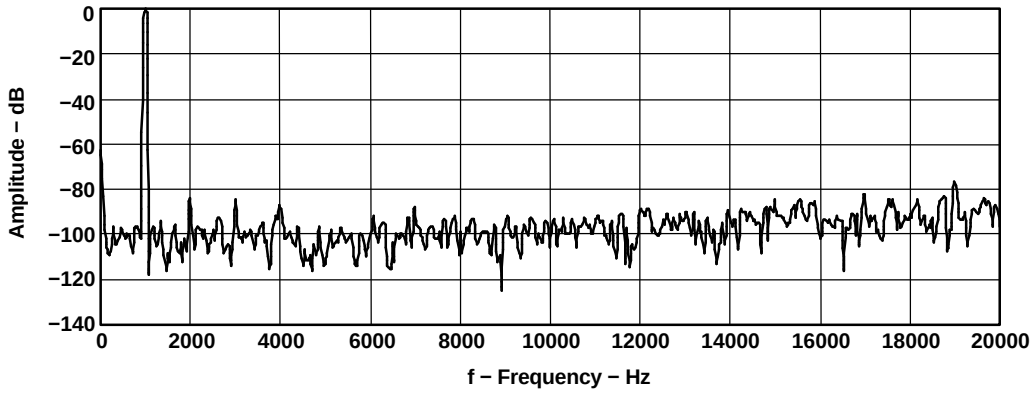


Figure 9. FFT—DAC Channel in FIR/IIR Bypass Mode (0 dB input)

PARAMETER MEASUREMENT INFORMATION (continued)

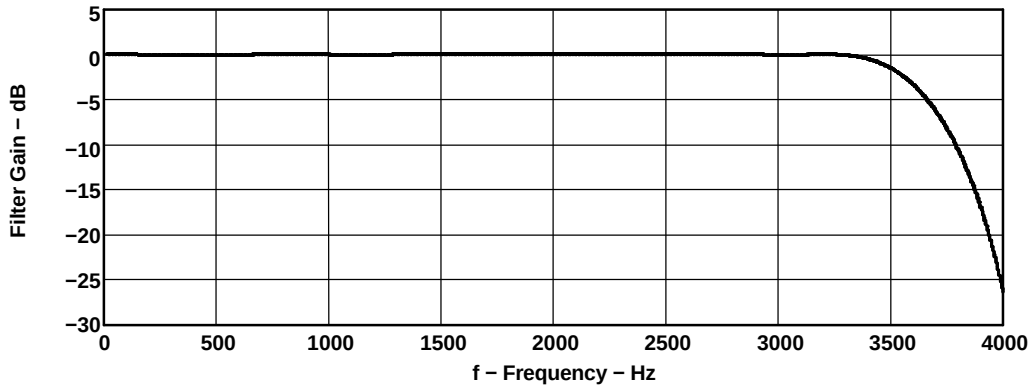


Figure 10. ADC FIR Frequency Response - HPF Off

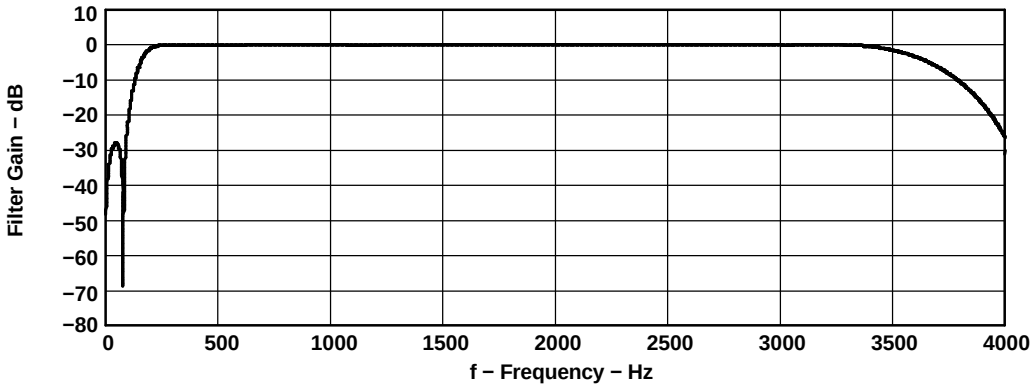


Figure 11. ADC FIR Frequency Response - HPF On

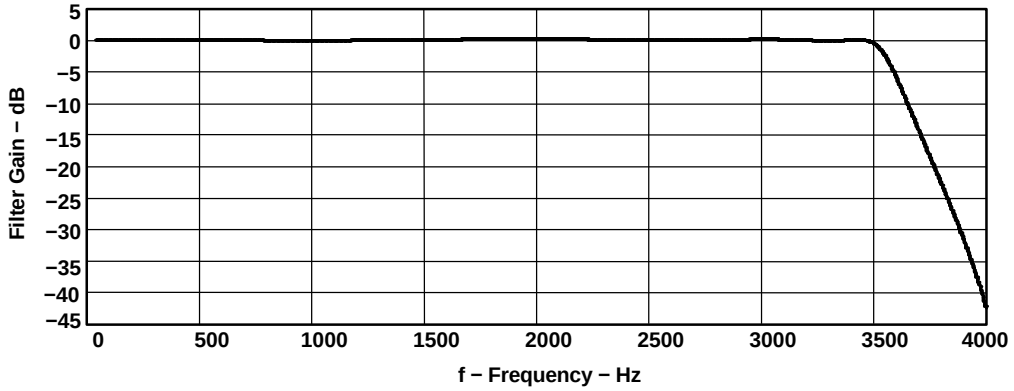


Figure 12. ADC IIR Frequency Response - HPF Off

PARAMETER MEASUREMENT INFORMATION (continued)

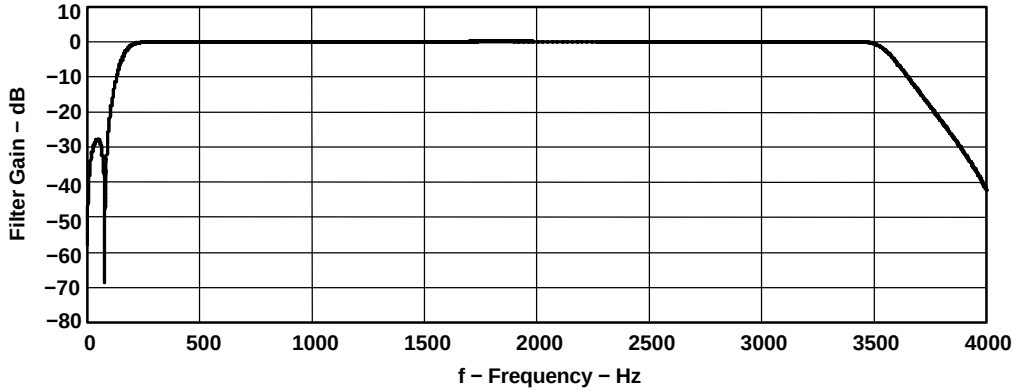


Figure 13. ADC IIR Frequency Response - HPF On

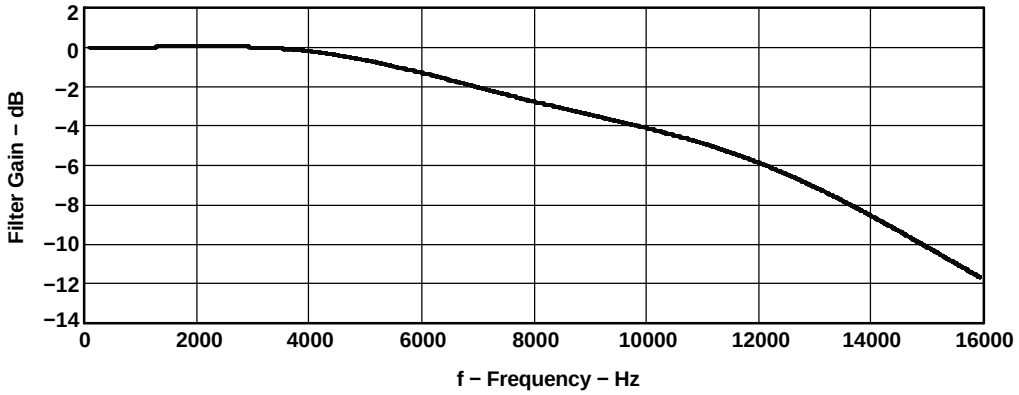


Figure 14. ADC Frequency Response - FIR/IIR Bypass Mode

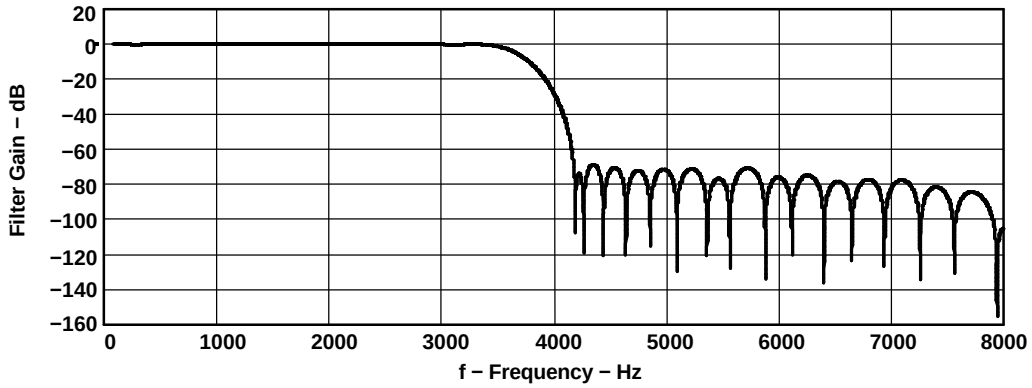


Figure 15. DAC FIR Frequency Response

PARAMETER MEASUREMENT INFORMATION (continued)

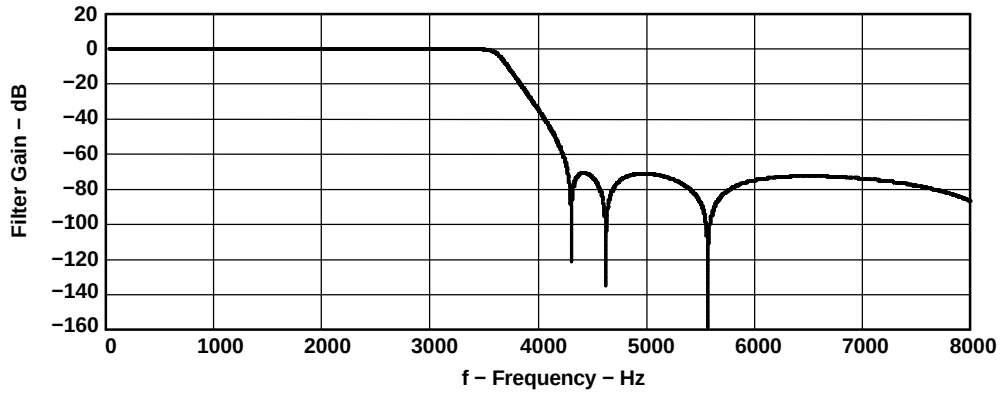


Figure 16. DAC IIR Frequency Response

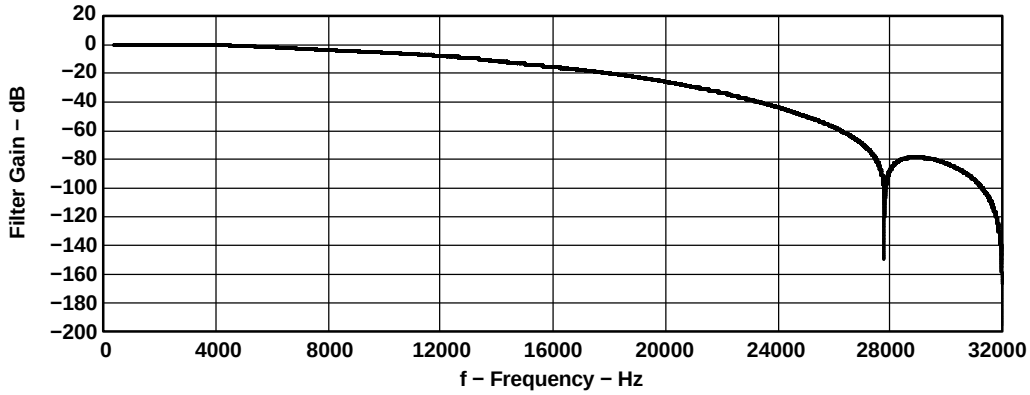


Figure 17. DAC Channel Frequency Response - FIR/IIR Bypass Mode

Functional Description

Operating Frequencies

The sampling frequency is the frequency of the frame sync (FS) signal where falling edge starts digital-data transfer for both ADC and DAC. The sampling frequency is derived from the master clock (MCLK) input by the following equations:

- Coarse sampling frequency (default):
  - The coarse sampling is selected by programming P = 8 in the control register 4, which is the default configuration of AIC2x on power-up or reset.
  - FS = Sampling (conversion) frequency = MCLK / (16 x M x N x 8)
- Fine sampling frequency (see Note 5):
  - FS = Sampling (conversion) frequency = MCLK/ (16 x M x N x P)

NOTE:

1. Use control register 4 to set the following values of M, N, and P
2. M = 1, 2, . . . , 128
3. N = 1, 2, . . . , 16
4. P = 1, 2, . . . , 8
5. The fine sampling rate needs an on-chip phase lock loop (frequency multiplier) to generate internal clocks. The output of the PLL is only used to generate internal clocks that are needed by the data converters. Other clocks such as the serial interface clocks in master mode are not generated from the PLL output. The clock generation scheme is as shown in Figure 18. The PLL requires the relationship between MCLK and P to meet the following condition: 10 MHz ≤ (MCLK/P) ≤ 25 MHz.

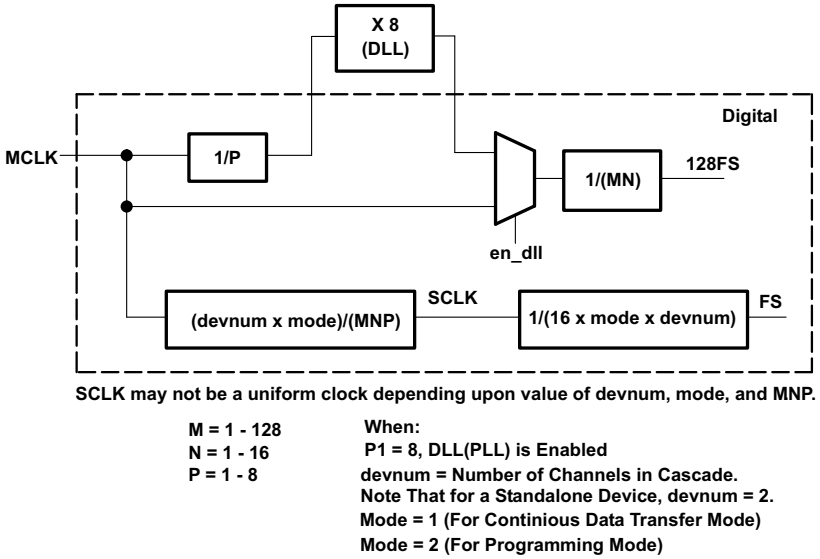


Figure 18. Clock Timing

6. Selecting the Fine sampling mode turns on the analog PLL, which starts generating after a finite time delay. The internal clocks are required to be present in order to enable the DAC output drivers. Therefore, turning on any output drivers immediately after turning on the PLL causes the output of the DAC to go to the common-mode voltage. While using the PLL, the output drivers must first be enabled before the PLL is enabled in order to ensure correct operation of the part. This implies that register 6B for channel 1 and channel 2 in the codec must be programmed before register 4.

Functional Description (continued)

7. Both equations of FS require that the following conditions should be met
   – (M x N x P) ≤ (devnum mode) if the FIR/IIR filter is not bypassed.
   – [Integer(M/4) x N x P] ≥ (devnum mode) if the FIR/IIR filter is bypassed.

   Where:

   devnum is the number of codec channels connecting in cascade (devnum = 2 for standalone AIC20) mode is equal to 1 for continuous data transfer mode and 2 for programming mode.
8. If the DAC OSR is set to 512, then M needs to be a multiple of 4. If the DAC OSR is set to 256, then M needs to be a multiple of 2. M can take any value between 1 and 128 if the OSR is set to 128.

Example:

The MCLK comes from the DSP C5402 CLKOUT and equals to 20.48 MHz and the conversion rate of 8 kHz is desired. First, set P = 1 to satisfy condition 5 so that (MCLK/P) = 20.48 MHz/1 = 20.48 MHz. Next, pick M = 10 and N = 16 to satisfy condition 65 and derive 8 kHz for FS. That is, FS = 20.48 MHz/ (16 x 10 x 16 x 1) = 8 kHz.

Internal Architecture

Analog Low Pass Filter

The built-in analog low pass antialiasing filter is a two-pole filter that has a 20-dB attenuation at 1 MHz.

Sigma-Delta ADC

The sigma-delta analog-to-digital converter is a sigma-delta modulator with 128x oversampling. The ADC provides high-resolution, low-noise performance using oversampling techniques.

Decimation Filter

The decimation filters consist of a sinc filter stage followed by either FIR filters or IIR filters selected by bit D5 of the control register 1. The FIR filter provides linear-phase output with $17/f_s$ group delay, whereas the IIR filter generates nonlinear phase output with negligible group delay. The decimation filters reduce the digital data rate to the sampling rate. This is accomplished by decimating with a ratio of 1:128. The output of the decimation filter is a 16-bit 2s-complement data word clocking at the sample rate selected for that particular data channel. The BW of the filter is (0.45 × FS) and scales linearly with the sample rate.

Sigma-Delta DAC

The sigma-delta digital-to-analog converter is a sigma-delta modulator with 128x oversampling. The DAC provides high-resolution, low-noise performance using oversampling techniques. The oversampling ratio (OSR) in DAC is programmable to 256/512 using bits D0-D1 of register 3C, the default being 128. The OSR of 512 is recommended when the FS is a maximum of 8 Ksps, and an OSR of 256 is recommended when the FS is a maximum of 16 Ksps. It is also required that the value of M used in programming the PLL be a multiple of 4 if the OSR is set to 512 and 2 if the OSR is set to 256

Interpolation Filter

The interpolation filters consist of either FIR or IIR filters selected by bit D5 of control register 1 followed by a sinc filter stage. The FIR filter provides linear-phase output with $18/f_s$ group delay, whereas the IIR filter generates nonlinear phase output with negligible group delay. The interpolation filter resamples the digital data at a rate of 128 times the incoming sample rate. The high-speed data output from the interpolation filter is then used in the sigma-delta DAC. The BW of the filter is (0.45 × FS) and scales linearly with the sample rate.

Functional Description (continued)

Analog/Digital Loopback

The analog and digital loopbacks provide a means of testing the data ADC/DAC channels and can be used for in-circuit system level tests. The analog loopback always has the priority to route the DAC low pass filter output into the analog input where it is then converted by the ADC to a digital word. The digital loopback routes the ADC output to the DAC input on the device. Analog loopback is enabled by writing a 1 to bit D2 in the control register 1. Digital loopback is enabled by writing a 1 to bit D1 in control register 1.

Analog Sidetone

The analog sidetone attenuates the analog input and mixes it with the output of the DAC. The control register 5C selects the attenuation level of the analog sidetone.

Digital Sidetone

The digital sidetone attenuates the ADC output and mixes it with the input of the DAC. The control register 5C selects the attenuation level of the digital sidetone.

Analog Input/Output

To produce excellent common-mode rejection of unwanted signal performance, the analog signal is processed differentially until it is converted to digital data. The signal source driving the analog inputs should have low source impedance for lowest noise performance and accuracy. To obtain maximum dynamic range, the signal must be ac coupled to the input terminal. The analog output is differential from the digital-to-analog converter.

Analog Crosspoint

The analog crosspoint is a lossless analog switch matrix controlled via the serial control port. It allows any source device to be connected to any sink device. Additionally, special summing connections with adjustable loss (7 × 3 dB steps) are included to implement sidetone for the headset and handset ports. (Also included is muting function on any of the sink devices). The control of the analog crosspoint, defined in the control register 6, is to allow any analog input or output to connect to a codec at one time. If more than one input is selected, these inputs are mixed together before the conversion. Caution needs to be taken to make sure that both DAC channels are not connected to the same output.

Analog Input Amplifier

The integrated programmable gain amplifier (PGA) controls the amplification of any analog input before the analog-to-digital converter converts the signal. The PGA's gain from 0 dB to 42 dB in 1.5-dB steps and 48 dB and 54 dB are selected using the control register 5A.

Microphone Bias

To operate electret microphones properly, a bias voltage and current are provided. Typically, the current drawn by the microphone is in the order of 100 µA to 800 µA and the bias voltage is specified across the microphone at 1.35 V or 2.35 V. The MICBIAS has good power supply noise rejection in the audio band and the bias voltage is selectable, via bit D3 of control register 1, for each interface.

Output Drivers

The HSNO and HDSO are output from two audio amplifiers to drive low-voltage speakers like those in the handset and headset. They can drive a load of 150 Ω. The drive amplifier is differential to minimize noise and EMC immunity problems. The frequency response is flat up to 26 kHz.

Speaker Driver

The SPKO is output from the audio amplifier that can drive an 8-Ω speaker load. The drive amplifier is differential to minimize noise and EMC immunity problems. The frequency response is flat up to 26 kHz.

Functional Description (continued)

IIR/FIR Control

Overflow Flags

The decimation IIR/FIR filter sets an overflow flag (bit D7) of control register 1 indicating that the input analog signal has exceeded the range of internal decimation filter calculations. The interpolation IIR/FIR filter sets an overflow flag (bit D4) of control register 1 indicating that the digital input has exceeded the range of internal interpolation filter calculations. When the IIR/FIR overflow flag is set in the register, it remains set until the user reads the register. Reading this value resets the overflow flag. These flags need to be reset after power up by reading the register. If FIR/IIR overflow occurs, the input signal should be attenuated by either the PGA or some other method.

IIR/FIR Bypass Mode

An option is provided to bypass IIR/FIR filter sections of the decimation filter and the interpolation filter. This mode is selected through bit D6 of control register 2 and effectively increases the frequency of the FS signal to four times normal output rate of the IIR/FIR-filter. For example, for a normal sampling rate of 8 Ksps (i.e., FS = 8 kHz) with IIR/FIR, if the IIR/FIR is bypassed, the frequency of FS is readjusted to 4×8 kHz = 32 kHz. The sync filters of the two paths can not be bypassed. A maximum of four devices in cascade can be supported in the IIR/FIR bypass mode.

In this mode , the ADC channel outputs data which has been decimated only till 4 FS. Similarly DAC channel input needs to be preinterpolated to 4 FS before being given to the device. This mode allows users the flexibility to implement their own filter in DSP for decimation and interpolation. M should be a multiple of 4 during IIR/FIR bypass mode.

System Reset and Power Management

Software and Hardware Reset

The TLV320AIC2x resets internal counters and registers in response to either of two events:

- A low-going reset pulse is applied to terminal RESET
- A 1 is written to the programmable software reset bits (D3 of control register 3A)

NOTE: The TLV320AIC2x requires a power-up reset applied to the RESET pin.

Either event resets the control registers and clears all sequential circuits in the device. The H/W RESET (active low) signal is at least 6 master clock periods long. As soon as the RESET input is applied, the TLV320AIC2x enters the initialization cycle that lasts for 132 MCLKs, during which the serial port of the DSP must be 3-stated. The initialization sequence performed by the AIC2x is known as Auto Cascade Detection (ACD). ACD is a mechanism that allows a device to know its address in a cascade chain. Up to 8 AIC2x devices can be cascaded together.

The Master device is the first device on the chain i.e. the FS of the Master is connected to the FS of the DSP.

During ACD, each device gets to know the number of devices in the chain as well as its relative position in the chain. This is done upon hardware reset. Therefore. after power up, a hardware reset must be completed. ACD requires 132 MCLKs after reset to complete operation. The number of MCLKs is independent of the number of devices in the chain.

Adjacent devices in the chain have their FS and FSD pins connected to each other. The master device's FS is connected to the FS pin of the DSP. The FSD pin on the last device in the chain is pulled high for master-slave configuration, and it is pulled low for stand-alone slave configuration.

The master device has the highest address i.e., the master device has address equal to total no of channels in cascade minus 1. For example, if 8 devices are cascaded, then the master device has address 15 and 14 followed by the next device which has 13 and 12 etc.

During the first 64 MCLKs, FS is configured as an output and FSD as an input.

During the next 64 MCLKs, FS is configured as an input and FSD as an output.

Functional Description (continued)

The Master device always has its FS configured as an output and the last slave in the cascade (i.e. channel with address 0) always has its FSD configured as an input.

To calculate the channel address, during the first 64 MCLKs, the device counts the number of clocks between ACD starting (reset) and the FSD going high.

During the next 64 MCLKs, the device counts the number of clocks till FS is pulled low.

The sum total of the counts in the first phase and the second phase is the number of devices in the channel.

For a cascaded system the rise time of H/W RESET must be less than the MCLK period and should satisfy setup time requirement of 2 ns with respect to MCLK rise-edge. If more than one codec is cascaded together, RESET must be synchronized to MCLK. Additionally all devices must see the same edge of MCLK within a window of 0.5 ns. This requirement does not exist for a single master or slave. MCLK and RESET can be asynchronous events.

Power Management

Most of the device (all except the digital interface) enters the power-down mode when D5 and D4, in control register 3A, are set to 1. When the $\overline{\text{PWRDN}}$ pin is low, the entire device is powered down. In either case, register contents are preserved and the output of the amplifier is held at midpoint voltage to minimize pops and clicks.

The amount of power drawn during software power down is higher than during a hardware power down because of the current required to keep the digital interface active. Additional differences between software and hardware power-down modes are detailed in the following paragraphs.

Software Power-Down

Data bits D5 and D4 of control register 3A are used by TLV320AIC2x to turn on or off the software power-down mode, which takes effect in the next frame FS. The ADC and DAC can be powered down individually. In the software power-down, the digital interface circuit is still active while the internal ADC and DAC channel and all differential analog outputs are disabled, and DOUT is put in 3-state in the data frame only. Register data in the control frame is still accepted via DIN, but data in the data frame is ignored. The device returns to normal operation when D7 and D6 of control register 3A are reset.

If the PLL is enabled (i.e., P is not set to 8), then executing a software power down and power up of the device causes the output drivers to go to the common-mode voltage. Therefore, before executing a software power down, the PLL must first be disabled (i.e., P should first be set to 8) before control register 3A is programmed. While bringing the codec out of software power down, the PLL should be re-enabled only after the codec is brought out of power down (i.e., register 3A must be programmed first followed by register 4).

Hardware Power-Down

The TLV320AIC2x requires the $\overline{\text{PWRDN}}$ signal to be synchronized with MCLK. When $\overline{\text{PWRDN}}$ is held low, the device enters hardware power-down mode. In this state, the internal clock control circuit and the differential outputs are disabled. All other digital I/Os are disabled and DIN can not accept any data input. The device can only be returned to normal operation by holding $\overline{\text{PWRDN}}$ high. When not holding the device in the hardware power-down mode, $\overline{\text{PWRDN}}$ must be tied high.

Smart Time Division Multiplexed Serial Port (SMARTDM)

The SMART time division multiplexed serial port (SMARTDM) uses the four wires of DOUT, DIN, SCLK, and FS to transfer data into and out of the AIC2x. The TLV320AIC2xs SMARTDM supports three serial interface configurations (see Table 1): stand-alone master, stand-alone slave, and master-slave cascade, employing a time division multiplexed (TDM) scheme (a cascade of only-slaves is not supported). The SMARTDM allows for a serial connection of up to 8 stereo codecs to a single serial port. Data communication in the three serial interface configurations can be carried out in either standard operation (Default) or turbo operation. Each operation has two modes: programming mode (default mode) and continuous data transfer mode. To switch from the programming mode to the continuous data transfer mode, set bit D6 of control register 1 to 1, which is reset automatically after switching back to programming mode. The TLV320AIC2x can be switched back from the continuous data transfer mode to the programming mode by setting the LSB of the data on DIN to 1, only if the data format is (15+1), as selected by bit 0 of control register 1. The SMARTDM automatically adjusts the number

Functional Description (continued)

of time slots per frame sync (FS) to match the number of codecs in the serial interface so that no time slot is wasted. Both the programming mode and the continuous data transfer mode of the TLV320AIC2x are compatible with the TLV320AIC12. The TLV320AIC2x provides primary/secondary communication and continuous data transfer with improvements and eliminates the requirements for hardware and software requests for secondary communication as seen in the TLV320AIC10. The TLV320AIC2x continuous data transfer mode now supports both master/slave stand-alone and cascade.

Table 1. Serial Interface Configurations

TLV320AIC2x CONNECTIONS	M/S PIN		FSD PIN		COMMENTS
	MASTER	SLAVE	MASTER	SLAVE	
Stand-alone	High	Low	Pull high	Low	
Master-slave cascade	High	Low	Connect to the next slave's FS (see Figure 23)		Last slave's FSD pin is pulled high
Slave-slave cascade	NA	NA	NA	NA	Not supported

Clock Source (MCLK, SCLK)

MCLK is the external master clock input. The clock circuit generates and distributes necessary clocks throughout the device. SCLK is the bit clock used to receive and transmit data synchronously. When the device is in the master mode, SCLK and FS are output and derived from MCLK in order to provide clocking the serial communications between the device and a digital signal processor (DSP). When in the slave mode, SCLK and FS are inputs. SCLK is controlled by TURBO bit (D7) in control register 2. In the standard operation (non-turbo, TURBO = 0), SCLK frequency is defined by:

- SCLK = (16 × FS × #Devices × mode)

Where:

- FS is the frame-sync frequency. #Device is the number of the codec channels in cascade. (#Device = 2 for stand-alone AIC2x) Mode is equal to 1 for continuous data transfer mode and 2 for programming mode.

Serial Data Out (DOUT)

DOUT is placed in the high-impedance state after transmission of the LSB is completed. In data frame, the data word is the ADC conversion result. In the control frame, the data is the register read results when requested by the read/write (R/W) bit. If a register read is not requested, the low eight bits of the secondary word are all zeroes. Valid data on DOUT is taken from the high-impedance state by the falling edge of frame-sync (FS). The first bit transmitted on the falling edge of FS is the MSB of valid data.

Serial Data In (DIN)

The data format of DIN is the same as that of DOUT, in which MSB is received first on the falling edge of first SCLK after FS. In a data frame, the data word is the input digital signal to the DAC channel. If (15+1)-bit data format is used, the LSB (D0) of every DAC channel is set to 1 to switch from the continuous data transfer mode to the programming mode. In a control frame, the data is the control and configuration data that sets the device for a particular function as described in Section 3.9, Control Register Programming.

Frame-Sync FS

The frame-sync signal (FS) indicates the device is ready to send and receive data. FS is an output if the M/S pin is connected to HI (master mode) and an input if the M/S pin is connected to LO (slave mode).

Data is valid on the falling edge of the FS signal.

The frequency of FS is defined as the sampling rate of the TLV320AIC2x and derived from the master clock MCLK as followed (see Section 3.1 Operating Frequencies for details):

- FS = MCLK / (16 × P × N × M)

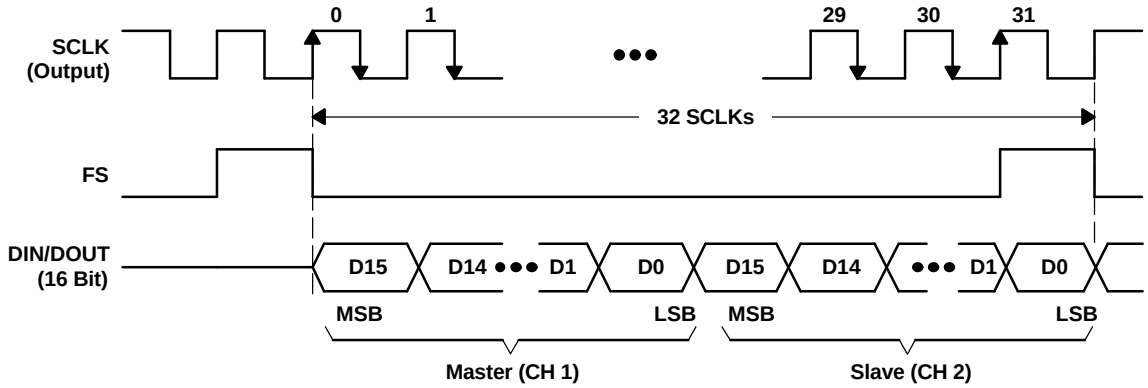


Figure 19. Timing Diagram for FS in the Continuous Transfer Mode

Cascade Mode and Frame-Sync Delayed (FSD)

In cascade mode, the DSP should be in slave mode, i.e., it receives all frame-sync pulses from the master though the master's FS. The master's FSD is output to the first slave and the first slave's FSD is output to the second slave device and so on. Figure 20 shows the cascade of four TLV320AIC2xs in which the closest one to DSP is the master and the rest are slaves. The FSD output of each device is input to the FS terminal of the succeeding device. Figure 21 shows the FSD timing sequence in the cascade.

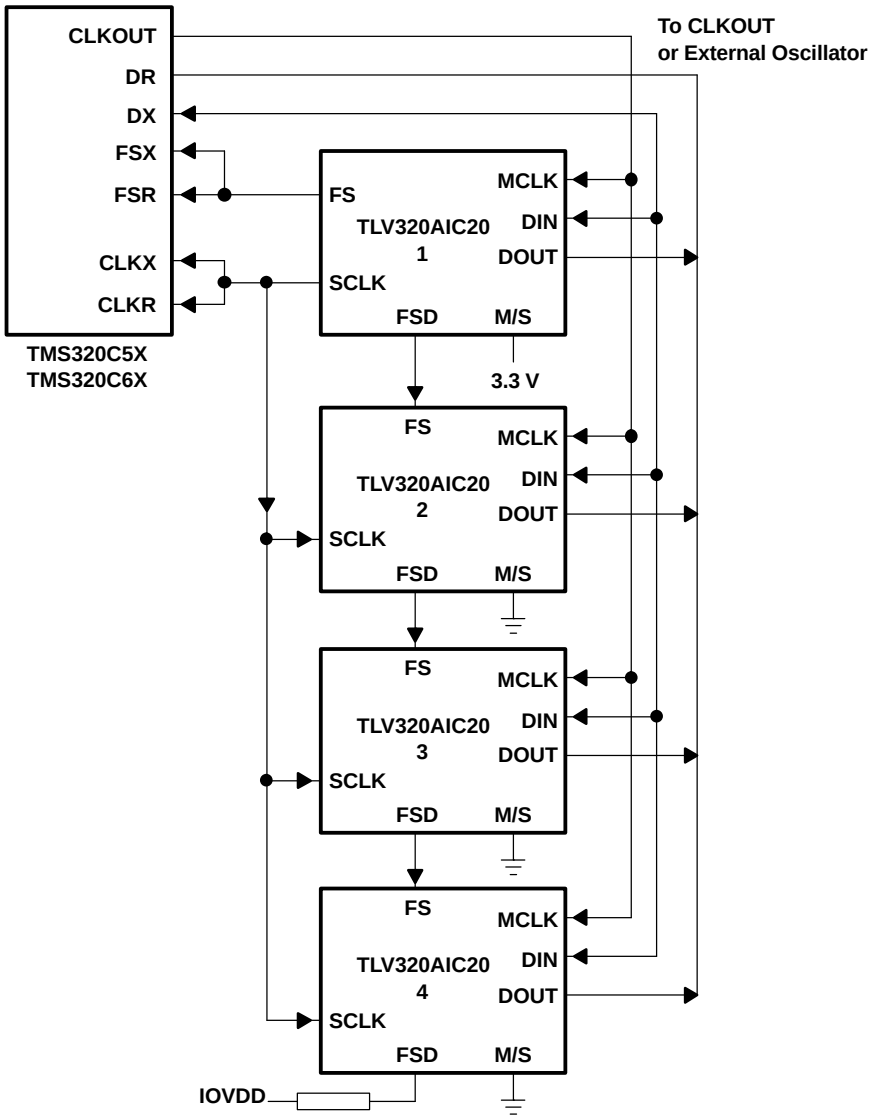


Figure 20. Cascade Connection (to DSP Interface)

Stand-Alone Slave

In the stand-alone slave connection, the FS and SCLK inputs must be synchronized to each other and programmed according to Section 3.1 (Operating Frequencies). The FS and SCLK input are not required to synchronize to the MCLK input but must remain active at all times to assure continuous sampling in the data converter. FSD must be connected to LOW for stand-alone-slave. FS is output for initial 132 MCLK and it is kept low. The host processor needs to keep the FS pin in high impedence state during this period to avoid contention.

Asynchronous Sampling (Codecs in cascade are sampled at different sampling frequency)

The AIC2x SMARTDM supports different sampling frequencies between the different channels in cascade, connecting to a single serial port in which all codecs are sampled at the same frequency of FS. For example: FS1 and FS2 are the desired sampling rates for CH1 and CH2 respectively:

1. FS = MCLK / (16 x M x N x P)
2. FS = n1 x FS1 (n1 = 1, 2, . . ., 8 defined in the control register 3A of CH1)
3. FS = n2 x FS2 (n2 = 1, 2, . . ., 8 defined in the control register 3A of CH2)

For validating the conversion data from this operation:

- For DAC: The DSP needs to give the same data for n1 samples. CH1 picks one of the n1 samples.
- For ADC: CH1 gives the same data for the n1 samples. DSP should pick one of the n1 samples.

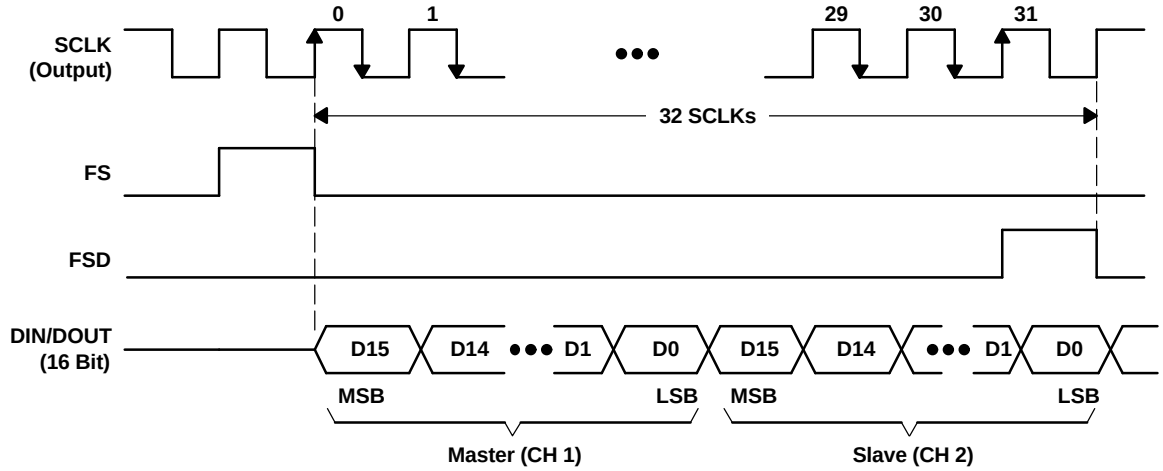


Figure 21. Timing Diagram for FSD Output

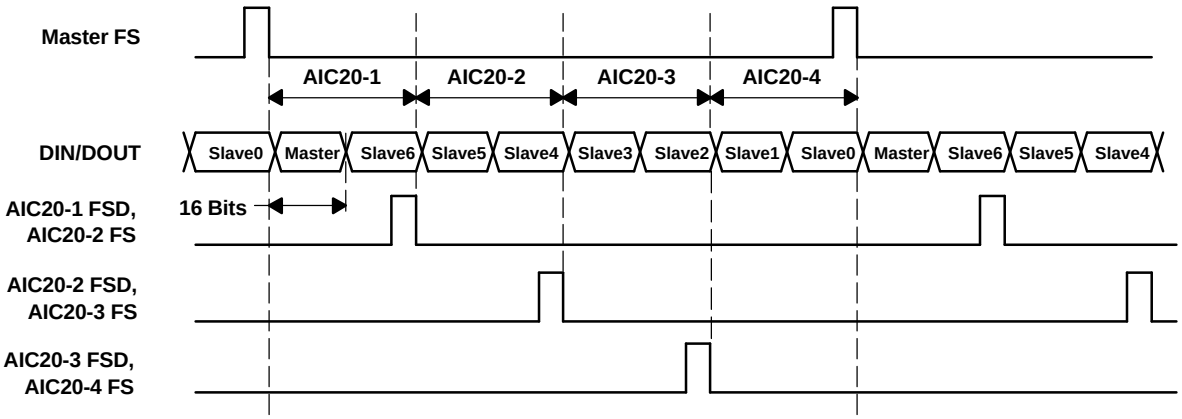


Figure 22. NOTE: AIC2x #4 FSD should be pulled high.

Programming Mode

In the programming mode, the FS signal starts the input/output data stream. Each period of FS contains two frames as shown in Figures 3-10 and 3-11: data frame and control frame. The data frame contains data transmitted from the ADC or to the DAC. The control frame contains data to program each codec control register. The SMARTDM automatically sets the number of time slots per frame equal to the number of codec channels in the interface. Each time slot contains 16-bit data. The SCLK is used to perform data transfer for the serial interface between the AIC2x codecs and the DSP. The frequency of SCLK varies, depending on the selected mode of serial interface. In the stand alone-mode, there are 64 SCLKs (or four time slots) per sampling period. In the master-slave cascade mode, the number of SLCKs equals 32x(number of codec channels in the cascade). The digital output data from the ADC is taken from DOUT. The digital input data for the DAC is applied to DIN. The synchronization clock for the serial communication data and the frame-sync is taken from SCLK. The frame-sync signal that starts the ADC and DAC data transfer interval is taken from FS. The SMARTDM also provides a turbo operation, in which the FS's frequency is always the device's sampling frequency, but SCLK is running at a much higher speed. Thus, there are more than 64 SCLKs for each AIC2x per sampling period, in which the data frame and control frame occupy only the first 64 SCLKs from the falling edge of the frame-sync FS.

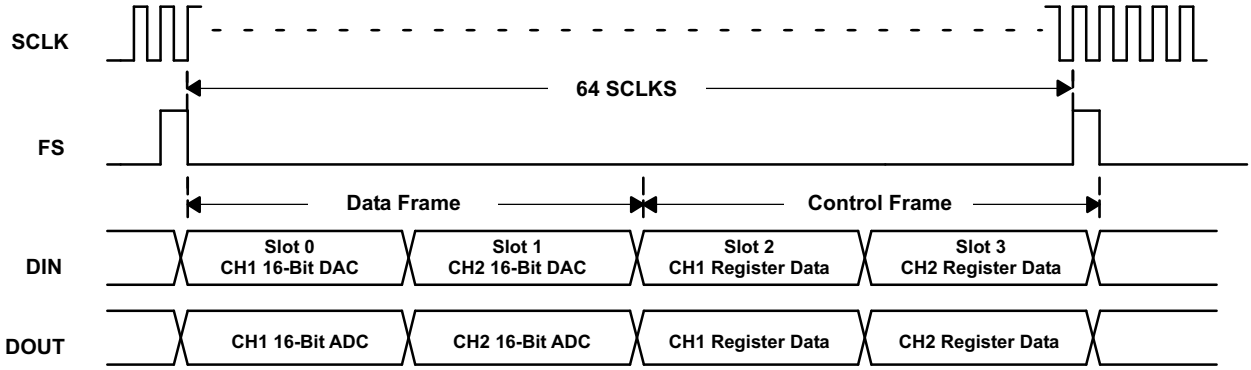
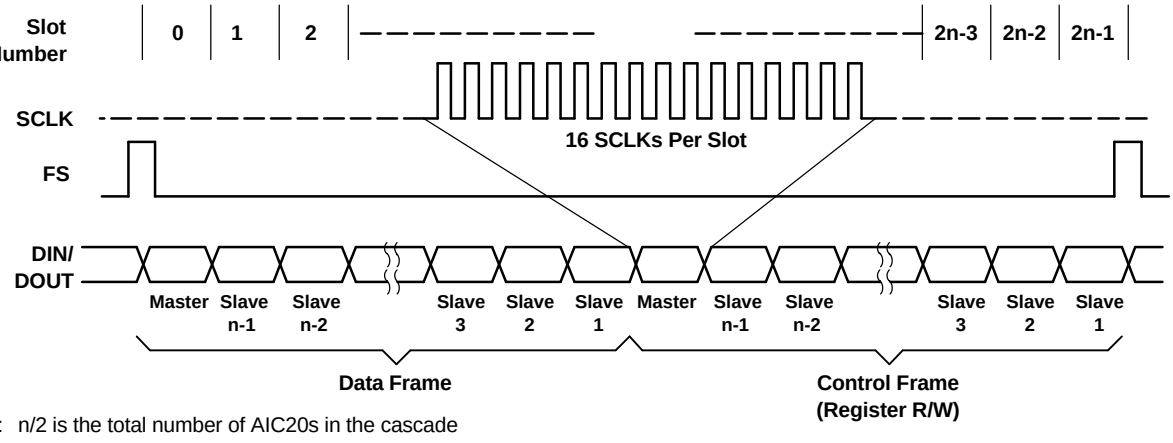


Figure 23. Programming Mode: Stand-Alone Timing



NOTE: n/2 is the total number of AIC20s in the cascade

Figure 24. Standard Operation/Programming Mode: Master-Slave Cascade Timing

Continuous Data Transfer Mode

The continuous data transfer mode, selected by setting bit D6 of each codec's control register 1 to 1, contains conversion data only. In continuous data transfer mode, the control frame is eliminated, and the period of FS signal contains only the data frame in which the 16-bit data is transferred contiguously, with no inactivity between bits. The control frame can be reactivated by setting the LSB of DIN data to 1 if the data is in the 15+1 format. To return the programming mode in the 16-bit DAC data format mode, write 0 in bit D6 of each codec's control register 1 using I^2C or S^2C, or do a hardware reset to come out of continuous data transfer mode. If continuous data transfer mode needs to be used with turbo mode, then the codec should first be set in turbo mode before it is switched from the default programming mode to the continuous data transfer mode.

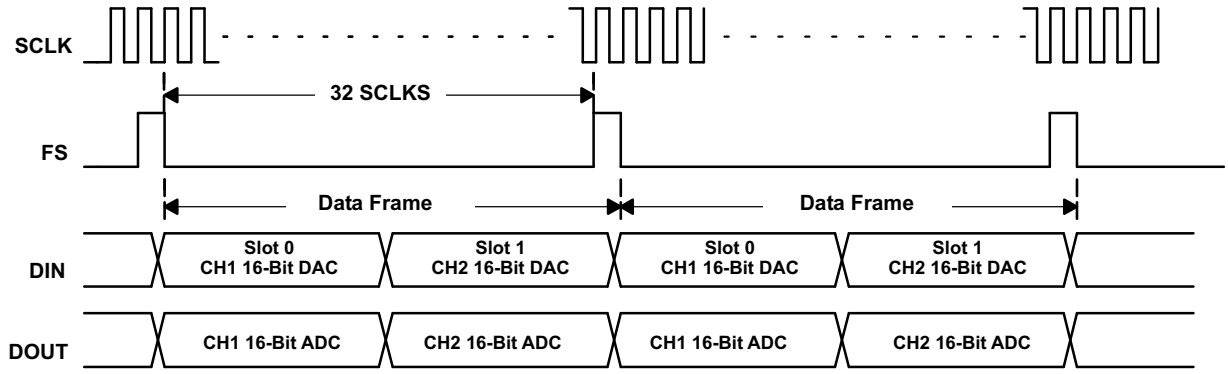
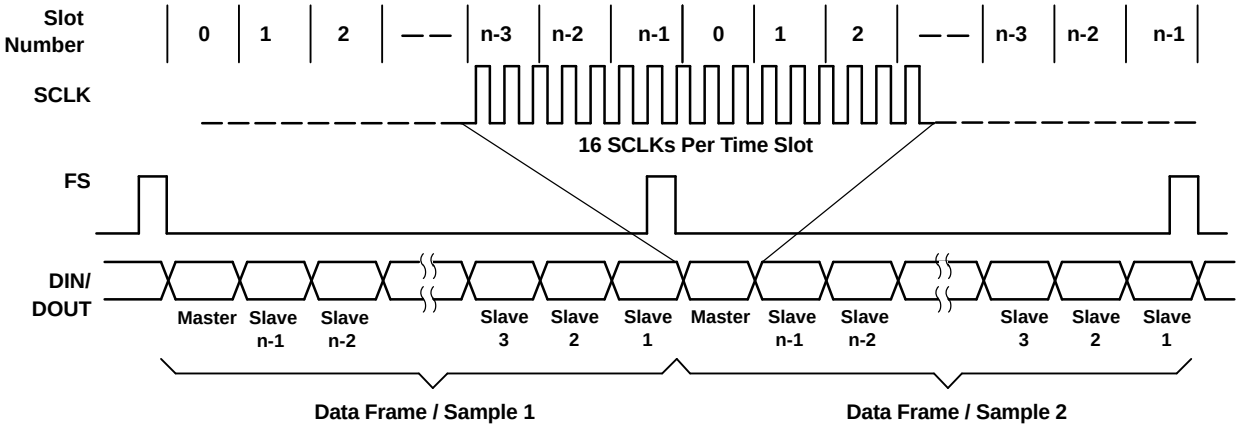


Figure 25. Standard Operation/Continuous Data Transfer Mode: Stand-Alone Timing



NOTE: n/2 is the total number of AIC20s in the cascade

Figure 26. Standard Operation/Continuous Data Transfer Mode: Master-Slave Cascade Timing

Turbo Operation (SCLK)

Setting TURBO = 1 (bit D7) in each codec's control register 2 enables the AIC2x's turbo mode that requires the following condition to be met:

- M × N > #Devices × mode

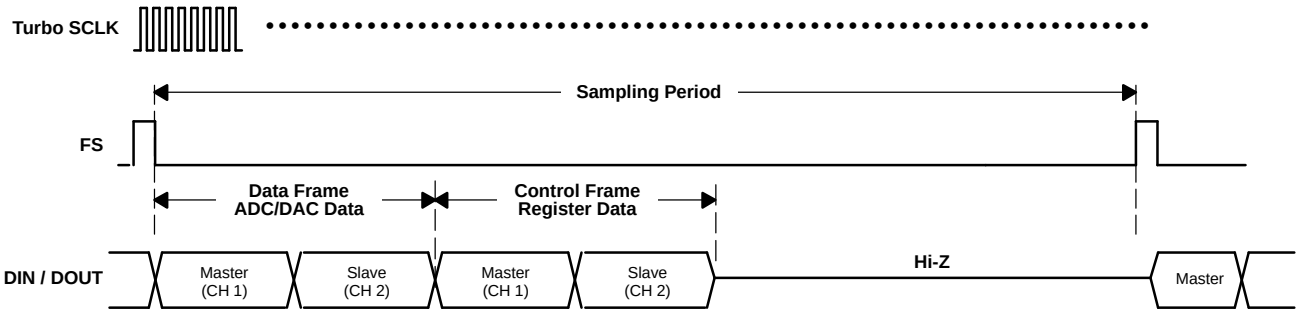
Where:

- M, N, and P are clock divider values defined in the control register 4. #Device is the number of codec channels in cascade. (Number of Device = 2 for stand-alone AIC2x) Mode is equal to 1 for continuous data transfer mode and 2 for programming mode.

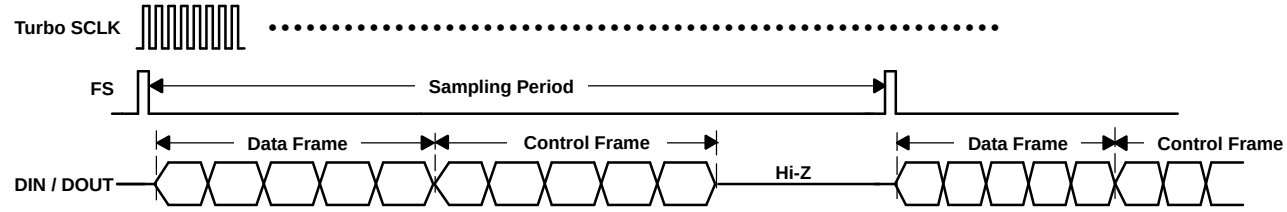
The turbo operation is useful for applications that require more bandwidth for multitasking processing per sampling period. In the turbo mode (see Figure 27), the FS frequency is always the device's sampling frequency, but the SCLK is running at much higher speed. The output SCLK frequency is equal to (MCLK/P) and up to a maximum speed of 25 MHz. The data/control frame is still 32-SCLK long and the FS is one-SCLK pulse. If the AIC2x is in slave mode and the device is not set to turbo mode, only the first FS is used to synchronize the data transfer. The AIC2x ignores all subsequent FS signals and utilizes an internally generated FS. However, if the AIC2x is set to turbo mode while in slave mode, then the data transfer synchronizes on every FS signal. Therefore, it is recommended that if the AIC2x is set to slave mode, then the turbo mode is used. Also note that in turbo mode, it is recommended that SCLK should be a multiple of 32 x FS.

TURBO PROGRAMMING MODE

Stand-Alone Case:

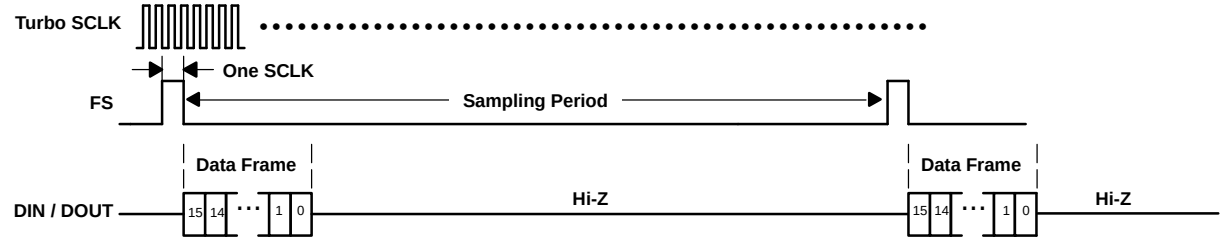


Cascade Case (Master + 4 Slaves):

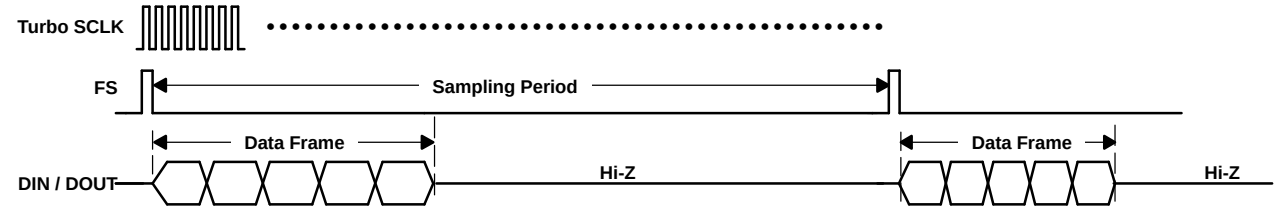


TURBO CONTINUOUS DATA TRANSFER MODE

Stand-Alone Case:



Cascade Case (Master + 4 Slaves):



NOTE: SCLK is not drawn to scale.

Figure 27. Timing Diagram for Turbo Operation

Control Register Programming

Each channel in the TLV320AIC2x contains six control registers that are used to program available modes of operation. All register programming occurs during the control frame through DIN. New configuration takes effect after a delay of one frame sync. The TLV320AIC2x is defaulted to the programming mode upon power up. Set bit 6 in control register 1 to switch to continuous data transfer mode. If the 15+1 data format of DIN has been selected, the LSB of the DIN to 1 to switch from continuous data transfer mode to programming set mode. Otherwise, either the device needs to be reset or the host port writes 0 to bit D6 of each codec's control register 1 during the continuous data transfer mode to switch back to the programming mode. The control registers are replicated for each channel in the AIC2x, and these need to be programmed separately for the individual channels. Register bits that control resources that are common to both channels are shadowed (i.e., writing to the appropriate register bit of one channel is automatically reflected in the register bits for the other channel). See the control register tables for a more detailed description of the exact register bits that are shadowed.

Data Frame Format

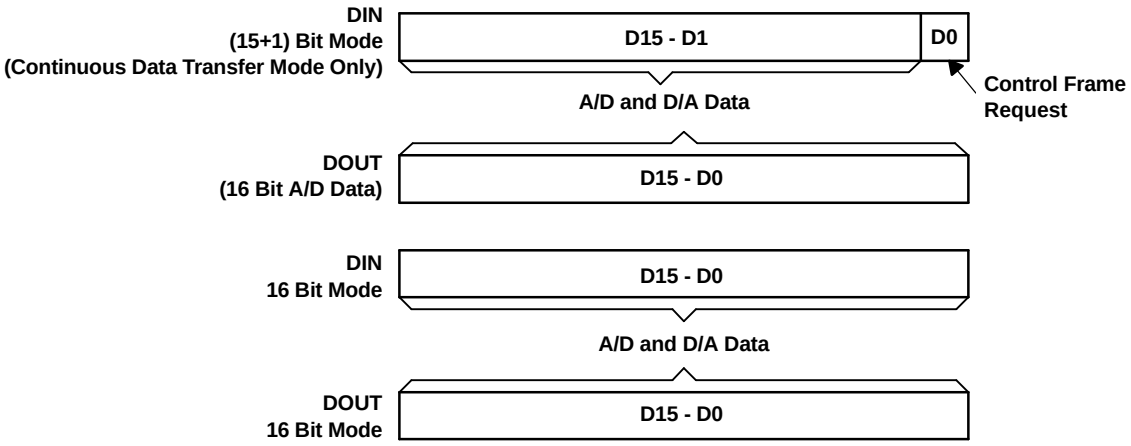


Figure 28. Data Frame Format

Control Frame Format (Programming Mode)

During the control frame, the DSP sends 16-bit words to each codec's time slot SMARTDM(TM) through DIN to read or write control registers in each codec shown in Table 4. The upper byte (Bits D15-D8) of the 16-bit control-frame word defines the read/write command. Bits D15-D13 define the control register address with register content occupied the lower byte D7-D0. Bit D12 is set to 0 for a write or to 1 for a read. Bit D11 in the write command is used to perform the broadcast mode. During a register write, the register content is located in the lower byte of DIN. During a register read, the register content is output in the lower byte of DOUT in the same control frame, whereas the lower byte of DIN is ignored.

Broadcast Register Write

Broadcast operation is very useful for a cascading system of SMARTDM codecs in which all register programming can be completed in one control frame. During the control frame and in any register-write time slot, if the broadcast bit (D11) is set to 1, the register content of that time slot is written into the specified register of all devices in cascade (see Figure 29). This reduces the DSP's overhead of doing multiple writes to program the same data into cascaded devices.

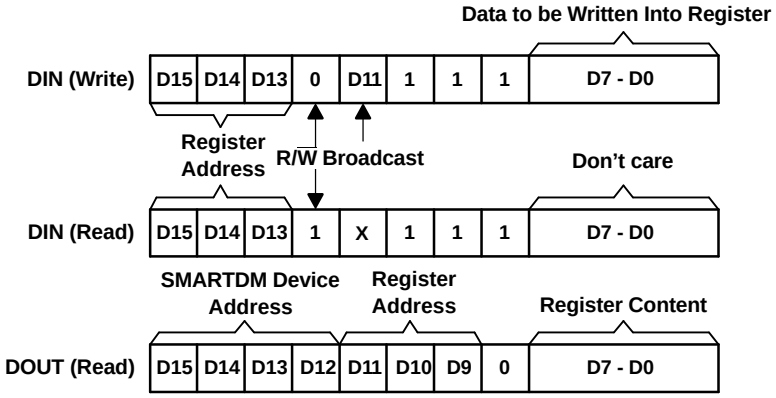
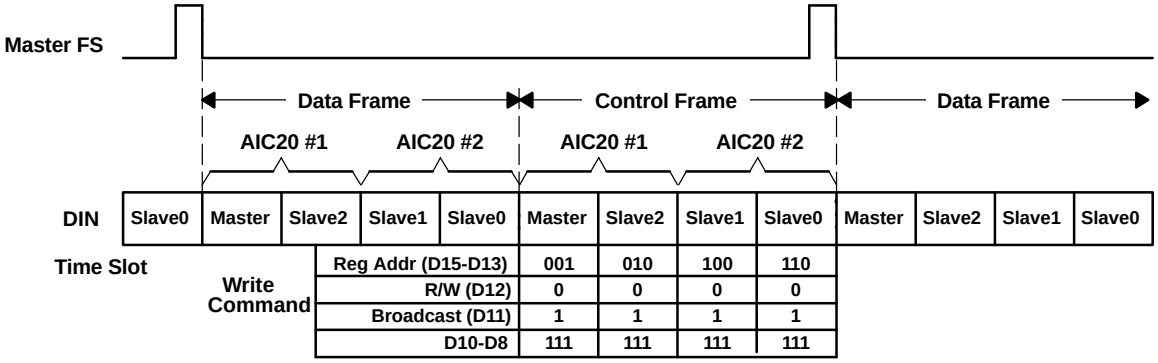


Figure 29. Control Frame Data Format



A. NOTE: In this example, the broadcast operation (D11 = 1) is used to program the four control registers of Reg.1, Reg.2, Reg.4, and Reg.6 in all four DSP codecs of two TLV320AIC2xs in cascade (Master, Slave2, Slave1, and Slave0) during the same frame (i.e., register 1 of the four codecs contains the same data).

Host Port Interface

The host port uses a 2-wire serial interface (SCL, SDA) to program channel six of each of the codec control registers, and selectable protocol between S^2C mode and I^2C mode. The S^2C is a write-only mode, and the I^2C is a read-write mode selected by bits D1-D0 (HPC bits) of control register 2. If the host interface is not needed, the two pins of SCL and SDA can be programmed to become general-purpose I/Os. If selected to be used as I/O pins, the SDA and SCL pins become output and input pins respectively, determined by D1 and D0.

Both S^2C and I^2C require a SMARTDM device address to communicate with the AIC2x. One of SMARTDM's advanced features is the automatic cascade detection (ACD) that enables SMARTDM to automatically detect the total number of codecs in the serial connection and use this information to assign each codec a distinct SMARTDM device address. Table 2 lists device addresses assigned to each codec in the cascade by the SMARTDM. The master always has the highest position in the cascade. For example in Figure 20, there is a total of 4 codecs in the cascade (i.e., one master and 3 slaves), then the device addresses in row 4 are used in which the master is codec 1 with a device address of 0000.

Table 2. SMARTDM Device Addresses

TOTAL CHAN-NELS	CHANNELS POSITION IN CASCADE (1 CODEC HAS 2 CHANNELS)															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1																0000
2															0001	0000
3														0010	0001	0000
4													0011	0010	0001	0000
5												0100	0011	0010	0001	0000
6											0101	0100	0011	0010	0001	0000
7										0110	0101	0100	0011	0010	0001	0000
8									0111	0110	0101	0100	0011	0010	0001	0000
9								1000	0111	0110	0101	0100	0011	0010	0001	0000
10							1001	1000	0111	0110	0101	0100	0011	0010	0001	0000
11						1010	1001	1000	0111	0110	0101	0100	0011	0010	0001	0000
12					1011	1010	1001	1000	0111	0110	0101	0100	0011	0010	0001	0000
13				1100	1011	1010	1001	1000	0111	0110	0101	0100	0011	0010	0001	0000
14			1101	1100	1011	1010	1001	1000	0111	0110	0101	0100	0011	0010	0001	0000
15		1110	1101	1100	1011	1010	1001	1000	0111	0110	0101	0100	0011	0010	0001	0000
16	1111	1110	1101	1100	1011	1010	1001	1000	0111	0110	0101	0100	0011	0010	0001	0000

S²C (Start-Stop Communication)

The S²C is a write-only interface selected by programming bits D1-D0 of control register 2 to 01. The SDA input is normally in a high state, pulled low (START bit) to start the communication, and pulled high (STOP bit) after the transmission of the LSB. Figure 30 shows the timing diagram of S²C. The S²C also supports a broadcast mode in which the same register of all devices in cascade is programmed in a single write. To use S²C's broadcast mode, execute the following steps:

1. Write 111 1000 1111 1111 after the start bit to enable the broadcast mode.
2. Write data to program control register as specified in Figure 30 with bits D14-D11 = XXXX (don't care).
3. Write 111 1000 0000 0000 after the start bit to disable the broadcast mode.

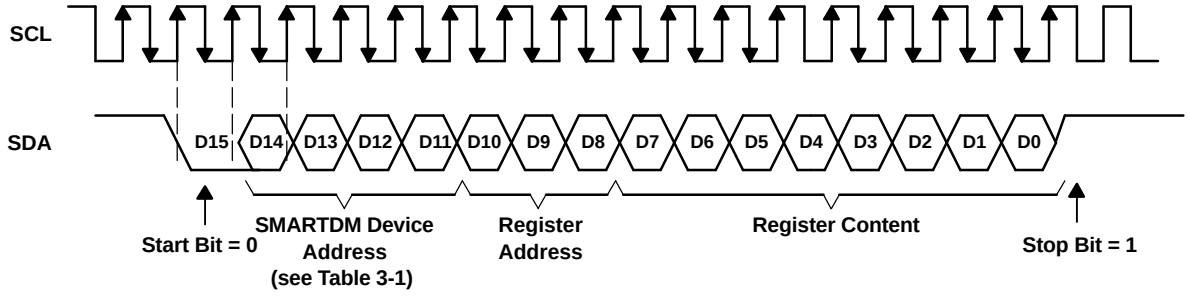


Figure 30. S²C Programming

I²C

- Each I²C read-from or write-to each codec control register is given by an index register address.
- Read/write sequence always starts with the first byte as I²C address followed by 0. During the second byte, default/broadcast mode is set and the index register address is initialized. For write operation control register, data to be written is given from the third byte onwards. For read operation, stop-start is performed after the second byte. Now the first byte is I²C address followed by 1. From the second byte onwards, control register data appears.
- Each time read/write is performed, the index register address is incremented so that the next read/write is performed on the next control register.
- During the first write cycle and all write cycles in the broadcast, only the device with address 0000 issues ACK to the I²C.
- Similarly, for a register with multiple sub-registers the sub-register index automatically increments with each read/write. For example, the first read/write to register 3 read/writes to register 3A, the next to register 3B and so forth until the last sub-register is reached. At this time the sub-register index wraps back around to the first sub-register

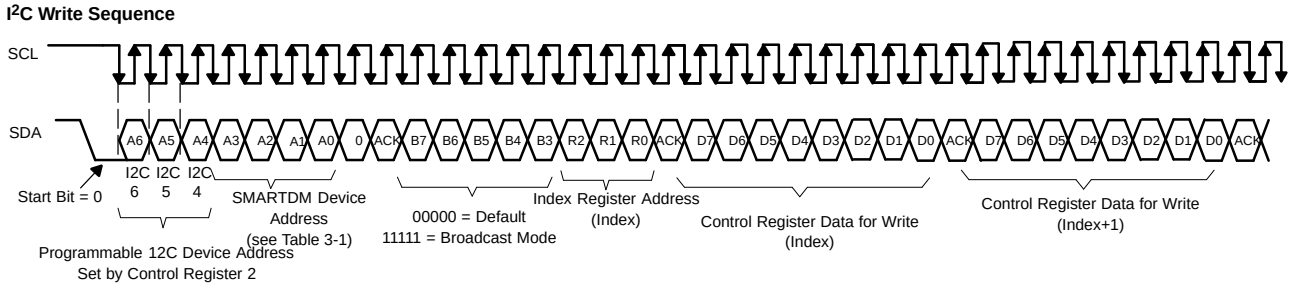


Figure 31. I²C Write Sequence

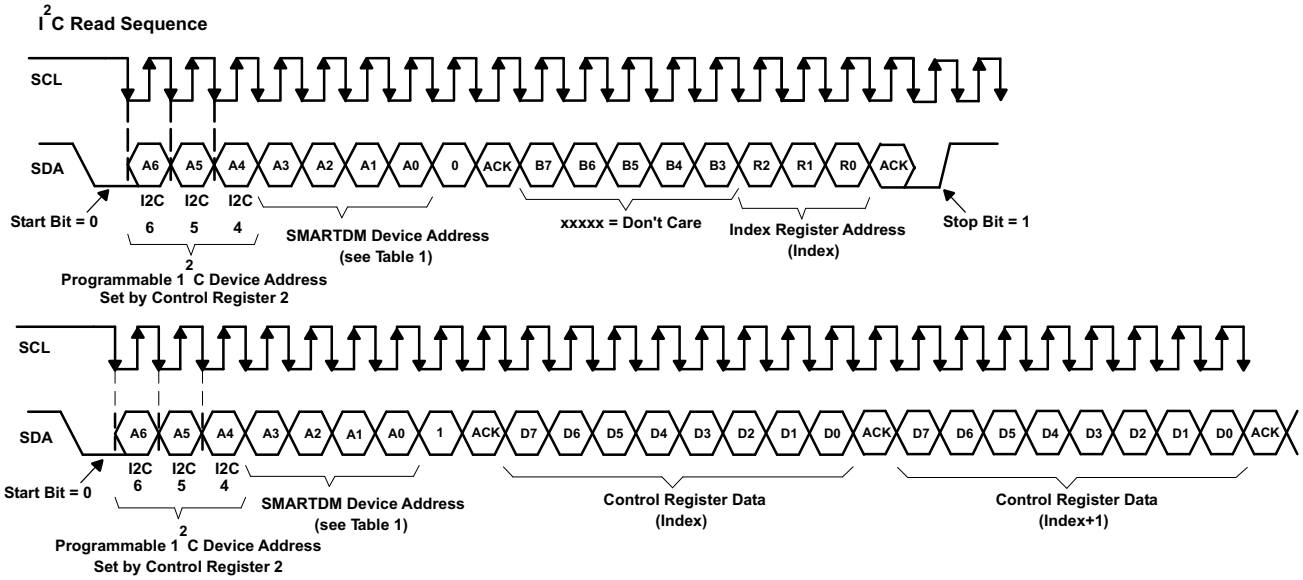


Figure 32. I²C Read Sequence

Each codec has an index register address. To perform a write operation, make the LSB of the first byte as 0 (write) (see Figure 33). During the second byte, the index register address is initialized and mode (broadcast/default) is set. From the third byte onwards, write data to the control register (given by index register) and increment the index register until stop or repeated start occurs. For operation, make the LSB of the first byte as 1 (read). From the second byte onwards, AIC starts transmitting data from the control register (given by the index register) and increments the index register. For setting the index register perform operation the same as write case for 2 bytes, and then give a stop or repeated start.

- S/Sr -> Start/Repeated Start.

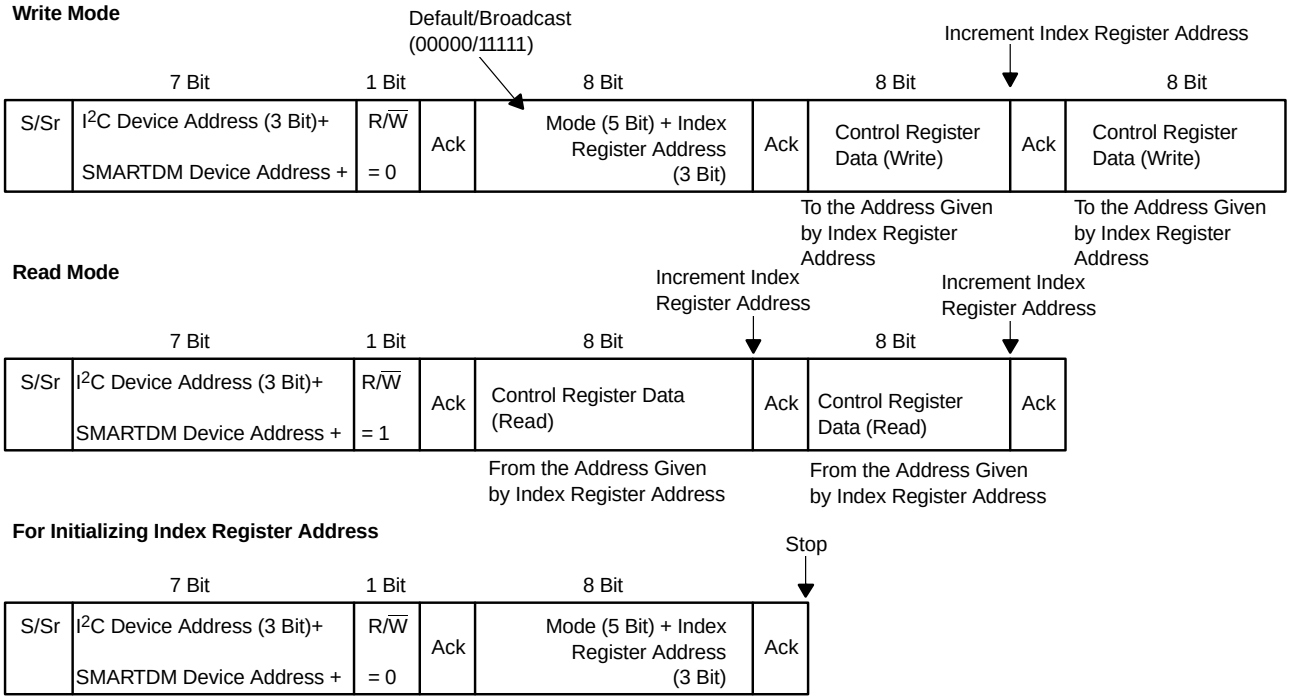


Figure 33. Index Register Addresses

Register Map

Each AIC2x codec consists of 2 channels. Each channel has 6 registers to enable the user to control various components. Registers that control resources that are common across the two channels are shadowed. This means that writing to the appropriate register in one channel automatically updates the contents of the same register in the other channel to reflect the change. For example, writing to register 4 in channel 1 automatically updates the contents of register 4 for channel 2 and vice versa. Refer to the individual register description for a more detailed description of the exact register bits that are shadowed. Bits D15 through D13 represent the control register address that is written with data carried in D7 through D0. Bit D12 determines a read or a write cycle to the addressed register. When D12 = 0, a write cycle is selected. When D12 = 1, a read cycle is selected. Bit D11 controls the broadcast mode as described above, in which the broadcast mode is enabled if D11 is set to 1. Always write 1s to the bits D10 through D8.

Table 3 shows the register map.

Table 3. Register Map

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register Address			RW	BC	1	1	1	Control Register Content							

Table 4. Register Addressing

REGISTER NO.	D15	D14	D13	REGISTER NAME
0	0	0	0	No operation
1	0	0	1	Control 1
2	0	1	0	Control 2
3	0	1	1	Control 3
4	1	0	0	Control 4
5	1	0	1	Control 5
6	1	1	0	Control 6

Control Register Content Description

Control Register 1(1)

D7	D6	D5	D4	D3	D2	D1	D0
ADOVF	CX	IIR	DAOVF	BIASV	ALB	DLB	DAC16
R	R/W/S	R/W	R	R/W/S	R/W	R/W	R/W/S

(1) NOTE: R = Read, W = Write, S = Shadowed

Control Register 1 Bit Summary

BIT	NAME	RESET VALUE	FUNCTION
D7	ADOVF	0	ADC over flow. This bit indicates whether the ADC is overflow. ADOVF = 0 No overflow ADOVF = 1 A/D is overflow.
D6	CX	0	Continuous data transfer mode. This bit selects between programming mode and continuous data transfer mode. CX = 0 Programming mode CX = 1 Continuous data transfer mode
D5	IIR	0	IIR Filter. This bit selects between FIR and IIR for decimation/interpolation low-pass filter. IIR = 0 FIR filter is selected IIR = 1 IIR filter is selected.
D4	DAOVF	0	DAC over flow. This bit indicates whether the DAC is overflow DAOVF = 0 No overflow DAOVF = 1 DAC is overflow
D3	BIASV	0	Bias voltage. This bit selects the output voltage for BIAS pin BIASV = 0 BIAS pin = 1.35 V BIASV = 1 BIAS pin = 2.35 V
D2	ALB	0	Analog loop back ALB = 0 Analog loopback disabled ALB = 1 Analog loopback enabled
D1	DLB	0	Digital loop back DLB = 0 Digital loopback disabled DLB = 1 Digital loopback enabled
D0	DAC16	0	DAC 16-bit data format. This bit applies to the continuous data transfer mode only to enable the 16-bit data format for DAC input.DAC16 = 0 DAC input data length is 15 bits. Writing a 1 to the LSB of the DAC input to switch from continuous data transfer mode to programming mode. DAC16 = 1 DAC input data length is 16 bit.

Control Register 2(1)

D7	D6	D5	D4	D3	D2	D1	D0
TURBO	DIFBP	I^2C6	I^2C5	I^2C4	GPO	HPC	
R/W/S	R/W/S	R/W/S	R/W/S	R/W/S	R/W/S	R/W/S	R/W/S

(1) NOTE: R = Read, W = Write, S = Shadowed

Control Register 2 Bit Summary

BIT	NAME	RESET VALUE	FUNCTION
D7	TURBO	0	Turbo mode. This bit is used to set the SCLK rate. TURBO = 0 SCLK = (16 × FS × number of device × mode) TURBO = 1 SCLK = MCLK/P (P is determined in register 4)
D6	DIFBP	0	Decimation/interpolation filter bypass. This bit is used to bypass both decimation and interpolation filters. DIFBP = 0 Decimation/interpolation filters are operated. DIFBP = 1 Decimation/interpolation filters are bypassed.
D5-D3	I^2Cx	100	I^2C device address. These three bits are programmable to define three MSBs of the I^2C device address (reset value is 100). These three bits are combined with the 4-bit SMARTDM device address to form 7-bit I^2C device address.

Control Register 2 Bit Summary (continued)

BIT	NAME	RESET VALUE	FUNCTION
D2	GPO	0	General-purpose output
D1-D0	HPC	00	Host port control bits. Write the following values into D1-D0 to select the appropriate configuration for two pins SDA and SCL. The SDA and SCL pins are used for I^2C interface if D1-D0 = 00. The SDA and SCL pins are used for S^2C interface if D1-D0 = 01. If D1-D0 = 10, the SDA pin = D2, input going into the SCL pin is output to DOUT (11), the SDA pin = control frame flag.

Control Register 3A (1)

D7	D6	D5	D4	D3	D2	D1	D0
00		PWDN		SWRS	ASRF		
R/W		R/W		R/W/S	R/W		

(1) NOTE: R = Read, W = Write

Control Register 3A Bit Summary

BIT	NAME	RESET VALUE	FUNCTION
D5-D4	PWDN	00	Power down PWDN = 00 No power down PWDN = 01 Power-down A/DPWDN = 10 Power-down D/APWDN = 11 Software power down the entire device
D3	SWRS	0	Software reset. Set this bit to 1 to reset the device.
D2-D0	ASRF	001	Asynchronous sampling rate factor. These three bits define the ratio n between FS frequency and the desired sampling frequency fs (Applied only if different sampling rate between CODEC1 and CODEC2 is desired) ASRF = 001, n = FS/fs = 1 ASRF = 010, n = FS/fs = 2 ASRF = 011, n = FS/fs = 3 ASRF = 100, n = FS/fs = 4 ASRF = 101, n = FS/fs = 5 ASRF = 110, n = FS/fs = 6 ASRF = 111, n = FS/fs = 7 ASRF = 000, n = FS/fs = 8

Control Register 3B (1)

D7	D6	D5	D4	D3	D2	D1	D0
01		8KBF	Reserved	MHNS	MHDS	MLDO	MSPK
R/W		R/W		R/W/S			

(1) NOTE: R = Read, W = Write

Control Register 3B Bit Summary

BIT	NAME	RESET VALUE	FUNCTION
D5	8KBF	0	8 kHz band pass filter. Set this bit to 1 to enable the band-bass filter [300 Hz -3.3 kHz] with the sampling rate at 8 kHz.
D4	Reserved	0	
D3	MHNS	0	Mute handset. This bit controls the MUTE function of handset output driver. MHNS = 0 Handset output driver is not MUTE. MHNS = 1 Handset output driver is MUTE.
D2	MHDS	0	Mute headset. This bit controls the MUTE function of headset output driver. MHDS = 0 Headset output driver is not MUTE. MHDS = 1 Headset output driver is MUTE.
D1	MLNO	0	Mute line output. This bit controls the MUTE function of the 600-Ω output driver. MLNO = 0 The 600-Ω output driver is not MUTE. MLNO = 1 The 600-Ω output driver is MUTE.
D0	MSPK	0	Mute 8-Ω speaker. This bit controls the MUTE function of the 8-Ω speaker driver. MSPK = 0 The 8-Ω speaker driver is not MUTE. MSPK = 1 The 8-Ω speaker driver is MUTE.

Control Register 3C(1)

D7	D6	D5	D4	D3	D2	D1	D0
10		Reserved	ICID			OSR	
R/W			R/W/S			R/W	

(1) NOTE: R = Read, W = Write, S = Shadowed

Control Register 3C Bit Summary

BIT	NAME	RESET VALUE	FUNCTION
D5	Reserved	0	
D4-D2	ICID	000	Chip ID. These two bits represent the device version number. ICID = 000 Version 1 ICID = 001 Version 2 ICID = 010 Version 3 ICID = 011 Version 4 ICID = 100 Version 5 ICID = 101 Version 6 ICID = 110 Version 7 ICID = 111 Version 8
D1-D0	OSR option	00	OSR option D1-D0 = X1 OSR for DAC Channel is 512 (Max FS = 8 Ksps) D1-D0 = 10 OSR for DAC Channel is 256 (Max FS = 16 Ksps) D1-D0 = 00 OSR for DAC Channel is 128 (Max FS = 26 Ksps)

Control Register 3D(1)

D7	D6	D5	D4	D3	D2	D1	D0
11		LCDAC					
R/W		R/W/S					

(1) NOTE: R = Read, W = Write, S = Shadowed

Control Register 3D Bit Summary

BIT	NAME	RESET VALUE	FUNCTION
D5-D0	LCDAC(1)	000000	LCD DAC. These bits represent the input value for the 6-bit LCD DAC.

(1) NOTE: See the Electrical Characteristics table for LCD DAC specification.

Control Register 4(1)

D7	D6	D5	D4	D3	D2	D1	D0
FSDIV	MNP						
R/W	R/W/S	R/W/S	R/W/S	R/W/S	R/W/S	R/W/S	R/W/S

(1) NOTE: R = Read, W = Write, S = Shadowed

Control Register 4 Bit Summary

BIT	NAME	RESET VALUE	FUNCTION
D7	FSDIV	0	Frame sync division factor FSDIV = 0 To write value of P to bits D2-D0 and value of N to bits D6-D3 FSDIV = 1 To write value of M to bits D6-D0

Control Register 4 Bit Summary (continued)

BIT	NAME	RESET VALUE	FUNCTION
D6-D0	MNP	—	Divider values of M, N, and P to be used in junction with the FSDIV bit for calculation of FS frequency according to the formula: FS = MCLK / (16 x M x N x P) where: M = 1, 2, .., 128 Determined by D6-D0 with FSDIV = 1 D7-D0 = 10000000 M = 128 D7-D0 = 10000001 M = 1 D7-D0 = 11111111 M = 127 N = 1, 2,.., 16 Determined by D6-D3 with FSDIV = 0, D6-D0 M, N, P D7-D0 = 00000xxx N = 16 D7-D0 = 00001xxx N = 1 D7-D0 = 01111xxx N = 15 P = 1, 2,.., 8 Determined by D2-D0 with FSDIV = 0 D7-D0 = 0xxxx000 P = 8 D7-D0 = 0xxxx001 P = 1 D7-D0 = 0xxxx111 P = 7

Control Register 5A (1)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	ADPGA					
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

(1) NOTE: R = Read, W = Write

Table 5. A/D PGA Gain

D5	D4	D3	D2	D1	D0	ADPGA
0	1	1	1	1	1	ADC input PGA gain = MUTE
0	1	1	1	1	0	ADC input PGA gain = 54 dB
0	1	1	1	0	1	ADC input PGA gain = 48 dB
0	1	1	1	0	0	ADC input PGA gain = 42 dB
0	1	1	0	1	1	ADC input PGA gain = 40.5 dB
0	1	1	0	1	0	ADC input PGA gain = 39 dB
0	1	1	0	0	1	ADC input PGA gain = 37.5 dB
0	1	1	0	0	0	ADC input PGA gain = 36 dB
0	1	0	1	1	1	ADC input PGA gain = 34.5 dB
0	1	0	1	1	0	ADC input PGA gain = 33 dB
0	1	0	1	0	1	ADC input PGA gain = 31.5 dB
0	1	0	1	0	0	ADC input PGA gain = 30 dB
0	1	0	0	1	1	ADC input PGA gain = 28.5 dB
0	1	0	0	1	0	ADC input PGA gain = 27 dB
0	1	0	0	0	1	ADC input PGA gain = 25.5 dB
0	1	0	0	0	0	ADC input PGA gain = 24 dB
0	0	1	1	1	1	ADC input PGA gain = 22.5 dB
0	0	1	1	1	0	ADC input PGA gain = 21 dB
0	0	1	1	0	1	ADC input PGA gain = 19.5 dB
0	0	1	1	0	0	ADC input PGA gain = 18 dB
0	0	1	0	1	1	ADC input PGA gain = 16.5 dB
0	0	1	0	1	0	ADC input PGA gain = 15 dB
0	0	1	0	0	1	ADC input PGA gain = 13.5 dB
0	0	1	0	0	0	ADC input PGA gain = 12 dB
0	0	0	1	1	1	ADC input PGA gain = 10.5 dB
0	0	0	1	1	0	ADC input PGA gain = 9 dB
0	0	0	1	0	1	ADC input PGA gain = 7.5 dB

Table 5. A/D PGA Gain (continued)

D5	D4	D3	D2	D1	D0	ADPGA
0	0	0	1	0	0	ADC input PGA gain = 6 dB
0	0	0	0	1	1	ADC input PGA gain = 4.5 dB
0	0	0	0	1	0	ADC input PGA gain = 3 dB
0	0	0	0	0	1	ADC input PGA gain = 1.5 dB
0	0	0	0	0	0	ADC input PGA gain = 0 dB

Control Register 5B(1)

D7	D6	D5	D4	D3	D2	D1	D0
0	1	DAPGA					
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

(1) NOTE: R = Read, W = Write

D/A PGA Gain

D5	D4	D3	D2	D1	D0	DAPGA
0	1	1	1	1	1	DAC input PGA gain = MUTE
0	1	1	1	1	0	DAC input PGA gain = -54 dB
0	1	1	1	0	1	DAC input PGA gain = -48 dB
0	1	1	1	0	0	DAC input PGA gain = -42 dB
0	1	1	0	1	1	DAC input PGA gain = -40.5 dB
0	1	1	0	1	0	DAC input PGA gain = -39 dB
0	1	1	0	0	1	DAC input PGA gain = -37.5 dB
0	1	1	0	0	0	DAC input PGA gain = -36 dB
0	1	0	1	1	1	DAC input PGA gain = -34.5 dB
0	1	0	1	1	0	DAC input PGA gain = -33 dB
0	1	0	1	0	1	DAC input PGA gain = -31.5 dB
0	1	0	1	0	0	DAC input PGA gain = -30 dB
0	1	0	0	1	1	DAC input PGA gain = -28.5 dB
0	1	0	0	1	0	DAC input PGA gain = -27 dB
0	1	0	0	0	1	DAC input PGA gain = -25.5 dB
0	1	0	0	0	0	DAC input PGA gain = -24 dB
0	0	1	1	1	1	DAC input PGA gain = -22.5 dB
0	0	1	1	1	0	DAC input PGA gain = -21 dB
0	0	1	1	0	1	DAC input PGA gain = -19.5 dB
0	0	1	1	0	0	DAC input PGA gain = -18 dB
0	0	1	0	1	1	DAC input PGA gain = -16.5 dB
0	0	1	0	1	0	DAC input PGA gain = -15 dB
0	0	1	0	0	1	DAC input PGA gain = -13.5 dB
0	0	1	0	0	0	DAC input PGA gain = -12 dB
0	0	0	1	1	1	DAC input PGA gain = -10.5 dB
0	0	0	1	1	0	DAC input PGA gain = -9 dB
0	0	0	1	0	1	DAC input PGA gain = -7.5 dB
0	0	0	1	0	0	DAC input PGA gain = -6 dB
0	0	0	0	1	1	DAC input PGA gain = -4.5 dB
0	0	0	0	1	0	DAC input PGA gain = -3 dB
0	0	0	0	0	1	DAC input PGA gain = -1.5 dB
0	0	0	0	0	0	DAC input PGA gain = 0 dB

Control Register 5C(1)

D7	D6	D5	D4	D3	D2	D1	D0
1	0	ASTG			DSTG		
	R/W	R/W	R/W	R/W	R/W	R/W	R/W

(1) NOTE: R = Read, W = Write

Analog Sidetone Gain

D5	D4	D3	DSTG
1	1	1	Analog sidetone gain = MUTE
1	1	0	Analog sidetone gain = -27 dB
1	0	1	Analog sidetone gain = -24 dB
1	0	0	Analog sidetone gain = -21 dB
0	1	1	Analog sidetone gain = -18 dB
0	1	0	Analog sidetone gain = -15 dB
0	0	1	Analog sidetone gain = -12 dB
0	0	0	Analog sidetone gain = -9 dB

Digital Sidetone Gain

D2	D1	D0	DSTG
1	1	1	Digital sidetone gain = MUTE
1	1	0	Digital sidetone gain = -27 dB
1	0	1	Digital sidetone gain = -24 dB
1	0	0	Digital sidetone gain = -21 dB
0	1	1	Digital sidetone gain = -18 dB
0	1	0	Digital sidetone gain = -15 dB
0	0	1	Digital sidetone gain = -12 dB
0	0	0	Digital sidetone gain = -9 dB

Control Register 5D(1)

D7	D6	D5	D4	D3	D2	D1	D0
1	1	SPKG		Reserved			
R/W	R/W	R/W/S		R/W			

(1) NOTE: R = Read, W = Write

Control Register 5D Bit Summary

BIT	NAME	RESET VALUE	FUNCTION
D5-D4	SPKG	00	Speaker Gain SPKG = 00 0 dB Gain SPKG = 01 1 dB Gain SPKG = 10 2 dB Gain SPKG = 11 3 dB Gain
D3-D0	Reserved	0000	

Control Register 6A(1)

D7	D6	D5	D4	D3	D2	D1	D0
0	HDSI2O	HNSI2O	CIDI	LINEI	MICI	HNSI	HDSI
R/W	R/W/S	R/W/S	R/W	R/W	R/W	R/W	R/W

(1) NOTE: R = Read, W = Write

Control Register 6A Bit Summary

BIT	NAME	RESET VALUE	FUNCTION
D6	HDSI2O	0	Headset input to output HDSI2O = 0 The headset input is not connected to the headset output. HDSI2O = 1 The headset input is connected to the headset output.
D5	HNSI2O	0	Handset input to output HNSI2O = 0 The handset input is not connected to the handset output. HNSI2O = 1 The handset input is connected to the handset output.
D4	CIDI	0	Caller ID input select CIDI = 0 The caller ID input is not connected to ADC channel. CIDI = 1 The caller ID input is connected to ADC channel.
D3	LINEI	0	Line input select LINEI = 0 The line driver input is not connected to ADC channel. LINEI = 1 The line driver input is connected to ADC channel.
D2	MICI	0	MIC input select MICI = 0 The microphone input is not connected to ADC channel. MICI = 1 The microphone input is connected to ADC channel.
D1	HNSI	0	Handset input select HNSI = 0 The handset input is not connected to ADC channel. HNSI = 1 The handset input is connected to ADC channel
D0	HDSI	0	Headset input select HDSI = 0 The headset input is not connected to ADC channel. HDSI = 1 The headset input is connected to ADC channel.

Control Register 6B(1)

D7	D6	D5	D4	D3	D2	D1	D0
1	Reserved	ASTOHD	ASTOHN	SPKO	LINEO	HNSO	HDSO
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W

(1) NOTE: R = Read, W = Write

Control Register 6B Bit Summary

BIT	NAME	RESET VALUE	FUNCTION
D6	Reserved	0	
D5	ASTOHD	0	Analog sidetone output select for headset. This bit connects the analog sidetone to headset output. ASTOHD = 0. The analog sidetone is not connected to headset output. ASTOHD = 1. The analog sidetone is connected to headset output.
D4	ASTOHN	0	Analog sidetone output select for handset. This bit connects the analog sidetone to handset output. ASTOHN = 0. The analog sidetone is not connected to handset output. ASTOHN = 1. The analog sidetone is connected to handset output.
D3	SPKO	0	Speaker output select. This bit connects the DAC output to the 8-Ω speaker driver SPKO = 0 The speaker driver output is not connected to DAC channel. SPKO = 1 The speaker driver output is connected to DAC channel.
D2	LINEO	0	Line output select. This bit connects the DAC output to the 600-Ω line driver LINEO = 0 The line driver output is not connected to DAC channel. LINEO = 1 The line driver output is connected to DAC channel.
D1	HNSO	0	Handset output select. This bit connects the DAC output to the 150-Ω handset driver HNSO = 0 The handset driver output is not connected to DAC channel. HNSO = 1 The handset driver output is connected to DAC channel.
D0	HDSO	0	Headset output select. This bit connects the DAC output to the 150-Ω headset driver HDSO = 0 The headset driver output is not connected to DAC channel. HDSO = 1 The headset driver output is connected to DAC channel.

Layout and Grounding Guidelines for TLV320AIC2x

TLV320AIC2x has a built-in analog antialias filter, which provides rejection to external noise at high frequencies that may couple into the device. Digital filters with high out-of-band attenuation also reject the external noise. If the differential inputs are used for the ADC channel, then the noise in the common-mode signal is also rejected by the high CMRR of TLV320AIC2x. Using external common-mode for microphone inputs also helps reject the external noise. However to extract the best performance from TLV320AIC2x, care must be taken in board design and layout to avoid coupling of external noise into the device.

TLV320AIC2x supports clock frequencies as high as 100 MHz. To avoid coupling of fast switching digital signals to analog signals, the digital and analog sections should be separated on the board. In TLV320AIC2x the digital and analog pins are kept separated to aid such a board layout. A separate analog ground plane must be used for the analog section of the board. The analog and digital ground planes should be shorted at only one place as close to TLV320AIC2x as possible. No digital trace should run under TLV320AIC2x to avoid coupling of external digital noise into the device. It is suggested to have the analog ground plane running below the TLV320AIC2x. The power-supplies must be decoupled close to the supply pins, preferably, with 0.1 µF ceramic capacitor and 10 µF tantalum capacitor following. The ground pin must be connected to the ground plane as close as possible to the TLV320AIC2x, so as to minimize any inductance in the path. Since the MCLK is expected to be a very high frequency signal, it is advisable to shield it with digital ground. For best performance of ADC in differential input mode, the differential signals must be routed close to each other in similar fashion, so that the noise coupling on both the signals is the same and can be rejected by the device.

Extra care has to be taken for the speaker driver outputs, as any trace resistance can cause a reduction in the maximum swing that can be seen at the speaker.

TLV320AIC2x-to-DSP Interface

The TLV320AIC2x interfaces gluelessly to the McBSP port of a C54x or C6x TI DSP. Figure 34 shows a single TLV320AIC2x connected to a C54x or C6x TI DSP.

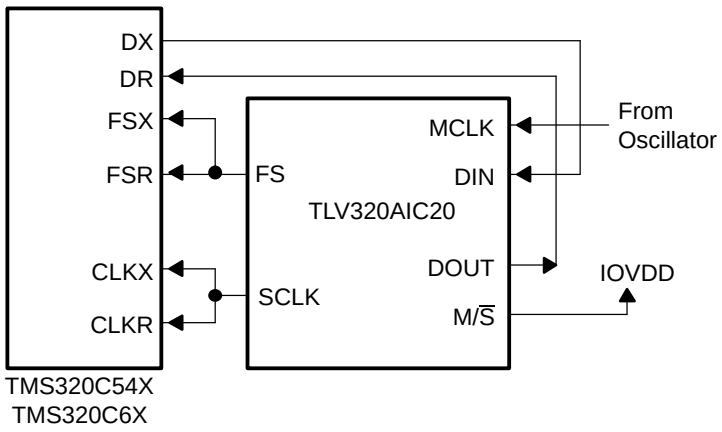


Figure 34. TLV320AIC2xs Interface to McBSP Port of C54x or C6x DSP

Hybrid Circuit External Connections

The TLV320AIC2x connected to the telephone line using the LINEI and LINEO hybrid circuit is shown in Figure 35.

Layout and Grounding Guidelines for TLV320AIC2x (continued)

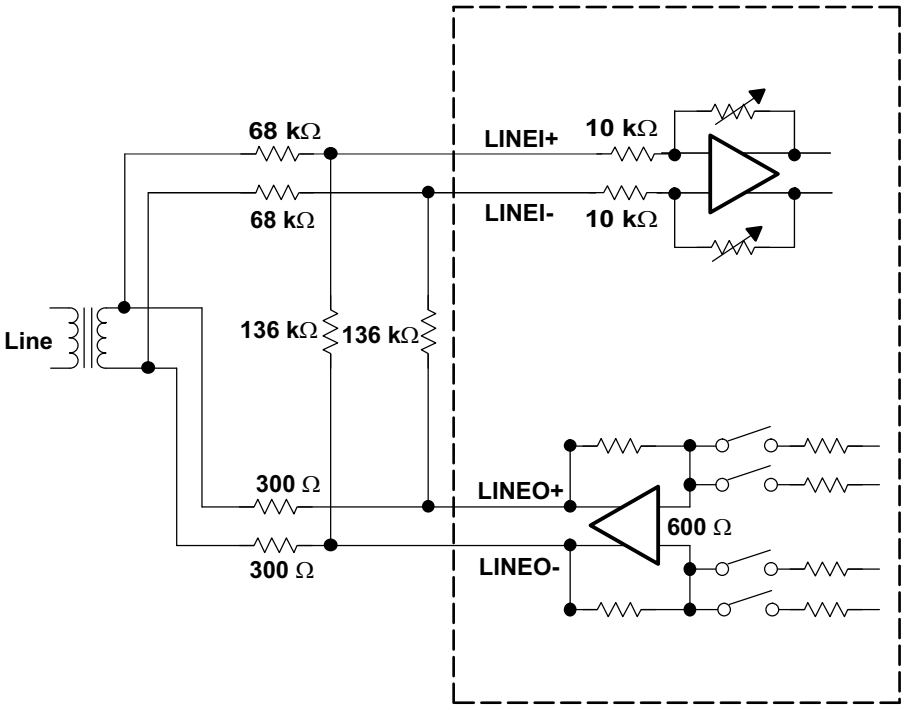


Figure 35. Hybrid Circuit External Connections

Microphone, Handset, and Headset External Connections

The microphone, headset, and handset external connections are shown in Figure 36. The suggested discrete components with their values also are included.

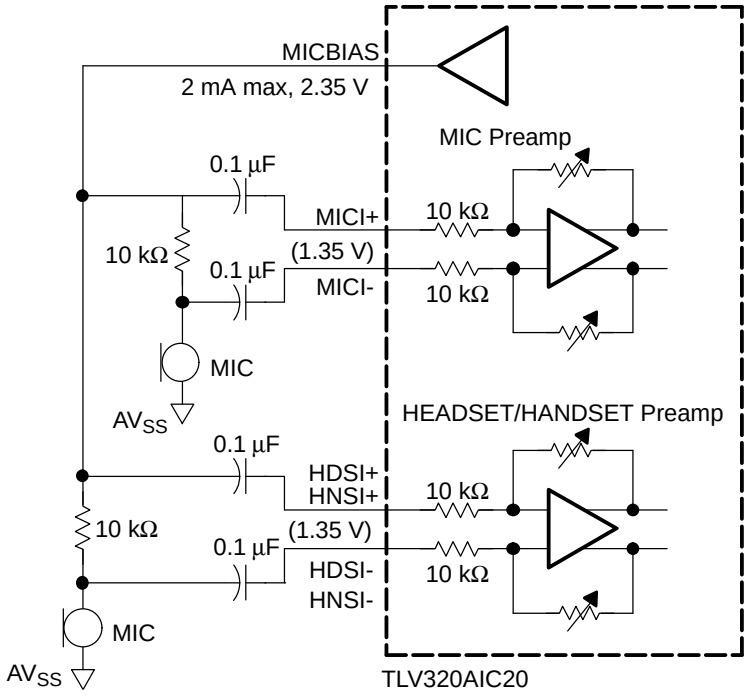


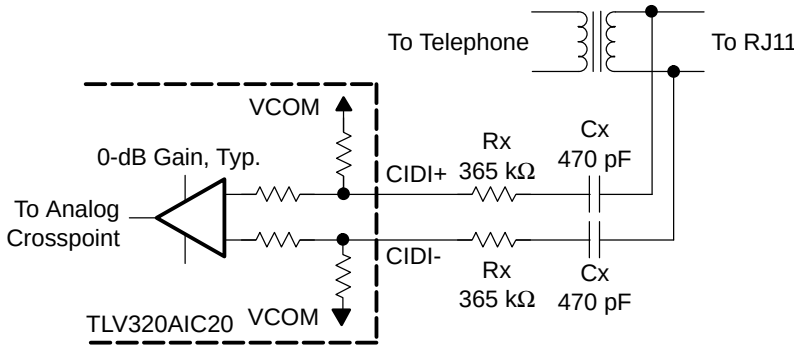
Figure 36. MIC/Handset/Headset External Connections

Layout and Grounding Guidelines for TLV320AIC2x (continued)

CallerID Interface

The callerID amplifier interface to the telephone line is shown in (A).

The value for Rx is 365 kΩ (E96 series, which has 1% tolerance). Cx is 470 pF (10% tolerance) of high-voltage rating. Voltage rating is decided based on the telecommunication standards of the country. The typical value is 1 kV. The callerID input can be used as a lower-performance line input. For this application, a larger value capacitor is required for Cx.

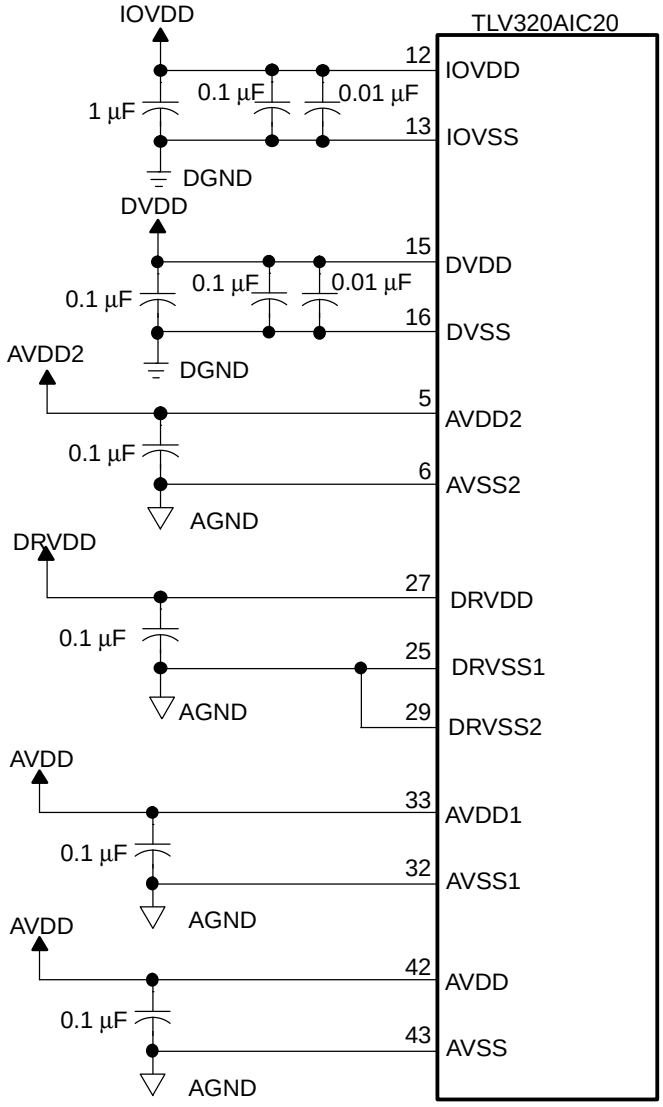


A. Typical Application Circuit for CallerID Amplifiers

Figure 37. Recommended Power-Supply Decoupling

The recommended power-supply decoupling for the TLV320AIC2x is shown in Figure 38. Both high frequency and bulk decoupling capacitors are suggested. The high-frequency capacitors should be X7R type capacitors or better. A 1-µF ceramic capacitor should be used to decouple the digital power supply.

Layout and Grounding Guidelines for TLV320AIC2x (continued)



DVDD = Digital Power
DGND = Digital Ground

AVDD/AVDD1/AVDD2= Analog Power
AGND = Analog Ground

DRVDD = Separate Analog Power

Figure 38. Recommended Decoupling

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
6PA24IPFBRG4	Active	Production	TQFP (PFB) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	320AIC24I
6PA24IPFBRG4.A	Active	Production	TQFP (PFB) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	320AIC24I
6PAIC20KIPFBRG4	Active	Production	TQFP (PFB) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	320AIC20K
6PAIC20KIPFBRG4.A	Active	Production	TQFP (PFB) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	320AIC20K
TLV320A24KIPFBRG4	Active	Production	TQFP (PFB) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	320AIC24K
TLV320AIC20CPFB	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	320AIC20C
TLV320AIC20CPFB.A	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	320AIC20C
TLV320AIC20IPFB	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	320AIC20I
TLV320AIC20IPFB.A	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	320AIC20I
TLV320AIC20IPFBG4	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	320AIC20I
TLV320AIC20IPFBG4.A	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	320AIC20I
TLV320AIC20IPFBR	Active	Production	TQFP (PFB) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	320AIC20I
TLV320AIC20IPFBR.A	Active	Production	TQFP (PFB) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	320AIC20I
TLV320AIC20KIPFB	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	320AIC20K
TLV320AIC20KIPFB.A	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	320AIC20K
TLV320AIC20KIPFBR	Active	Production	TQFP (PFB) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	320AIC20K
TLV320AIC20KIPFBR.A	Active	Production	TQFP (PFB) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	320AIC20K
TLV320AIC24CPFB	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	320AIC24C
TLV320AIC24CPFB.A	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	320AIC24C
TLV320AIC24CPFBG4	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	320AIC24C

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV320AIC24CPFBG4.A	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	320AIC24C
TLV320AIC24CPFBR	Active	Production	TQFP (PFB) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	320AIC24C
TLV320AIC24CPFBR.A	Active	Production	TQFP (PFB) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	320AIC24C
TLV320AIC24IPFB	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	320AIC24I
TLV320AIC24IPFB.A	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	320AIC24I
TLV320AIC24IPFBR	Active	Production	TQFP (PFB) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	320AIC24I
TLV320AIC24IPFBR.A	Active	Production	TQFP (PFB) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	320AIC24I
TLV320AIC24KIPFB	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	320AIC24K
TLV320AIC24KIPFB.A	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	320AIC24K
TLV320AIC24KIPFBG4	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	320AIC24K
TLV320AIC24KIPFBR	Active	Production	TQFP (PFB) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	320AIC24K
TLV320AIC24KIPFBR.A	Active	Production	TQFP (PFB) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	320AIC24K
TLV320AIC25CPFB	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	320AIC25C
TLV320AIC25CPFB.A	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	320AIC25C
TLV320AIC25CPFBG4	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	320AIC25C
TLV320AIC25CPFBG4.A	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	320AIC25C
TLV320AIC25CPFBR	Active	Production	TQFP (PFB) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	320AIC25C
TLV320AIC25CPFBR.A	Active	Production	TQFP (PFB) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	320AIC25C

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

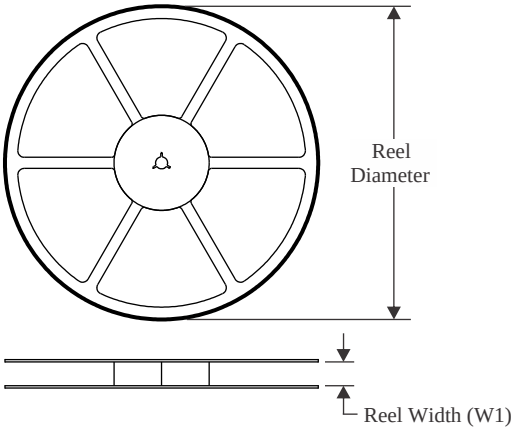
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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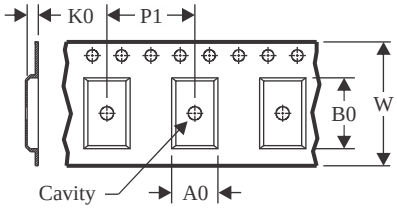
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

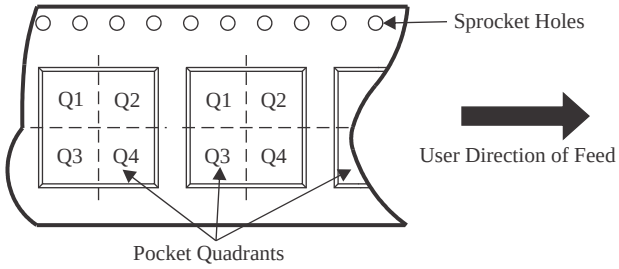


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

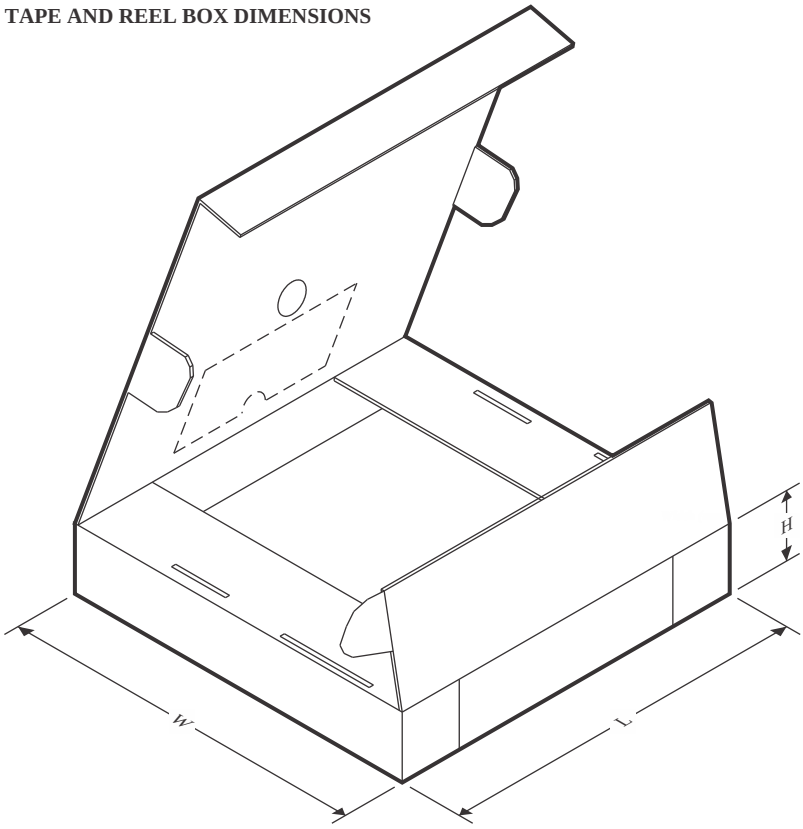
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
6PA24IPFBRG4	TQFP	PFB	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2
6PAIC20KIPFBRG4	TQFP	PFB	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2
TLV320AIC20IPFBR	TQFP	PFB	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2
TLV320AIC20KIPFBR	TQFP	PFB	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2
TLV320AIC24CPFBR	TQFP	PFB	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2
TLV320AIC24IPFBR	TQFP	PFB	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2
TLV320AIC24KIPFBR	TQFP	PFB	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2
TLV320AIC25CPFBR	TQFP	PFB	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2

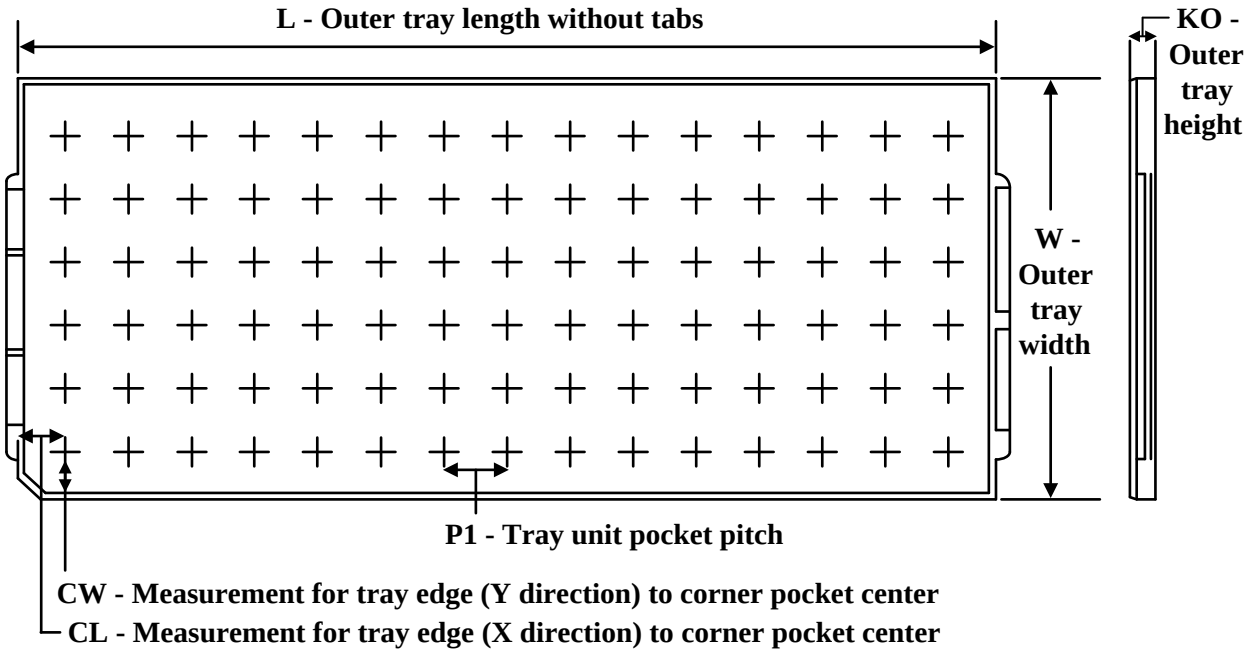
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
6PA24IPFBRG4	TQFP	PFB	48	1000	350.0	350.0	43.0
6PAIC20KIPFBRG4	TQFP	PFB	48	1000	350.0	350.0	43.0
TLV320AIC20IPFBR	TQFP	PFB	48	1000	350.0	350.0	43.0
TLV320AIC20KIPFBR	TQFP	PFB	48	1000	350.0	350.0	43.0
TLV320AIC24CPFBR	TQFP	PFB	48	1000	350.0	350.0	43.0
TLV320AIC24IPFBR	TQFP	PFB	48	1000	350.0	350.0	43.0
TLV320AIC24KIPFBR	TQFP	PFB	48	1000	350.0	350.0	43.0
TLV320AIC25CPFBR	TQFP	PFB	48	1000	350.0	350.0	43.0

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
TLV320AIC20CPFB	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
TLV320AIC20CPFB.A	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
TLV320AIC20IPFB	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
TLV320AIC20IPFB.A	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
TLV320AIC20IPFBG4	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
TLV320AIC20IPFBG4.A	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
TLV320AIC20KIPFB	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
TLV320AIC20KIPFB.A	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
TLV320AIC24CPFB	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
TLV320AIC24CPFB.A	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
TLV320AIC24CPFBG4	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
TLV320AIC24CPFBG4.A	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
TLV320AIC24IPFB	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
TLV320AIC24IPFB.A	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
TLV320AIC24KIPFB	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
TLV320AIC24KIPFB.A	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
TLV320AIC24KIPFBG4	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25

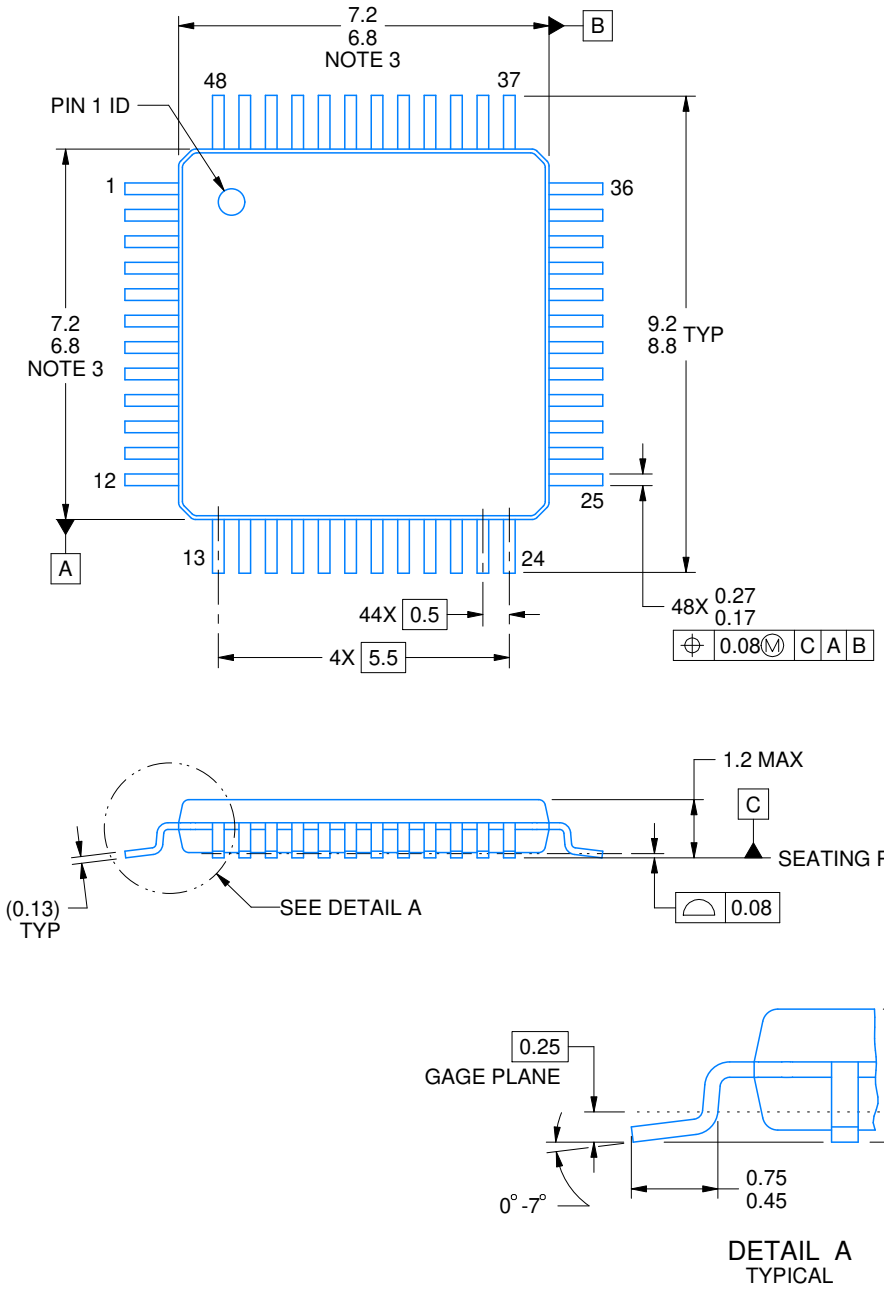
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
TLV320AIC25CPFB	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
TLV320AIC25CPFB.A	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
TLV320AIC25CPFBG4	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
TLV320AIC25CPFBG4.A	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25

PACKAGE OUTLINE

PFB0048A

TQFP - 1.2 mm max height

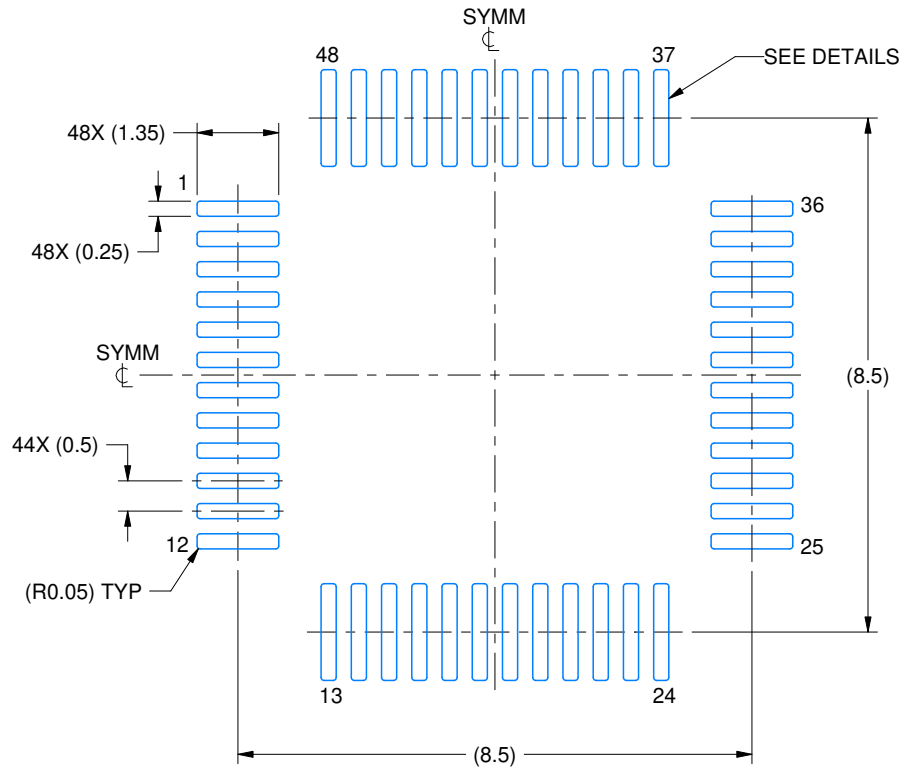
PLASTIC QUAD FLATPACK



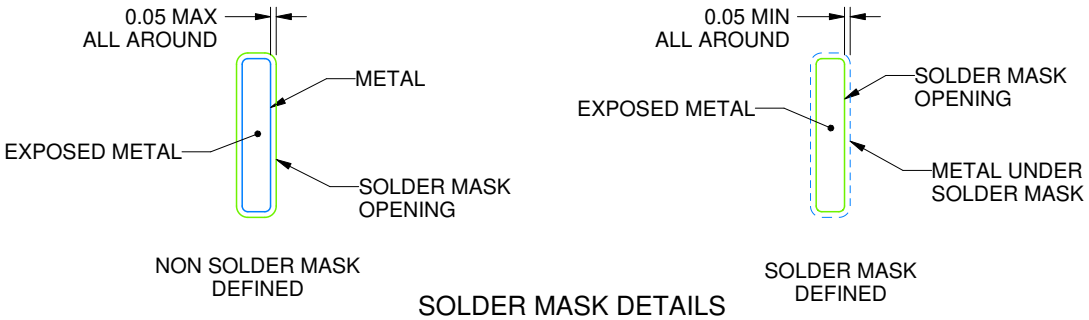
4215157/A 03/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

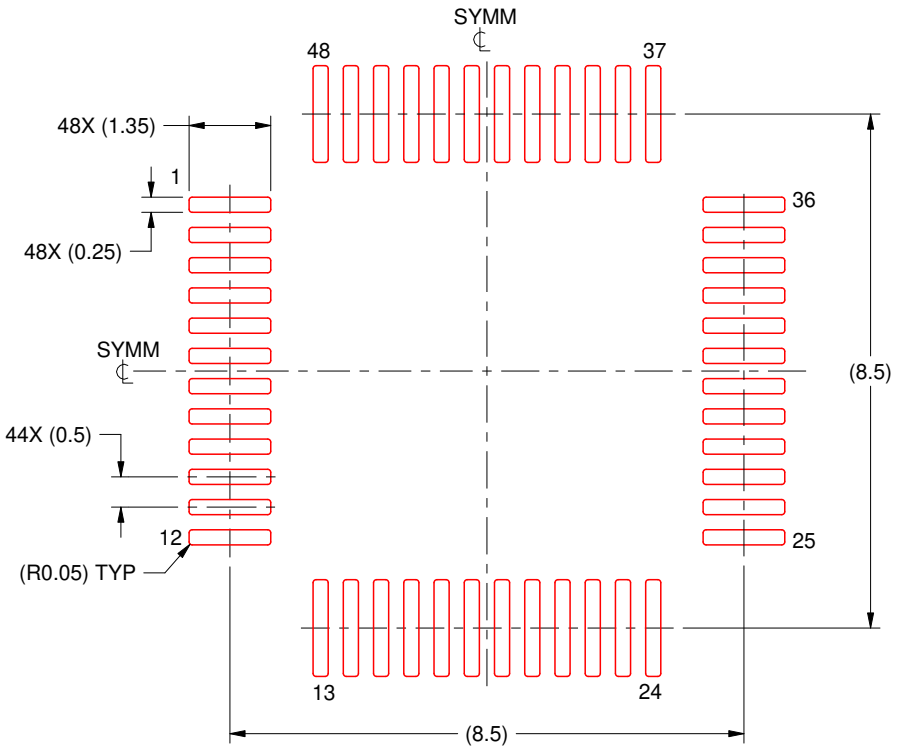


SOLDER MASK DETAILS

4215157/A 03/2024

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
SCALE:8X

4215157/A 03/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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