TEXAS INSTRUMENTS

Evaluation Module

User's Guide

October 2002

DAC Digital Audio/Speaker

SLEA006

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It is important to operate this EVM within the input voltage range of 26.5V and the output voltage range of 100 mV and 10 V rms.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

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During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Preface

Read This First

About This Manual

This application report describes the operation of the TAS5101SE EVM. For proper operation, the TAS5101SE EVM requires an accessory card, DAV-EQ102, to provide analog or S/PDIF inputs, volume control, and equalization functions. The DAV-EQ102 volume and equalization are handled by an onboard TAS3103. This document contains descriptions and schematics for a stereo application. The board described is an example design that can be customized for specific applications.

How to Use This Manual

This manual takes the reader through the considerations for designing a single-ended amplifier using the TAS5101 output stage.

Notational Conventions

The name TAS5101SE EVM is used synonymously with DA-REF210.

Related Documentation From Texas Instruments

- *True Digital Audio Amplifier TAS5010 Digital Audio PWM Processor* data sheet, Literature number SLAS328
- *AS5101 True Digital Stereo Audio Amplifier With PWM Stereo Power Output Stage* data sheet, Literature number SLES039
- Digital Amplifier Design Guide, Literature number SLAS117
- *Digital Audio Measurements* application report, Literature number SLAA114

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Quick-Start Guide (With DAVEQ-102)

Overview

The unit is composed of two boards, a controller board and a digital amplifier board. The controller board contains the circuitry for analog input (PCM1802), S/PDIF coaxial input, or TOSLINK input (DIR1703), a TAS3013 digital audio processor, and a PIC12C671 microcontroller. The unit is shipped with the volume adjusted by varying the H-bridge drive (PVDD) power supply from 12 to 26.5 V. However, the TAS3103 digital audio processor can be enabled and used to provide volume control and other audio processing functions such as filtering, audio enhancement, and audio delay. The microcontroller performs general-purpose housekeeping functions such as power-on reset and amplifier closed-loop control.

There is a red LED on the controller board. The red LED is lit when 12 to 26.5-V dc has been applied to the board and the amplifier has been enabled. A blinking red LED indicates that an undervoltage, overcurrent, or overtemperature error has occurred.

Startup

1) Select the audio input source using the jumpers close to the connectors that connect the controller board to the amplifier board. Jumper identification is silkscreened on the surface of the board.

2) Connect a source of 8 V dc to J4 on the controller board, using the supplied cable.

3) Connect a source of 12 to 26.5 V dc to the amplifier board PVDD connector, using the supplied cable.

4) Connect speakers to the speaker terminals on the amplifier board, using the supplied cables.

5) Connect a source of audio. Turn on the 8-V dc power supply.

6) Turn on the 12 to 26.5-V dc PVDD power supply.

7) Press the ON button on the controller (near the J4 connector) to enable the output.

8) Play audio.

Power Off

1) Stop the audio.

2) Press the button on the controller board to mute the output.

3) Turn off the 26.5-V dc power supply.

4) Turn off the 8-V dc power supply.

S/PDIF Inputs to the DIR1703 Receiver

The S/PDIF input can be either TOSLINK or coaxial. The DIR1703 automatically selects the input that is connected. If both inputs are connected simultaneously, the DIR1703 does not lock and there is no output.

The system must be configured for the S/PDIF (JP5 in, JP6 out, and JP7 out) or for the DAP (JP5 out, JP6 in, and JP7 out) to enable S/PDIF input. If the DAP is used, it must be controlled by the TAS3103 EVM software GUI.

Analog Input to the PCM1802 Analog-to-Digital Converter

The stacked RCA connectors on the controller board are the analog input connectors. It has several different gain settings (see the schematic of the DAVEQ-102). The input circuit is currently jumpered for 1.1 V rms, full-scale.

The system must be configured for the ADC (JP5 out, JP6 out, JP7 in) or for the DAP (JP5 out, JP6 in, and JP7 out) to accept analog input. If the DAP is used, it must be controlled by the TAS3103 EVM software GUI.

TAS3013 Digital Audio Processor

To use the TAS3103, disconnect JP5 and JP7, and connect JP6. In addition, the GUI cable must be connected to a parallel port on a PC running Windows 98. The TAS3103 is controlled using the TAS3103 EVM GUI program with the appropriate configuration files for this system.

The EVM GUI program is contained in the program CD. The CD also contains the instructions for installation and operation.

During operation, the SDIN1 mixer controls the S/PDIF and TOSLINK data inputs. The SDIN2 mixer controls the analog input data and must be enabled with a new configuration file.

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Chapter 1

TAS5101SE EVM Input Description

This chapter describes the digital inputs to the TAS5101SE EVM.

1.1 Description of Data Inputs

The input to the TAS5101SE evaluation module (EVM) is a 22-pin connector (J1) with 0.1” pin spacing. It contains the digital audio input port (I^2S), a reset signal for the TAS5010 modulator, and the $\overline{\text{SHUTDOWN}}$ output signal from the TAS5101. It contains the 3.3-V logic power supply input for the board. There is also a digital input, DBSPD, that signals the TAS5010 modulator when the sample rate exceeds 96 KHz.

Additionally, the other end of the board contains a 2-pin connector for the PVDD 12-V to 27-V power supply.

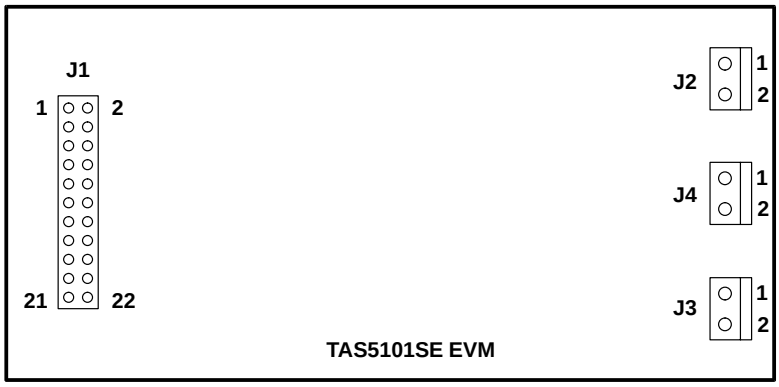
Table 1–1. Input Connector (J1) Pin Functions

Pin	Name	Function
1	PVDD	PVDD output to controller board, *do not attempt to power this PCB from this pin.*
2	DGND	Digital ground for logic signals
3	DGND	Digital ground for logic signals
4	+3.3 V-In	Digital power supply input
5	DGND	Digital ground for logic signals
6	+3.3 V-In	Digital power supply input
7	DGND	Digital ground for logic signals
8	$\overline{\text{SHUTDOWN}}$	Fault indication from TAS5101; set low by short circuit, overtemperature, etc.
9	DGND	Digital ground for logic signals
10	$\overline{\text{RESET_5K}}$	Logic low resets the TAS5010 modulator
11	DGND	Digital ground for logic signals
12	MCLK_IN	Master clock for digital audio input
13	DGND	Digital ground for logic signals
14	$\overline{\text{POWERDOWN}}$	Logic low puts the TAS5010 modulator in power-down (low current) mode
15	DGND	Digital ground for logic signals
16	DBSPD	Logic high signals TAS5010 modulator the presence of a sample rate > 48 kHz
17	DGND	Digital ground for logic signals
18	$\overline{\text{MUTE}}$	Logic low stops the PWM data from the TAS5010 to the TAS5101
19	DGND	Digital ground for logic signals
20	SCLK	Bit clock for audio data
21	SDIN	Digital audio data
22	LRCLK	Digital audio frame sync, signals either right or left channel data

1.2 Description of Power Inputs

A 2-pin connector, J4, is placed between the speaker output connectors. It is the power input connector (PVDD connector).

Figure 1–1. Connector Diagram



Chapter 2

Description of Outputs

Because this is a stereo audio amplifier, there are two outputs, the right and left audio channels. This amplifier can drive a 4-Ω load to greater than 15 W rms with less than 0.1% distortion.

Two 2-pin connectors, J2 and J3, are placed on either side of the power input connector (PVDD connector). They are the speaker output connectors.

Connect the speakers/load resistors as shown in Figure 2–1.

Figure 2–1. TAS5101SE EVM Output Connectors

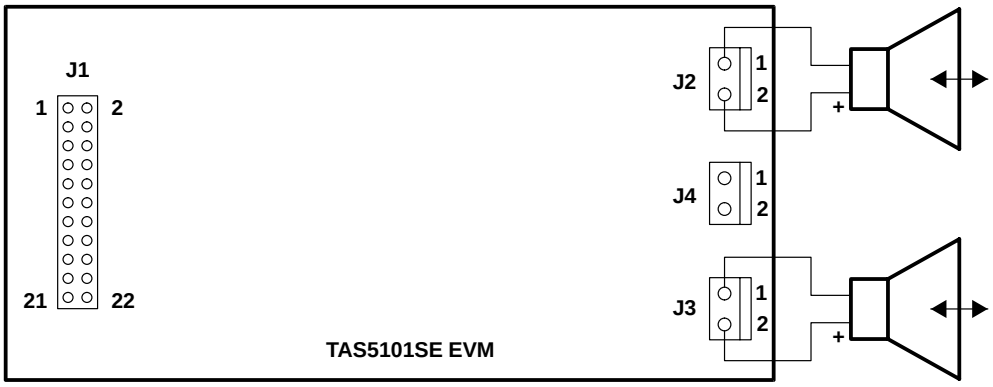


Table 2–1. Left Speaker Output (J2)

Pin	Name	Function
1	PVDD/2	Pseudo differential connection point for speaker
2	Output_L	Left audio output to speaker

Table 2–2. Right Speaker Output (J3)

Pin	Name	Function
1	PVDD/2	Pseudo differential connection point for speaker
2	Output_R	Right audio output to speaker

Chapter 3

Powering the TAS5101SE EVM

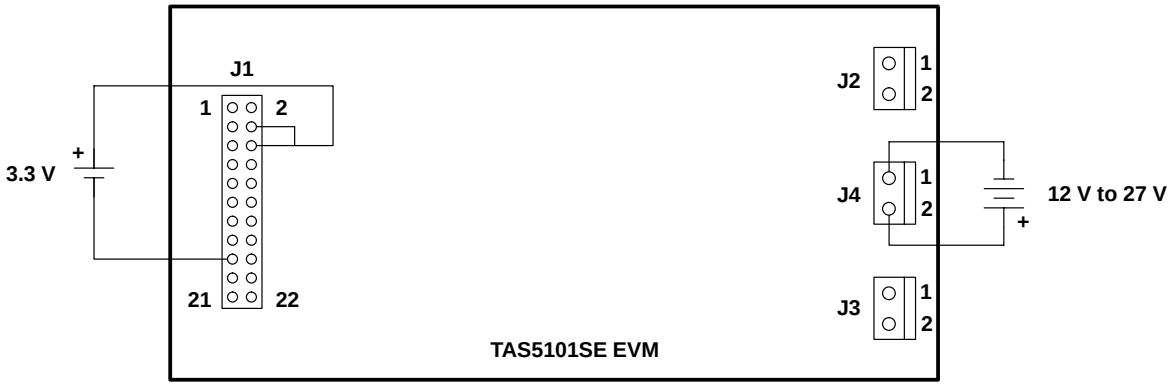
3.1 Power Supplies

The system requires two power supplies, PVDD and DVDD. PVDD is the power for the output stage and is generally 12 V to 27 V dc. It should be capable of supplying at least 2 A to allow adequate margin for full power operation under the various speaker impedances from 4 Ω to 8 Ω. The ripple and noise should be as low as possible; however, little or no performance degradation occurs when power supply ripple and noise is limited to less than 150 mV rms.

DVDD supplies 3.3 V to the digital logic in the TAS5010 and the TAS5101. The combination of both integrated circuits draws less than 50 mA. For optimum performance, the ripple and noise should be less than 50 mV rms.

3.2 Power Supply Connection

Figure 3–1. Power Supply Connections



With the power supplies turned off:

1) Connect the source of PVDD to J4. Pin 2 is positive.

2) Connect the source of DVDD to J1. Pins 4 and 6 are positive.

Table 3–1. Main Power Input Connector (J4)

Pin	Name	Function
1	PVSS	Output power ground
2	PVDD	Output stage power supply (12 V to 27 V)

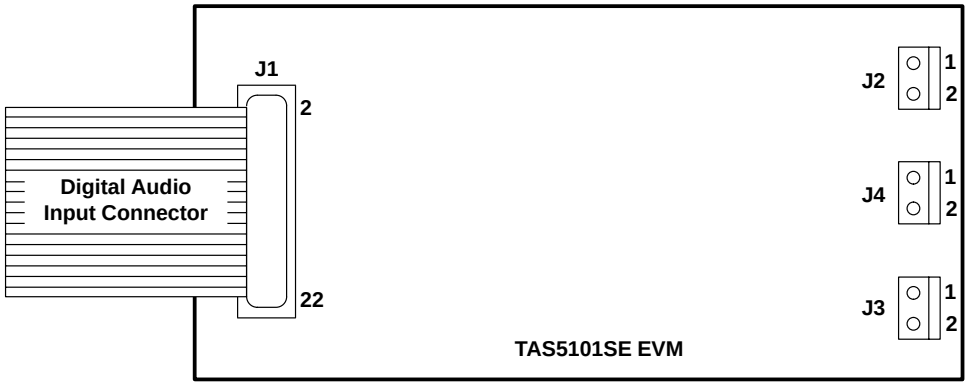
Chapter 4

Digital Audio Input/Interface

The TAS5101SE EVM supports many common digital audio input formats.

Connect a source of digital audio (I^2S, unless the board has been reconfigured for another format) to J1, as shown in Figure 4–1.

Figure 4–1. Digital Audio Input Connection (J1)



4.1 Changing the Audio Input Format

The bottom of the board contains a grouping of R0603 resistor pads that determine the audio input format. The TAS5101SE EVM is shipped configured for I^2S format. To change the format, move/replace the resistors as described in Table 4–1.

Table 4–1. Audio Input Jumper Options

Mode	MOD2	MOD1	MOD0	Format
0	R3A = open/R3B = 0 Ω	R2A = open/R2B = 0 Ω	R1A = open/R1B = 0 Ω	16-bit; MSB first; right justified
1	R3A = open/R3B = 0 Ω	R2A = open/R2B = 0 Ω	R1A = 10 kΩ/R1B = open	20-bit, MSB first; right justified
2	R3A = open/R3B = 0 Ω	R2A = 10 kΩ/R2B = open	R1A = open/R1B = 0 Ω	24-bit; MSB first; right justified
3	R3A = open/R3B = 0 Ω	R2A = 10 kΩ/R2B = open	R1A = 10 kΩ/R1B = open	16-bit; I^2S
4	R3A = 10 kΩ/R3B = open	R2A = open/R2B = 0 Ω	R1A = open/R1B = 0 Ω	20-bit; I^2S
5	R3A = 10 kΩ/R3B = open	R2A = open/R2B = 0 Ω	R1A = 10 kΩ/R1B = open	24-bit I^2S
6	R3A = 10 kΩ/R3B = open	R2A = 10 kΩ/R2B = open	R1A = open/R1B = 0 Ω	16-bit; MSB first; left justified
7	R3A = 10 kΩ/R3B = open	R2A = 10 kΩ/R2B = open	R1A = 10 kΩ/R1B = open	16-bit; DSP frame

4.2 Interfacing the TAS5101SE EVM

As discussed in previous sections, a source of digital audio connected to J1 is required to get an audio output from the TAS5101SE EVM.

4.3 Description of Control Signals

4.3.1 $\overline{\text{SHUTDOWN}}$

A logic low on J1 pin 8 signals that the TAS5101 has been shut down by an error condition, such as a short circuit, overtemperature, or a low-voltage condition. A reset signal must be sent to J1 pin 10 to clear this condition. $\overline{\text{SHUTDOWN}}$ is generally used, along with $\overline{\text{RESET_5K}}$, in conjunction with the system controller (microcontroller) to implement a closed-loop control system for error reset. The system controller provides a delay of approximately 4 mS between error and resetting. Lastly, the system controller can be used to turn off the amplifier if error conditions persist.

4.3.2 $\overline{\text{RESET_5K}}$

A logic low on J1 pin 10 resets the TAS5010 modulator, which in turn resets the TAS5101. This signal is used to initialize the TAS5010 for operation and to reset error conditions, when they occur, on the TAS5101.

4.3.3 $\overline{\text{POWERDOWN}}$ (Active Low)

A logic low on J1 pin 14 places the TAS5010 modulator in the low-power (power-down) mode.

4.3.4 DBSPD (Double Speed)

A logic high on J1 pin 16 signals the TAS5010 modulator that a sampling frequency in excess of 96 kHz is being used.

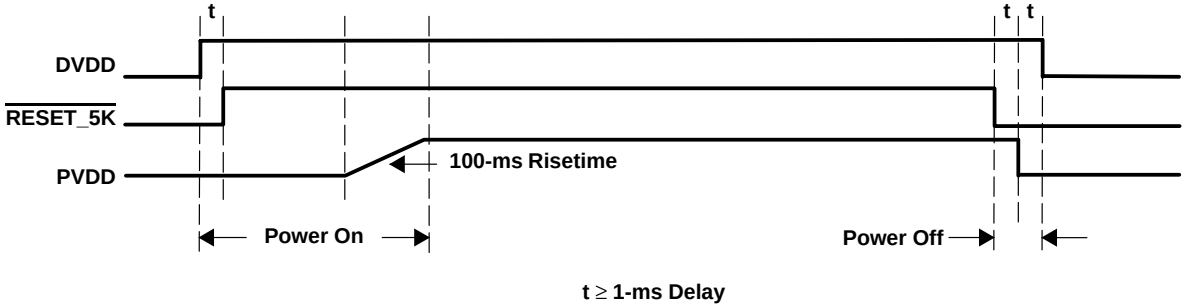
4.3.5 $\overline{\text{MUTE}}$

A logic low on J1 pin 18 signals the TAS5010 modulator to mute.

4.4 Power-On Sequence

1) Ensure that the $\overline{\text{RESET_5K}}$ input is low.
2) With the digital audio off, turn on the PVDD power supply and wait 1 s for the output capacitors to charge.
3) Turn on the DVDD power supply and allow it to stabilize, approximately 0.5 s.
4) Set $\overline{\text{RESET_5K}}$ high.
5) Enable the digital audio input data.
6) Listen to the audio or measure it.

Figure 4–2. Power-On Sequence



4.5 Power-Off Sequence

1) Stop the digital audio.
2) Set the $\overline{\text{RESET_5K}}$ signal low.
3) Turn off the DVDD power supply and wait for approximately 0.5 s.
4) Turn off the PVDD power supply.

Chapter 5

Technical Description

This chapter describes the operation of the functional sections of the TAS5101SE EVM. See the schematics in Appendix A for reference.

5.1 Audio Input Section

Digital audio input is applied to the TAS5101SE EVM through J1. The standard signals, MCLK, SCLK, LRCLK, and SDIN are connected to the TAS5010 (U1). The digital audio modes, left-justified, right-justified, and I^2S are set by resistor jumper options on the bottom of the PCB. Table 4–1 describes the installation options for the mode resistors.

The TAS5010 converts the digital audio input to PWM output signals for the TAS5101. It also supplies the $\overline{\text{VALID}}$ signal that is used for $\overline{\text{RESET}}$ and $\overline{\text{HiZ}}$ on the TAS5101.

5.2 Audio Output

After receiving the PWM input on pins 1, 2, 15, and 16, the TAS5101 amplifies the PWM signal for a high-current output to the load (speaker).

Left Channel Demodulation:
Pins 27 and 28 are connected in parallel and should be connected together on the PCB. The high-current PWM passes to the demodulation filter consisting of L1 and C15. The values 10 µH and 1 µF work well in this application; however, they can be changed as necessary, provided that the new filter provides adequate attenuation at the modulation frequency (384 kHz) and does not exhibit excessive Q (which would cause peaks in the audio frequency response).

Right Channel Demodulation:
Because this is a stereo application, the same criteria for operation apply to both channels.

The bootstrap capacitors, C4 and C7, provide a low-noise voltage source to the high-side gate drive MOSFETs and help to minimize the number of external, high-voltage supplies necessary to power the device. The value of these capacitors works well at 0.033 µF. If the value of these capacitors is

increased, the TAS5101 may not power up properly because of the slower charge time of a larger capacitor. If the value is decreased, noise problems may be encountered.

The value of the LDR capacitors, C37 and C39, should be left at 0.1 μF. As mentioned in the discussion of the bootstrap capacitors, there is a trade-off between amplifier noise performance and capacitor charge time. The LDRs provide bias voltage for internal components and are used to minimize additional external power supplies. One should not attempt to use these LDRs to drive external circuitry.

5.3 Power Supplies

The TAS5101SE EVM requires two power supply voltages, a 3.3-V logic supply (DVDD) and a PVDD output power supply (18 V to 27 V).

A 12-V to 27-V power supply is applied to all of the points in the circuit above labeled PVDD. A slight amount of confusion could result from the convention of naming the voltage on each of the 45-nH inductors PVDD. This was done because the 45-nH inductors are actually PCB traces approximately 2” long by 0.06” wide in 2-oz. copper. (See SLAA117 for more details.) They are part of tuned circuits that, along with the snubber circuits, and the PVDD bulk capacitor C26 (if used), help to reduce EMI and improve the THD+N performance of the amplifier. If used, the PVDD bulk capacitor should be a low-ESR type. The Panasonic FC series works well in this application, but other low-ESR capacitors may be acceptable.

By using two 470-μF capacitors in series as a pseudo differential output, the power supply rejection (PSRR) is improved to greater than 50 dB; however, crosstalk isolation is decreased to about 27 dB. In many applications, this is adequate. Also, the PVDD bulk capacitor can be eliminated (1500 μF at 35 V) in order to reduce cost. Under the condition of no PVDD bulk capacitor, the amplifier generally meets its THD+N specification of better than 0.1% to within –3 dB of full output. From –3 dB to full output, the distortion rises to about 0.25%.

The crosstalk isolation of the pseudo differential configuration, discussed previously, can be improved by using two pairs of 470-μF capacitors, one pair for each of the channels. This configuration maintains the PSRR and increases the channel separation.

The final configuration to be considered is a large capacitor, 470 μF or larger, in series with each output and a PVDD bulk capacitor of 1500 μF or greater. This gives good channel separation; however, the PSRR suffers and more consideration must be given to the PVDD power supply.

PCB Layout Consideration

Because PCB layout varies from application to application, the snubber network is generally tuned for a particular PCB. In order to tune the snubber network, monitor the PWM output at the TAS5101 pins with a fast oscilloscope. The probe should have a very short ground. Record the value of overshoot and

undershoot. Then change the values of the snubber resistors and capacitors to reduce the overshoot and undershoot. Resistor values can vary between 0.5 Ω and 2.7 Ω. Resistors should be of the MELF or mini-MELF type. Capacitor values can vary between 0.1 μF and 0.27μF. Caution should be exercised when tuning the snubber network, because device reliability can be affected (see SLAA117 for details).

When reviewing the Gerber files contained in this document, notice the large number of vias that connect the top ground plane to the bottom ground plane. These vias provide a very low-impedance RF connection between the planes. This connection improves the audio performance and also reduces EMI radiation from the board.

Decoupling capacitors were placed on all power pins on the TAS5101 and the TAS5010 with a goal of no more than 0.050” trace length in the decoupling path.

5.4 Power-On/-Off Depop Circuit

Power On

Refer to the schematics in Section 7 for reference.

In order to prevent speaker artifacts (pops) at power on and power off, the following technique is used.

$\overline{\text{RESET_5K}}$ is held low prior to applying power. This causes $\overline{\text{VALID}}$ from the TAS5010 to stay low. This action holds the TAS5101 in reset. Because $\overline{\text{HiZ}}$ is connected to $\overline{\text{VALID}}$, the output of the TAS5101 is high-impedance when power is applied.

DVDD is then enabled to the TAS5101. Applying DVDD first ensures that no errors occur which could cause audio artifacts or damage the device.

Simultaneously, the unregulated power supply to the DVDD voltage regulator, generally about 8 V, is applied to CR1, CR2, and CR3. Applying this voltage to CR3 places a bias voltage on the LDRs in the TAS5101. Prebiasing the LDRs allows them to provide a small amount of gate bias to the output MOSFETs. This prevents an erroneous transition in the output that can cause a pop.

Because the LDRs are active, current flows out of PVDD2 into PVDD1 (if PVDD1 and PVDD2 are connected together). This causes the outputs to slowly rise to the bias voltage/2. In the case of a power supply with an output that rises rapidly, internal protection circuits may be activated momentarily. This does not harm the TAS5101; however, a pop can occur. CR1 and CR2 have been placed in series with the PVDD2 power supplies to eliminate this condition.

After DVDD has been enabled for about 100 ms, PVDD can be turned on without audio artifacts.

After PVDD has stabilized, $\overline{\text{RESET_5K}}$ can be set high and audio can be sent to the EVM.

When valid audio data is received by the TAS5010, the signal $\overline{\text{VALID}}$ goes high. This action sets $\overline{\text{HiZ}}$ and Pin 14, $\overline{\text{RESET_MUTE}}$ high. The TAS5101 begins to modulate its output.

After valid audio clocks are removed from the TAS5010 $\overline{\text{VALID}}$ goes low. This operation immediately asserts $\overline{\text{HiZ}}$ low and $\overline{\text{RESET}}$ low. The net effect of $\overline{\text{VALID}}$ going low is to make $\overline{\text{HiZ}}$ and $\overline{\text{RESET}}$ at approximately the same time.

The second part of eliminating/reducing power-on artifacts is to ensure that the output bias circuit is charged at power on. The voltage dividers consisting of R33/R34, R32/R29, and R23/R24 place PVDD/2 on each side of the output. Because the voltage is the same on each side of the load, the differential voltage is zero.

The charge time of the circuit is greater than one second, so the charging of the output capacitors, C3 and C5, does not produce any audible artifacts.

Power Off

To remove power from the system, stop the audio data and clear the signal $\overline{\text{RESET_5K}}$ low. Then turn off PVDD, followed shortly thereafter by DVDD. The output capacitors, C3 and C5, slowly discharge through R24, R32, and R34.

5.5 Calculating Low-Frequency Response

Because the output circuit, made up of C3 and C5, is an ac-coupled psuedo differential configuration, the output of the amplifier is controlled by the cutoff

The low frequency response of the amplifier, $f_{-3dB\ low}$, can be calculated by the equation:frequency of these two capacitors.

$$f_{-3\ dB\ low} = 1/[(2\pi)\times R_L\times(C3||C4)]$$

The voltage rating of these capacitors is PVDD/2, because of the voltage divider made up of R23 and R24. Of course, some margin should be allowed for ambient temperature rise and normal derating.

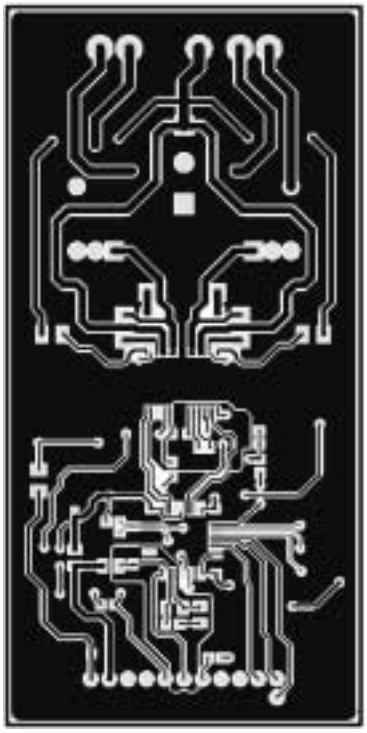
Chapter 6

Printed-Circuit Board Layout

As with any high-performance device operating at high frequency, PCB layout is extremely important. The TAS5101SE EVM PCB is fabricated from two-layer, 0.062” FR4 glass epoxy material with 2-oz. copper foil. It is 1.9” by 3.9”. Care has been taken to pour copper around all traces and good design practices have been used for trace layout. The PVDD circuit has been optimized for layout considerations. A solid ground plane was used and many vias were added to ensure excellent connection between the top and bottom layers. These vias improve thermal performance and reduce EMI. The top and bottom layers are continuous around the perimeter of both layers. Plane splits were used for AVDD, the power supply for the TAS5010 PLL, and also to allow DVSS to remain clean and minimize switching noise that can cause ground bounce.

6.1 Component Side (Top Layer)

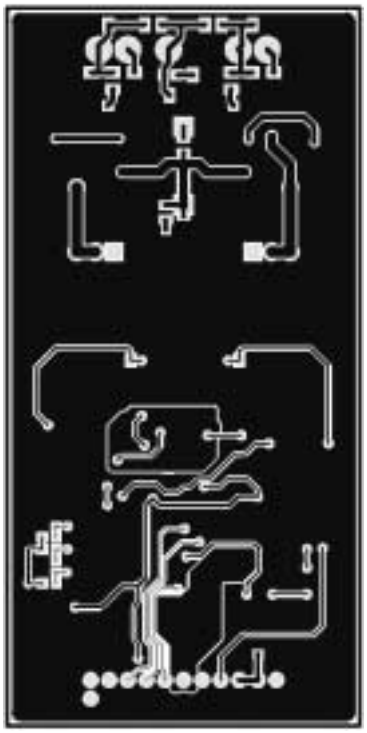
Figure 6–1. PCB Top Layer



6.2 PCB Bottom Layer

This is a view of the bottom of the TAS5101SE EVM as one would see it by looking through the top of the board. This view is presented to allow the top and bottom layers to be placed on top of each other and the pads aligned.

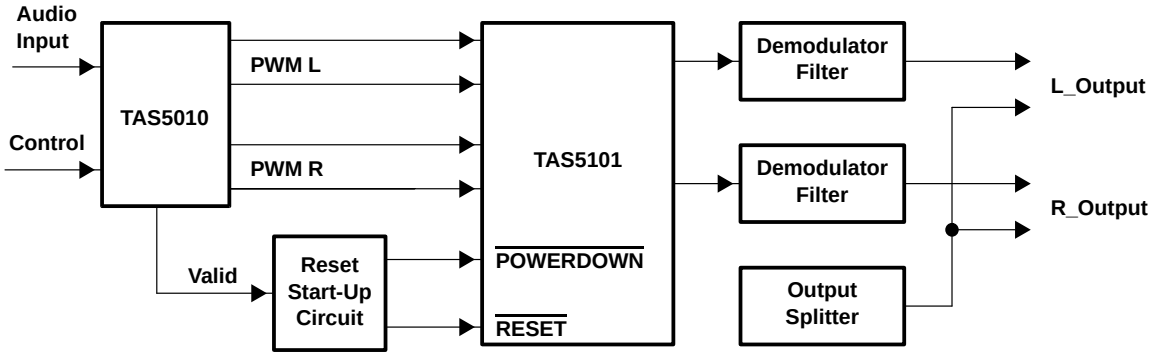
Figure 6–2. PCB Bottom Layer



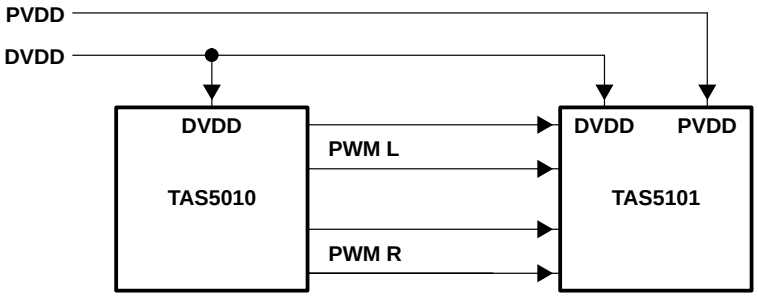
Chapter 7

Schematics

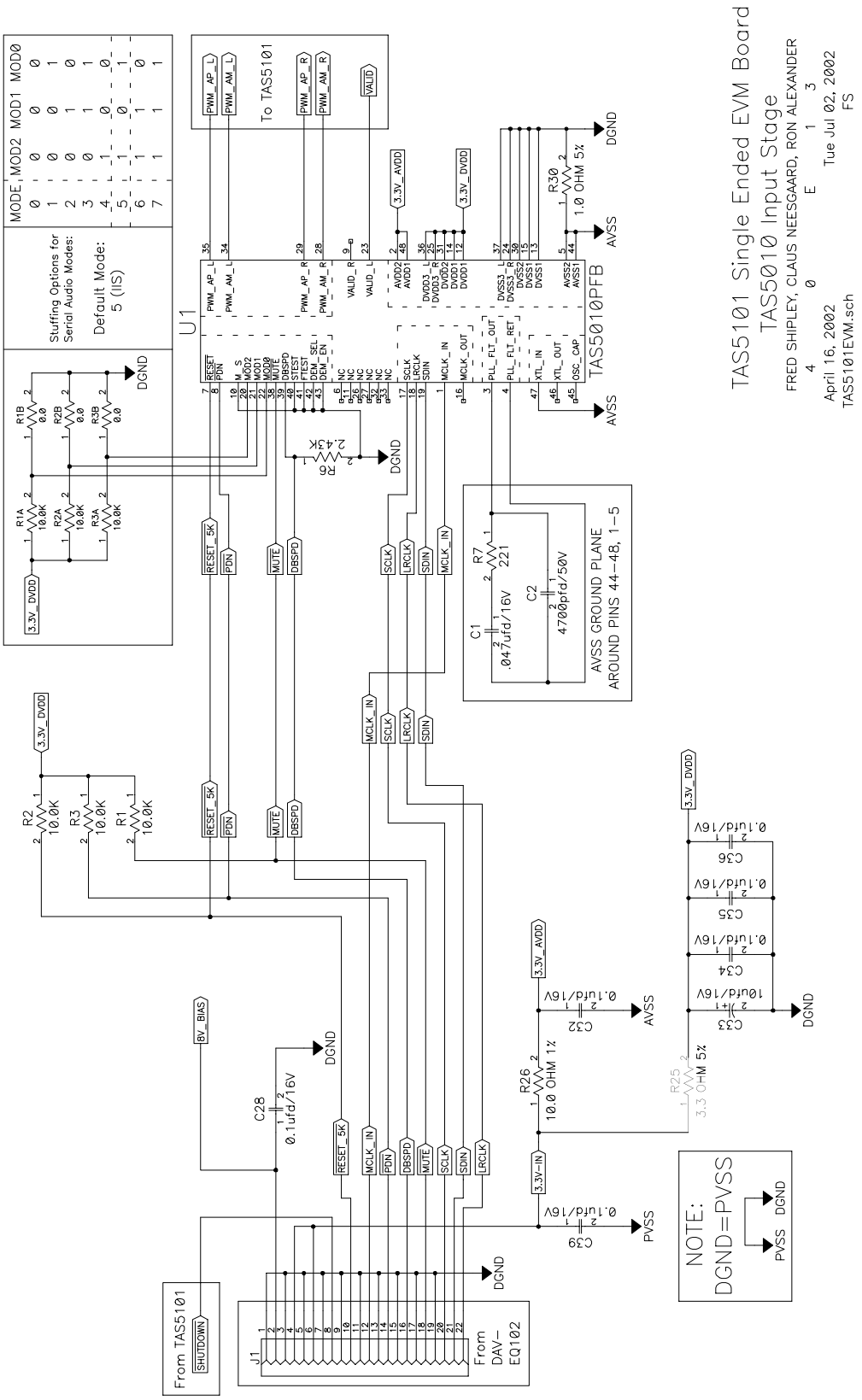
7.1 Signal Block Diagram



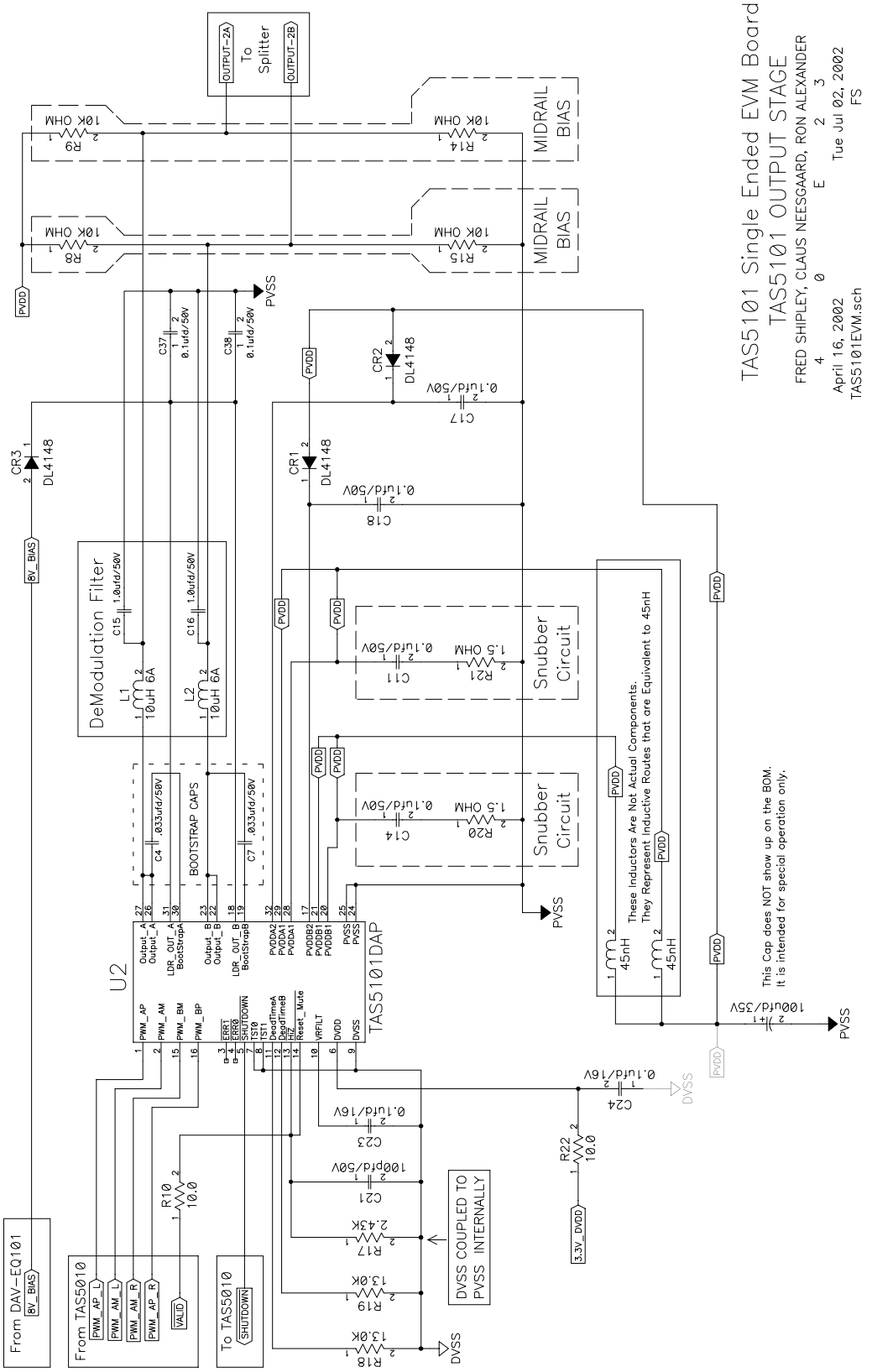
7.2 Power Block Diagram



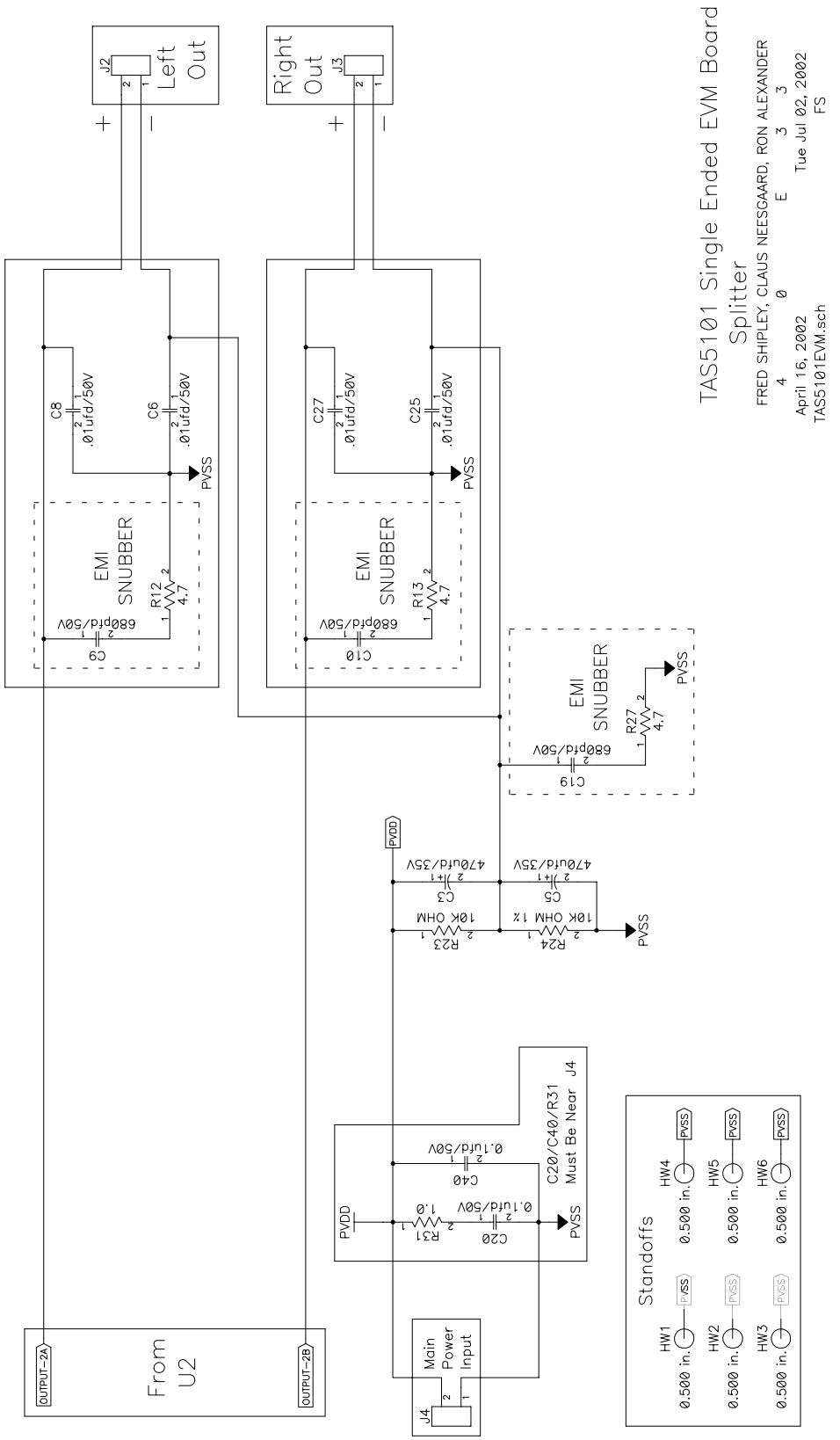
7.3 Audio Input Schematic



7.4 Audio Output Schematic



7.5 Output Splitter Schematic

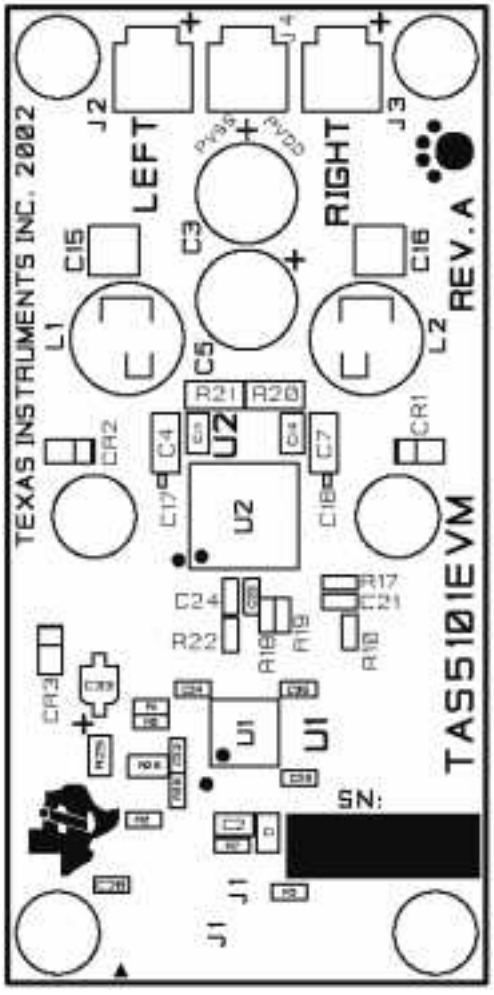


Chapter 8

PCB Component Placement

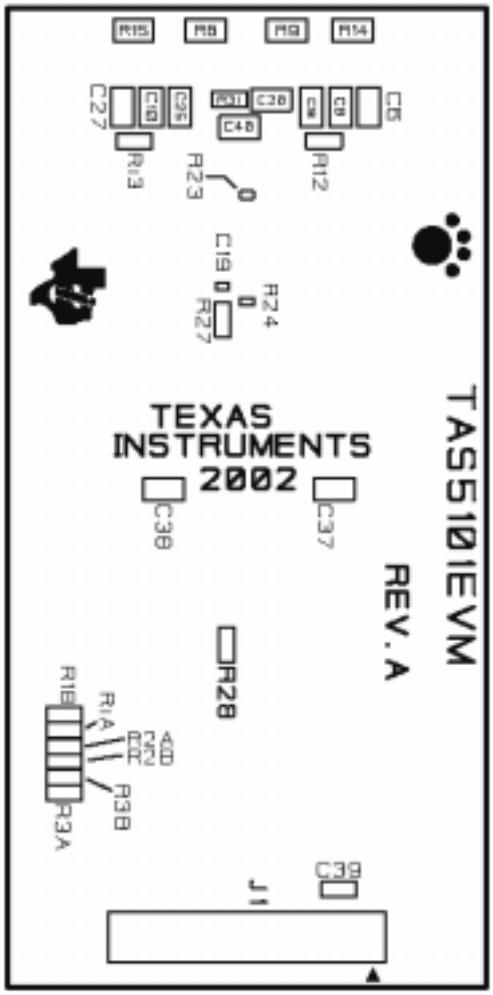
8.1 Top Layer

Figure 8–1. Top Layer Component Placement



8.2 Bottom Layer Component Placement

Figure 8–2. Bottom Layer Component Placement



Chapter 9

TAS5101SE EVM Performance Synopsis

Table 9–1. Performance Synopsis

Parameter	Test Conditions	Typical Value	Units
Power output	4 W at 26.5 V, < 0.1% distortion	15	W rms
Frequency response	–3 dB	40 to 20,000	Hz
THD+N	15 W, 1000 Hz, 4 Ω	0.09	%
Dynamic range	1000 Hz, –60 dB	> 93	dB
SNR	EIAJ	> 93	dB
Crosstalk	2 W at 1000 Hz	–37	dB
Idle channel tones	0 dB input	–118	dB

Appendix A

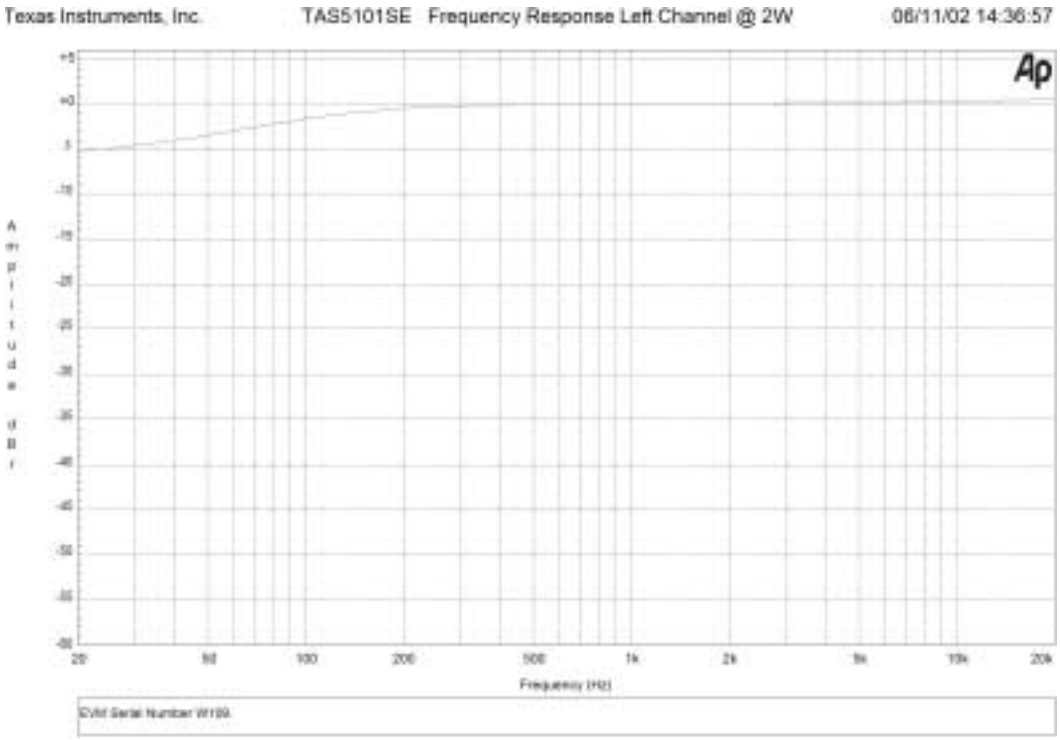
Amplifier Performance Tests

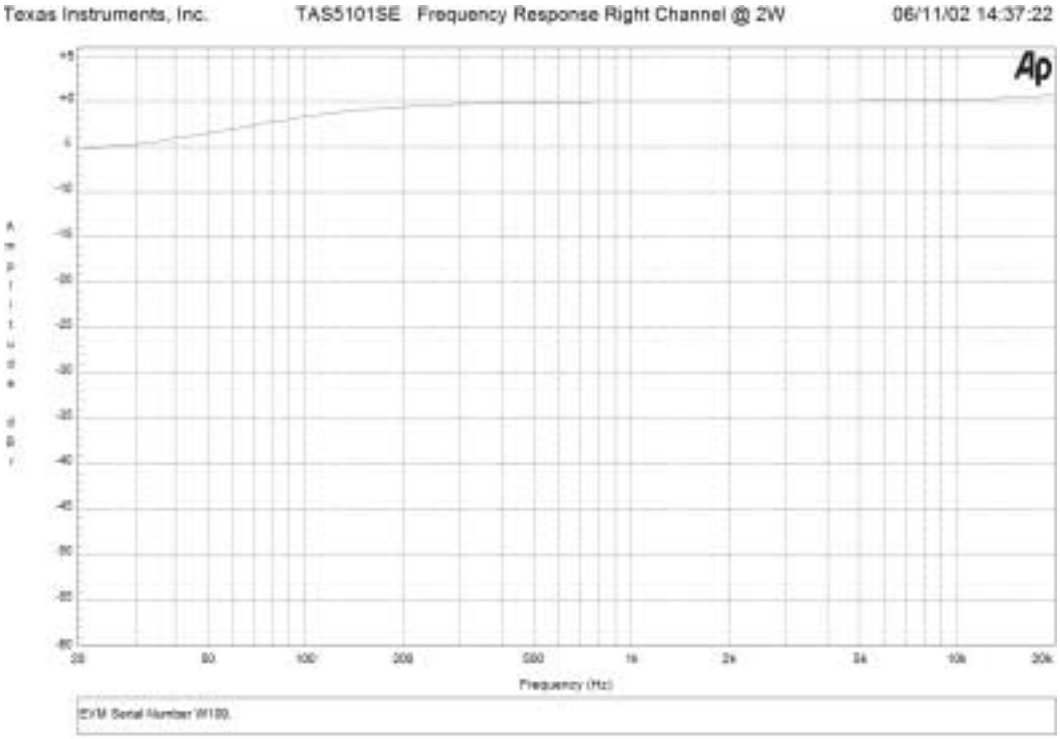
All tests were preformed using a System Two™ Cascade audio measurement system by Audio Precision™. An AES 17 filter in the audio measurement system was enabled for all tests to limit out-of-band noise, unless otherwise noted. The right and left audio output channels had 4-Ω load resistors.

The TAS5101SE EVM was powered at 26.5 V by a Hewlett-Packard laboratory power supply.

The digital input was driven from the audio measurement system through a DAV-EQ100 S/PDIF to I^2S converter board that was mounted on the TAS5101SE EVM.

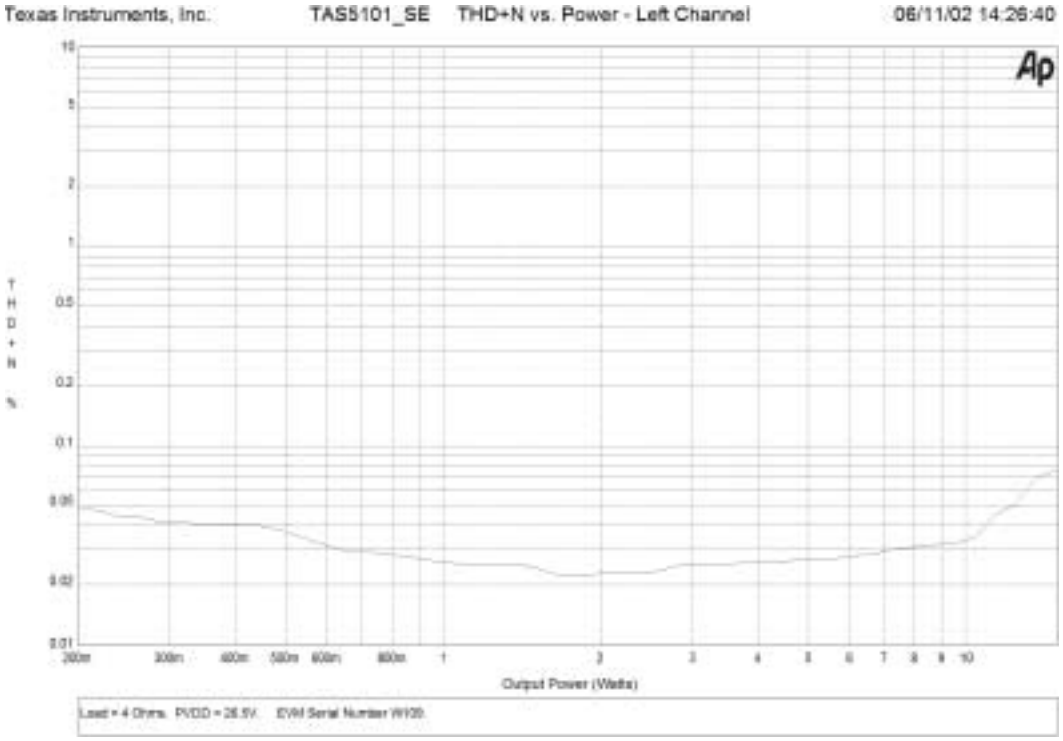
A.1 Frequency Response

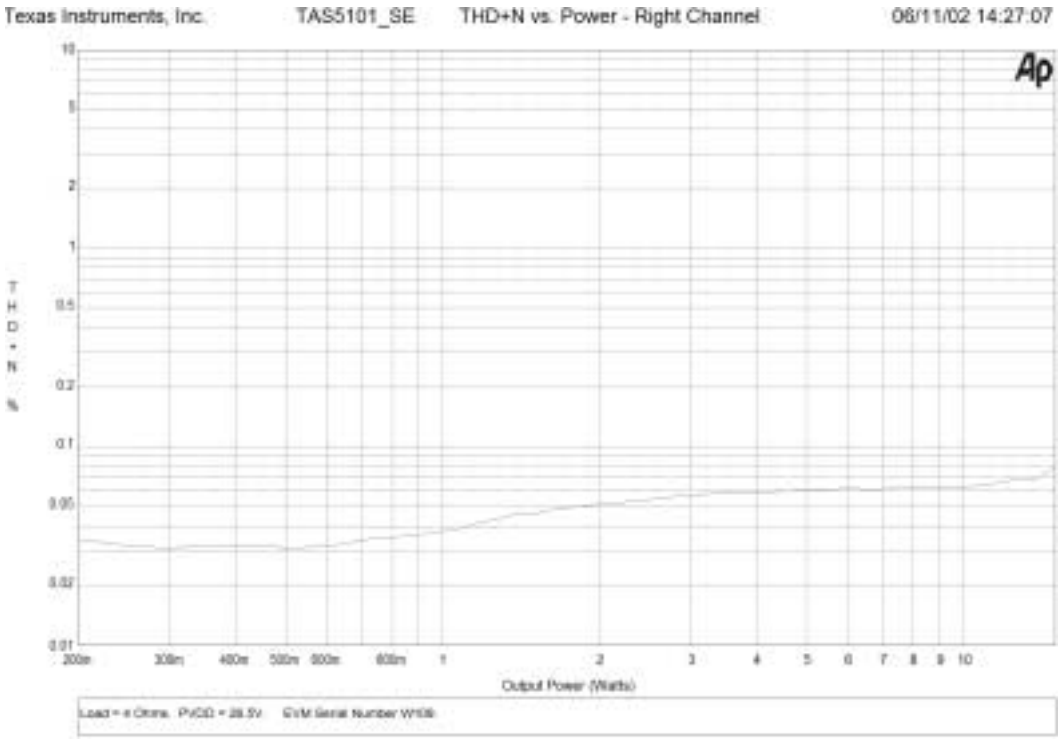




A.2 THD+N vs Power

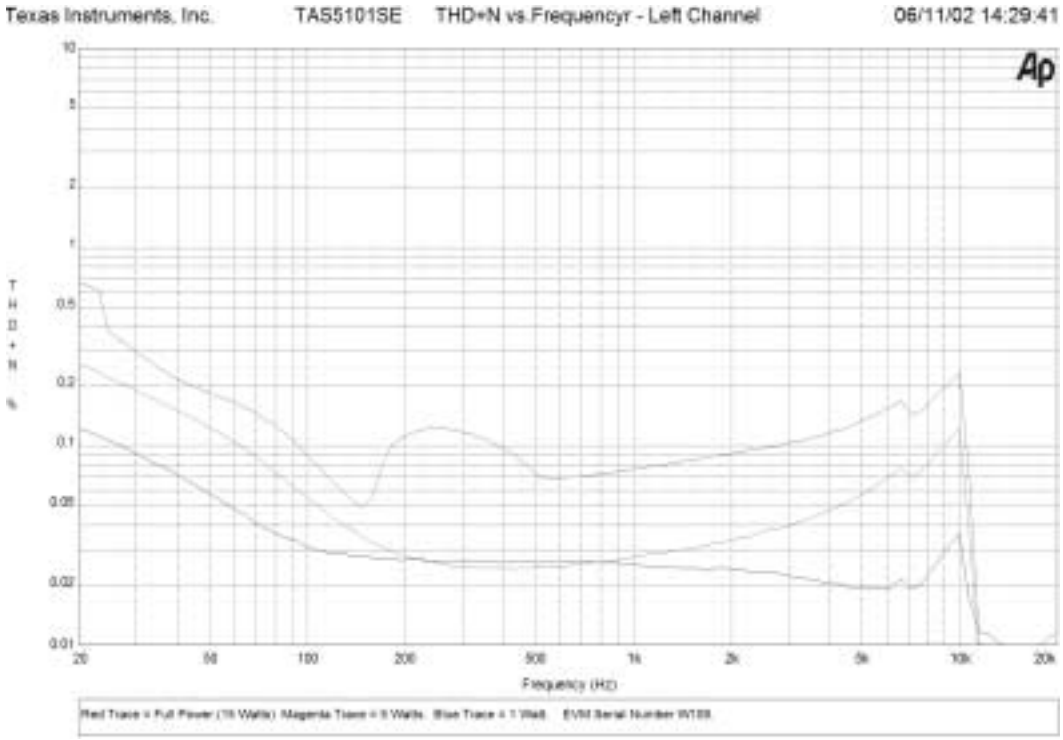
The input signal was 1000 Hz. Because a 4-Ω load resistor was used, the maximum power output was about 15 W rms. The TAS5101SE EVM can drive a 4-Ω load, with minimal performance degradation, and provide an output power of greater than 15 W with less than 0.1% distortion.

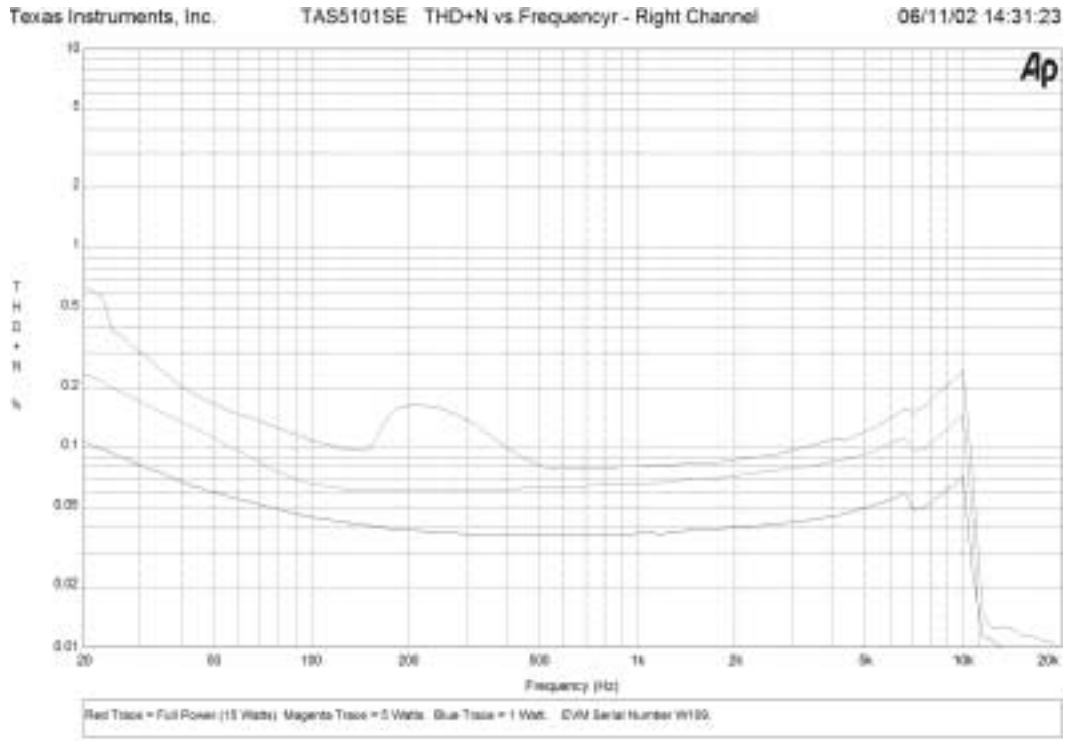




A.3 THD+N vs Frequency

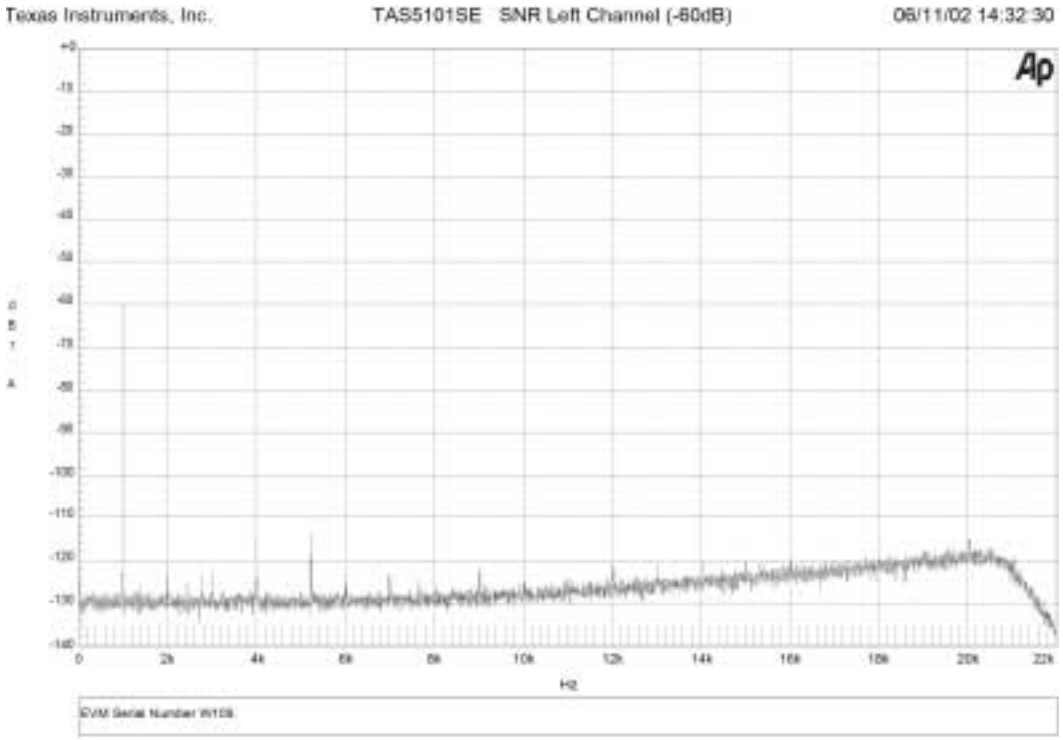
This test was run at three power levels, 1 W, 5 W, and 15 W (full power). The load resistance was 4 Ω. Because the output is ac coupled, the distortion is a little high at the low frequencies. The low frequency cutoff ($f_{-3dB\ low}$) is about 50 Hz. This can be improved by using larger capacitors in the output splitter circuit.

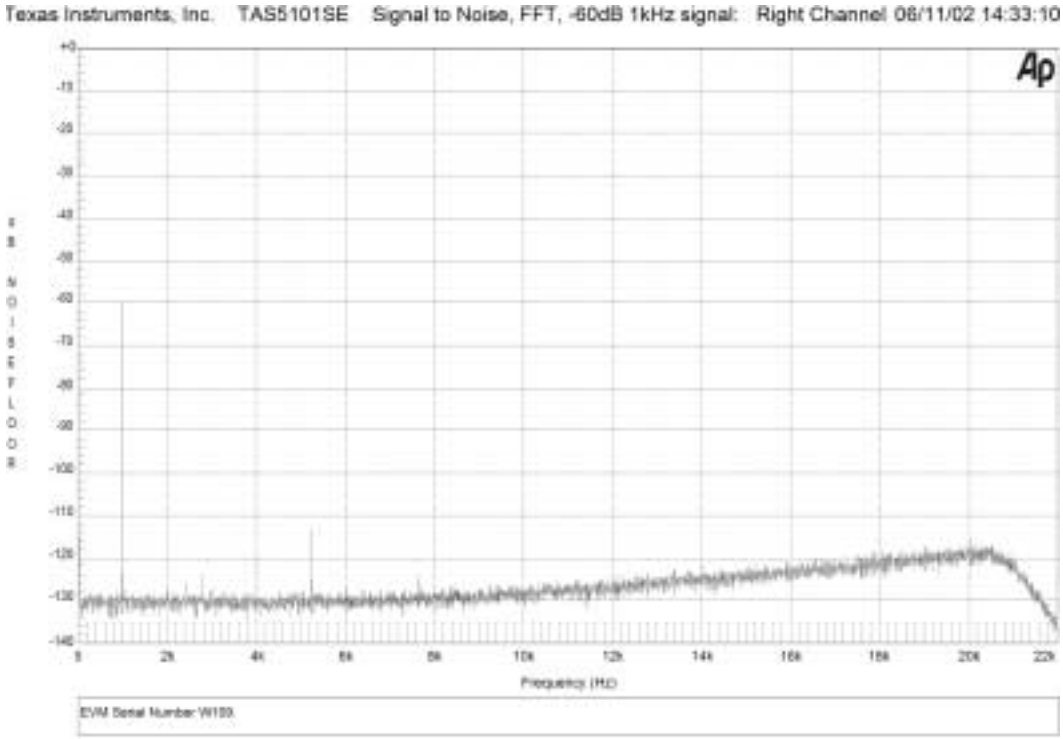



Texas Instruments, Inc.
TAS5101SE THD+N vs Frequencyr - Right Channel
06/11/02 14:31:23
Ap
THD+N %
10
5
2
1
0.5
0.2
0.1
0.05
0.02
0.01
20
50
100
200
500
1k
2k
5k
10k
20k
Frequency (Hz)
Red Trace = Full Power (15 Watts) Magenta Trace = 5 Watts Blue Trace = 1 Watt. EVM Serial Number W109.

A.4 Dynamic Range

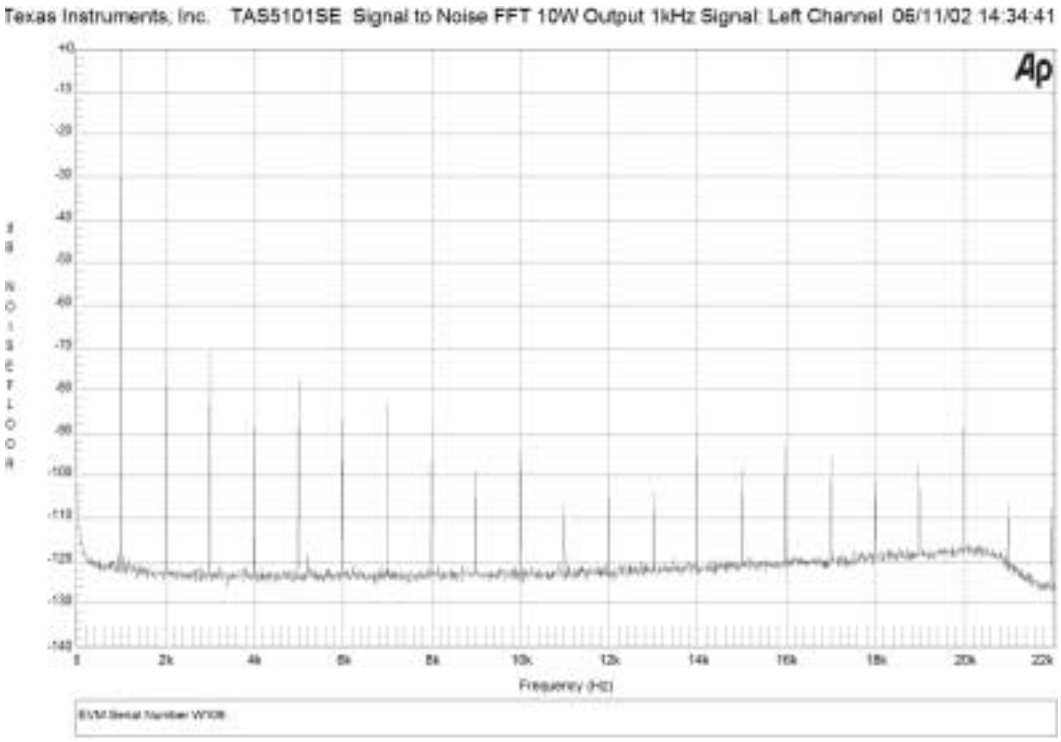
Low frequency noise is seen because the amplifier is ac-coupled. A 1000 Hz, –60 dB input signal was used.

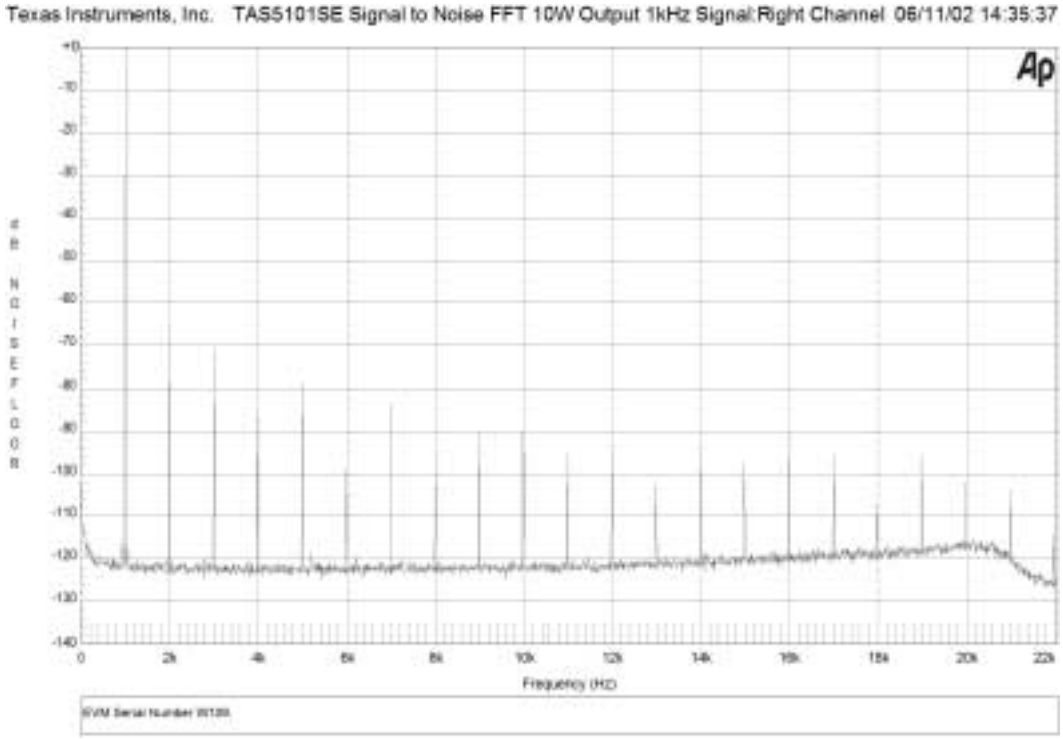




A.5 FFT—10 Watts

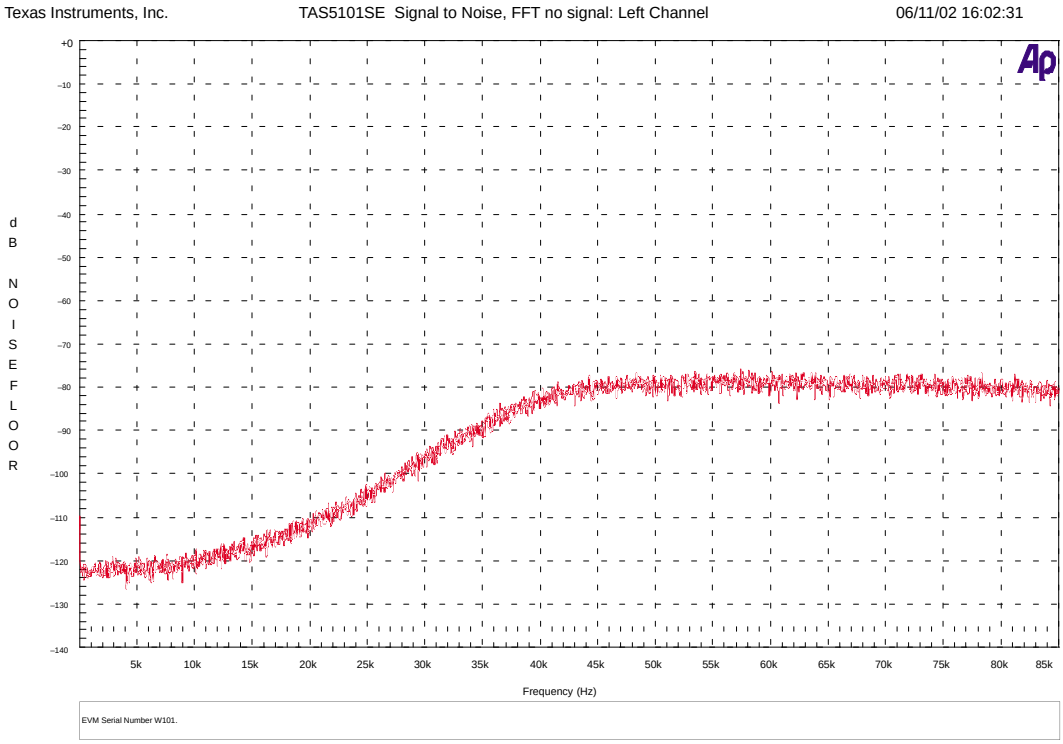
This test was performed at 10 W power into a 4-Ω load. The power supply voltage was 26.5 V. A full-scale, 1000-Hz input signal was used.

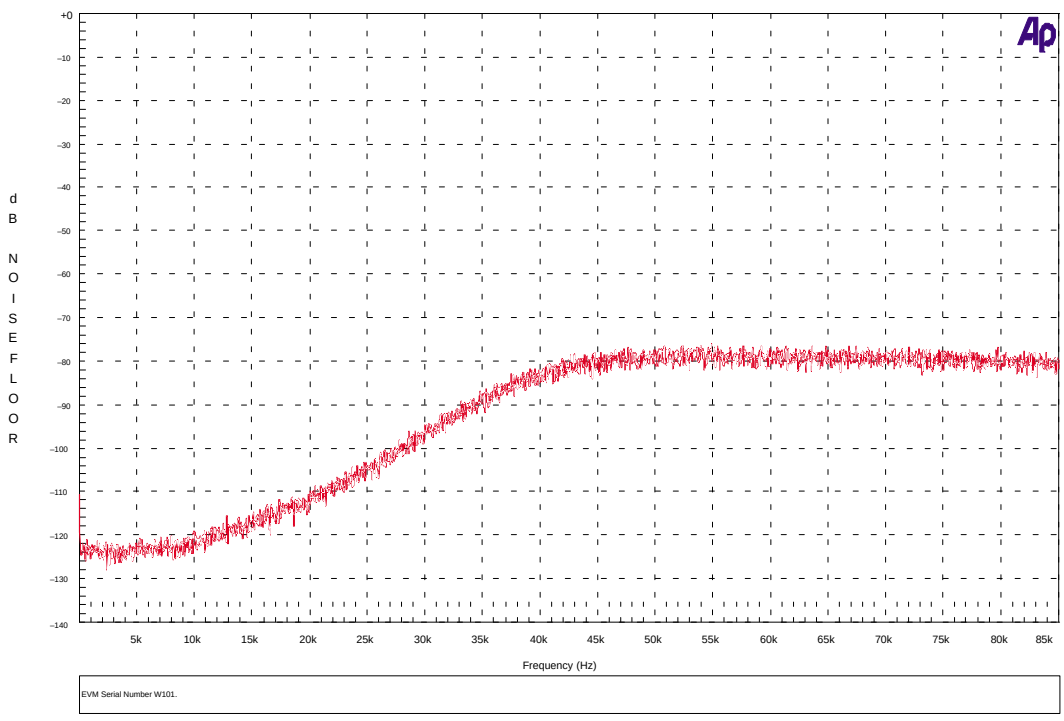




A.6 FFT—Signal to Noise

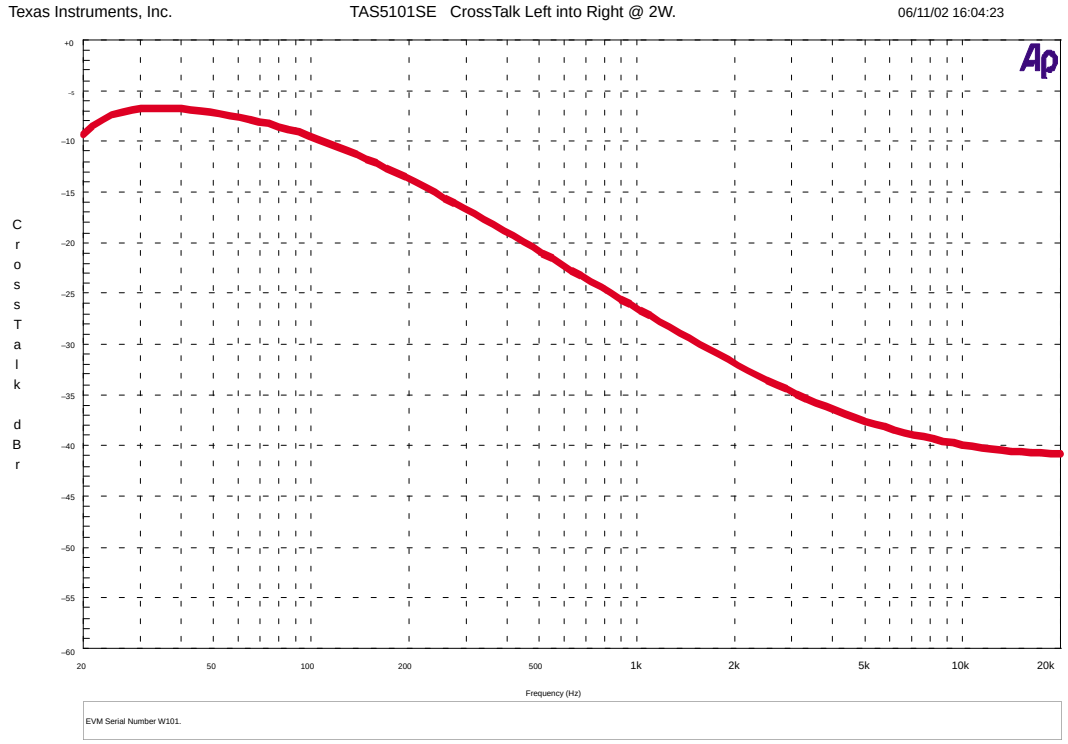
This test was executed from 10 Hz to 85 KHz with no filtering enabled on the audio measurement system so that the complete noise floor could be observed. No input signal was applied.



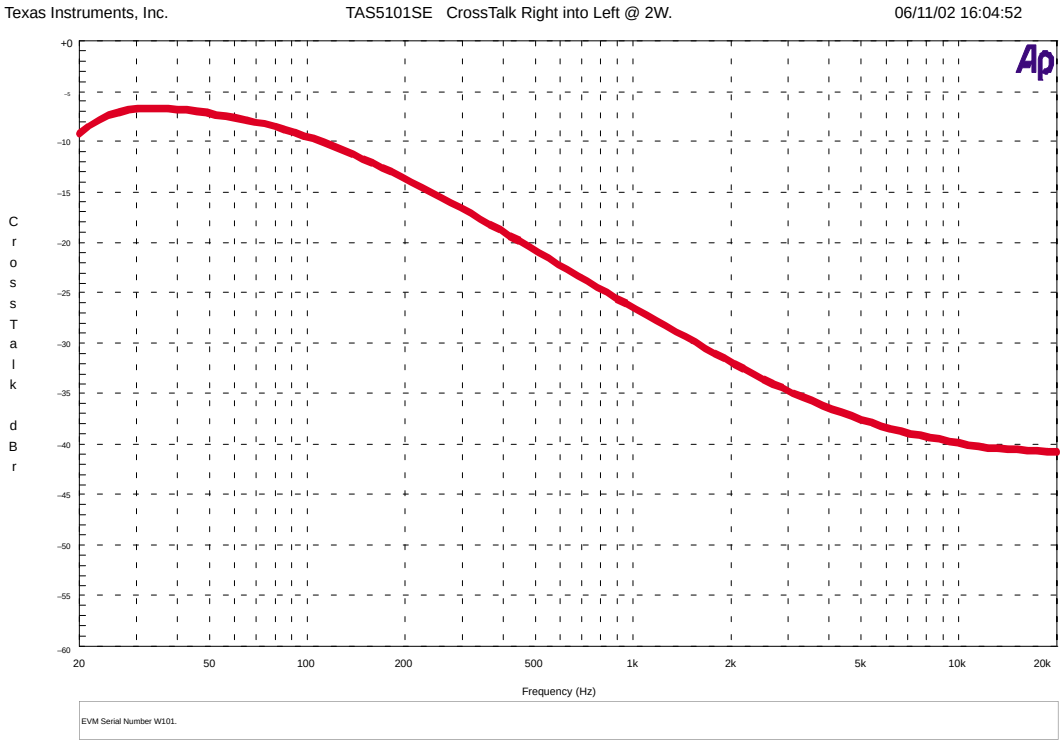


A.7 Crosstalk

The crosstalk present in this amplifier configuration is adequate for some applications. It can easily be improved by increasing the size of the capacitors in the output pseudo-differential circuit (output splitter). If further improvement is required, using a separate splitter for each channel further increases the crosstalk isolation.



Crosstalk


Texas Instruments, Inc.
TAS5101SE CrossTalk Right into Left @ 2W.
06/11/02 16:04:52
+0
-5
-10
-15
-20
-25
-30
-35
-40
-45
-50
-55
-60
CrossTalk dBr
20
50
100
200
500
1k
2k
5k
10k
20k
Frequency (Hz)
EVM Serial Number W101.

A.8 Short-Circuit Tests

Extensive short-circuit testing was performed both with sine wave input and a 3/4-scale dc level. Over 1000 short circuit tests were performed on each of five different TAS5101SE EVMs, both with closed-loop control resetting the amplifier while the short circuit was applied and without closed loop control.

The TAS5101SE EVM was not damaged by these tests.

Appendix B

Bill of Materials (BOM)

B.1 Bill of Materials for TAS5101EVM

TI-SEMICONDUCTORS								
ITEM	**Description**	**Ref. Designators**	**QTY**	**MFG.**	**Mfg:Part No.**	**Vendor**	**Vendor Part No.**	**Alternate Part No.**
1	Digital audio PWM processor	U1	1	Texas Instruments	TAS5010PFBR	Digi-Key	TAS5010PFBR	No alternate part number
2	30-W digital amp power stage	U2	1	Texas Instruments	TAS5101DAP	Texas Instruments	TAS5101DAP	No alternate part number
SEMICONDUCTORS								
ITEM	**Description**	**Ref. Designators**	**QTY**	**MFG.**	**Mfg:Part No.**	**Vendor**	**Vendor Part No.**	**Alternate Part No.**
3	SW rectifier, 0.15-A 75-V SMT miniMELF	CR1, CR2, CR3, CR4	4	Micro Commercial Co.	DL4148	Digi-Key	DL4148MSCT	DL4148MSTR
CAPACITORS								
ITEM	**Description**	**Ref. Designators**	**QTY**	**MFG**	**Mfg:Part No.**	**Vendor**	**Vendor Part No.**	**Alternate Part No.**
4	CAP 100-pF 50vV CERM 0603 NPO	C21	1	Panasonic	ECU-V1H101JCV	Digi-Key	PCC101ACVTR	PCC101ACVCT
5	CAP 0.1-pF 16-V CERM 0603 X7R	C23, C24, C32, C34, C35, C36, C39, C28	8	Panasonic	ECJ-1VB1C104K	Digi-Key	PCC1762TR	PCC1762CT
6	CAP 680-pF 50-V CERM 0805 NPO	C9, C10, C19	3	Panasonic	ECJ-2VC1H681J	Digi-Key	PCC681CGTR	PCC681CGCT
7	CAP 4700-pF 50-V CERM 0805 X7R	C2	1	Panasonic	ECJ-2VB1H472K	Digi-Key	PCC472BNTR	PCC472BNCT
8	CAP 0.01-µF 50-V CERM 0805 X7R	C6, C8, C25, C27	4	Panasonic	ECJ-2VB1H103K	Digi-Key	PCC103BNTR	PCC103BNCT
9	CAP 0.047-µF 16-V CERM 0805 X7R	C1	1	Panasonic	ECJ-2VB1C473K	Digi-Key	PCC1808TR	PCC1808CT
10	CAP 0.1-µF 50-V CERM 0805 X7R	C11, C14, C17, C18, C20, C37, C38, C40	8	Panasonic	ECJ-2YB1H104K	Digi-Key	PCC1840TR	PCC1840CT
11	CAP 0.033-µF 50-V CERM 1206 X7R	C4, C7	2	Panasonic	ECU-VIH333KBW	Digi-Key	PCC333BTR	PCC333BCT
12	CAP 1.0-µF 50V polyester	C15, C16	2	WIMA	MKS02-1.0UFD/50/10	Wofford	MKS02-1.0UFD/50/10	No alternate part number

13	CAP 10-µF 16-V ALUM ELEC SM-VSA	C33	1	Panasonic	ECE-V1CS100SR	Digi-Key	PCE3061TR	PCE3061CT
14	CAP 470-µF 35-V ALUM ELEC M-series	C3, C5	2	Panasonic	ECA-1VM471	Digi-Key	P10386TB	P5168
RESISTORS								
ITEM	**Description**	**Ref. Designators**	**QTY**	**MFG**	**Mfg:Part No.**	**Vendor**	**Vendor Part No.**	**Alternate Part No.**
15	RES 0.0-? 1/16-W 5% SMD 0603	R1B, R2B, R3B	3	Panasonic	ERJ-3GEY0R00V	Digi-Key	P0.0GTR	P0.0GCT
16	RES 1.0-? 1/10-W 5% SMD 0603	R28, R31, R30	3	Panasonic	ERJ-3RQJ1R0V	Digi-Key	P1.0AHTR	P1.0AHCT
17	RES 4.7-? 1/16-W 5% SMD 0603	R12, R13, R27	3	Panasonic	ERJ-3GEYJ4R7V	Digi-Key	P4.7GTR	P4.7GCT
18	RES 10.0-? 1/16-W 1% SMD 0603	R10, R22	2	Panasonic	ERJ-3EKF10R0V	Digi-Key	P10.0HTR	P10.0HCT
19	RES 221-? 1/16-W 1% SMD 0603	R7	1	Panasonic	ERJ-3EKF2210V	Digi-Key	P221HTR	P221HCT
20	RES 2.43-k? 1/16-W 1% SMD 0603	R6, R17	2	Panasonic	ERJ-3EKF2431V	Digi-Key	P2.43KHTR	P2.43KHCT
21	RES 10.0-k? 1/16-W 1% SMD 0603	R1, R1A, R2, R2A, R3, R3A	6	Panasonic	ERJ-3EKF1002V	Digi-Key	P10.0KHTR	P10.0KHCT
22	RES 13.0-k? 1/16-W 1% SMD 0603	R18, R19	2	Panasonic	ERJ-3EKF1302V	Digi-Key	P13.0KHTR	P13.0KHCT
23	RES 3.3-? 1/10-W 5% SMD 0805	R25	1	Panasonic	ERJ-6RQJ3R3V	Digi-Key	P3.3BTR	P3.3BCT
24	RES 10.0-? 1/10-W 1% SMD 0805	R26	1	Panasonic	ERJ-6ENF10R0V	Digi-Key	P10.0CTR	P10.0CCT
25	RES 10.0-k? 1/10-W 1% SMD 0805	R8, R9, R14, R15, R23, R24	6	Panasonic	ERJ-6ENF1002V	Digi-Key	P10.0KCTR	P10.0KCCT
26	RES 1.5-? 50-V 1% SMD MELF-MMA0204	R20, R21	2	BC Components	MMA020450BL1R5F	MIT	MMA020450BL1R5F	No alternate part number

INDUCTORS								
ITEM	**Description**	**Ref. Designators**	**QTY**	**MFG**	**Mfg:Part No.**	**Vendor**	**Vendor Part No.**	**Alternate Part No.**
27	Inductor, 10-uH 6-A	L1, L2	2	TOKIN	SBPSC-11R310-100A	TOKIN	SBPSC-11R310-100A	No alternate part number
JACK, HEADERS AND CONNECTORS								
ITEM	**Description**	**Ref. Designators**	**QTY**	**MFG**	**Mfg:Part No.**	**Vendor**	**Vendor Part No.**	**Alternate Part No.**
28	Header, 2-pin male, PCB, TIN, w/lock	J2, J3, J4	3	JST	B2P-VH	Wofford	B2P-VH	No alternate part number
29	Header, male – 2×11 gold round pins, dual row	J1	1	Samtec	BDL-111-G-E	Samtec	BDL-111-G-E	No alternate part number
STANDOFF HARDWARE								
ITEM	**Description**	**Ref. Designators**	**QTY**	**MFG**	**Mfg:Part No.**	**Vendor**	**Vendor Part No.**	**Alternate Part No.**
30	Standoff 4-40 threaded M/F 0.50 in. ALUM-HEX	HW1, HW2, HW3, HW4, HW5, HW6	6	Keystone Electronics	8401	Digi-Key	8401K	No alternate part number
31	Screw, phillips machine, 4-40 0.375 in, zinc/steel	HW1, HW2, HW3, HW4, HW5, HW6	6	Building Fasteners	PMS 440 0038 PH	Digi-Key	H781	No alternate part number
32	Lockwasher, #4 internal-tooth, zinc/steel	HW1, HW2, HW3, HW4, HW5, HW6	6	Building Fasteners	INT LWZ 004	Digi-Key	H236	No alternate part number
33	Hex nut, 4-40, zinc/steel	HW1, HW2, HW3, HW4, HW5, HW6	6	Building Fasteners	HNZ440	Digi-Key	H216	No alternate part number