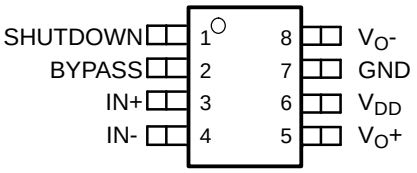
350-mW MONO AUDIO POWER AMPLIFIER WITH DIFFERENTIAL INPUTS

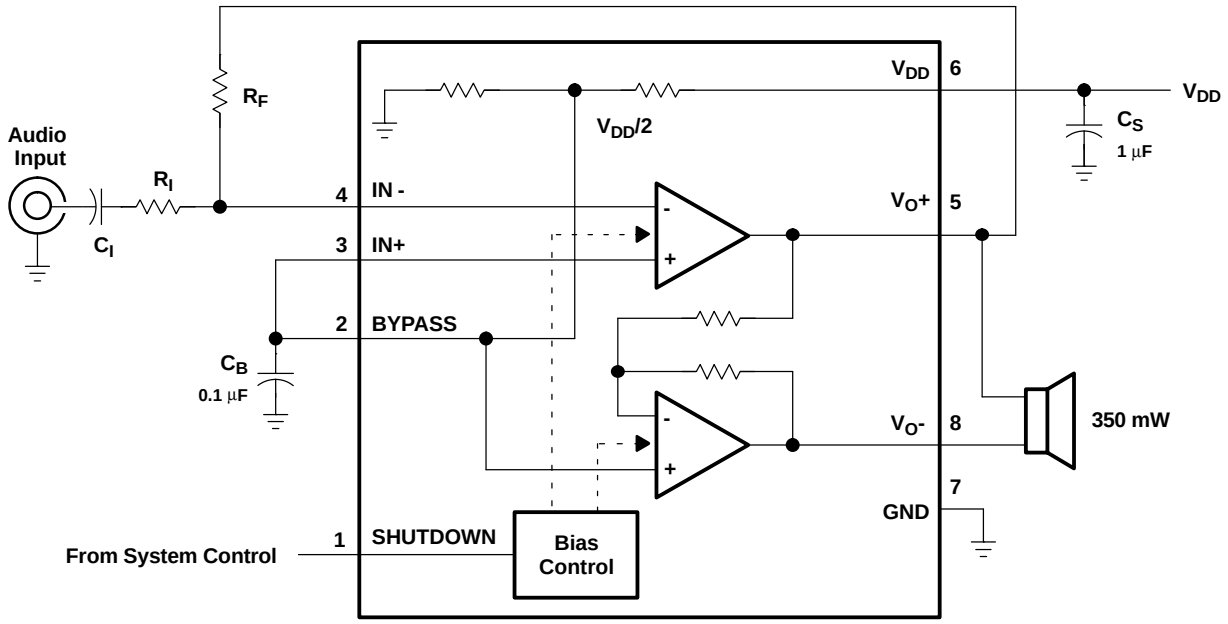
- **Fully Specified for 3.3-V and 5-V Operation**
- **Wide Power Supply Compatibility 2.5 V – 5.5 V**
- **Output Power for R_L = 8 Ω**
  - **– 350 mW at V_{DD} = 5 V**
  - **– 250 mW at V_{DD} = 3.3 V**
- **Ultralow Supply Current in Shutdown Mode . . . 0.15 µA**
- **Thermal and Short-Circuit Protection**
- **Surface-Mount Packaging**
  - **– SOIC**
  - **– PowerPAD™ MSOP**

D OR DGN PACKAGE (TOP VIEW)



DESCRIPTION

The TPA321 is a bridge-tied load (BTL) audio power amplifier developed especially for low-voltage applications where internal speakers are required. Operating with a 3.3-V supply, the TPA321 can deliver 250 mW of continuous power into a BTL 8-Ω load at less than 1% THD+N throughout voice band frequencies. Although this device is characterized out to 20 kHz, its operation was optimized for narrower band applications such as cellular communications. The BTL configuration eliminates the need for external coupling capacitors on the output in most applications, which is particularly important for small battery-powered equipment. This device features a shutdown mode for power-sensitive applications with a quiescent current of 0.15 µA during shutdown. The TPA321 is available in an 8-pin SOIC surface-mount package and the surface-mount PowerPAD™ MSOP, which reduces board space by 50% and height by 40%.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES		MSOP SYMBOLIZATION
	SMALL OUTLINE(1) (D)	MSOP(1) (DGN)	
–40°C to 85°C	TPA321D	TPA321DGN	AJB

(1) The D and DGN packages are available taped and reeled. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA321DR).

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		UNIT
V_{DD}	Supply voltage	6 V
V_I	Input voltage	–0.3 V to V_{DD} +0.3 V
	Continuous total power dissipation	Internally limited (see Dissipation Rating Table)
T_A	Operating free-air temperature range	–40°C to 85°C
T_J	Operating junction temperature range	–40°C to 150°C
T_{stg}	Storage temperature range	–65°C to 150°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
D	725 mW	5.8 mW/°C	464 mW	377 mW
DGN	2.14 W(1)	17.1 mW/°C	1.37 W	1.11 W

(1) See the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD™ package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before mentioned document.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_{DD}	Supply voltage		2.5	5.5	V
V_{IH}	High-level voltage	SHUTDOWN	0.9 V_{DD}		V
V_{IL}	Low-level voltage	SHUTDOWN		0.1 V_{DD}	V
T_A	Operating free-air temperature		–40	85	°C

ELECTRICAL CHARACTERISTICS

at specified free-air temperature, V_{DD} = 3.3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\|V_{OO}\|$	Output offset voltage (measured differentially)	SHUTDOWN = 0 V, R_L = 8 Ω, R_F = 10 kΩ		5	20	mV
PSRR	Power supply rejection ratio	V_{DD} = 3.2 V to 3.4 V		85		dB
I_{DD}	Supply current (see Figure 3)	SHUTDOWN = 0 V, R_F = 10 kΩ		0.7	1.5	mA
$I_{DD(SD)}$	Supply current, shutdown mode (see Figure 4)	SHUTDOWN = V_{DD}, R_F = 10 kΩ		0.15	5	µA
$\|I_{IH}\|$	High-level input current	SHUTDOWN, V_{DD} = 3.3 V, V_I = 3.3 V			1	µA
$\|I_{IL}\|$	Low-level input current	SHUTDOWN, V_{DD} = 3.3 V, V_I = 0 V			1	µA

OPERATING CHARACTERISTICS

V_{DD} = 3.3 V, T_A = 25°C, R_L = 8 Ω

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power(1)	THD = 0.5%,	See Figure 9		250		mW
THD + N	Total harmonic distortion plus noise	P_O = 250 mW, A_V = -2 V/V,	f = 20 Hz to 4 kHz, See Figure 7		1.3%		
	Maximum output power bandwidth	A_V = -2 V/V, THD = 3%, See Figure 7			10		kHz
B_1	Unity-gain bandwidth	Open loop,	See Figure 15		1.4		MHz
	Supply ripple rejection ratio	f = 1 kHz, C_B = 1 µF, See Figure 2			71		dB
V_n	Noise output voltage	A_V = –1 V/V, R_L = 32 Ω ,	C_B = 0.1 µF, See Figure 19		15		µV(rms)

(1) Output power is measured at the output terminals of the device at f = 1 kHz.

ELECTRICAL CHARACTERISTICS

at specified free-air temperature, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\|V_{OO}\|$	Output offset voltage (measured differentially)	SHUTDOWN = 0 V, R_L = 8 Ω, R_F = 10 kΩ		5	20	mV
PSRR	Power supply rejection ratio	V_{DD} = 4.9 V to 5.1 V		78		dB
I_{DD}	Supply current (see Figure 3)	SHUTDOWN = 0 V, R_F = 10 kΩ		0.7	1.5	mA
$I_{DD(SD)}$	Supply current, shutdown mode (see Figure 4)	SHUTDOWN = V_{DD}, R_F = 10 kΩ		0.15	5	µA
$\|I_{IH}\|$	High-level input current	SHUTDOWN, V_{DD} = 5.5 V, V_I = V_{DD}			1	µA
$\|I_{IL}\|$	Low-level input current	SHUTDOWN, V_{DD} = 5.5 V, V_I = 0 V			1	µA

OPERATING CHARACTERISTICS

V_{DD} = 5 V, T_A = 25°C, R_L = 8 Ω

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power	THD = 0.5%,	See Figure 13		700		mW
THD + N	Total harmonic distortion plus noise	P_O = 350 mW, A_V = –2 V/V,	f = 20 Hz to 4 kHz, See Figure 11		1%		
	Maximum output power bandwidth	A_V = –2 V/V, THD = 2%, See Figure 11			10		kHz
B_1	Unity-gain bandwidth	Open loop,	See Figure 16		1.4		MHz
	Supply ripple rejection ratio	f = 1 kHz, C_B = 1 µF, See Figure 2			65		dB
V_n	Noise output voltage	A_V = -1 V/V, R_L = 32 Ω ,	C_B = 0.1 µF, See Figure 20		15		µV(rms)

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BYPASS	2	I	BYPASS is the tap to the voltage divider for internal mid-supply bias. This terminal should be connected to a 0.1-µF to 1-µF capacitor when used as an audio amplifier.
GND	7		GND is the ground connection.
IN-	4	I	IN- is the inverting input. IN- is typically used as the audio input terminal.
IN+	3	I	IN+ is the noninverting input. IN+ is typically tied to the BYPASS terminal for SE operations.
SHUTDOWN	1	I	SHUTDOWN places the entire device in shutdown mode when held high (I_{DD} ~ 0.15 µA).
V_{DD}	6		V_{DD} is the supply voltage terminal.
V_O+	5	O	V_O+ is the positive BTL output.
V_O-	8	O	V_O- is the negative BTL output.

PARAMETER MEASUREMENT INFORMATION

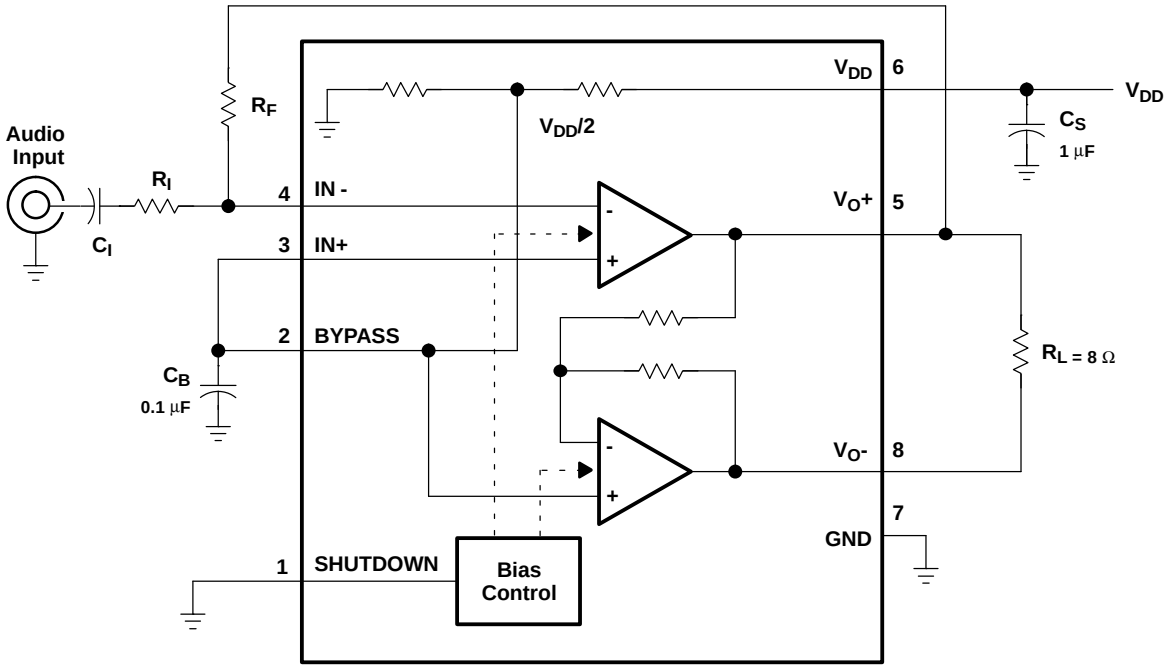


Figure 1. Test Circuit

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
k_{SVR}	Supply voltage rejection ratio	vs Frequency	2
I_{DD}	Supply current	vs Supply voltage	3, 4
P_O	Output power	vs Supply voltage	5
		vs Load resistance	6
THD+N	Total harmonic distortion plus noise	vs Frequency	7, 8, 11, 12
		vs Output power	9, 10, 13, 14
	Open-loop gain and phase	vs Frequency	15, 16
	Closed-loop gain and phase	vs Frequency	17, 18
V_n	Output noise voltage	vs Frequency	19, 20
P_D	Power dissipation	vs Output power	21, 22

SUPPLY VOLTAGE REJECTION RATIO vs FREQUENCY

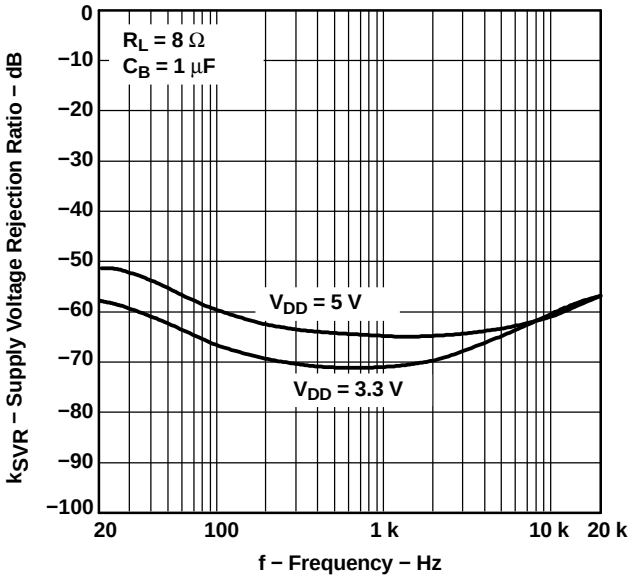


Figure 2.

SUPPLY CURRENT vs SUPPLY VOLTAGE

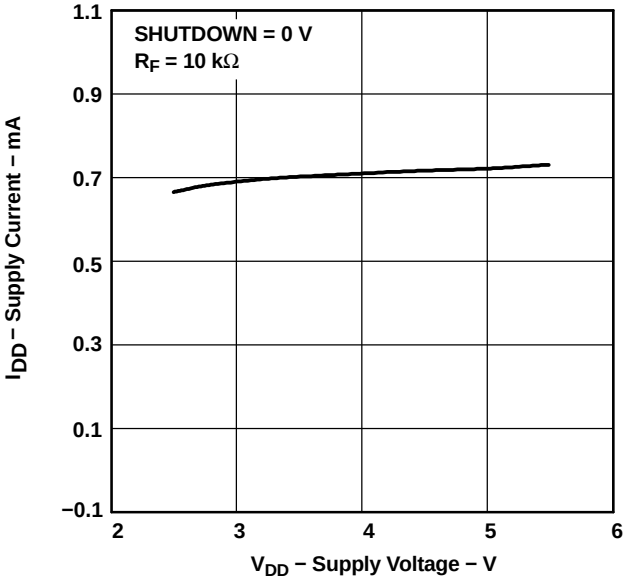


Figure 3.

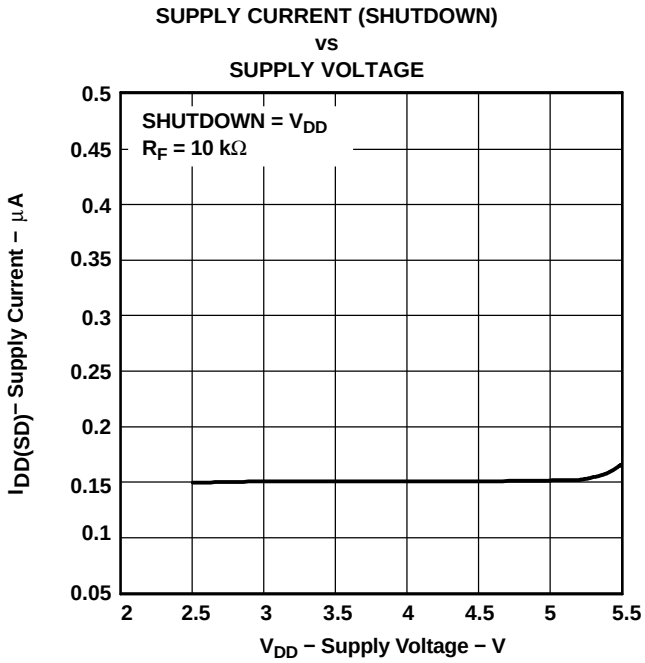
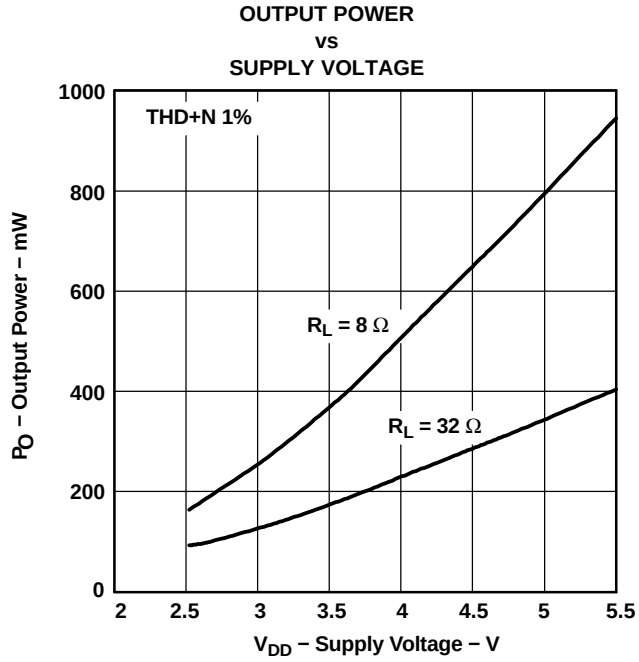


Figure 4.



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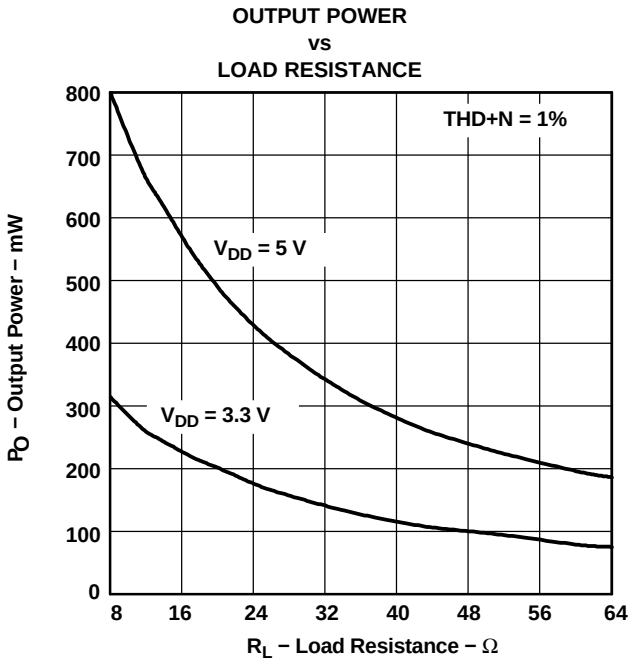

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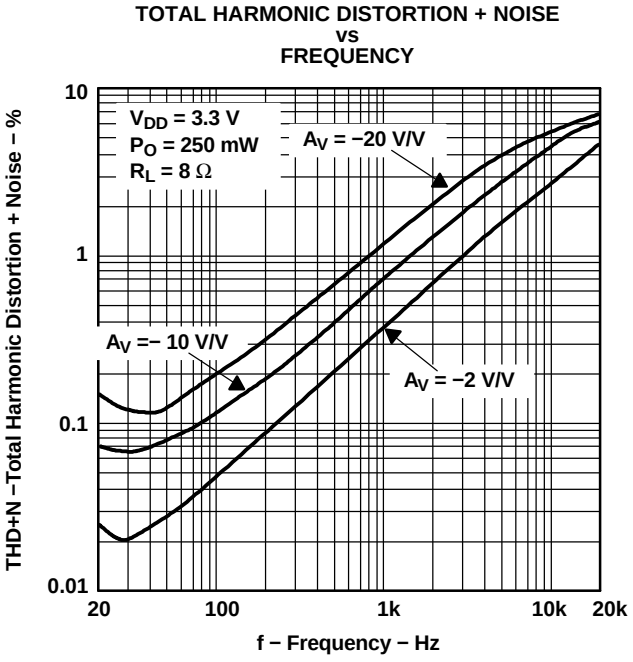

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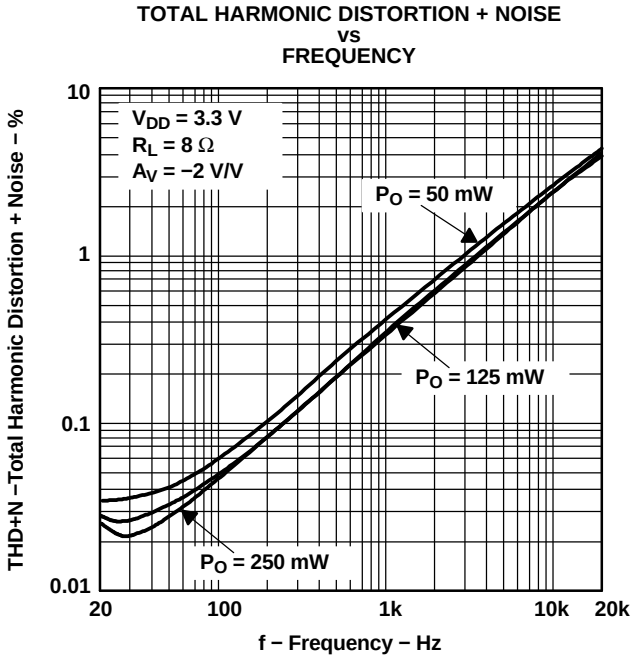

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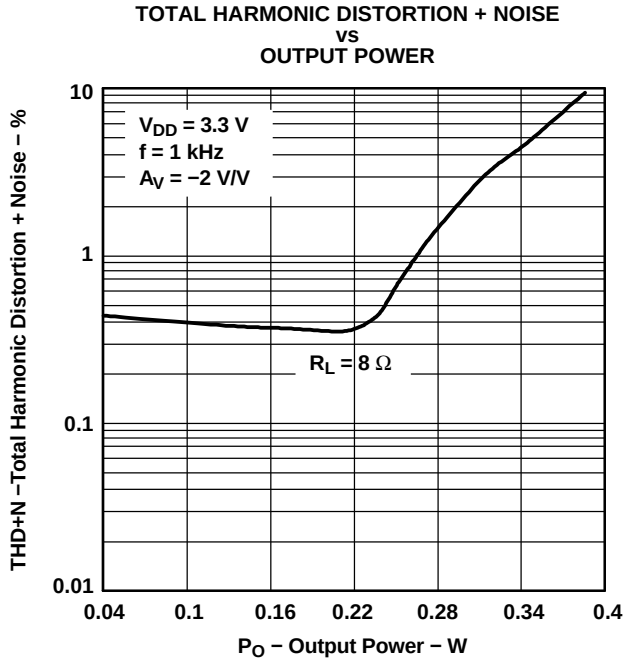

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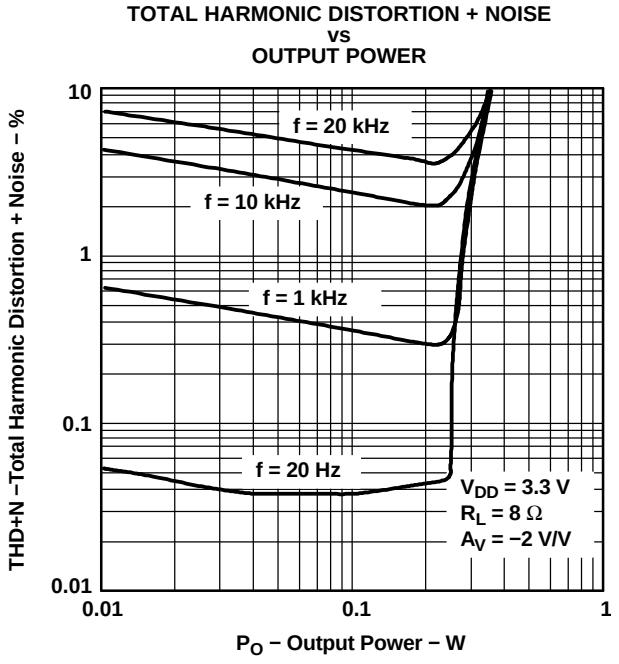

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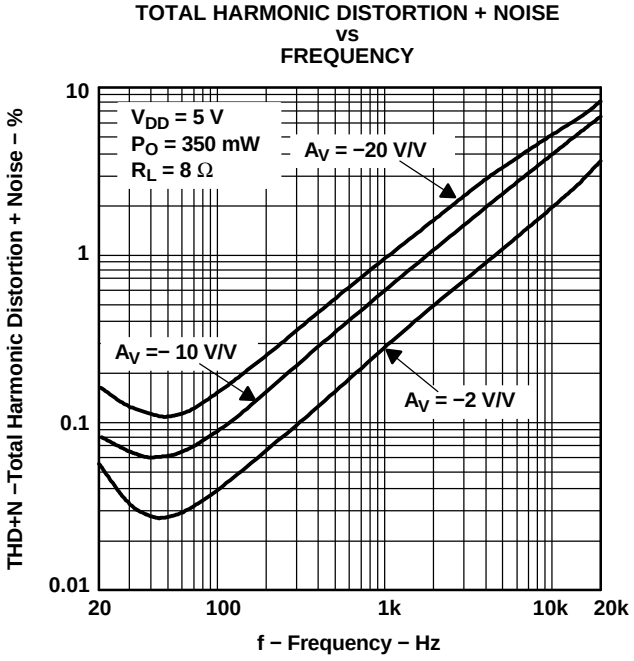
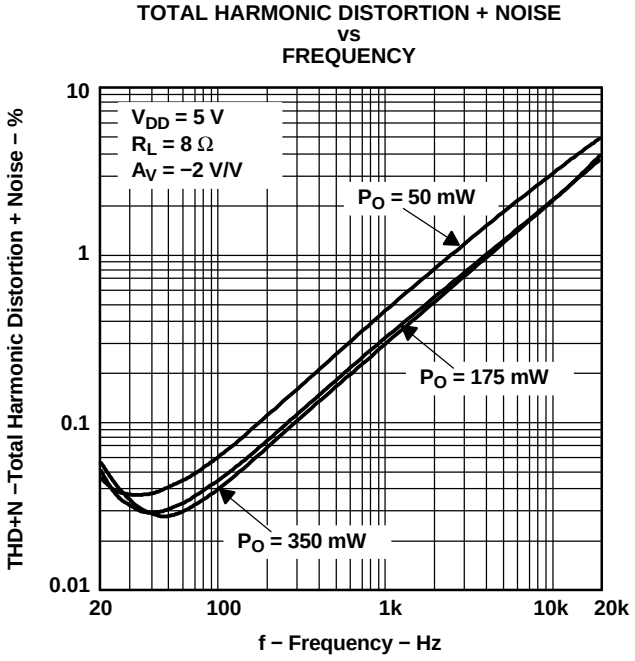


Figure 11.



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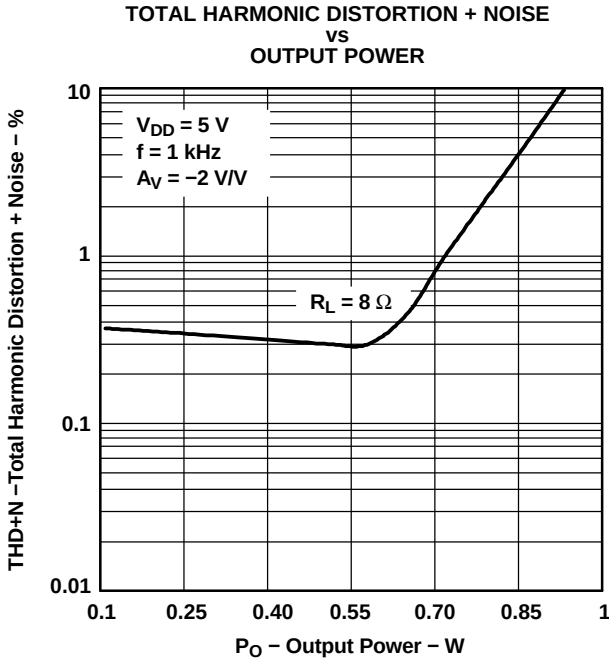
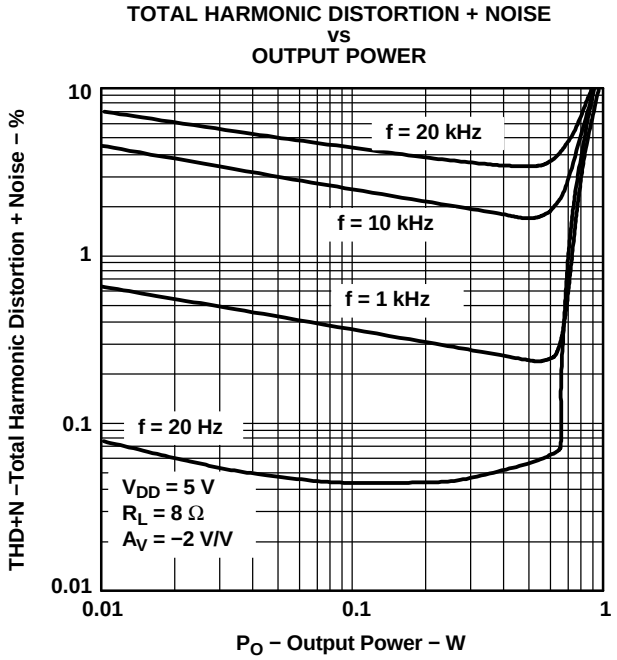


Figure 13.



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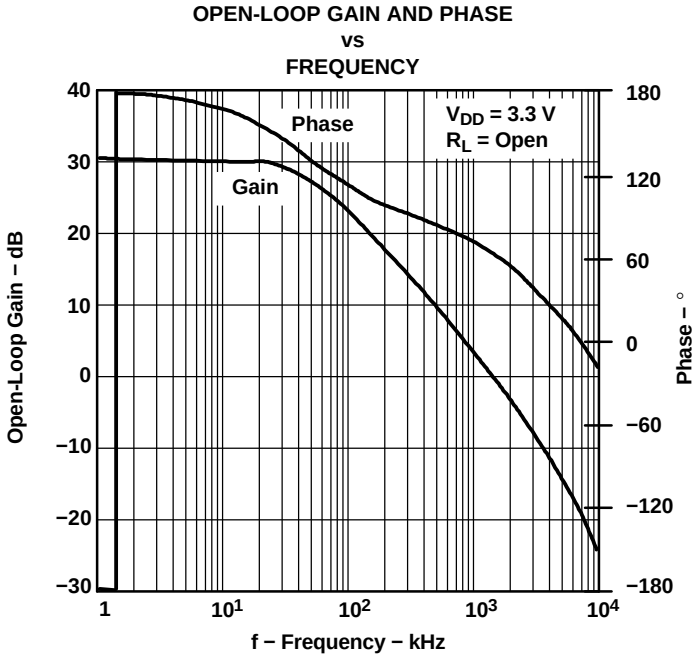

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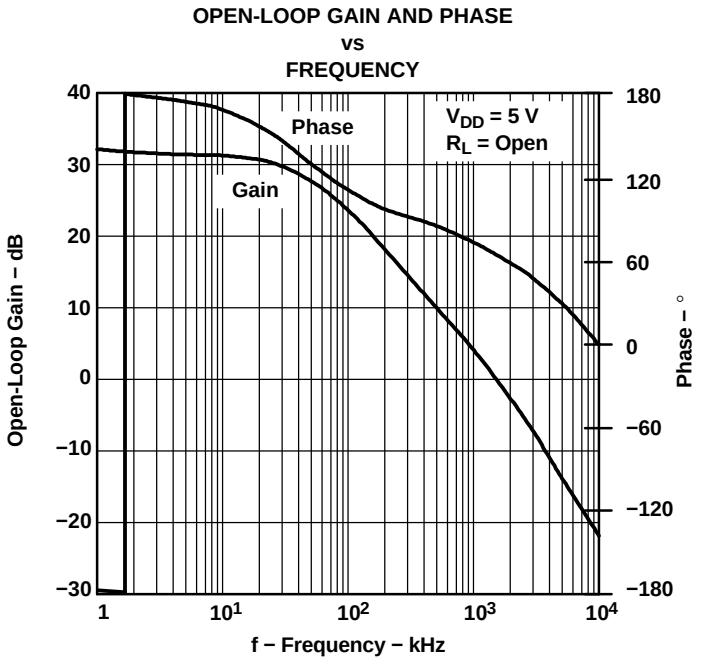
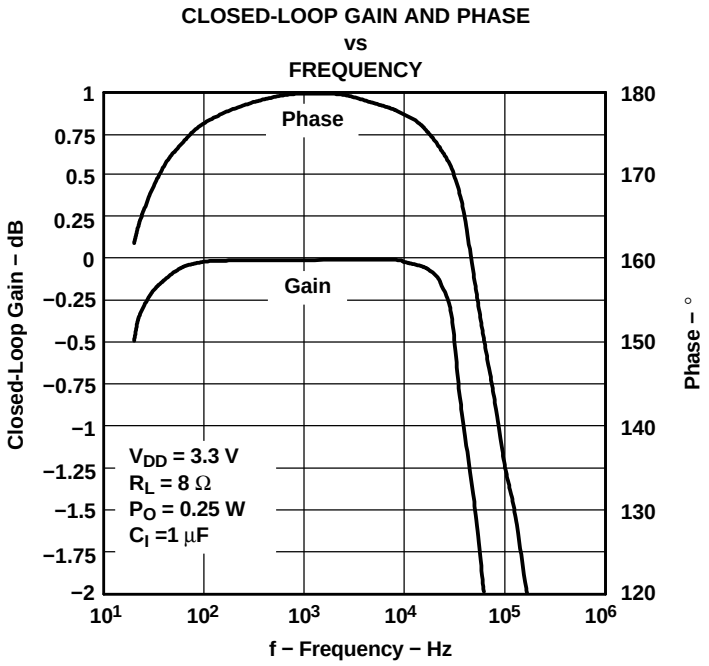


Figure 16.



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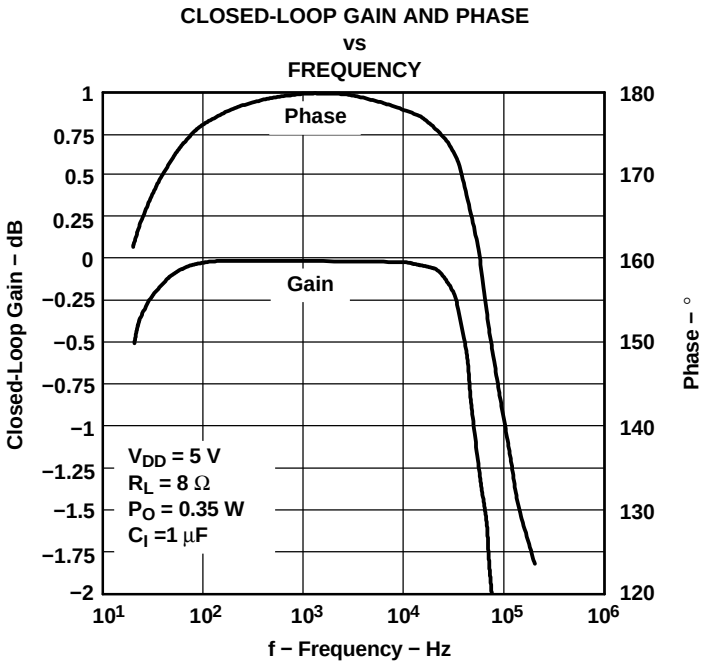

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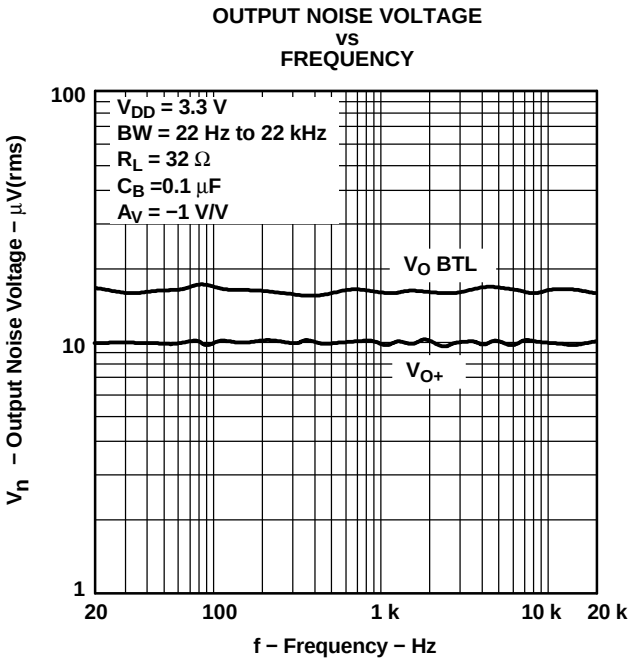

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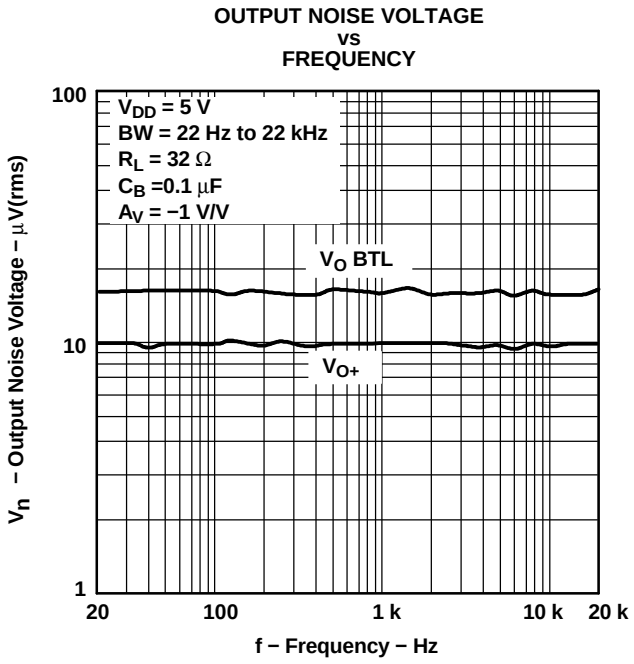


Figure 20.

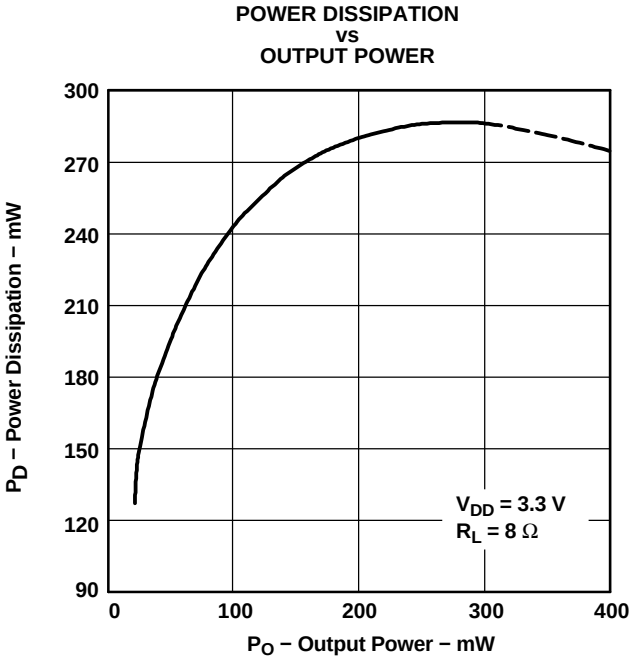


Figure 21.

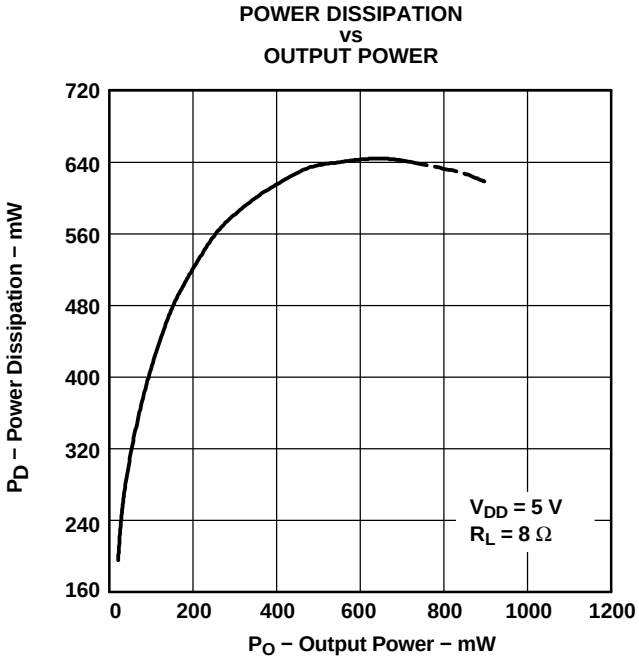


Figure 22.

APPLICATION INFORMATION

BRIDGE-TIED LOAD

Figure 23 shows a linear audio power amplifier (APA) in a BTL configuration. The TPA321 BTL amplifier consists of two linear amplifiers driving both ends of the load. There are several potential benefits to this differential drive configuration but power to the load should be initially considered. The differential drive to the speaker means that as one side is slewing up, the other side is slewing down, and vice versa. This, in effect, doubles the voltage swing on the load as compared to a ground-referenced load. Plugging $2 \times V_{O(PP)}$ into the power equation, where voltage is squared, yields 4× the output power from the same supply rail and load impedance (see Equation 1).

$$V_{(RMS)} = \frac{V_{O(PP)}}{2\sqrt{2}}$$

$$\text{Power} = \frac{V_{(RMS)}^{2}}{R_L} \tag{1}$$

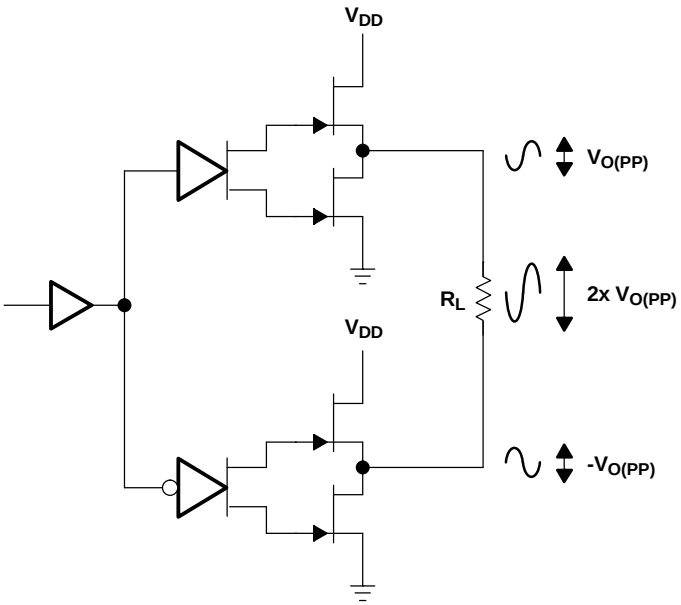


Figure 23. Bridge-Tied Load Configuration

In a typical portable handheld equipment sound channel operating at 3.3 V, bridging raises the power into an 8-Ω speaker from a single-ended (SE, ground reference) limit of 62.5 mW to 250 mW. In sound power that is a 6-dB improvement, which is loudness that can be heard. In addition to increased power, there are frequency response concerns. Consider the single-supply SE configuration shown in Figure 24. A coupling capacitor is required to block the dc offset voltage from reaching the load. These capacitors can be quite large (approximately 33 µF to 1000 µF) so they tend to be expensive, heavy, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system. This frequency limiting effect is due to the high pass filter network created with the speaker impedance and the coupling capacitance and is calculated with Equation 2.

$$f_c = \frac{1}{2\pi R_L C_C} \tag{2}$$

For example, a 68-µF capacitor with an 8-Ω speaker would attenuate low frequencies below 293 Hz. The BTL configuration cancels the dc offsets, eliminating the need for the blocking capacitors. Low-frequency performance is then limited only by the input network and speaker response. Cost and PCB space are also minimized by eliminating the bulky coupling capacitor.

APPLICATION INFORMATION (continued)

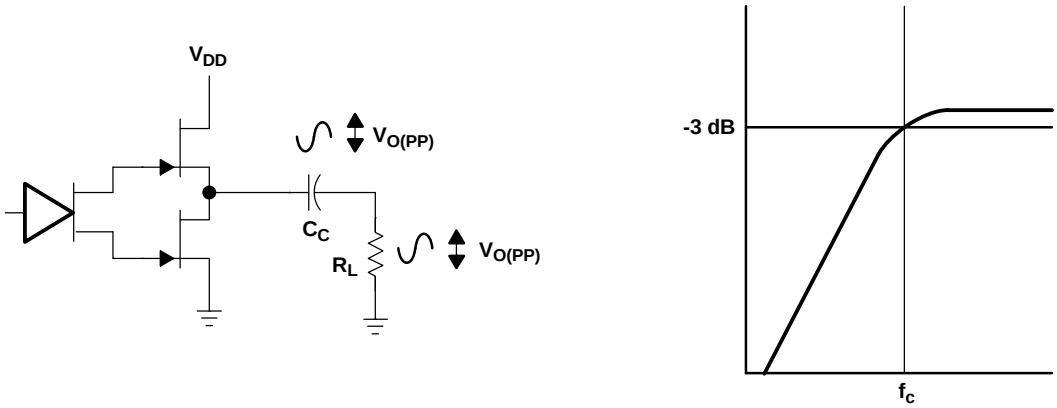


Figure 24. Single-Ended Configuration and Frequency Response

Increasing power to the load does carry a penalty of increased internal power dissipation. The increased dissipation is understandable considering that the BTL configuration produces 4× the output power of a SE configuration. Internal dissipation versus output power is discussed further in the *thermal considerations* section.

BTL AMPLIFIER EFFICIENCY

Linear amplifiers are inefficient. The primary cause of these inefficiencies is voltage drop across the output stage transistors. There are two components of the internal voltage drop. One is the headroom or dc voltage drop that varies inversely to output power. The second component is due to the sine-wave nature of the output. The total voltage drop can be calculated by subtracting the RMS value of the output voltage from V_{DD}. The internal voltage drop multiplied by the RMS value of the supply current, $I_{DD(RMS)}$, determines the internal power dissipation of the amplifier.

An easy-to-use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load. To accurately calculate the RMS values of power in the load and in the amplifier, the current and voltage waveform shapes must first be understood (see Figure 25).

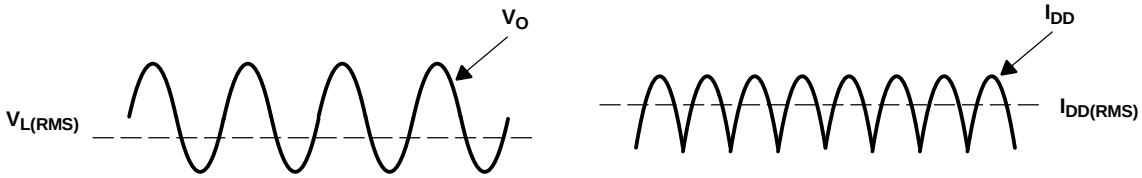


Figure 25. Voltage and Current Waveforms for BTL Amplifiers

Although the voltages and currents for SE and BTL are sinusoidal in the load, currents from the supply are different between SE and BTL configurations. In an SE application the current waveform is a half-wave rectified shape, whereas in BTL it is a full-wave rectified waveform. This means RMS conversion factors are different. Keep in mind that for most of the waveform both the push and pull transistors are not on at the same time, which supports the fact that each amplifier in the BTL device only draws current from the supply for half the waveform. The following equations are the basis for calculating amplifier efficiency.

APPLICATION INFORMATION (continued)

$$\text{Efficiency} = \frac{P_L}{P_{SUP}}$$

where

$$P_L = \frac{V_{L(RMS)}^2}{R_L} = \frac{V_p^2}{2R_L}$$

$$V_{L(RMS)} = \frac{V_P}{\sqrt{2}}$$

$$P_{SUP} = V_{DD}\, I_{DD(RMS)} = \frac{V_{DD}\, 2V_P}{\pi R_L}$$

$$I_{DD(RMS)} = \frac{2V_P}{\pi R_L} \tag{3}$$

$$\text{Efficiency of a BTL configuration} = \frac{\pi V_P}{2V_{DD}} = \frac{\pi \left(\frac{P_L R_L}{2}\right)^{1/2}}{2V_{DD}} \tag{4}$$

Table 1 employs Equation 4 to calculate efficiencies for three different output power levels. The efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a nearly flat internal power dissipation over the normal operating range. The internal dissipation at full output power is less than in the half-power range. Calculating the efficiency for a specific system is the key to proper power supply design.

Table 1. Efficiency vs Output Power in 3.3-V 8-Ω BTL Systems

OUTPUT POWER (W)	EFFICIENCY (%)	PEAK-to-PEAK VOLTAGE (V)	INTERNAL DISSIPATION (W)
0.125	33.6	1.41	0.26
0.25	47.6	2.00	0.29
0.375	58.3	2.45 (1)	0.28

(1) High-peak voltage values cause the THD to increase.

A final point to remember about linear amplifiers (either SE or BTL) is how to manipulate the terms in the efficiency equation to utmost advantage when possible. Note that in Equation 4, V_{DD} is in the denominator. This indicates that as V_{DD} goes down, efficiency goes up.

APPLICATION SCHEMATICS

Figure 26 is a schematic diagram of a typical handheld audio application circuit, configured for a gain of –10 V/V.

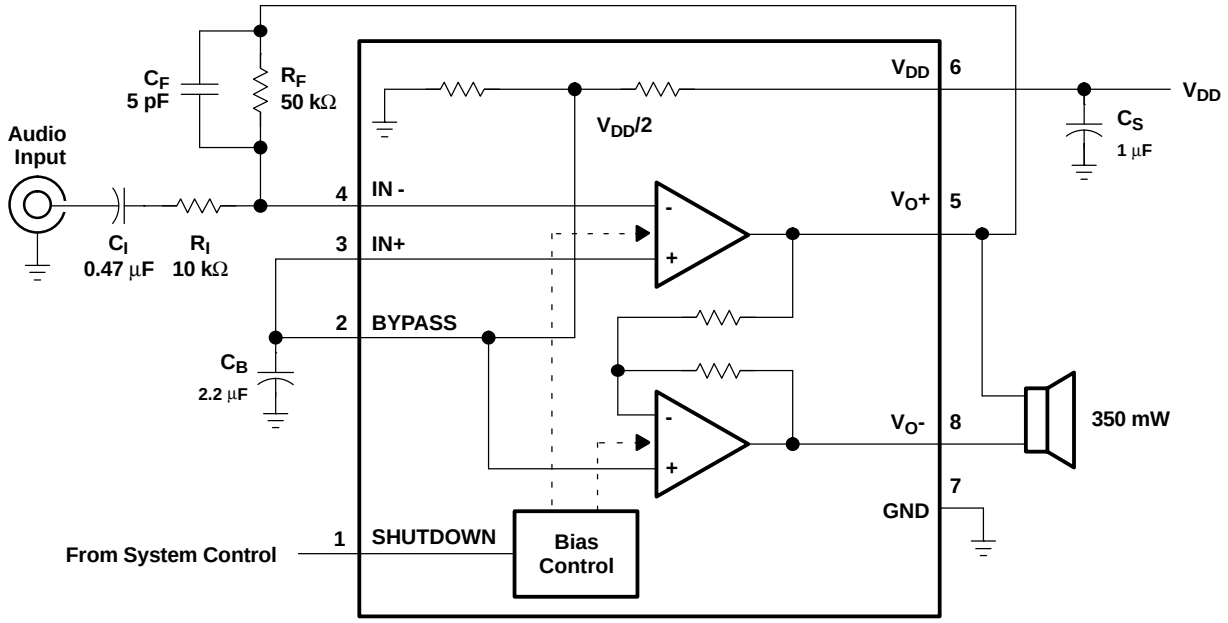


Figure 26. TPA321 Application Circuit

Figure 27 is a schematic diagram of a typical handheld audio application circuit, configured for a gain of –10 V/V with a differential input.

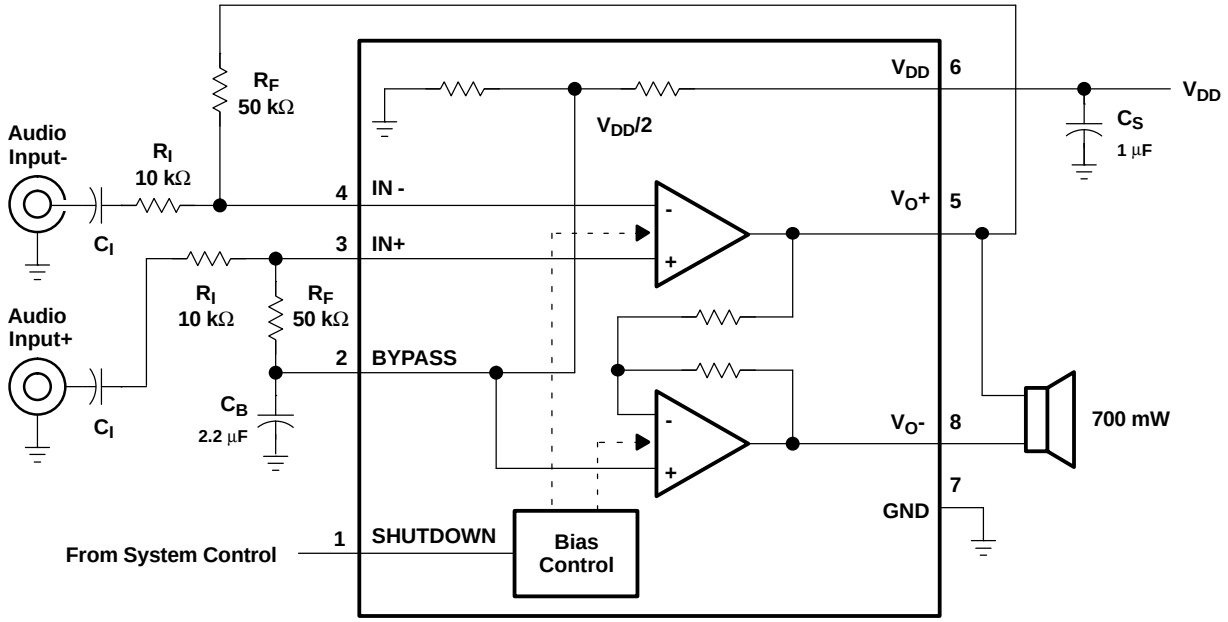


Figure 27. TPA321 Application Circuit With Differential Input

It is important to note that using the additional R_F resistor connected between IN+ and BYPASS causes $V_{DD}/2$ to shift slightly, which could influence the THD+N performance of the amplifier. Although an additional external operational amplifier could be used to buffer BYPASS from R_F, tests in the lab have shown that the THD+N performance is only minimally affected by operating in the fully differential mode as shown in Figure 27. The following sections discuss the selection of the components used in Figure 26 and Figure 27.

COMPONENT SELECTION

Gain Setting Resistors, R_F and R_I

The gain for each audio input of the TPA321 is set by resistors R_F and R_I according to Equation 5 for BTL mode.

$$\text{BTL Gain} = A_V = -2\left(\frac{R_F}{R_I}\right) \tag{5}$$

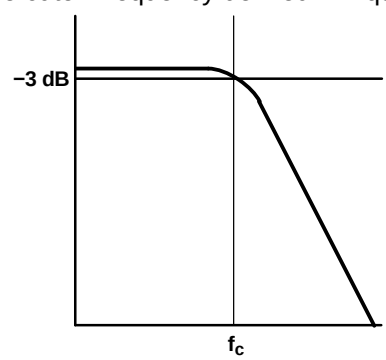
BTL mode operation brings about the factor 2 in the gain equation due to the inverting amplifier mirroring the voltage swing across the load. Given that the TPA321 is a MOS amplifier, the input impedance is high; consequently, input leakage currents are not generally a concern, although noise in the circuit increases as the value of R_F increases. In addition, a certain range of R_F values is required for proper start-up operation of the amplifier. Taken together, it is recommended that the effective impedance seen by the inverting node of the amplifier be set between 5 kΩ and 20 kΩ. The effective impedance is calculated in Equation 6.

$$\text{Effective Impedance} = \frac{R_F R_I}{R_F + R_I} \tag{6}$$

As an example, consider an input resistance of 10 kΩ and a feedback resistor of 50 kΩ. The BTL gain of the amplifier would be –10 V/V, and the effective impedance at the inverting terminal would be 8.3 kΩ, which is well within the recommended range.

For high-performance applications metal film resistors are recommended because they tend to have lower noise levels than carbon resistors. For values of R_F above 50 kΩ, the amplifier tends to become unstable due to a pole formed from R_F and the inherent input capacitance of the MOS input structure. For this reason, place a small compensation capacitor (C_F) of approximately 5 pF in parallel with R_F when R_F is greater than 50 kΩ. In effect, this creates a low-pass filter network with the cutoff frequency defined in Equation 7.

$$f_C = \frac{1}{2\pi R_F C_F} \tag{7}$$

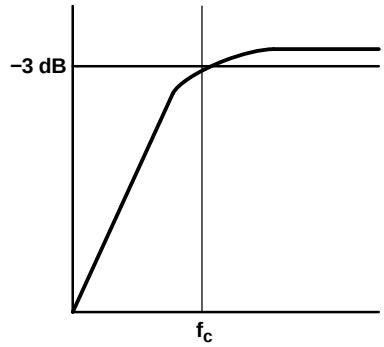


For example, if R_F is 100 kΩ and C_F is 5 pF then f_c is 318 kHz, which is well outside of audio range.

Input Capacitor, C_I

In the typical application, input capacitor C_I is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and R_I form a high-pass filter with the corner frequency determined in Equation 8.

$$f_C = \frac{1}{2\pi R_I C_I} \tag{8}$$



The value of C_I is important to consider as it directly affects the bass (low-frequency) performance of the circuit. Consider the example where R_I is 10 kΩ and the specification calls for a flat bass response down to 40 Hz. Equation 8 is reconfigured as Equation 9.

$$C_I = \frac{1}{2\pi R_I f_C} \tag{9}$$

In this example, C_I is 0.40 µF, so one would likely choose a value in the range of 0.47 µF to 1 µF. A further consideration for this capacitor is the leakage path from the input source through the input network (R_I, C_I) and the feedback resistor (R_F) to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications, as the dc level there is held at $V_{DD}/2$, which is likely higher than the source dc level. It is important to confirm the capacitor polarity in the application.

Power Supply Decoupling, C_S

The TPA321 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 µF, placed as close as possible to the device V_{DD} lead, works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 µF or greater placed near the audio power amplifier is recommended.

Midrail Bypass Capacitor, C_B

The midrail bypass capacitor, C_B, is the most critical capacitor and serves several important functions. During start-up or recovery from shutdown mode, C_B determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier, which appears as degraded PSRR and THD + N. The capacitor is fed from a 250-kΩ source inside the amplifier. To keep the start-up pop as low as possible, the relationship shown in Equation 10 should be maintained, which insures the input capacitor is fully charged before the bypass capacitor is fully charged and the amplifier starts up.

$$\frac{10}{\left(C_B \times 250\ \text{k}\Omega\right)} \le \frac{1}{\left(R_F + R_I\right) C_I} \tag{10}$$

As an example, consider a circuit where C_B is 2.2 µF, C_I is 0.47 µF, R_F is 50 kΩ, and R_I is 10 kΩ. Inserting these values into the Equation 10 we get:

$$18.2 \le 35.5$$

which satisfies the rule. Bypass capacitor, C_B, values of 2.2-µF to 1-µF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

USING LOW-ESR CAPACITORS

Low-ESR capacitors are recommended throughout this application. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance, the more the real capacitor behaves like an ideal capacitor.

5-V VERSUS 3.3-V OPERATION

The TPA321 operates over a supply range of 2.5 V to 5.5 V. This data sheet provides full specifications for 5-V and 3.3-V operation, as these are considered to be the two most common standard voltages. There are no special considerations for 3.3-V versus 5-V operation with respect to supply bypassing, gain setting, or stability. The most important consideration is that of output power. Each amplifier in TPA321 can produce a maximum voltage swing of V_{DD} –1 V. This means, for 3.3-V operation, clipping starts to occur when $V_{O(PP)}$ = 2.3 V as opposed to $V_{O(PP)}$ = 4 V at 5 V. The reduced voltage swing subsequently reduces maximum output power into an 8-Ω load before distortion becomes significant.

Operation from 3.3-V supplies, as can be shown from the efficiency formula in Equation 4, consumes approximately two-thirds the supply power for a given output-power level than operation from 5-V supplies.

HEADROOM AND THERMAL CONSIDERATIONS

Linear power amplifiers dissipate a significant amount of heat in the package under normal operating conditions. A typical music CD requires 12 dB to 15 dB of dynamic headroom to pass the loudest portions without distortion as compared with the average power output. The TPA321 data sheet shows that when the TPA321 is operating from a 5-V supply into a 8-Ω speaker, 350 mW peaks are available. Converting watts to dB:

$$P_{dB} = 10\,\mathrm{Log}\frac{P_W}{P_{ref}} = 10\mathrm{Log}\,\frac{350\ \mathrm{mW}}{1\ \mathrm{W}} = -4.6\ \mathrm{dB}$$

Subtracting the headroom restriction to obtain the average listening level without distortion yields:

4.6 dB – 15 dB = –19.6 dB (15-dB headroom)

4.6 dB – 12 dB = –16.6 dB (12-dB headroom)

4.6 dB – 9 dB = –13.6 dB (9-dB headroom)

4.6 dB – 6 dB = –10.6 dB (6-dB headroom)

4.6 dB – 3 dB = –7.6 dB (3-dB headroom)

Converting dB back into watts:

$$P_W = 10^{PdB/10} \times P_{ref}$$

= 11 mW (15 dB headroom)

= 22 mW (12-dB headroom)

= 44 mW (9-dB headroom)

= 88 mW (6-dB headroom)

= 175 mW (3-dB headroom)

This is valuable information to consider when attempting to estimate the heat dissipation requirements for the amplifier system. Comparing the absolute worst case, which is 350 mW of continuous power output with 0 dB of headroom, against 12-dB and 15-dB applications drastically affects maximum ambient temperature ratings for the system. Using the power dissipation curves for a 5-V, 8-Ω system, the internal dissipation in the TPA321 and maximum ambient temperatures is shown in Table 2.

Table 2. TPA321 Power Rating, 5-V, 8-Ω BTL

PEAK OUTPUT POWER (mW)	AVERAGE OUTPUT POWER	POWER DISSIPATION (mW)	MAXIMUM AMBIENT TEMPERATURE
			0 CFM
350	350 mW	600	46°C
350	175 mW (3 dB)	500	64°C
350	88 mW (6 dB)	380	85°C
350	44 mW (9 dB)	300	98°C
350	22 mW (12 dB)	200	115°C
350	11 mW (15 dB)	180	119°C

Table 2 shows that the TPA321 can be used to its full 350-mW rating without any heat sinking in still air up to 46°C.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPA321D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPA321
TPA321D.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPA321
TPA321DGN	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AJB
TPA321DGN.A	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AJB
TPA321DGNR	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AJB
TPA321DGNR.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AJB
TPA321DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPA321
TPA321DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TPA321

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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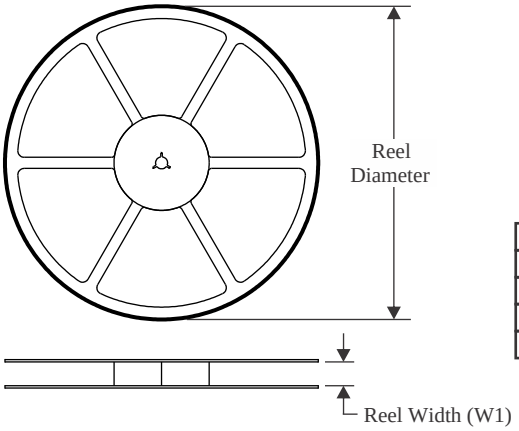
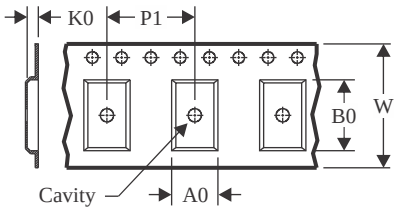
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

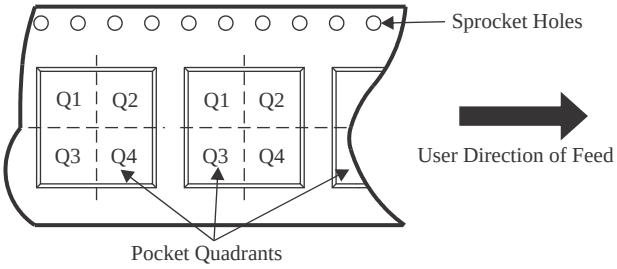


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

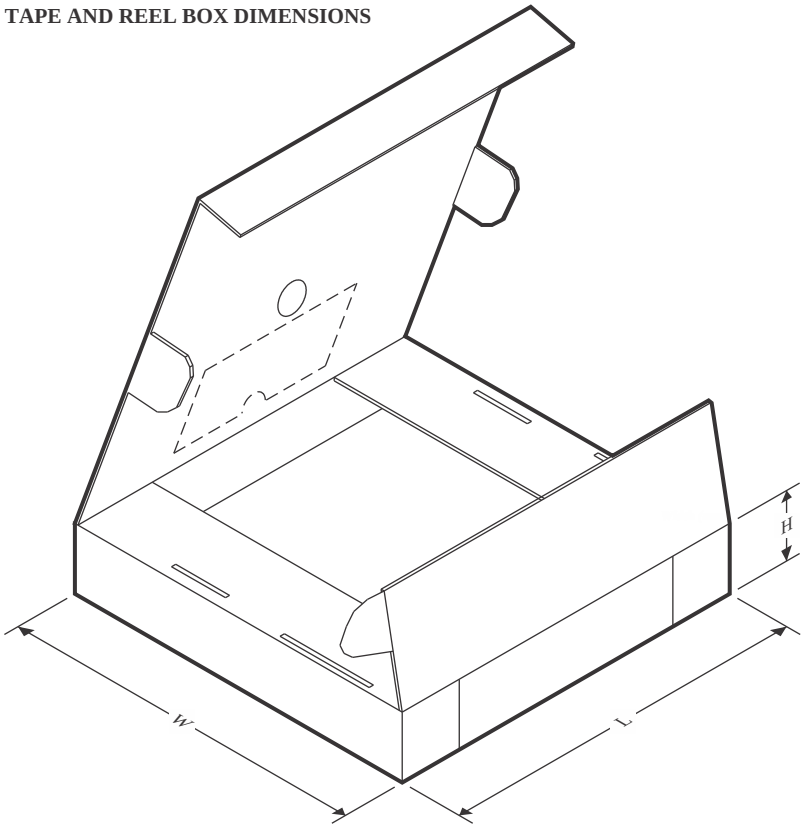
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA321DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPA321DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

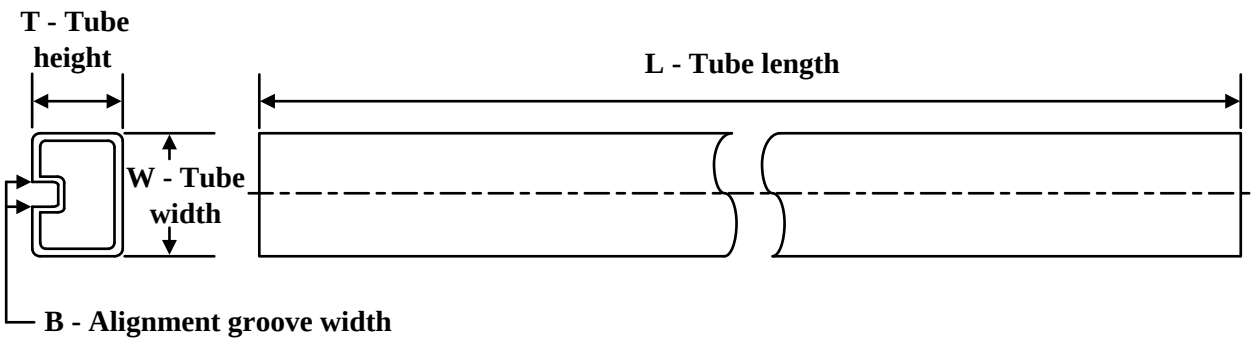
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA321DGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
TPA321DR	SOIC	D	8	2500	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPA321D	D	SOIC	8	75	505.46	6.76	3810	4
TPA321D.A	D	SOIC	8	75	505.46	6.76	3810	4

GENERIC PACKAGE VIEW

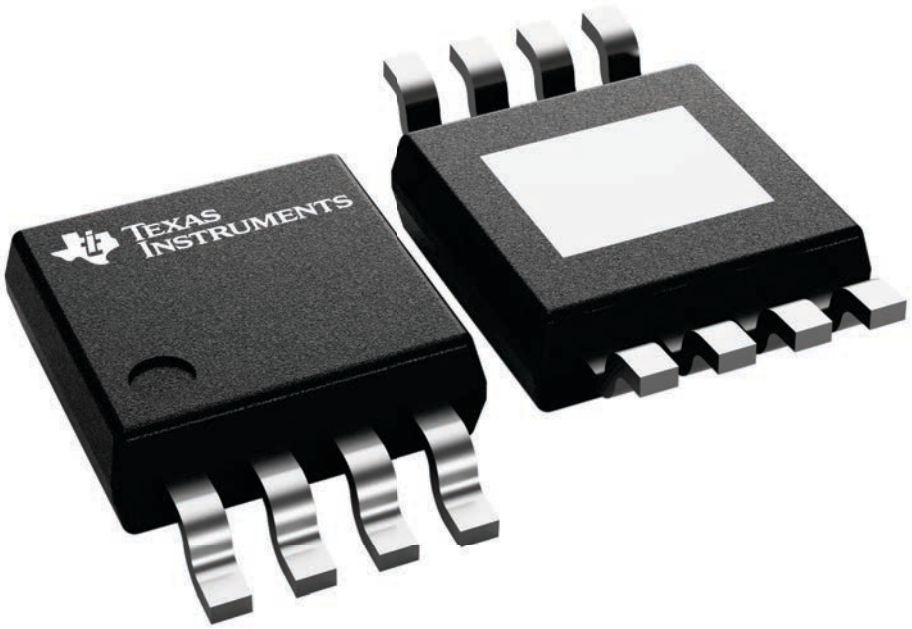
DGN 8

PowerPAD™ HVSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

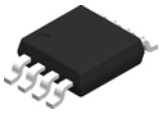
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/B

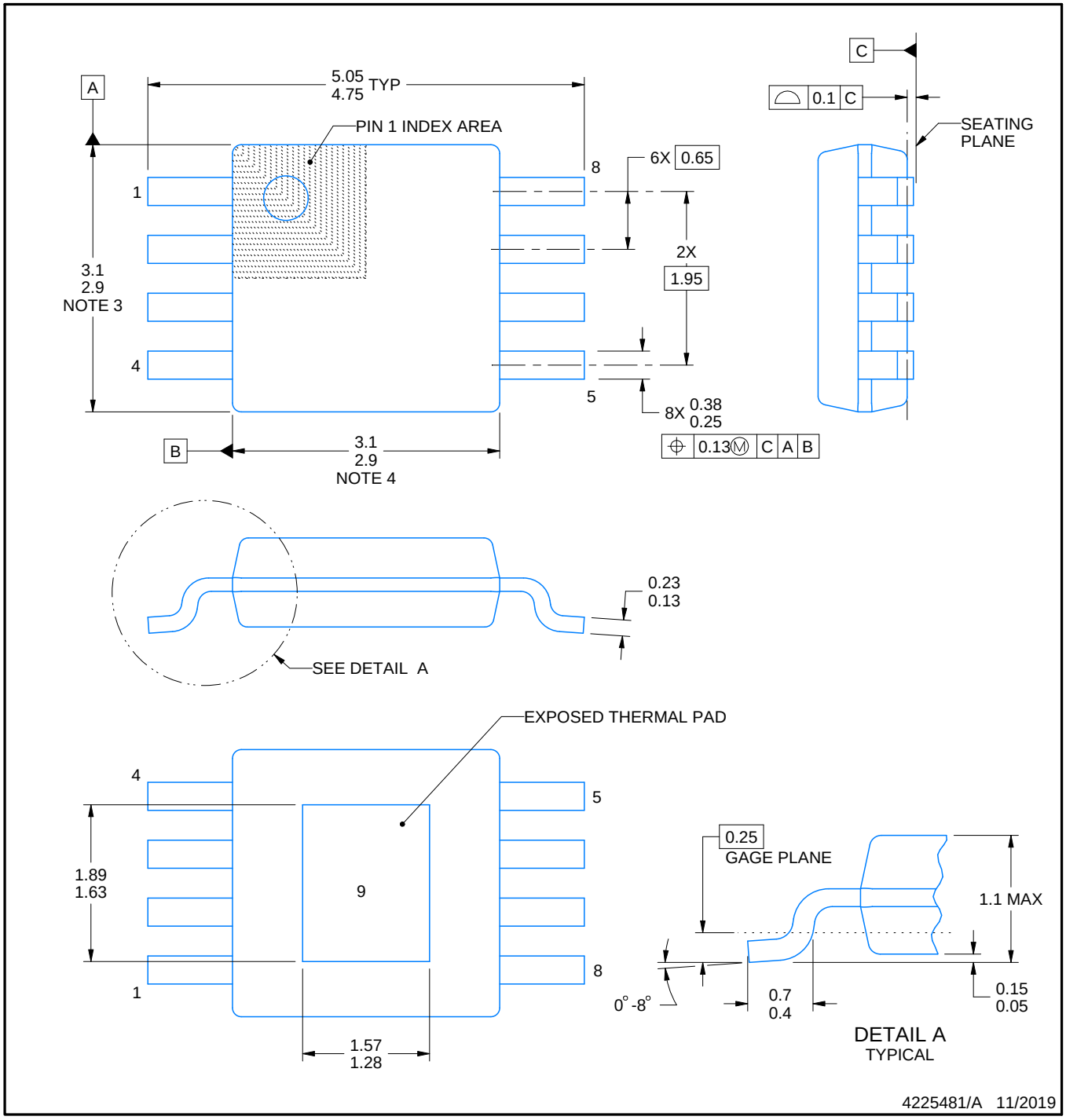
PACKAGE OUTLINE

DGN0008D



PowerPAD™ VSSOP - 1.1 mm max height

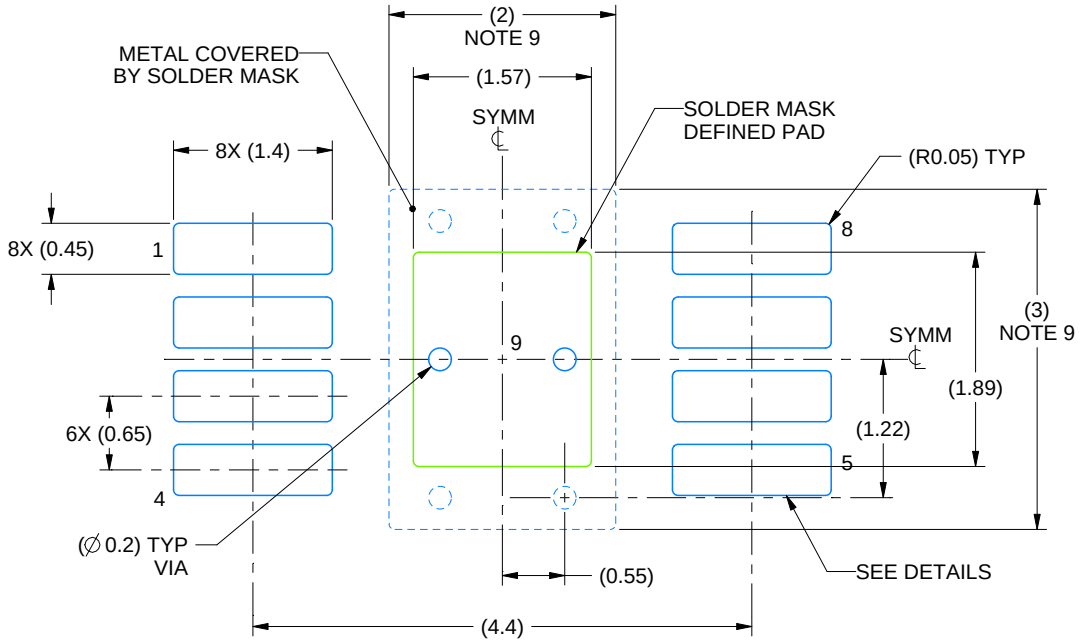
SMALL OUTLINE PACKAGE



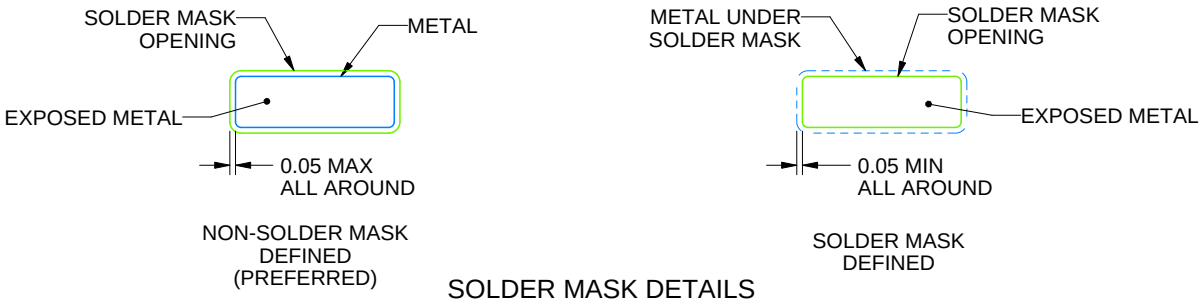
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

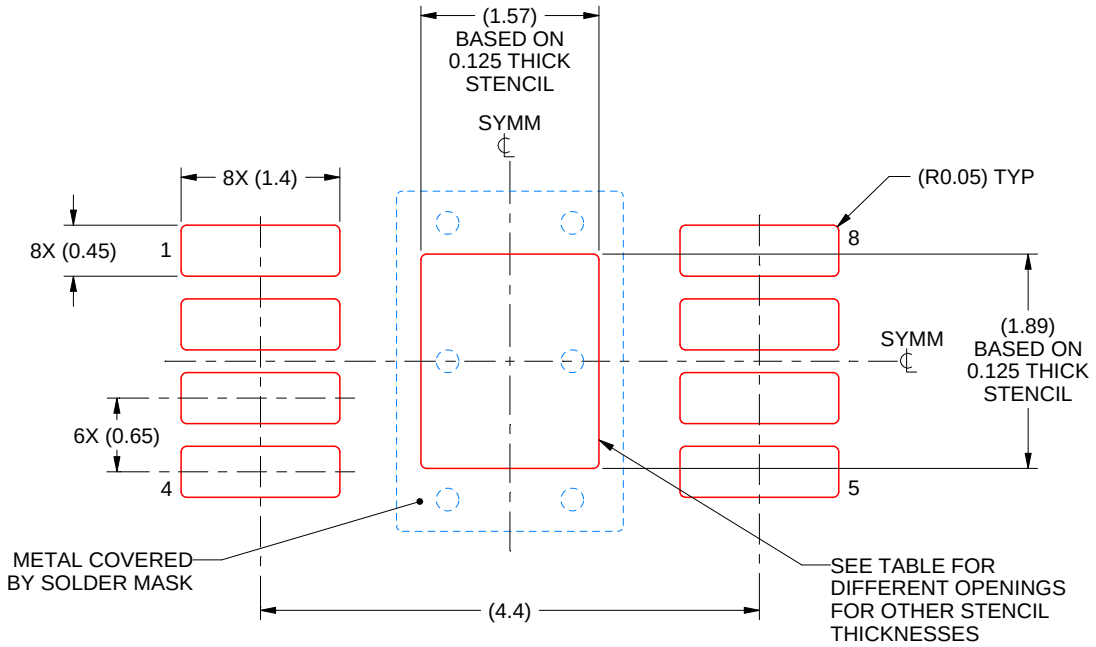


SOLDER MASK DETAILS

4225481/A 11/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



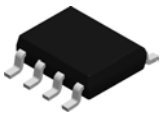
SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

4225481/A 11/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

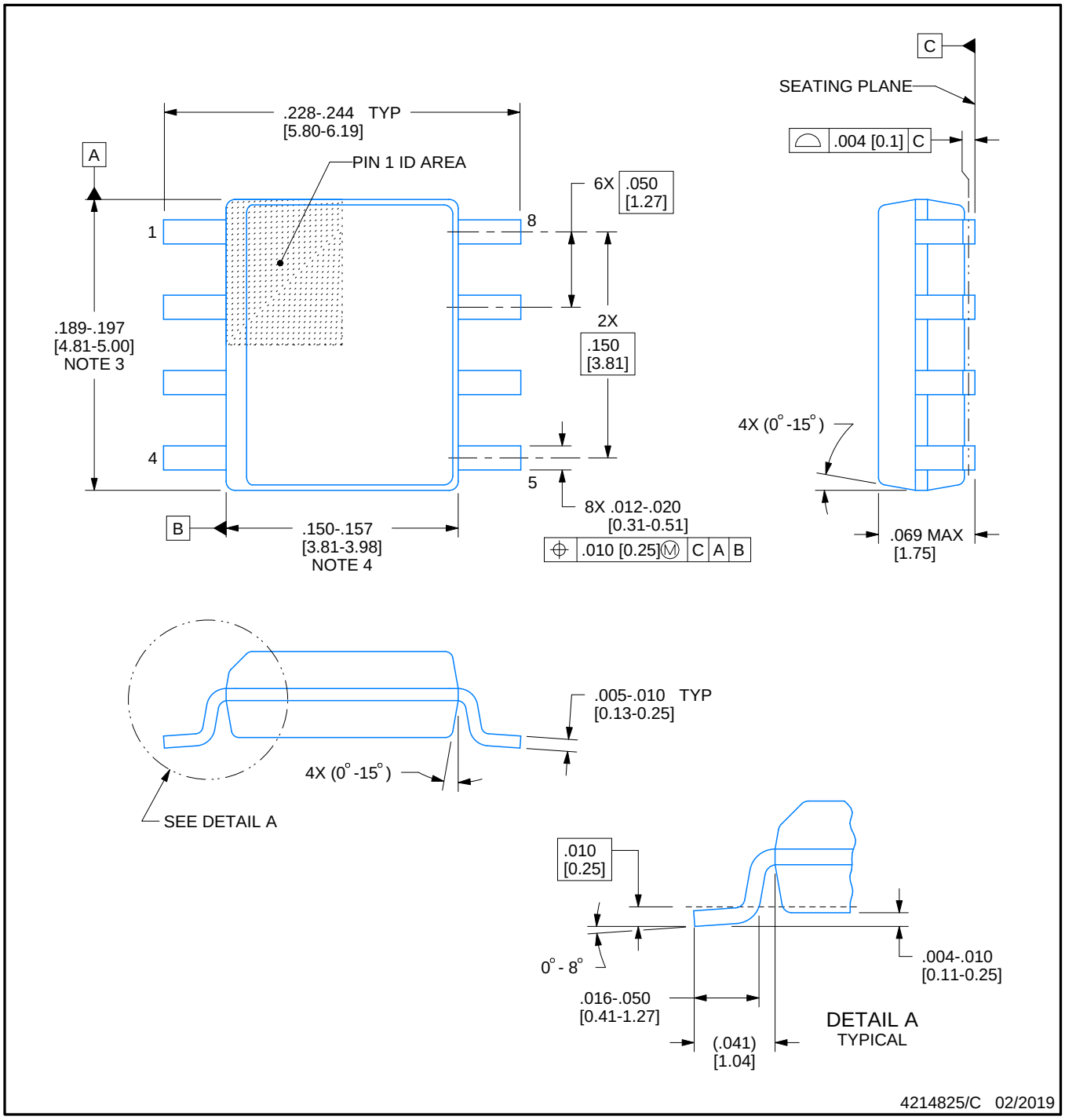


PACKAGE OUTLINE

D0008A

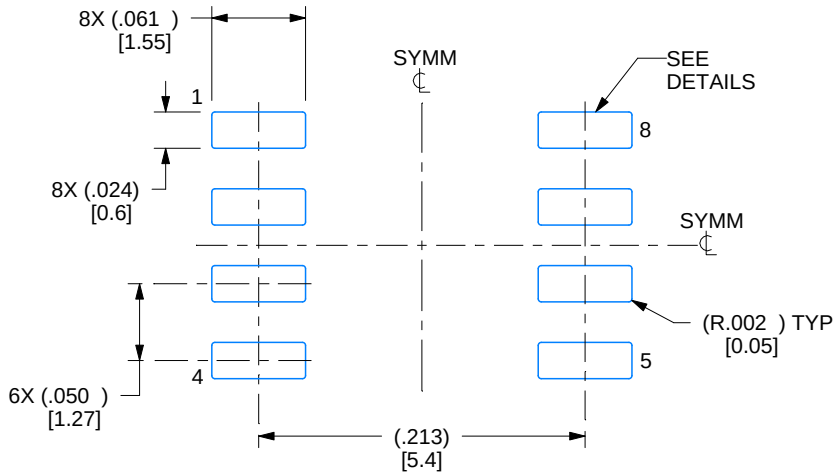
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

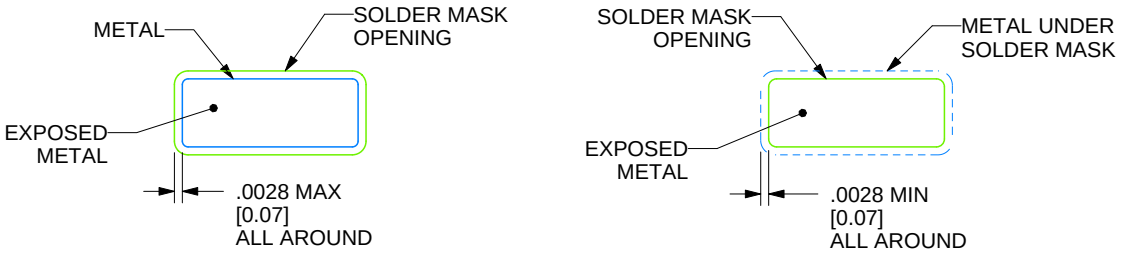


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

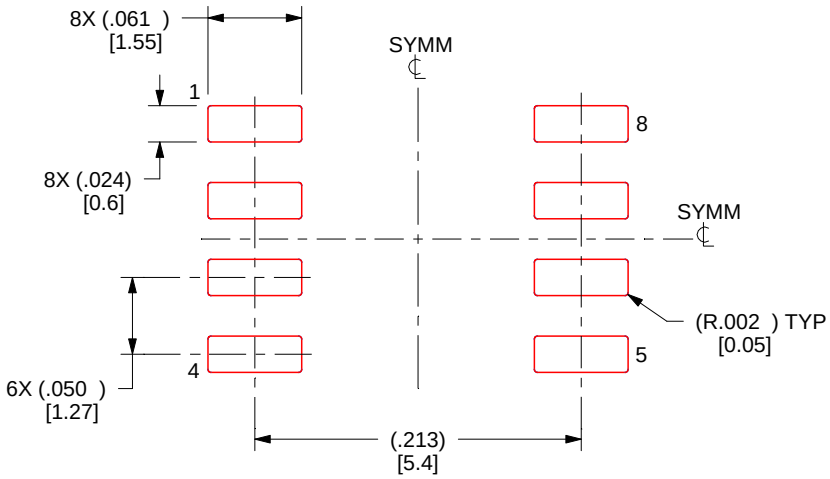


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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