Not Recommended for New Designs

SMJ320C31, SMJ320LC31, SMQ320LC31 DIGITAL SIGNAL PROCESSORS

SGUS026G − APRIL 1998 − REVISED SEPTEMBER 2006

- Processed to MIL-PRF-38535 (QML)
- Operating Temperature Ranges:
  - Military (M) −55°C to 125°C
  - Special (S) −55°C to 105°C
- SMD Approval
- High-Performance Floating-Point Digital Signal Processor (DSP):
  - SMJ320C31-60 (5 V)
    33-ns Instruction Cycle Time
    330 Million Operations Per Second (MOPS), 60 Million Floating-Point Operations Per Second (MFLOPS), 30 Million Instructions Per Second (MIPS)
  - SMJ320C31-50 (5 V)
    40-ns Instruction Cycle Time
    275 MOPS, 50 MFLOPS, 25 MIPS
  - SMJ320C31-40 (5 V)
    50-ns Instruction Cycle Time
    220 MOPS, 40 MFLOPS, 20 MIPS
  - SMJ320LC31-40 (3.3 V)
    50-ns Instruction Cycle Time
    220 MOPS, 40 MFLOPS, 20 MIPS
  - SMQ320LC31-40 (3.3 V)
    50-ns Instruction Cycle Time
    220 MOPS, 40 MFLOPS, 20 MIPS
- 32-Bit High-Performance CPU
- 16-/32-Bit Integer and 32-/40-Bit Floating-Point Operations
- 32-Bit Instruction and Data Words, 24-Bit Addresses
- Two 1K Word × 32-Bit Single-Cycle Dual-Access On-Chip RAM Blocks
- Boot-Program Loader
- 64-Word × 32-Bit Instruction Cache
- Eight Extended-Precision Registers
- Two Address Generators With Eight Auxiliary Registers and Two Auxiliary Register Arithmetic Units (ARAUs)
- Two Low-Power Modes
- On-Chip Memory-Mapped Peripherals:
  - One Serial Port Supporting 8-/16-/24-/32-Bit Transfers
  - Two 32-Bit Timers
  - One-Channel Direct Memory Access (DMA) Coprocessor for Concurrent I/O and CPU Operation
- Fabricated Using Enhanced Performance Implanted CMOS (EPIC™) Technology by Texas Instruments (TI)
- Two- and Three-Operand Instructions
- 40 / 32-Bit Floating-Point / Integer Multiplier and Arithmetic Logic Unit (ALU)
- Parallel ALU and Multiplier Execution in a Single Cycle
- Block-Repeat Capability
- Zero-Overhead Loops With Single-Cycle Branches
- Conditional Calls and Returns
- Interlocked Instructions for Multiprocessing Support
- Bus-Control Registers Configure Strobe-Control Wait-State Generation
- Validated Ada Compiler
- Integer, Floating-Point, and Logical Operations
- 32-Bit Barrel Shifter
- One 32-Bit Data Bus (24-Bit Address)
- Packaging
  - 132-Lead Ceramic Quad Flatpack With Nonconductive Tie-Bar (HFG Suffix)
  - 141-Pin Ceramic Staggered Pin Grid- Array Package (GFA Suffix)
  - 132-Lead TAB Frame
  - 132-Lead Plastic Quad Flatpack (PQ Suffix)

description

The SMJ320C31, SMJ320LC31, and SMQ320LC31 digital signal processors (DSPs) are 32-bit, floating-point processors manufactured in 0.6-µm triple-level-metal CMOS technology. The devices are part of the SMJ320C3x generation of DSPs from Texas Instruments.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

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description (continued)

The SMJ320C3x internal busing and special digital-signal-processing instruction set have the speed and flexibility to execute up to 60 MFLOPS. The SMJ320C3x optimizes speed by implementing functions in hardware that other processors implement through software or microcode. This hardware-intensive approach provides performance previously unavailable on a single chip.

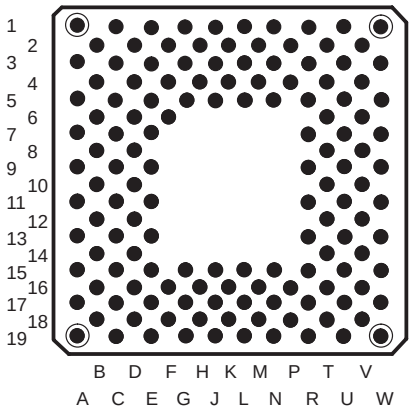
The SMJ320C3x can perform parallel multiply and ALU operations on integer or floating-point data in a single cycle. Each processor also possesses a general-purpose register file, a program cache, dedicated ARAUs, internal dual-access memories, one DMA channel supporting concurrent I/O, and a short machine-cycle time. High performance and ease of use are results of these features.

General-purpose applications are greatly enhanced by the large address space, multiprocessor interface, internally and externally generated wait states, one external interface port, two timers, one serial port, and multiple-interrupt structure. The SMJ320C3x supports a wide variety of system applications from host processor to dedicated coprocessor.

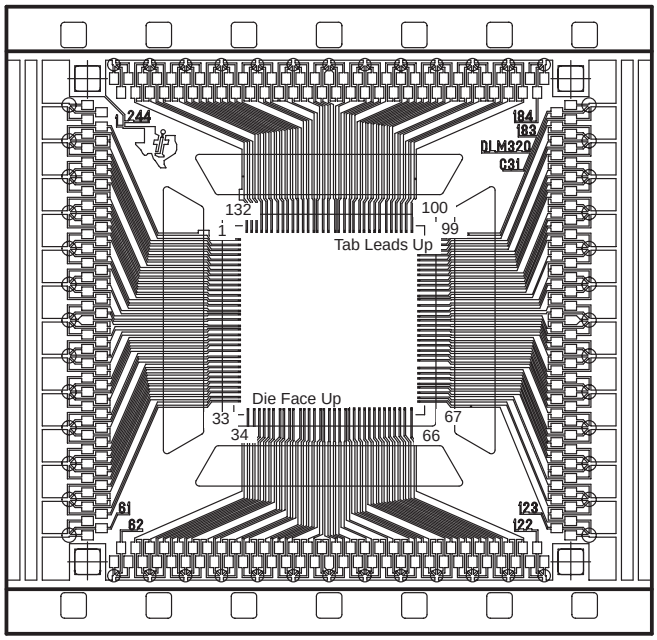
High-level-language support is easily implemented through a register-based architecture, large address space, powerful addressing modes, flexible instruction set, and well-supported floating-point arithmetic.

For additional information when designing for cold temperature operation, please see Texas Instruments application report *320C3x, 320C4x and 320MCM42x Power-up Sensitivity at Cold Temperature*, literature number SGUA001.

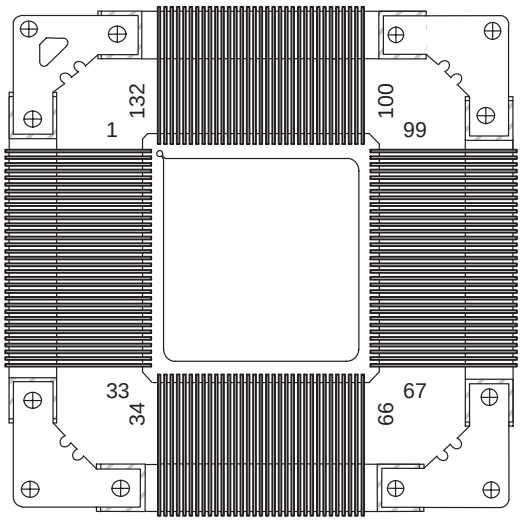
141-PIN GFA STAGGERED GRID ARRAY PACKAGE (BOTTOM VIEW)



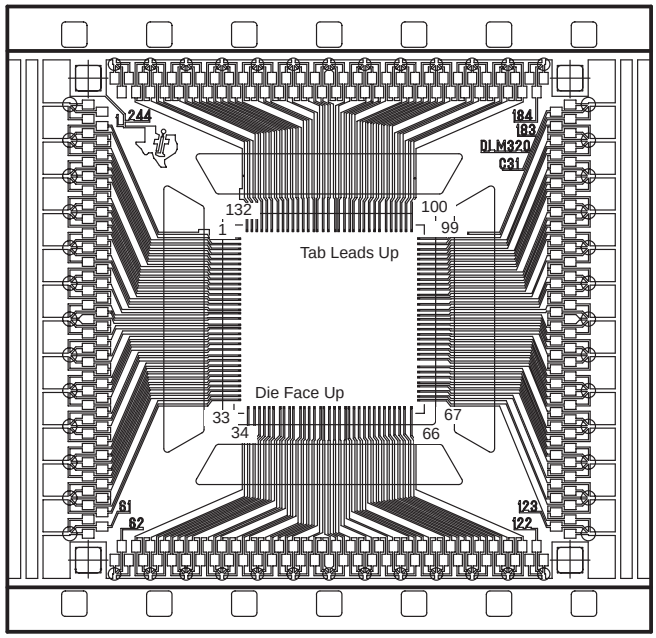
TA PACKAGE (TOP VIEW)



132-PIN HFG QUAD FLATPACK (TOP VIEW)



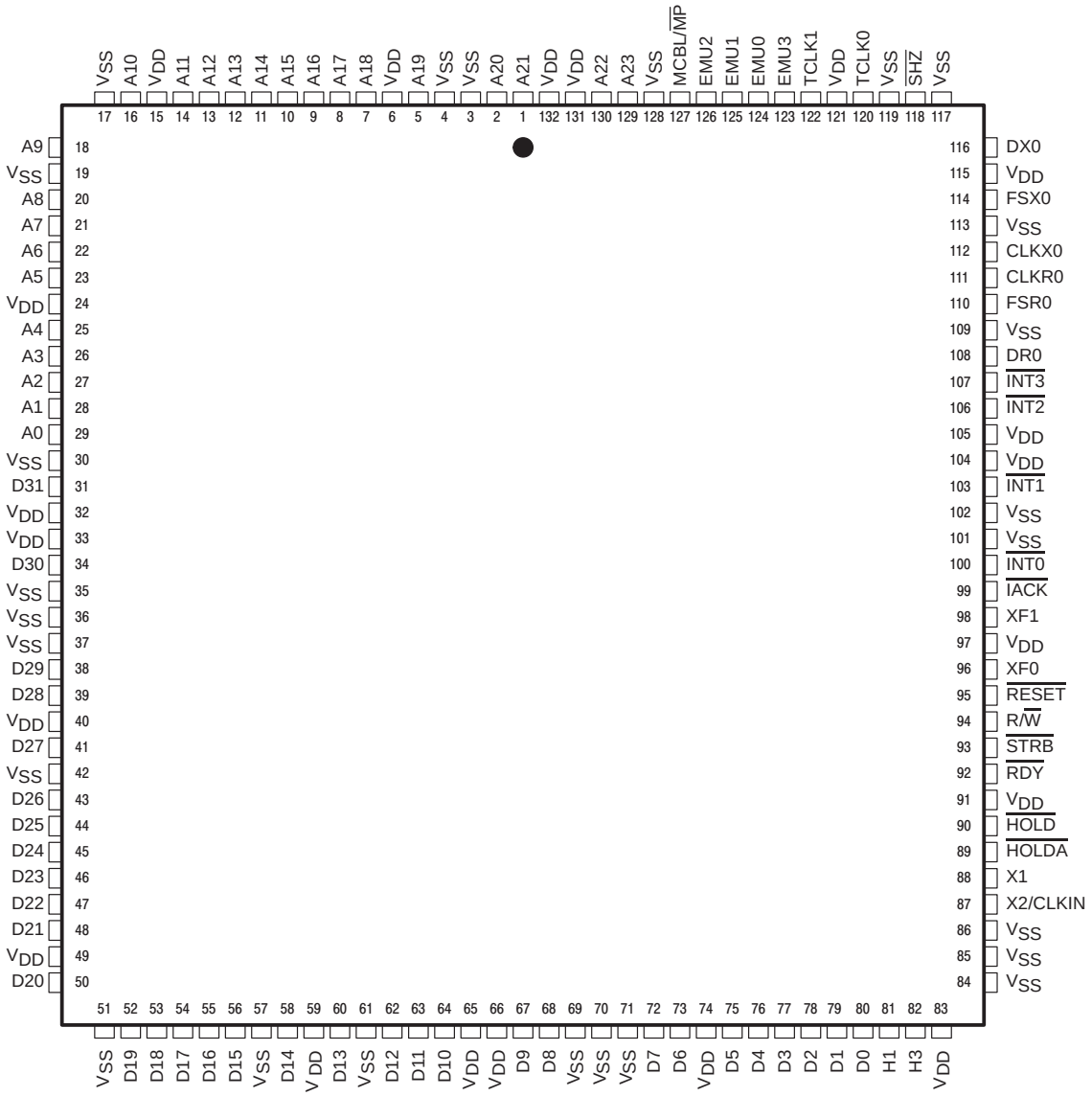
TB PACKAGE (TOP VIEW)



SMQ320LC31 pinout (top view)

The SMQ320LC31 device is also packaged in a132-pin plastic quad flatpack (PQ Suffix). The full part numbers are SMQ320LC31PQM40 and 5962-9760601NXB.

PQ PACKAGE
(TOP VIEW)



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Terminal Assignments

PIN NUMBER			NAME	PIN NUMBER			NAME
PQ PKG	HFG PKG	GFA PKG		PQ PKG	HFG PKG	GFA PKG	
29	12	L1	A0	64	47	W9	D10
28	11	K2	A1	63	46	U9	D11
27	10	J1	A2	62	45	V8	D12
26	9	J3	A3	60	43	W7	D13
25	8	G1	A4	58	41	U7	D14
23	6	F2	A5	56	39	V6	D15
22	5	E1	A6	55	38	W5	D16
21	4	E3	A7	54	37	U5	D17
20	3	D2	A8	53	36	V4	D18
18	1	C1	A9	52	35	W3	D19
16	131	C3	A10	50	33	U3	D20
14	129	B2	A11	48	31	V2	D21
13	128	A1	A12	47	30	W1	D22
12	127	C5	A13	46	29	R3	D23
11	126	B4	A14	45	28	T2	D24
10	125	A3	A15	44	27	U1	D25
9	124	C7	A16	43	26	N3	D26
8	123	B6	A17	41	24	P2	D27
7	122	C9	A18	39	22	R1	D28
5	120	B8	A19	38	21	L3	D29
2	117	A7	A20	34	17	M2	D30
1	116	A9	A21	31	14	N1	D31
130	113	B10	A22	108	91	C19	DR0
129	112	A11	A23	116	99	C17	DX0
111	94	E17	CLKR0	124	107	B14	EMU0
112	95	A19	CLKX0	125	108	A13	EMU1
80	63	W19	D0	126	109	B12	EMU2
79	62	V16	D1	123	106	A15	EMU3
78	61	W17	D2	110	93	D18	FSR0
77	60	U13	D3	114	97	B18	FSX0
76	59	V14	D4	81	73	P18	$\overline{\text{HOLD}}$
75	58	W15	D5	82	72	R19	$\overline{\text{HOLDA}}$
73	56	U11	D6	90	64	V18	H1
72	55	V12	D7	89	65	U17	H3
68	51	W11	D8	99	82	H18	$\overline{\text{IACK}}$
67	50	V10	D9	100	83	J17	$\overline{\text{INT0}}$

† CV_{SS}, V_{SSL}, and IV_{SS} are on the same plane.
‡ AV_{DD}, DV_{DD}, CV_{DD}, and PV_{DD} are on the same plane.
§ V_{SUBS} connects to die metallization. Tie this pin to clean ground.

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Terminal Assignments (Continued)

PIN				PIN			
NUMBER			NAME	NUMBER			NAME
PQ PKG	HFG PKG	GFA PKG		PQ PKG	HFG PKG	GFA PKG	
103	86	E19	$\overline{INT1}$	30	18	P4	V_{SSL}†
106	89	F18	$\overline{INT2}$	35	19	T10	V_{SSL}†
107	90	G17	$\overline{INT3}$	36	20	K4	DV_{SS}
127	110	C11	MCBL/$\overline{MP}$	37	25	T4	IV_{SS}†
92	77	L19	R/$\overline{W}$	42	34	G3	DV_{SS}
95	75	N17	$\overline{RDY}$	51	40	K16	CV_{SS}†
94	78	K18	$\overline{RESET}$	57	44	T8	IV_{SS}†
118	101	A17	$\overline{SHZ}$	61	52	T12	DV_{SS}
93	76	M18	$\overline{STRB}$	69	53	R11	V_{SSL}†
120	103	B16	TCLK0	70	54	J15	V_{SSL}†
	105	C15	TCLK1	71	67	W13	DV_{SS}
	121	G5	AV_{DD}‡	84	68	D10	CV_{SS}†
6	130	E7	AV_{DD}‡	85	69	D16	IV_{SS}†
15	7	E5	AV_{DD}‡	86	84	T16	DV_{SS}
24	15	N5	V_{DDL}	101	85	D12	V_{SSL}†
32	16	R5	V_{DDL}	102	92	F16	CV_{SS}†
33	23	H4	DV_{DD}‡	109	96	H16	IV_{SS}†
40	32	J5	DV_{DD}‡	113	100	D14	V_{SUBS}§
49	42	T14	DV_{DD}‡	117	102	U15	DV_{SS}
59	48	R7	V_{DDL}	119	111	C13	CV_{SS}†
65	49	R9	V_{DDL}	128	71	T18	X1
66	57	R13	DV_{DD}‡	88	70	U19	X2/CLKIN
74	66	R15	DV_{DD}‡	87	79	J19	XF0
83	74	P16	CV_{DD}‡	96	81	G19	XF1
91	80	N15	CV_{DD}‡	98		F6	No Connect
97	87	G15	V_{DDL}			D4	DV_{SS}
104	88	E15	V_{DDL}			N19	DV_{SS}
105	98	L15	PV_{DD}‡			R17	DV_{SS}
115	104	E9	PV_{DD}‡			L17	DV_{SS}
121	114	E13	V_{DDL}			M16	DV_{SS}
131	115	E11	V_{DDL}			D6	DV_{SS}
132	118	L5	V_{SSL}†			A5	DV_{SS}
3	119	H2	DV_{SS}			D8	DV_{SS}
4	132	M4	CV_{SS}†				
17	2	F4	DV_{SS}				
19	13	T6	CV_{SS}†				

† CV_{SS}, V_{SSL}, and IV_{SS} are on the same plane.
‡ AV_{DD}, DV_{DD}, CV_{DD}, and PV_{DD} are on the same plane.
§ V_{SUBS} connects to die metallization. Tie this pin to clean ground.

Terminal Functions

TERMINAL NAME	QTY	TYPE†	DESCRIPTION	CONDITIONS WHEN SIGNAL IS Z TYPE‡		
PRIMARY-BUS INTERFACE						
D31−D0	32	I/O/Z	32-bit data port	S	H	R
A23−A0	24	O/Z	24-bit address port	S	H	R
R/$\overline{W}$	1	O/Z	Read/write. R/$\overline{W}$ is high when a read is performed and low when a write is performed over the parallel interface.	S	H	R
$\overline{STRB}$	1	O/Z	External-access strobe	S	H	
$\overline{RDY}$	1	I	Ready. $\overline{RDY}$ indicates that the external device is prepared for a transaction completion.			
$\overline{HOLD}$	1	I	Hold. When $\overline{HOLD}$ is a logic low, any ongoing transaction is completed. A23−A0, D31−D0, $\overline{STRB}$, and R/$\overline{W}$ are placed in the high-impedance state and all transactions over the primary-bus interface are held until $\overline{HOLD}$ becomes a logic high or until the NOHOLD bit of the primary-bus-control register is set.			
$\overline{HOLDA}$	1	O/Z	Hold acknowledge. $\overline{HOLDA}$ is generated in response to a logic low on $\overline{HOLD}$. $\overline{HOLDA}$ indicates that A23−A0, D31−D0, $\overline{STRB}$, and R/$\overline{W}$ are in the high-impedance state and that all transactions over the bus are held. $\overline{HOLDA}$ is high in response to a logic high of $\overline{HOLD}$ or the NOHOLD bit of the primary-bus-control register is set.	S		
CONTROL SIGNALS						
$\overline{RESET}$	1	I	Reset. When $\overline{RESET}$ is a logic low, the device is in the reset condition. When $\overline{RESET}$ becomes a logic high, execution begins from the location specified by the reset vector.			
$\overline{INT3}$−$\overline{INT0}$	4	I	External interrupts			
$\overline{IACK}$	1	O/Z	Interrupt acknowledge. $\overline{IACK}$ is generated by the IACK instruction. $\overline{IACK}$ can be used to indicate the beginning or the end of an interrupt-service routine.	S		
MCBL/$\overline{MP}$	1	I	Microcomputer boot-loader/microprocessor mode-select			
$\overline{SHZ}$	1	I	Shutdown high impedance. When active, $\overline{SHZ}$ shuts down the device and places all pins in the high-impedance state. $\overline{SHZ}$ is used for board-level testing to ensure that no dual-drive conditions occur. **CAUTION:** A low on $\overline{SHZ}$ corrupts the device memory and register contents. Reset the device with $\overline{SHZ}$ high to restore it to a known operating condition.			
XF1, XF0	2	I/O/Z	External flags. XF1 and XF0 are used as general-purpose I/Os or to support interlocked processor instruction.	S		R
SERIAL PORT 0 SIGNALS						
CLKR0	1	I/O/Z	Serial port 0 receive clock. CLKR0 is the serial shift clock for the serial port 0 receiver.	S		R
CLKX0	1	I/O/Z	Serial port 0 transmit clock. CLKX0 is the serial shift clock for the serial port 0 transmitter.	S		R
DR0	1	I/O/Z	Data-receive. Serial port 0 receives serial data on DR0.	S		R
DX0	1	I/O/Z	Data-transmit output. Serial port 0 transmits serial data on DX0.	S		R
FSR0	1	I/O/Z	Frame-synchronization pulse for receive. The FSR0 pulse initiates the data-receive process using DR0.	S		R
FSX0	1	I/O/Z	Frame-synchronization pulse for transmit. The FSX0 pulse initiates the data-transmit process using DX0.	S		R
TIMER SIGNALS						
TCLK0	1	I/O/Z	Timer clock 0. As an input, TCLK0 is used by timer 0 to count external pulses. As an output, TCLK0 outputs pulses generated by timer 0.	S		
TCLK1	1	I/O/Z	Timer clock 1. As an input, TCLK0 is used by timer 1 to count external pulses. As an output, TCLK1 outputs pulses generated by timer 1.	S		

† I = input, O = output, Z = high-impedance state
‡ S = $\overline{SHZ}$ active, H = $\overline{HOLD}$ active, R = $\overline{RESET}$ active

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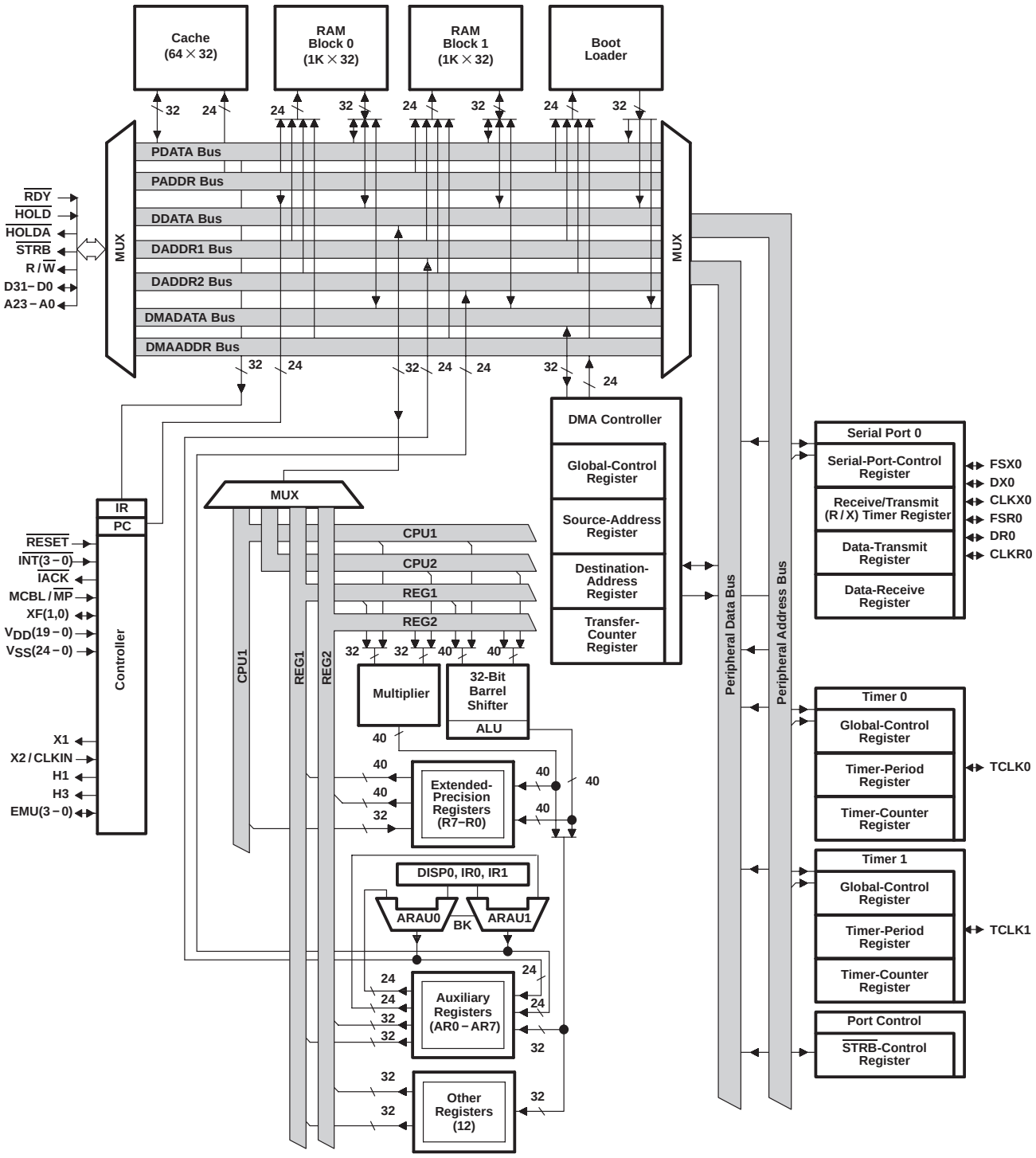
Terminal Functions (Continued)

TERMINAL NAME	TERMINAL QTY	TYPE†	DESCRIPTION	CONDITIONS WHEN SIGNAL IS Z TYPE‡
SUPPLY AND OSCILLATOR SIGNALS				
H1	1	O/Z	External H1 clock. H1 has a period equal to twice CLKIN.	S
H3	1	O/Z	External H3 clock. H3 has a period equal to twice CLKIN.	S
V_{DD}	20	I	5-V supply for ’C31 devices and 3.3-V supply for ’LC31 devices. All must be connected to a common supply plane.§	
V_{SS}	25	I	Ground. All grounds must be connected to a common ground plane.	
X1	1	O	Output from the internal-crystal oscillator. If a crystal is not used, X1 should be left unconnected.	
X2/CLKIN	1	I	Internal-oscillator input from a crystal or a clock	
RESERVED¶				
EMU2−EMU0	3	I	Reserved for emulation. Use pullup resistors to V_{DD}	
EMU3	1	O/Z	Reserved for emulation	S

† I = input, O = output, Z = high-impedance state
‡ S = $\overline{SHZ}$ active, H = HOLD active, R = $\overline{RESET}$ active
§ Recommended decoupling capacitor value is 0.1 µF.
¶ Follow the connections specified for the reserved pins. Use 18-kΩ−22-kΩ pullup resistors for best results. All V_{DD} supply pins must be connected to a common supply plane, and all ground pins must be connected to a common ground plane.

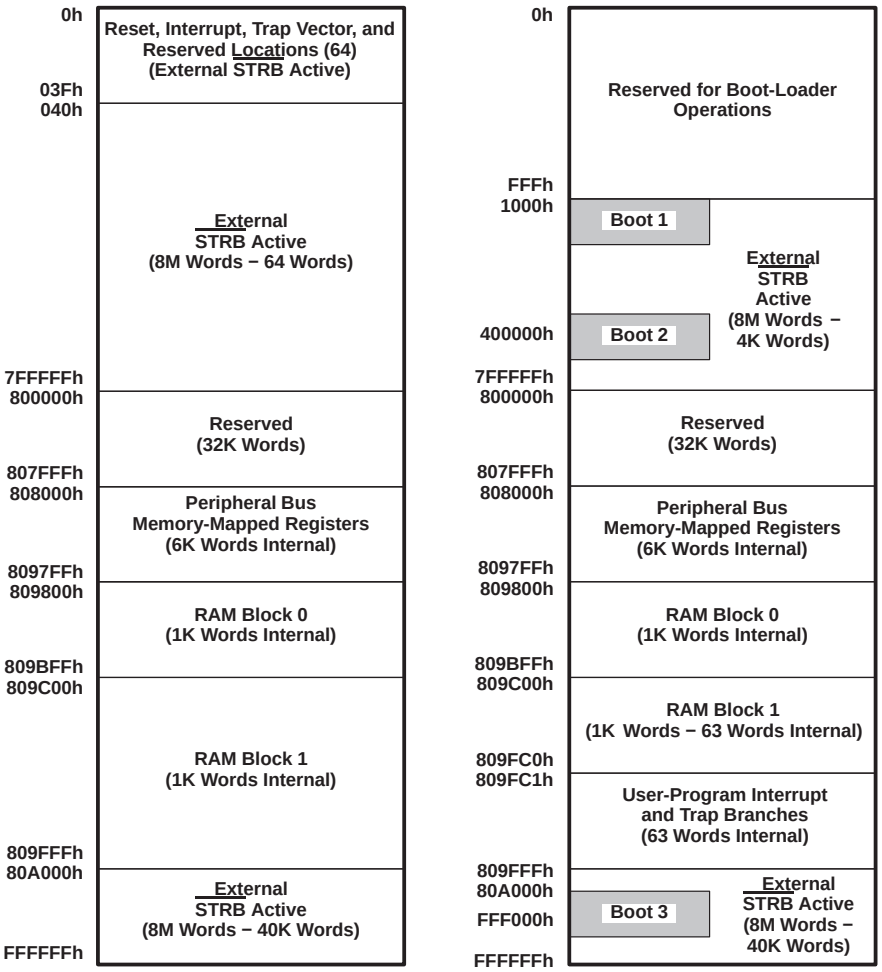
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functional block diagram



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memory map†

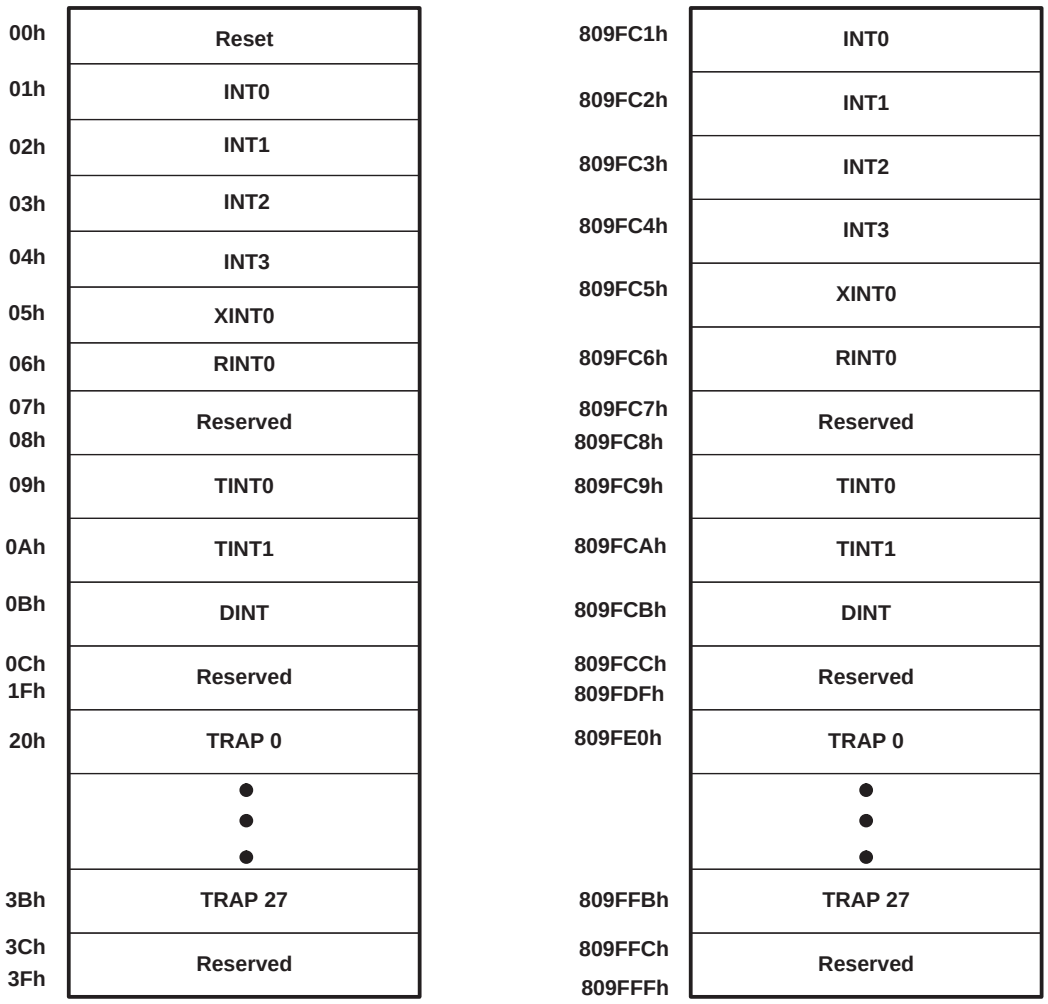


† Figure 1 depicts the memory map for the SMJ320C31. See the *TMS320C3x Users Guide* (literature number SPRU031) for a detailed description of this memory mapping.

Figure 1. SMJ320C31 Memory Map

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memory map (continued)



(a) Microprocessor Mode

(b) Microcomputer / Boot-Loader Mode

Figure 2. Reset, Interrupt, and Trap Vector/Branches Memory-Map Locations

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memory map (continued)

808000h	DMA Global Control
808004h	DMA Source Address
808006h	DMA Destination Address
808008h	DMA Transfer Counter
808020h	Timer 0 Global Control
808024h	Timer 0 Counter
808028h	Timer 0 Period Register
808030h	Timer 1 Global Control
808034h	Timer 1 Counter
808038h	Timer 1 Period Register
808040h	Serial Global Control
808042h	FSX/DX/CLKX Serial Port Control
808043h	FSR/DR/CLKR Serial Port Control
808044h	Serial R/X Timer Control
808045h	Serial R/X Timer Counter
808046h	Serial R/X Timer Period Register
808048h	Data-Transmit
80804Ch	Data-Receive
808064h	Primary-Bus Control

†Shading denotes reserved address locations

Figure 3. Peripheral Bus Memory-Mapped Registers†

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absolute maximum ratings over specified temperature range (unless otherwise noted)†

	’C31	’LC31
Supply voltage, V_{DD} (see Note 1)	−0.3 V to 7 V	−0.3 V to 5 V
Input voltage, V_I	−0.3 V to 7 V	−0.3 V to 5 V
Output voltage, V_O	−0.3 V to 7 V	−0.3 V to 5 V
Continuous power dissipation (worst case) (see Note 2)	1.7 W (for SMJ320C31-33)	850 mW (for SMJ320LC31-33)
Operating case temperature, T_C	−55°C to 125°C	− −55°C to 125°C
Storage temperature, T_{stg}	− 65°C to 150°C	− 65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to V_{SS}.

2. Actual operating power is less. This value was obtained under specially produced worst-case test conditions for the TMS320C31-33 and the TMS320LC31-33, which are not sustained during normal device operation. These conditions consist of continuous parallel writes of a checkerboard pattern to both primary and extension buses at the maximum rate possible. See normal (I_{CC}) current specification in the electrical characteristics table and also read *Calculation of TMS320C30 Power Dissipation Application Report* (literature number SPRA020).

recommended operating conditions (see Note 3)

			’C31			’LC31			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{DD}	Supply voltage (DV_{DD}, etc.)		4.75	5	5.25	3.13	3.3	3.47	V
V_{SS}	Supply voltage (CV_{SS}, etc.)			0			0		V
V_{IH}	High-level input voltage (except $\overline{RESET}$)		2.1		V_{DD} + 0.3*	1.8		V_{DD} + 0.3*	V
	High-level input voltage ($\overline{RESET}$)		2.2		V_{DD} + 0.3*	2.2		V_{DD} + 0.3*	V
V_{IL}	Low-level input voltage		− 0.3*		0.8	− 0.3*		0.6	V
I_{OH}	High-level output current				− 300			− 300	µA
I_{OL}	Low-level output current				2			2	mA
T_C	Operating case temperature	’320C31-40	−55		125				°C
		’320C31-50	−55		125				
		’320C31-60	−55		105				
		’320LC31-40				−55		125	
V_{TH}	High-level input voltage for CLKIN		3.0		V_{DD} + 0.3*	2.5		V_{DD} + 0.3*	V

* This parameter is not production tested.

NOTE 3: All voltage values are with respect to V_{SS}. All input and output voltage levels are TTL-compatible. CLKIN can be driven by a CMOS clock.

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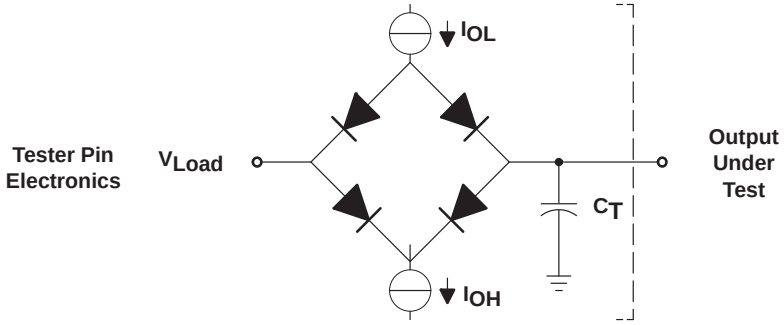
electrical characteristics over recommended ranges of supply voltage (unless otherwise noted) (see Note 3)†

PARAMETER		TEST CONDITIONS			'C31			'LC31			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{OH}	High-level output voltage	V_{DD} = MIN, I_{OH} = MAX			2.4	3		2			V
V_{OL}	Low-level output voltage	V_{DD} = MIN, I_{OH} = MAX				0.3	0.6			0.4	V
I_Z	High-impedance current	V_{DD} = MAX			− 20		+ 20	− 20		+ 20	µA
I_I	Input current	V_I = V_{SS} to V_{DD}			− 10		+ 10	− 10		+ 10	µA
I_{IP}	Input current (with internal pullup)	Inputs with internal pullups§			− 600		20	− 600		10	µA
I_{CC}	Supply current¶#	T_A = 25°C, V_{DD} = MAX	f_x = 40 MHz	'C31-40 'LC31-40		160	400		150	300	mA
			f_x = 50 MHz	'C31-50		200	425				
			f_x = 60 MHz	'C31-60		225	475				
I_{DD}	Supply current	Standby, IDLE2 Clocks shut off				50			20		µA
C_i	Input capacitance	All inputs except CLKIN					15*			15*	pF
		CLKIN					25			25	
C_o	Output capacitance						20*			20*	pF

† All input and output voltage levels are TTL compatible.
‡ For 'C31, all typical values are at V_{DD} = 5 V, T_A = 25°C. For 'LC31, all typical values are at V_{DD} = 3.3 V, T_A = 25°C.
§ Pins with internal pullup devices: $\overline{INT3}$−$\overline{INT0}$, MCBL/$\overline{MP}$.
¶ Actual operating current is less than this maximum value. This value was obtained under specially produced worst-case test conditions, which are not sustained during normal device operation. These conditions consist of continuous parallel writes of a checkerboard pattern to both primary and expansion buses at the maximum rate possible. See *Calculation of TMS320C30 Power Dissipation Application Report* (literature number SPRA020).
# f_x is the input clock frequency.
* This parameter is not production tested.

NOTE 3: All voltage values are with respect to V_{SS}. All input and output voltage levels are TTL-compatible. CLKIN can be driven by a CMOS clock.

PARAMETER MEASUREMENT INFORMATION



Where: I_{OL} = 2 mA (all outputs)
I_{OH} = 300 µA (all outputs)
V_{LOAD} = Selected to emulate 50-Ω termination (typical value = 1.54 V).
C_T = 80-pF typical load-circuit capacitance

Figure 4. SMJ320C31 Test Load Circuit

signal transition levels for ’C31 (see Figure 5 and Figure 6)

TTL-level outputs are driven to a minimum logic-high level of 2.4 V and to a maximum logic-low level of 0.6 V. Output transition times are specified as follows:

- For a high-to-low transition on a TTL-compatible output signal, the level at which the output is said to be no longer high is 2 V and the level at which the output is said to be low is 1 V.
- For a low-to-high transition, the level at which the output is said to be no longer low is 1 V and the level at which the output is said to be high is 2 V.

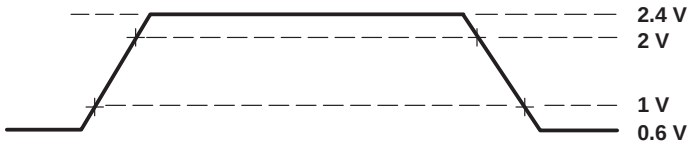


Figure 5. TTL-Level Outputs

Transition times for TTL-compatible inputs are specified as follows:

- For a high-to-low transition on an input signal, the level at which the input is said to be no longer high is 2.1 V and the level at which the input is said to be low is 0.8 V.
- For a low-to-high transition on an input signal, the level at which the input is said to be no longer low is 0.8 V and the level at which the input is said to be high is 2.1 V.

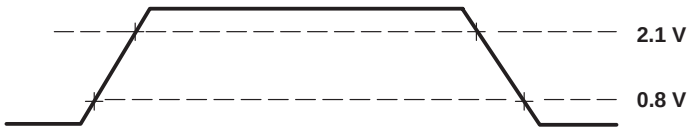
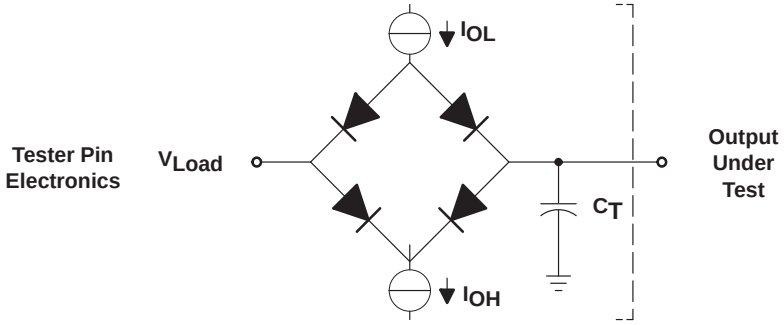


Figure 6. TTL-Level Inputs

PARAMETER MEASUREMENT INFORMATION



Where: I_{OL} = 2 mA (all outputs)
I_{OH} = 300 µA (all outputs)
V_{LOAD} = 2.15 V
C_T = 80-pF typical load-circuit capacitance

Figure 7. SMJ320LC31 Test Load Circuit

signal transition levels for ’LC31 (see Figure 8 and Figure 9)

Outputs are driven to a minimum logic-high level of 2 V and to a maximum logic-low level of 0.4 V. Output transition times are specified as follows:

- For a high-to-low transition on an output signal, the level at which the output is said to be no longer high is 2 V and the level at which the output is said to be low is 1 V.
- For a low-to-high transition, the level at which the output is said to be no longer low is 1 V and the level at which the output is said to be high is 2 V.

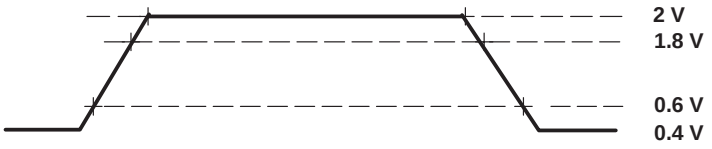


Figure 8. ’LC31 Output Levels

Transition times for inputs are specified as follows:

- For a high-to-low transition on an input signal, the level at which the input is said to be no longer high is 1.8 V and the level at which the input is said to be low is 0.6 V.
- For a low-to-high transition on an input signal, the level at which the input is said to be no longer low is 0.6 V and the level at which the input is said to be high is 1.8 V.

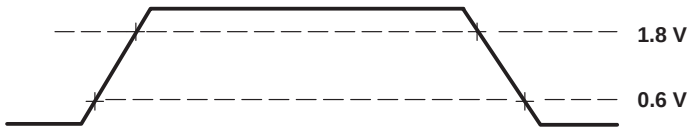


Figure 9. ’LC31 Input Levels

Not Recommended for New Designs

PARAMETER MEASUREMENT INFORMATION

timing parameter symbology

Timing parameter symbols used herein were created in accordance with JEDEC Standard 100-A. In order to shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows, unless otherwise noted:

A	A23−A0	H	H1 and H3
ASYNCH	Asynchronous reset signals	HOLD	$\overline{\text{HOLD}}$
C	CLKX0	HOLDA	$\overline{\text{HOLDA}}$
CI	CLKIN	IACK	$\overline{\text{IACK}}$
CLKR	CLKR0	INT	$\overline{\text{INT3}}$−$\overline{\text{INT0}}$
CONTROL	Control signals	RDY	$\overline{\text{RDY}}$
D	D31−D0	RW	R/$\overline{\text{W}}$
DR	DR	RESET	$\overline{\text{RESET}}$
DX	DX	S	$\overline{\text{STRB}}$
FS	FSX/R	SCK	CLKX/R
FSX	FSX0	SHZ	$\overline{\text{SHZ}}$
FSR	FSR0	TCLK	TCLK0, TCLK1, or TCLKx
GPI	General-purpose input	XF	XF0, XF1, or XFx
GPIO	General-purpose input/output; peripheral pin	XFIO	XFx switching from input to output
GPO	General-purpose output		

Not Recommended for New Designs

timing

Timing specifications apply to the SMJ320C31 and SMJ320LC31.

X2/CLKIN, H1, and H3 timing

The following table defines the timing parameters for the X2/CLKIN, H1, and H3 interface signals.

timing parameters for X2/CLKIN, H1, H3 (see Figure 10, Figure 11, Figure 12, and Figure 13)

NO.			’C31-40 ’LC31-40		’C31-50		’C31-60		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
1	$t_{f(CI)}$	Fall time, CLKIN		5*		5*		4*	ns
2	$t_{w(CIL)}$	Pulse duration, CLKIN low $t_{c(CI)}$ = min	9		7		6		ns
3	$t_{w(CIH)}$	Pulse duration, CLKIN high $t_{c(CI)}$ = min	9		7		6		ns
4	$t_{r(CI)}$	Rise time, CLKIN		5*		5*		4*	ns
5	$t_{c(CI)}$	Cycle time, CLKIN	25	303	20	303	16.67	303	ns
6	$t_{f(H)}$	Fall time, H1 and H3		3		3		3	ns
7	$t_{w(HL)}$	Pulse duration, H1 and H3 low	P−5†		P−5†		P−4†		ns
8	$t_{w(HH)}$	Pulse duration, H1 and H3 high	P−6†		P−6†		P−5†		ns
9	$t_{r(H)}$	Rise time, H1 and H3		3		3		3	ns
10	$t_{d(HL-HH)}$	Delay time. from H1 low to H3 high or from H3 low to H1 high	0	4	0	4	0	4	ns
11	$t_{c(H)}$	Cycle time, H1 and H3	50	606	40	606	33.3	606	ns

† $P = t_{c(CI)}$
* This parameter is not production tested.

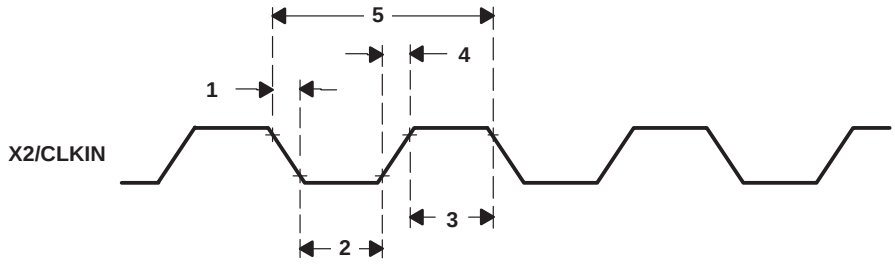


Figure 10. Timing for X2/CLKIN

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X2/CLKIN, H1, and H3 timing (continued)

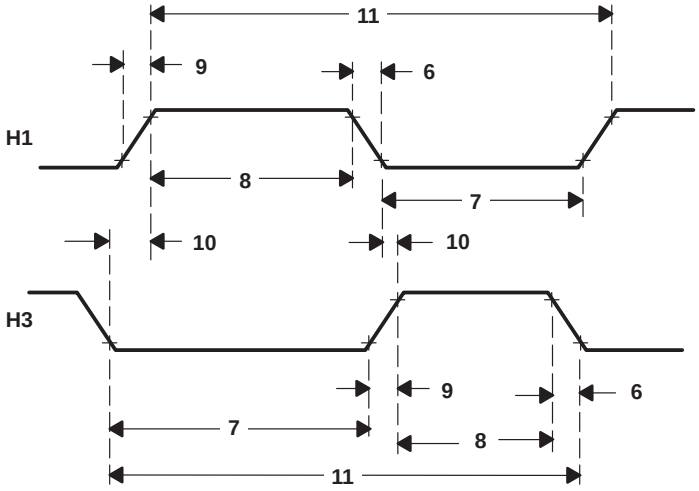


Figure 11. Timing for H1 and H3

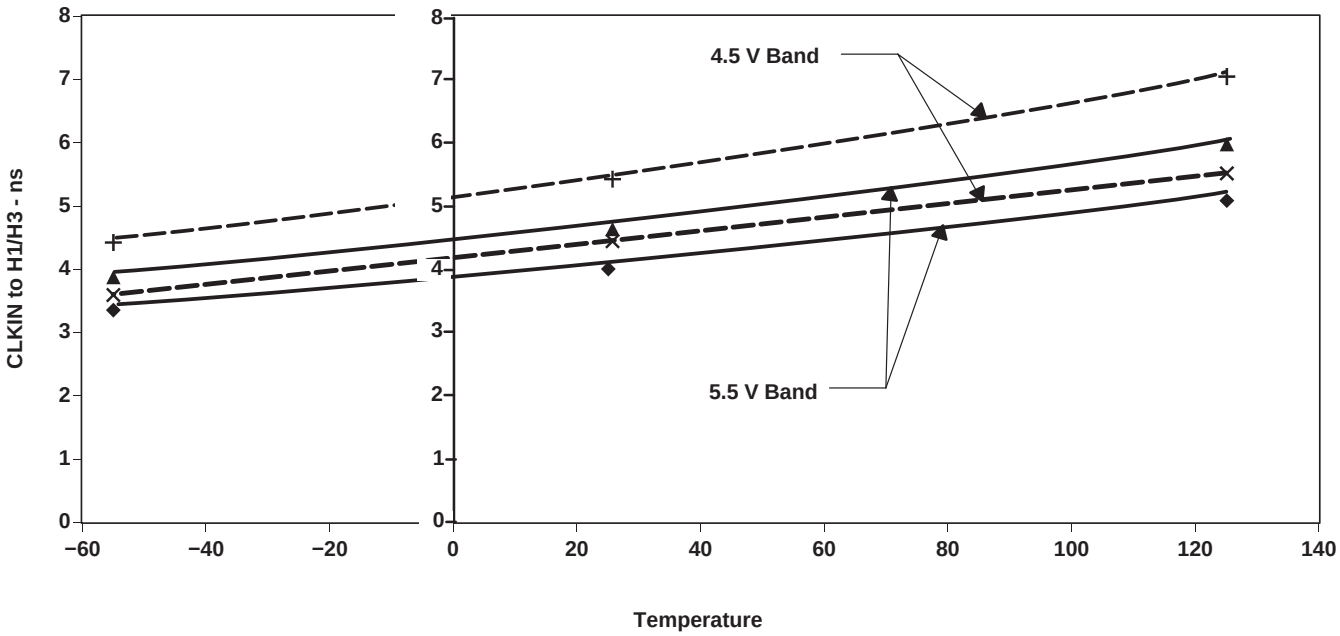


Figure 12. SMJ320C31 CLKIN to H1/H3 as a Function of Temperature (Typical)

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X2/CLKIN, H1, and H3 timing (continued)

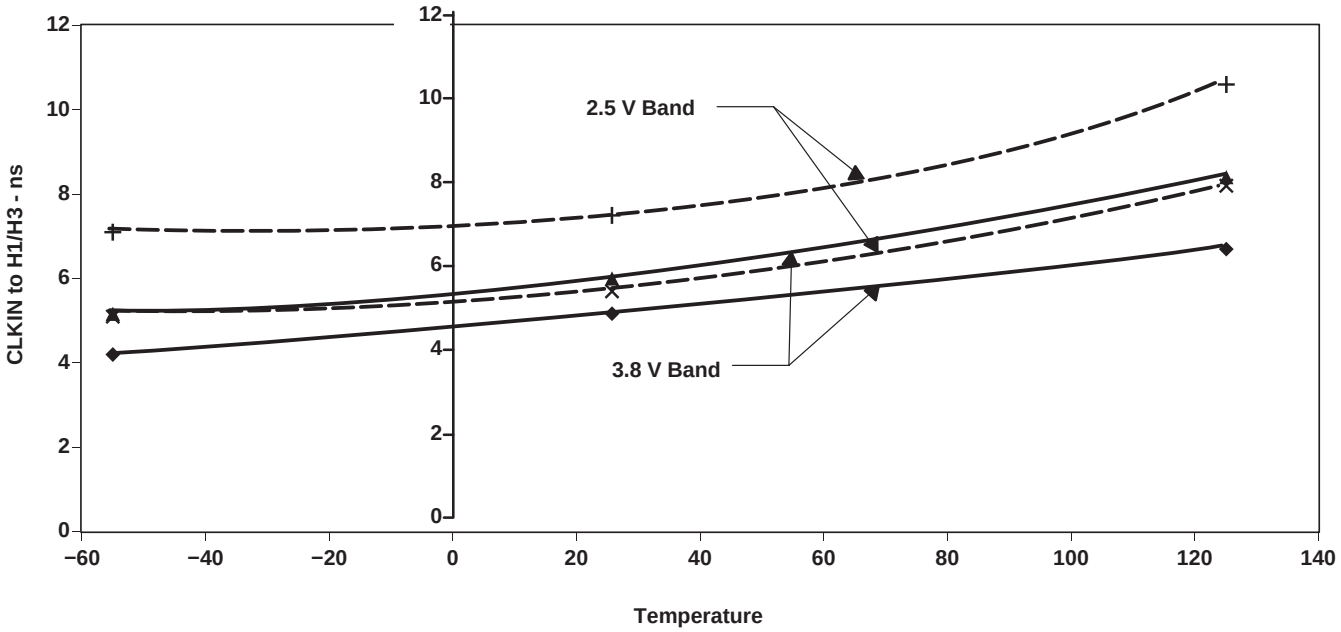


Figure 13. SMJ320LC31 CLKIN to H1/H3 as a Function of Temperature (Typical)

Not Recommended for New Designs

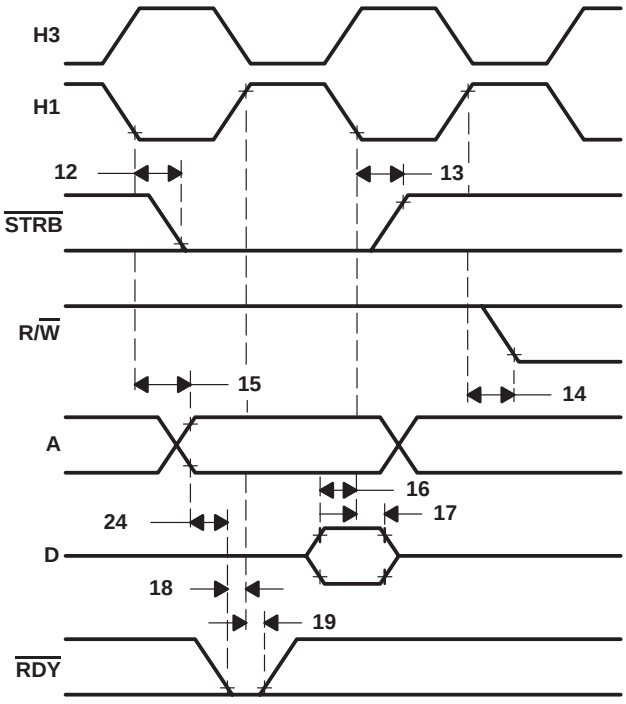
memory read/write timing

The following table defines memory read/write timing parameters for $\overline{\text{STRB}}$.

timing parameters for memory ($\overline{\text{STRB}}$ = 0) read/write (see Figure 14 and Figure 15)†

NO.			'C31-40 'LC31-40		'C31-50		'C31-60		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
12	$t_{d(H1L-SL)}$	Delay time, H1 low to $\overline{\text{STRB}}$ low	0*	6	0*	5	0*	5	ns
13	$t_{d(H1L-SH)}$	Delay time, H1 low to $\overline{\text{STRB}}$ high	0*	6	0*	5	0*	5	ns
14	$t_{d(H1H-RWL)R}$	Delay time, H1 high to R/$\overline{\text{W}}$ low (read)	0*	9	0*	7	0*	6	ns
15	$t_{d(H1L-A)}$	Delay time, H1 low to A valid	0*	10	0*	10	0*	8	ns
16	$t_{su(D-H1L)R}$	Setup time, D before H1 low (read)	14		10		9		ns
17	$t_{h(H1L-D)R}$	Hold time, D after H1 low (read)	0		0		0		ns
18	$t_{su(RDY-H1H)}$	Setup time, $\overline{\text{RDY}}$ before H1 high	8		6		5		ns
19	$t_{h(H1H-RDY)}$	Hold time, $\overline{\text{RDY}}$ after H1 high	0		0		0		ns
20	$t_{d(H1H-RWH)W}$	Delay time, H1 high to R/$\overline{\text{W}}$ high (write)		9		7		6	ns
21	$t_{v(H1L-D)W}$	Valid time, D after H1 low (write)		17		14		12	ns
22	$t_{h(H1H-D)W}$	Hold time, D after H1 high (write)	0		0		0		ns
23	$t_{d(H1H-A)W}$	Delay time, H1 high to A valid on back-to-back write cycles (write)		15		14		10	ns
24	$t_{d(A-RDY)}$	Delay time, $\overline{\text{RDY}}$ from A valid		7*		6*		6*	ns

† See Figure 16 for address bus timing variation with load capacitance greater than typical load-circuit capacitance (C_T = 80 pF).
* This parameter is not production tested.



NOTE A: $\overline{\text{STRB}}$ remains low during back-to-back read operations.

Figure 14. Timing for Memory ($\overline{\text{STRB}}$ = 0) Read

memory read/write timing (continued)

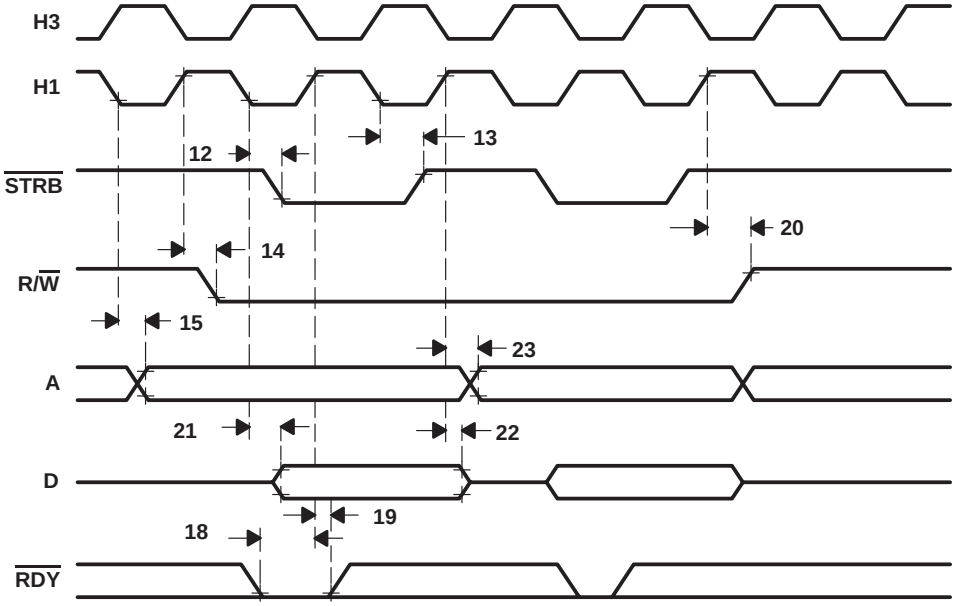
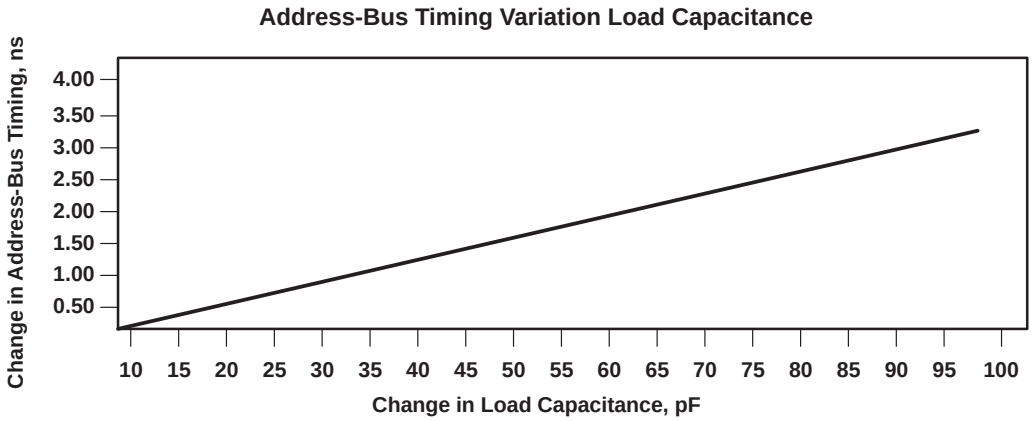


Figure 15. Timing for Memory ($\overline{\text{STRB}}$ = 0) Write



NOTE A: 30 pF/ns slope

Figure 16. Address-Bus Timing Variation With Load Capacitance (see Note A)

Not Recommended for New Designs

XF0 and XF1 timing when executing LDFI or LDII

The following table defines the timing parameters for XF0 and XF1 during execution of LDFI or LDII.

timing for XF0 and XF1 when executing LDFI or LDII for SMJ320C31 (see Figure 17)

NO.			’C31-40		’LC31-40		’C31-50		’C31-60		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
25	$t_{d(H3H-XF0L)}$	Delay time, H3 high to XF0 low		13		13		12		11	ns
26	$t_{su(XF1-H1L)}$	Setup time, XF1 before H1 low	9		10		8		8		ns
27	$t_{h(H1L-XF1)}$	Hold time, XF1 after H1 low	0		0		0		0		ns

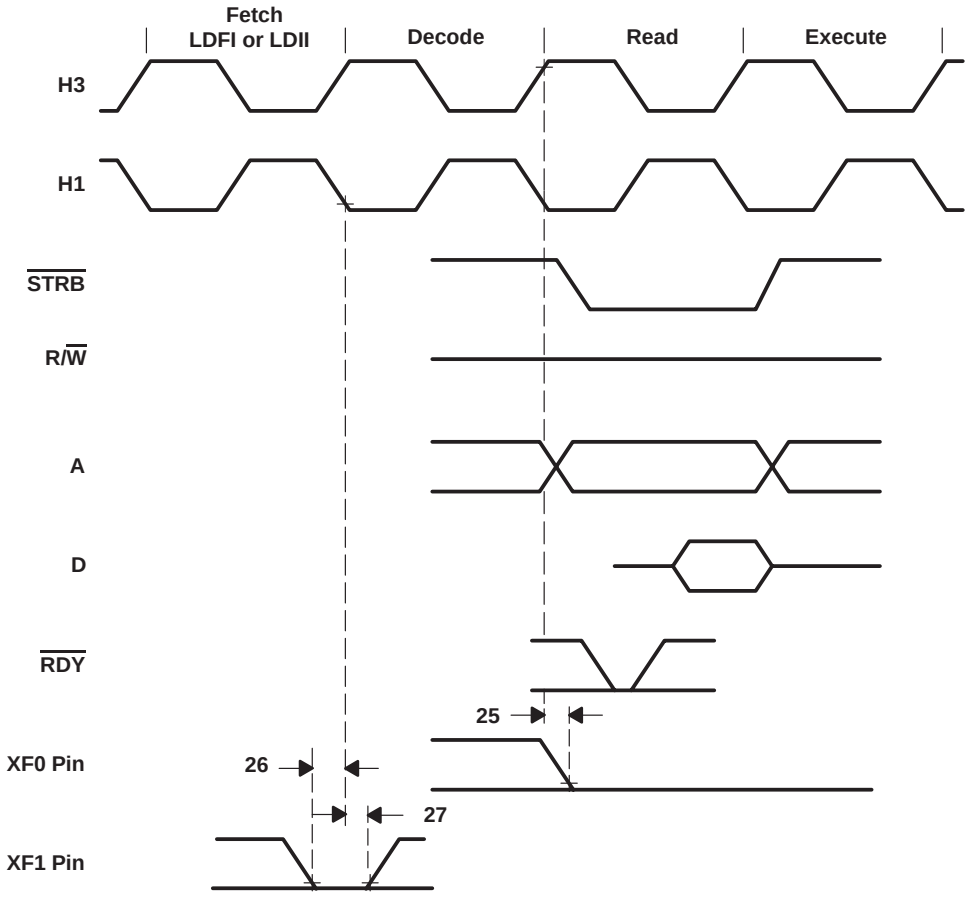


Figure 17. Timing for XF0 and XF1 When Executing LDFI or LDII

Not Recommended for New Designs

XF0 timing when executing STFI and STII†

The following table defines the timing parameters for the XF0 pin during execution of STFI or STII.

timing for XF0 when executing STFI or STII (see Figure 18)

NO.		’C31-40 ’LC31-40		’C31-50		’C31-60		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
28	$t_{d(H3H-XF0H)}$ Delay time, H3 high to XF0 high		13		12		11	ns

† XF0 is always set high at the beginning of the execute phase of the interlock-store instruction. When no pipeline conflicts occur, the address of the store is also driven at the beginning of the execute phase of the interlock-store instruction. However, if a pipeline conflict prevents the store from executing, the address of the store will not be driven until the store can execute.

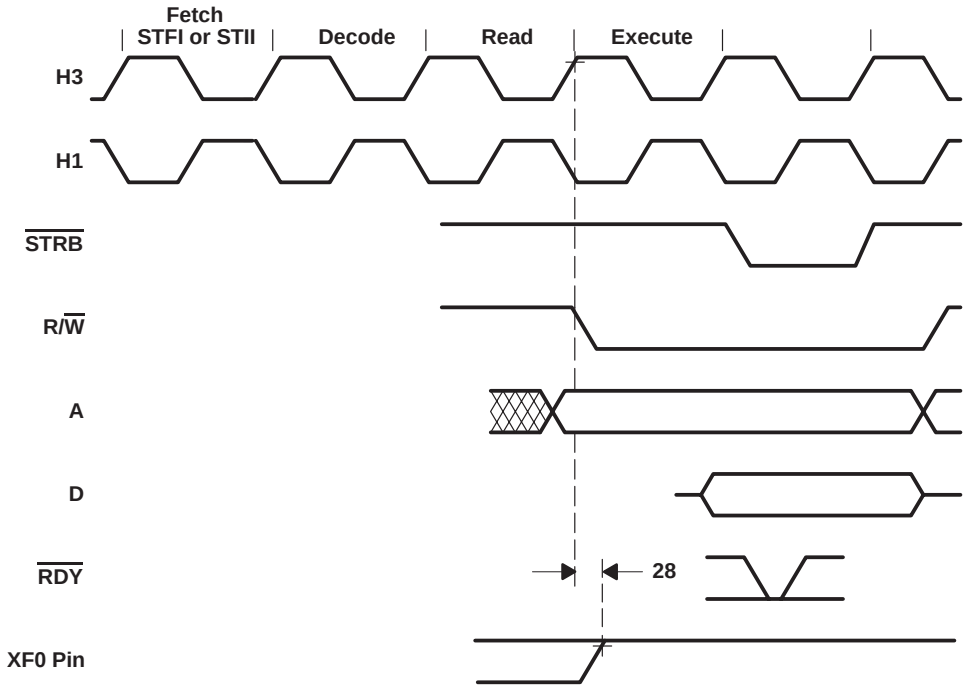


Figure 18. Timing for XF0 When Executing an STFI or STII

Not Recommended for New Designs

XF0 and XF1 timing when executing SIGI

The following table defines the timing parameters for the XF0 and XF1 pins during execution of SIGI.

timing for XF0 and XF1 when executing SIGI for SMJ320C31 (see Figure 19)

NO.			’C31-40		’LC31-40		’C31-50		’C31-60		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
29	$t_{d(H3H-XF0L)}$	Delay time, H3 high to XF0 low		13		13		12		11	ns
30	$t_{d(H3H-XF0H)}$	Delay time, H3 high to XF0 high		13		13		12		11	ns
31	$t_{su(XF1-H1L)}$	Setup time, XF1 before H1 low	9		10		8		8		ns
32	$t_{h(H1L-XF1)}$	Hold time, XF1 after H1 low	0		0		0		0		ns

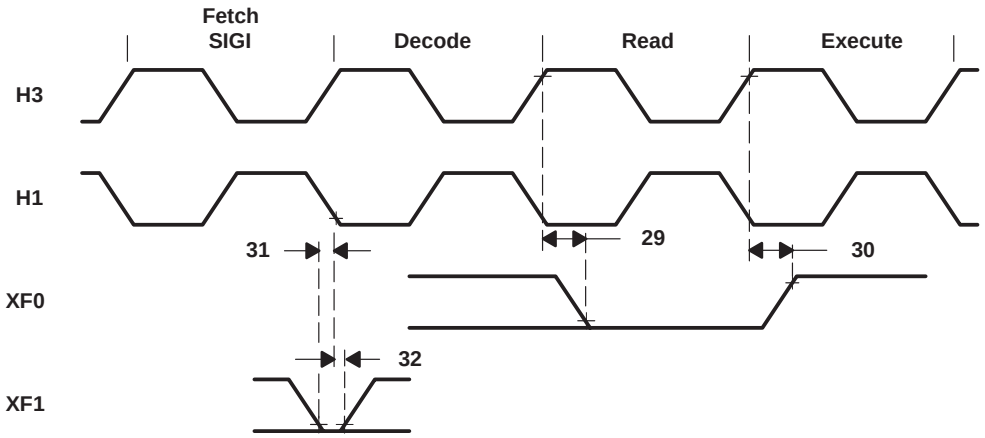


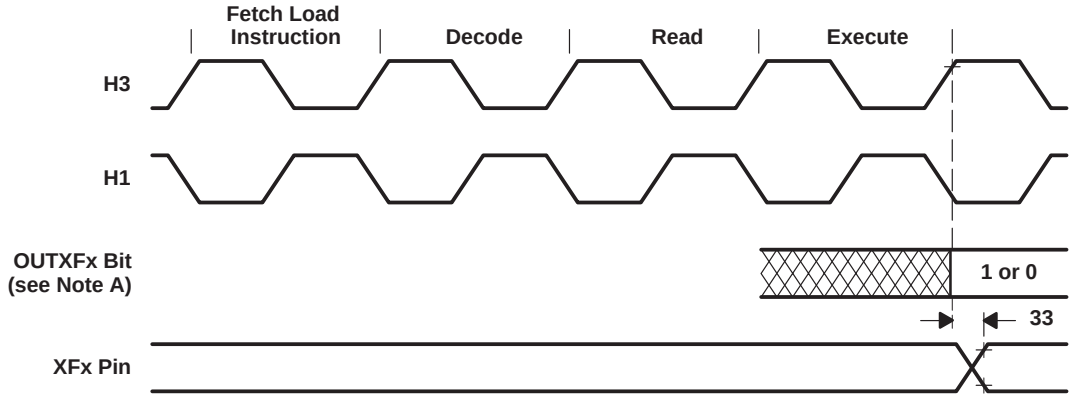
Figure 19. Timing for XF0 and XF1 When Executing SIGI

loading when XF is configured as an output

The following table defines the timing parameter for loading the XF register when the XFx pin is configured as an output.

timing for loading the XF register when configured as an output pin (see Figure 20)

NO.			’C31-40 ’LC31-40		’C31-50		’C31-60		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
33	$t_{v(H3H-XF)}$	Valid time, H3 high to XFx		13		12		11	ns



NOTE A: OUTXFx represents either bit 2 or 6 of the IOF register.

Figure 20. Timing for Loading XF Register When Configured as an Output Pin

Not Recommended for New Designs

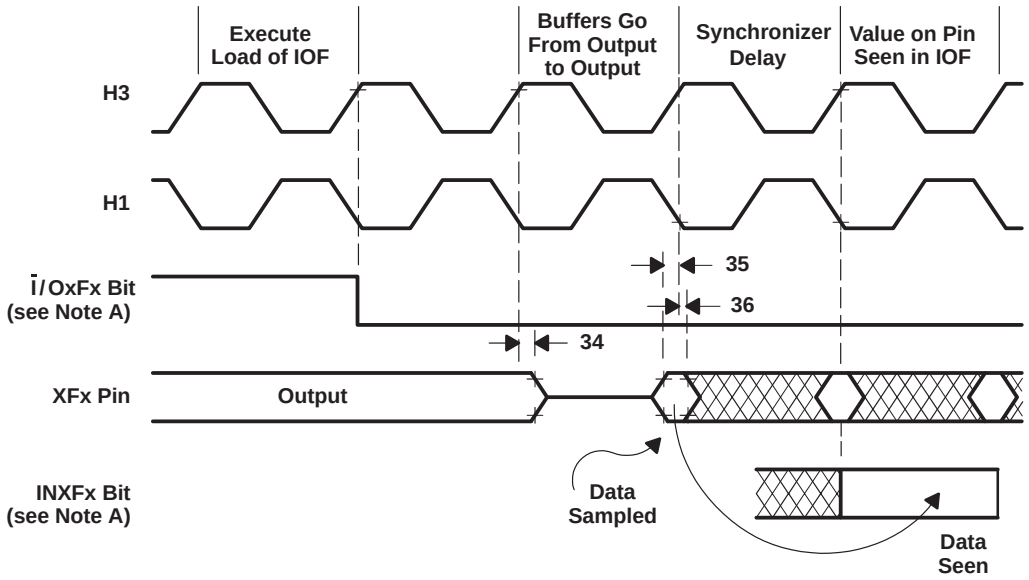
changing XFx from an output to an input

The following table defines the timing parameters for changing the XFx pin from an output pin to an input pin.

timing of XFx changing from output to input mode for SMJ320C31 (see Figure 21)

NO.			’C31-40		’LC31-40		’C31-50		’C31-60		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
34	$t_{h(H3H-XF)}$	Hold time, XFx after H3 high		13*		13*		12*		11*	ns
35	$t_{su(XF-H1L)}$	Setup time, XFx before H1 low	9		10		8		8		ns
36	$t_{h(H1L-XF)}$	Hold time, XFx after H1 low	0		0		0		0		ns

* This parameter is not production tested.



NOTE A: I/OxFx represents either bit 1 or bit 5 of the IOF register, and INXFx represents either bit 3 or bit 7 of the IOF register.

Figure 21. Timing for Change of XFx From Output to Input Mode

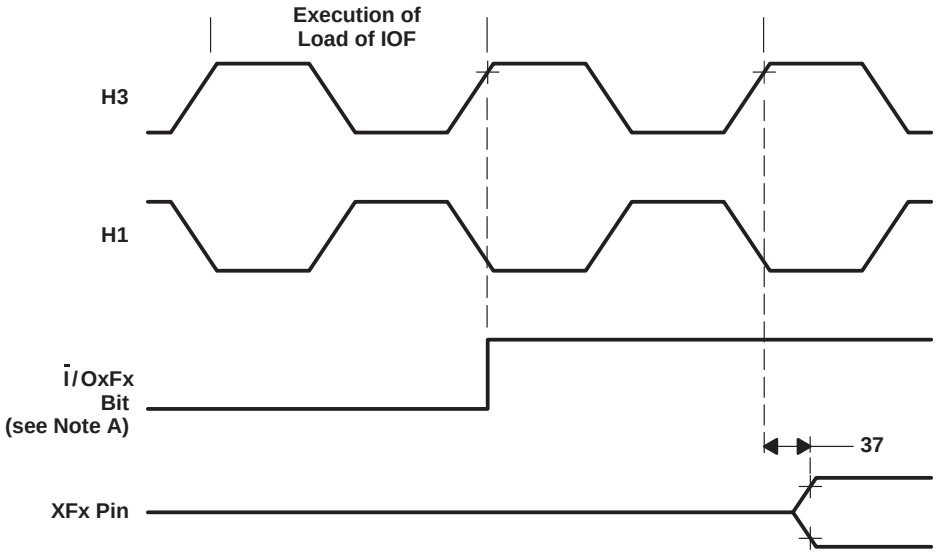
Not Recommended for New Designs

changing XFx from an input to an output

The following table defines the timing parameter for changing the XFx pin from an input pin to an output pin.

timing for XFx changing from input to output mode (see Figure 22)

NO.			’C31-40 ’LC31-40		’C31-50		’C31-60		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
37	$t_{d(H3H-XFIO)}$	Delay time, H3 high to XFx switching from input to output		17		17		16	ns



NOTE A: I/OxFx represents either bit 1 or bit 5 of the IOF register.

Figure 22. Timing for Change of XFx From Input to Output Mode

reset timing

RESET is an asynchronous input that can be asserted at any time during a clock cycle. If the specified timings are met, the exact sequence shown in Figure 23 occurs; otherwise, an additional delay of one clock cycle is possible.

The asynchronous reset signals include XF0/1, CLKX0, DX0, FSX0, CLKR0, DR0, FSR0, and TCLK0/1.

Resetting the device initializes the primary- and expansion-bus control registers to seven software wait states and therefore results in slow external accesses until these registers are initialized.

HOLD is an asynchronous input and can be asserted during reset.

Not Recommended for New Designs

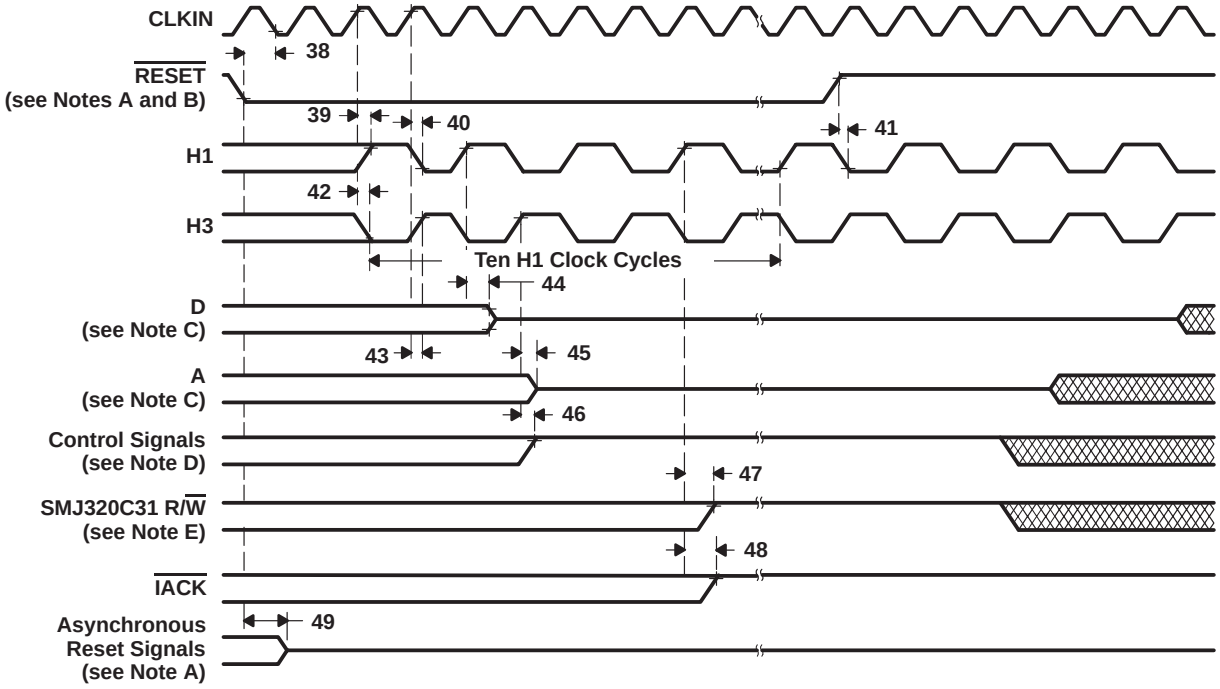
$\overline{\text{RESET}}$ timing (see Figure 23)

NO.			’C31-40		’LC31-40		’C31-50		’C31-60		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
38	$t_{su(RESET-CIL)}$	Setup time, $\overline{\text{RESET}}$ before CLKIN low	10	P†*	10	P†*	10	P†*	7	P†*	ns
39	$t_{d(CLKINH-H1H)}$	Delay time, CLKIN high to H1 high (see Note 4)	2	14	2	14	2	10	2	10	ns
40	$t_{d(CLKINH-H1L)}$	Delay time, CLKIN high to H1 low (see Note 4)	2	14	2	14	2	10	2	10	ns
41	$t_{su(RESETH-H1L)}$	Setup time, $\overline{\text{RESET}}$ high before H1 low and after ten H1 clock cycles	9		9		7		6		ns
42	$t_{d(CLKINH-H3L)}$	Delay time, CLKIN high to H3 low (see Note 4)	2	14	2	14	2	10	2	10	ns
43	$t_{d(CLKINH-H3H)}$	Delay time, CLKIN high to H3 high (see Note 4)	2	14	2	14	2	10	2	10	ns
44	$t_{dis(H1H-DZ)}$	Disable time, H1 high to D (high impedance)		15*		13*		12*		11*	ns
45	$t_{dis(H3H-AZ)}$	Disable time, H3 high to A (high impedance)		9*		9*		8*		7*	ns
46	$t_{d(H3H-CONTROLH)}$	Delay time, H3 high to control signals high		9*		9*		8*		7*	ns
47	$t_{d(H1H-RWH)}$	Delay time, H1 high to R/$\overline{\text{W}}$ high		9*		9*		8*		7*	ns
48	$t_{d(H1H-IACKH)}$	Delay time, H1 high to $\overline{\text{IACK}}$ high		9*		9*		8*		7*	ns
49	$t_{dis(RESETL-ASYNCH)}$	Disable time, $\overline{\text{RESET}}$ low to asynchronous reset signals disabled (high impedance)		21*		21*		17*		14*	ns

† $P = t_{c(CI)}$
* This parameter is not production tested.
NOTE 4: See Figure 12 and Figure 13 for typical temperature dependence.

Not Recommended for New Designs

$\overline{\text{RESET}}$ timing (continued)



NOTES: A. Asynchronous reset signals include XF0/1, CLKX0, DX0, FSX0, CLKR0, DR0, FSR0, and TCLK0/1.
B. $\overline{\text{RESET}}$ is an asynchronous input and can be asserted at any point during a clock cycle. If the specified timings are met, the exact sequence shown occurs; otherwise, an additional delay of one clock cycle is possible.
C. In microprocessor mode, the reset vector is fetched twice, with seven software wait states each time. In microcomputer mode, the reset vector is fetched twice, with no software wait states.
D. Control signals include $\overline{\text{STRB}}$.
E. The R/$\overline{\text{W}}$ outputs are placed in a high-impedance state during reset and can be provided with a resistive pullup, nominally 18−22 kΩ, if undesirable spurious writes are caused when these outputs go low.

Figure 23. Timing for $\overline{\text{RESET}}$

Not Recommended for New Designs

interrupt response timing

The following table defines the timing parameters for the $\overline{\text{INT}}$ signals.

timing for $\overline{\text{INT3}}$–$\overline{\text{INT0}}$ response (see Figure 24)

NO.			’C31-40		’LC31-40		’C31-50		’C31-60		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
50	$t_{su(INT-H1L)}$	Setup time, $\overline{\text{INT3}}$–$\overline{\text{INT0}}$ before H1 low	13		15		11		8		ns
51	$t_{w(INT)}$	Pulse duration, interrupt to ensure only one interrupt	P	2P†*	P	2P†*	P	2P†*	P	2P†*	ns

† P = $t_{c(H)}$
* This parameter is not production tested.

The interrupt ($\overline{\text{INT}}$) pins are asynchronous inputs that can be asserted at any time during a clock cycle. The SMJ320C3x interrupts are level-sensitive, not edge-sensitive. Interrupts are detected on the falling edge of H1. Therefore, interrupts must be set up and held to the falling edge of H1 for proper detection. The CPU and DMA respond to detected interrupts on instruction-fetch boundaries only.

For the processor to recognize only one interrupt on a given input, an interrupt pulse must be set up and held to:

- A minimum of one H1 falling edge
- No more than two H1 falling edges

The SMJ320C3x can accept an interrupt from the same source every two H1 clock cycles.

If the specified timings are met, the exact sequence shown in Figure 24 occurs; otherwise, an additional delay of one clock cycle is possible.

Not Recommended for New Designs

timing parameters for $\overline{\text{INT3}}$−$\overline{\text{INT0}}$ response (continued)

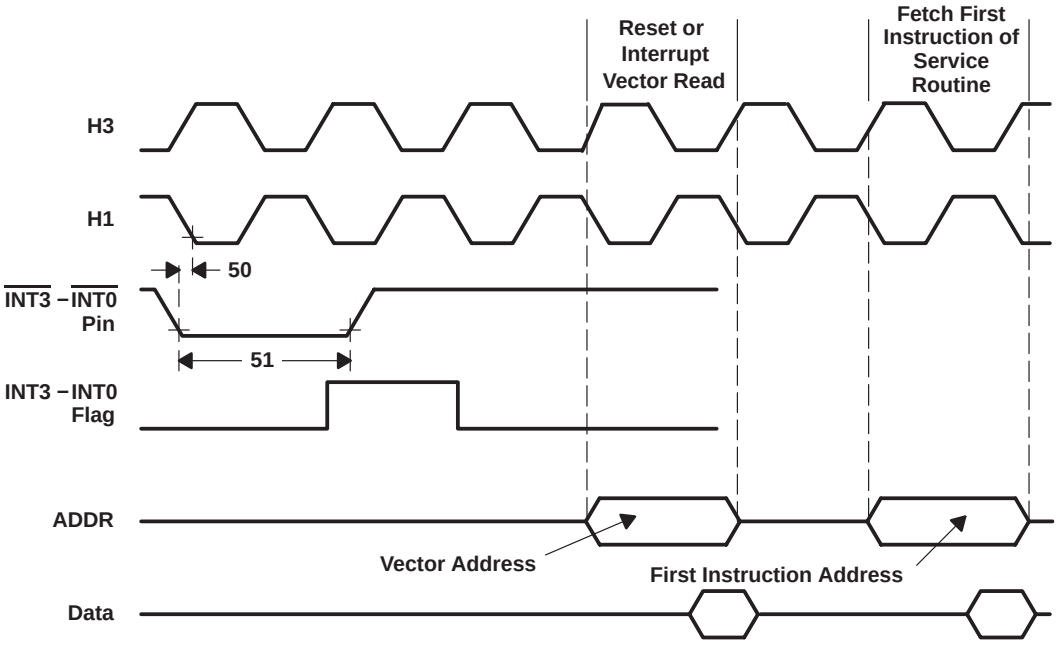


Figure 24. Timing for $\overline{\text{INT3}}$−$\overline{\text{INT0}}$ Response

Not Recommended for New Designs

interrupt-acknowledge timing

The $\overline{\text{IACK}}$ output goes active on the first half-cycle (HI rising) of the decode phase of the IACK instruction and goes inactive at the first half-cycle (HI rising) of the read phase of the IACK instruction.

timing for $\overline{\text{IACK}}$ (see Note 5 and Figure 25)

NO.			’C31-40 ’LC31-40		’C31-50		’C31-60		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
52	$t_{d(H1H-IACKL)}$	Delay time, H1 high to $\overline{\text{IACK}}$ low		9		7		6	ns
53	$t_{d(H1H-IACKH)}$	Delay time, H1 high to $\overline{\text{IACK}}$ high		9		7		6	ns

NOTE 5: $\overline{\text{IACK}}$ goes active on the first half-cycle (H1 rising) of the decode phase of the IACK instruction and goes inactive at the first half-cycle (H1 rising) of the read phase of the IACK instruction. Because of pipeline conflicts, $\overline{\text{IACK}}$ remains low for one cycle even if the decode phase of the IACK instruction is extended.

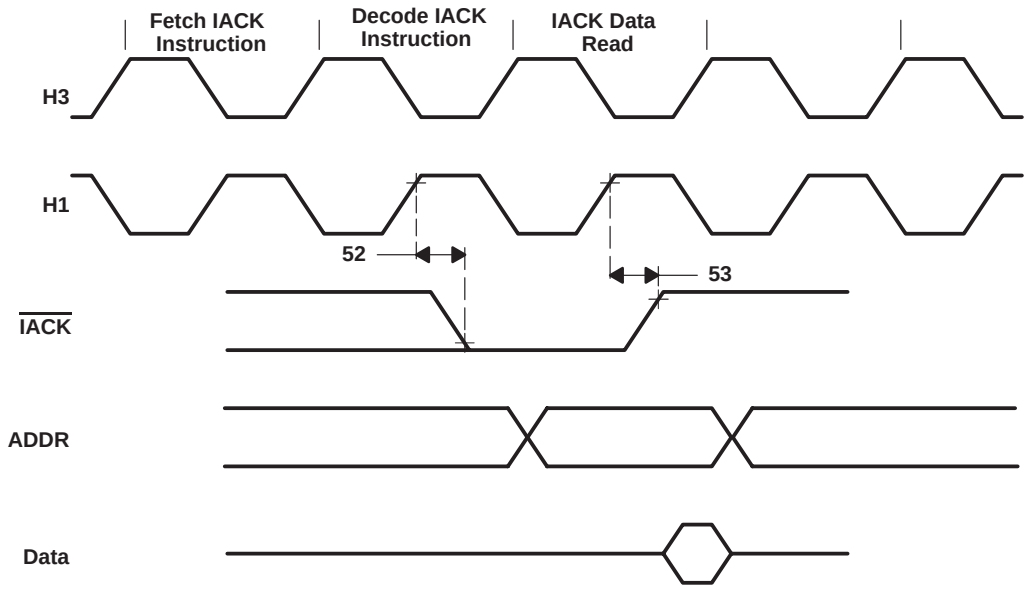


Figure 25. Timing for $\overline{\text{IACK}}$

Not Recommended for New Designs

serial-port timing for SMJ320C31-40 and SMJ320LC31-40 (see Figure 26 and Figure 27)

NO.				’C31-40 ’LC31-40		UNIT
				MIN	MAX	
54	$t_{d(H1H-SCK)}$	Delay time, H1 high to internal CLKX/R			13	ns
55	$t_{c(SCK)}$	Cycle time, CLKX/R	CLKX/R ext	$t_{c(H)}$x2.6		ns
			CLKX/R int	$t_{c(H)}$x2	$t_{c(H)}$x2^{32}	
56	$t_{w(SCK)}$	Pulse duration, CLKX/R high/low	CLKX/R ext	$t_{c(H)}$+10		ns
			CLKX/R int	[$t_{c(SCK)}$/2]−5	[$t_{c(SCK)}$/2]+5	
57	$t_{r(SCK)}$	Rise time, CLKX/R			7	ns
58	$t_{f(SCK)}$	Fall time, CLKX/R			7	ns
59	$t_{d(C-DX)}$	Delay time, CLKX to DX valid	CLKX ext		30	ns
			CLKX int		17	
60	$t_{su(DR-CLKRL)}$	Setup time, DR before CLKR low	CLKR ext	9		ns
			CLKR int	21		
61	$t_{h(CLKRL-DR)}$	Hold time, DR from CLKR low	CLKR ext	9		ns
			CLKR int	0		
62	$t_{d(C-FSX)}$	Delay time, CLKX to internal FSX high/low	CLKX ext		27	ns
			CLKX int		15	
63	$t_{su(FSR-CLKRL)}$	Setup time, FSR before CLKR low	CLKR ext	9		ns
			CLKR int	9		
64	$t_{h(SCKL-FS)}$	Hold time, FSX/R input from CLKX/R low	CLKX/R ext	9		ns
			CLKX/R int	0		
65	$t_{su(FSX-C)}$	Setup time, external FSX before CLKX	CLKX ext	−[$t_{c(H)}$−8]*	[$t_{c(SCK)}$/2]−10*	ns
			CLKX int	[$t_{c(H)}$−21]*	$t_{c(SCK)}$/2*	
66	$t_{d(CH-DX)V}$	Delay time, CLKX to first DX bit, FSX precedes CLKX high	CLKX ext		30*	ns
			CLKX int		18*	
67	$t_{d(FSX-DX)V}$	Delay time, FSX to first DX bit, CLKX precedes FSX			30*	ns
68	$t_{d(CH-DXZ)}$	Delay time, CLKX high to DX high impedance following last data bit			17*	ns

* This parameter is not production tested.

Not Recommended for New Designs

serial-port timing for SMJ320C31-50 (see Figure 26 and Figure 27)

NO.				'31-50 MIN	'31-50 MAX	UNIT
54	$t_{d(H1H-SCK)}$	Delay time, H1 high to internal CLKX/R			10	ns
55	$t_{c(SCK)}$	Cycle time, CLKX/R	CLKX/R ext	$t_{c(H)}$x2.6		ns
			CLKX/R int	$t_{c(H)}$x2	$t_{c(H)}$x2^{32}	
56	$t_{w(SCK)}$	Pulse duration, CLKX/R high/low	CLKX/R ext	$t_{c(H)}$+10		ns
			CLKX/R int	$[t_{c(SCK)}/2]-5$	$[t_{c(SCK)}/2]+5$	
57	$t_{r(SCK)}$	Rise time, CLKX/R			6	ns
58	$t_{f(SCK)}$	Fall time, CLKX/R			6	ns
59	$t_{d(C-DX)}$	Delay time, CLKX to DX valid	CLKX ext		24	ns
			CLKX int		16	
60	$t_{su(DR-CLKRL)}$	Setup time, DR before CLKR low	CLKR ext	9		ns
			CLKR int	17		
61	$t_{h(CLKRL-DR)}$	Hold time, DR from CLKR low	CLKR ext	7		ns
			CLKR int	0		
62	$t_{d(C-FSX)}$	Delay time, CLKX to internal FSX high/low	CLKX ext		22	ns
			CLKX int		15	
63	$t_{su(FSR-CLKRL)}$	Setup time, FSR before CLKR low	CLKR ext	7		ns
			CLKR int	7		
64	$t_{h(SCKL-FS)}$	Hold time, FSX/R input from CLKX/R low	CLKX/R ext	7		ns
			CLKX/R int	0		
65	$t_{su(FSX-C)}$	Setup time, external FSX before CLKX	CLKX ext	$-[t_{c(H)}-8]$*	$[t_{c(SCK)}/2]-10$*	ns
			CLKX int	$-[t_{c(H)}-21]$*	$t_{c(SCK)}/2$*	
66	$t_{d(CH-DX)V}$	Delay time, CLKX to first DX bit, FSX precedes CLKX high	CLKX ext		24*	ns
			CLKX int		14*	
67	$t_{d(FSX-DX)V}$	Delay time, FSX to first DX bit, CLKX precedes FSX			24*	ns
68	$t_{d(CH-DXZ)}$	Delay time, CLKX high to DX high impedance following last data bit			14*	ns

* This parameter is not production tested.

Not Recommended for New Designs

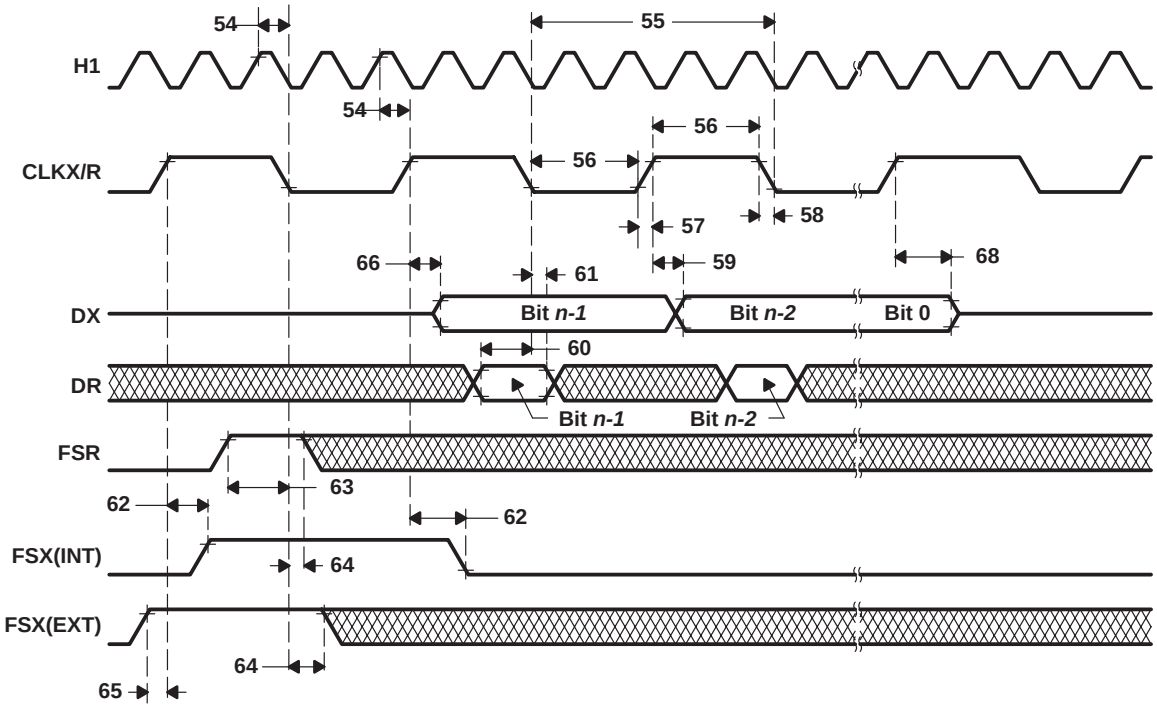
serial-port timing for SMJ320C31-60 (see Figure 26 and Figure 27)

NO.				’C31-60 MIN	’C31-60 MAX	UNIT
54	$t_{d(H1H-SCK)}$	Delay time, H1 high to internal CLKX/R			8	ns
55	$t_{c(SCK)}$	Cycle time, CLKX/R	CLKX/R ext	$t_{c(H)}$x2.6		ns
			CLKX/R int	$t_{c(H)}$x2	$t_{c(H)}$x2^{32}	
56	$t_{w(SCK)}$	Pulse duration, CLKX/R high/low	CLKX/R ext	$t_{c(H)}$+10		ns
			CLKX/R int	[$t_{c(SCK)}$/2]−5	[$t_{c(SCK)}$/2]+5	
57	$t_{r(SCK)}$	Rise time, CLKX/R			5	ns
58	$t_{f(SCK)}$	Fall time, CLKX/R			5	ns
59	$t_{d(C-DX)}$	Delay time, CLKX to DX valid	CLKX ext		20	ns
			CLKX int		15	
60	$t_{su(DR-CLKRL)}$	Setup time, DR before CLKR low	CLKR ext	8		ns
			CLKR int	15		
61	$t_{h(CLKRL-DR)}$	Hold time, DR from CLKR low	CLKR ext	6		ns
			CLKR int	0		
62	$t_{d(C-FSX)}$	Delay time, CLKX to internal FSX high/low	CLKX ext		20	ns
			CLKX int		14	
63	$t_{su(FSR-CLKRL)}$	Setup time, FSR before CLKR low	CLKR ext	6		ns
			CLKR int	6		
64	$t_{h(SCKL-FS)}$	Hold time, FSX/R input from CLKX/R low	CLKX/R ext	6		ns
			CLKX/R int	0		
65	$t_{su(FSX-C)}$	Setup time, external FSX before CLKX	CLKX ext	−[$t_{c(H)}$ − 8]*	[$t_{c(SCK)}$/2] − 10*	ns
			CLKX int	−[$t_{c(H)}$ − 21]*	$t_{c(SCK)}$/2*	
66	$t_{d(CH-DX)V}$	Delay time, CLKX to first DX bit, FSX precedes CLKX high	CLKX ext		20*	ns
			CLKX int		12*	
67	$t_{d(FSX-DX)V}$	Delay time, FSX to first DX bit, CLKX precedes FSX			20*	ns
68	$t_{d(CH-DXZ)}$	Delay time, CLKX high to DX high impedance following last data bit			12*	ns

* This parameter is not production tested.

data-rate timing modes

Unless otherwise indicated, the data-rate timings shown in Figure 26 and Figure 27 are valid for all serial-port modes, including handshake. For a functional description of serial-port operation, see subsection 8.2.12 of the *TMS320C3x User's Guide* (literature number SPRU031).

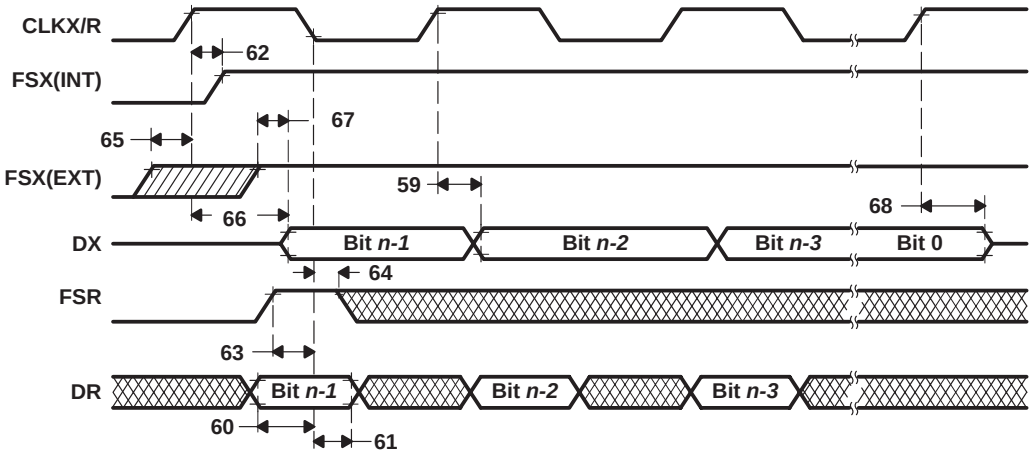


NOTES: A. Timing diagrams show operations with CLKXP = CLKRP = FSXP = FSRP = 0.
B. Timing diagrams depend on the length of the serial-port word, where n = 8, 16, 24, or 32 bits, respectively.

Figure 26. Timing for Fixed Data-Rate Mode

Not Recommended for New Designs

data-rate timing modes (continued)



NOTES: A. Timing diagrams show operation with CLKXP = CLKRP = FSXP = FSRP = 0.
B. Timing diagrams depend on the length of the serial-port word, where n = 8, 16, 24, or 32 bits, respectively.
C. The timings that are not specified expressly for the variable data-rate mode are the same as those that are specified for the fixed data-rate mode.

Figure 27. Timing for Variable Data-Rate Mode

Not Recommended for New Designs

$\overline{\text{HOLD}}$ timing

$\overline{\text{HOLD}}$ is an asynchronous input that can be asserted at any time during a clock cycle. If the specified timings are met, the exact sequence shown in Figure 27 occurs; otherwise, an additional delay of one clock cycle is possible.

The NOHOLD bit of the primary-bus control register overrides the $\overline{\text{HOLD}}$ signal. When this bit is set, the device comes out of hold and prevents future hold cycles.

Asserting $\overline{\text{HOLD}}$ prevents the processor from accessing the primary bus. Program execution continues until a read from or a write to the primary bus is requested. In certain circumstances, the first write is pending, thus allowing the processor to continue until a second write is encountered.

timing for $\overline{\text{HOLD}}$/$\overline{\text{HOLDA}}$ (see Figure 28)

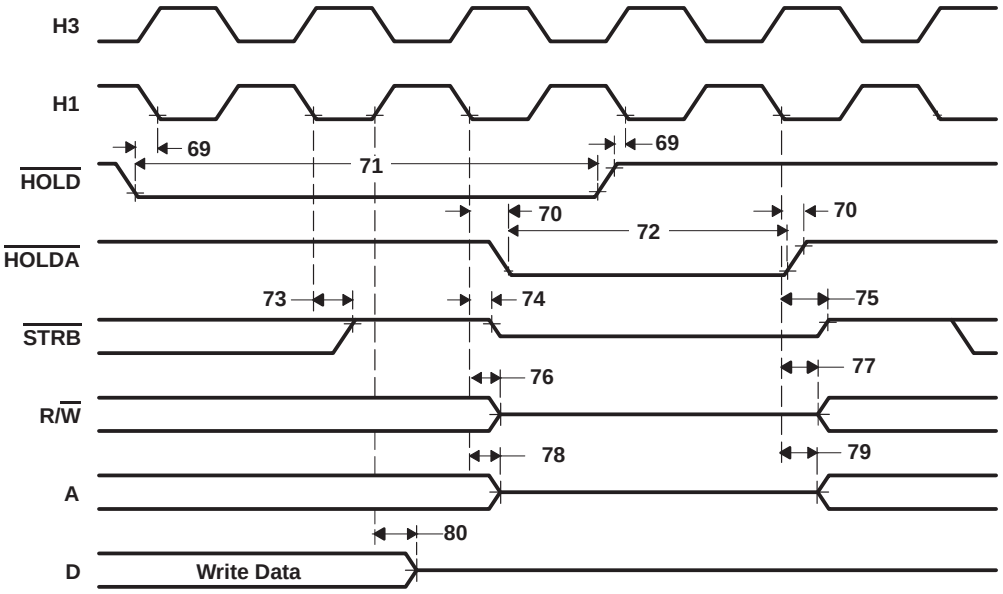
NO.			’C31-40		’LC31-40		’C31-50		’C31-60		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
69	$t_{su(HOLD-H1L)}$	Setup time, $\overline{\text{HOLD}}$ before H1 low	13		13		10		8		ns
70	$t_{v(H1L-HOLDA)}$	Valid time, $\overline{\text{HOLDA}}$ after H1 low	0†	9	0*	9	0*	7	0*	6	ns
71	$t_{w(HOLD)}$†	Pulse duration, $\overline{\text{HOLD}}$ low	$2t_{c(H)}$		$2t_{c(H)}$		$2t_{c(H)}$		$2t_{c(H)}$		ns
72	$t_{w(HOLDA)}$	Pulse duration, $\overline{\text{HOLDA}}$ low	$t_{cH}-5$*		$t_{cH}-5$*		$t_{cH}-5$*		$t_{cH}-5$*		ns
73	$t_{d(H1L-SH)H}$	Delay time, H1 low to $\overline{\text{STRB}}$ high for a $\overline{\text{HOLD}}$	0*	9	0*	9	0*	7	0*	6	ns
74	$t_{dis(H1L-S)}$	Disable time, H1 low to $\overline{\text{STRB}}$ to the high-impedance state	0*	9*	0*	9*	0*	7*	0*	7*	ns
75	$t_{en(H1L-S)}$	Enable time, H1 low to $\overline{\text{STRB}}$ enabled (active)	0*	9	0*	9	0*	7	0*	6	ns
76	$t_{dis(H1L-RW)}$	Disable time, H1 low to R/$\overline{\text{W}}$ to the high-impedance state	0*	9*	0*	9*	0*	8*	0*	7*	ns
77	$t_{en(H1L-RW)}$	Enable time, H1 low to R/$\overline{\text{W}}$ enabled (active)	0*	9	0*	9	0*	7	0*	6	ns
78	$t_{dis(H1L-A)}$	Disable time, H1 low to address to the high-impedance state	0*	9*	0*	10*	0*	8*	0*	7*	ns
79	$t_{en(H1L-A)}$	Enable time, H1 low to address enabled (valid)	0*	13	0*	13	0*	10	0*	11?	ns
80	$t_{dis(H1H-D)}$	Disable time, H1 high to data to the high-impedance state	0*	12*	0*	9*	0*	10*	0*	7*	ns

† $\overline{\text{HOLD}}$ is an asynchronous input and can be asserted at any point during a clock cycle. If the specified timings are met, the exact sequence shown in Figure 28 occurs; otherwise, an additional delay of one clock cycle is possible.

* This parameter is not production tested.

Not Recommended for New Designs

$\overline{\text{HOLD}}$ timing (continued)



NOTE A: $\overline{\text{HOLDA}}$ goes low in response to $\overline{\text{HOLD}}$ going low and continues to remain low until one H1 cycle after $\overline{\text{HOLD}}$ goes back high.

Figure 28. Timing for $\overline{\text{HOLD}}$/$\overline{\text{HOLDA}}$

Not Recommended for New Designs

general-purpose I/O timing

Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1. The contents of the internal control registers associated with each peripheral define the modes for these pins.

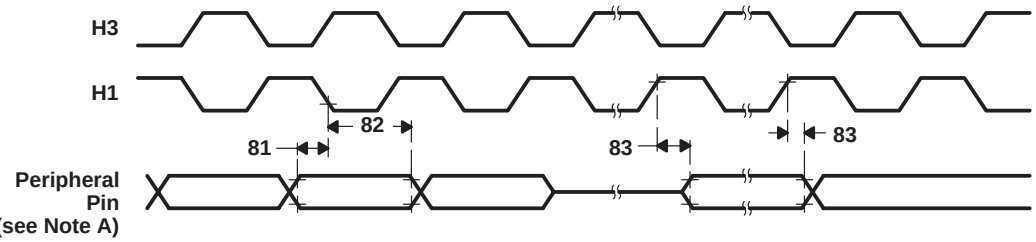
peripheral pin I/O timing

The table, timing parameters for peripheral pin general-purpose I/O, defines peripheral pin general-purpose I/O timing parameters.

timing requirements for peripheral pin general-purpose I/O (see Note 6 and Figure 29)

NO.			’C31-33		’C31-40 ’LC31-40		’C31-50		’C31-60		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
81	$t_{su(GPIO-H1L)}$	Setup time, general-purpose input before H1 low	12		10		9		8		ns
82	$t_{h(H1L-GPIO)}$	Hold time, general-purpose input after H1 low	0		0		0		0		ns
83	$t_{d(H1H-GPIO)}$	Delay time, general-purpose output after H1 high		15		13		10		8	ns

NOTE 6: Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1. The modes of these pins are defined by the contents of internal-control registers associated with each peripheral.



NOTE A: Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1.

Figure 29. Timing for Peripheral Pin General-Purpose I/O

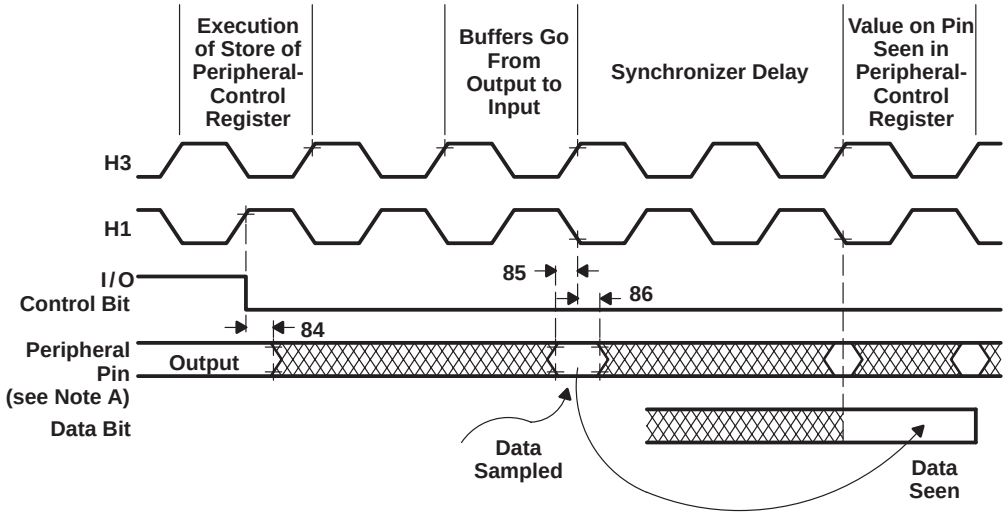
changing the peripheral pin I/O modes

The following tables show the timing parameters for changing the peripheral pin from a general-purpose output pin to a general-purpose input pin and vice versa.

timing requirements for peripheral pin changing from general-purpose output to input mode (see Note 6 and Figure 30)

NO.			'C31-40 'LC31-40		'C31-50		'C31-60		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
84	$t_{h(H1H)}$	Hold time, peripheral pin after H1 high		13		10		8	ns
85	$t_{su(GPIO-H1L)}$	Setup time, peripheral pin before H1 low	9		9		8		ns
86	$t_{h(H1L-GPIO)}$	Hold time, peripheral pin after H1 low	0		0		0		ns

NOTE 6: Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1. The modes of these pins are defined by the contents of internal-control registers associated with each peripheral.



NOTE A: Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1.

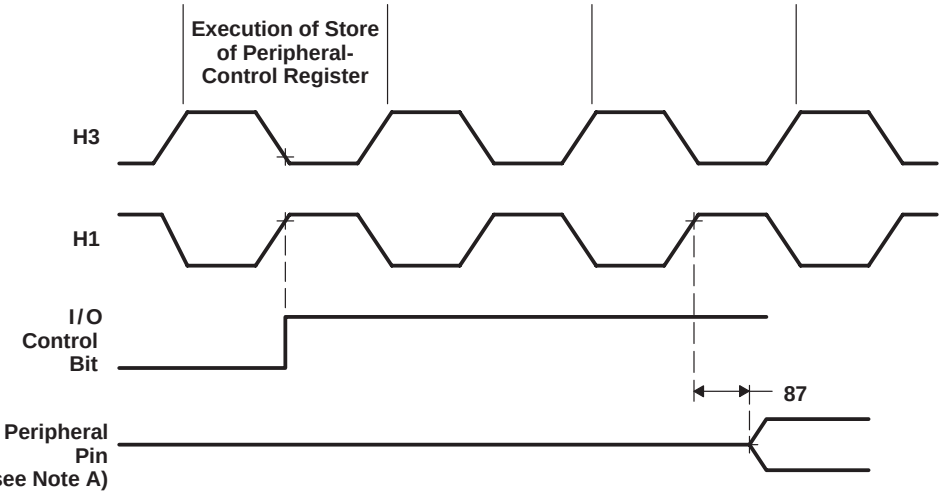
Figure 30. Timing for Change of Peripheral Pin From General-Purpose Output to Input Mode

Not Recommended for New Designs

timing for peripheral pin changing from general-purpose input to output mode (see Note 6 and Figure 31)

NO.			’C31-40 ’LC31-40		’C31-50		’C31-60		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
87	$t_{d(H1H-GPIO)}$	Delay time, H1 high to peripheral pin switching from input to output		13		10		8	ns

NOTE 6: Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1. The modes of these pins are defined by the contents of internal-control registers associated with each peripheral.



NOTE A: Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1.

Figure 31. Timing for Change of Peripheral Pin From General-Purpose Input to Output Mode

Not Recommended for New Designs

timer pin timing

Valid logic-level periods and polarity are specified by the contents of the internal control registers.

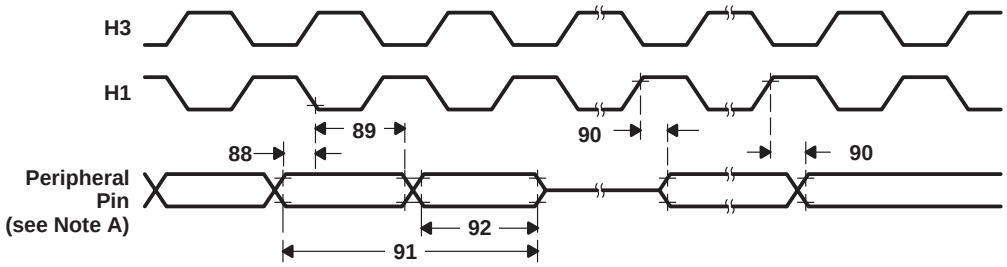
The following tables define the timing requirements for the timer pin.

timing for timer pin (see Figure 32 and Note 7)

NO.				’C31-40, ’LC31-40 ’C31-50		’C31-60		UNIT
				MIN	MAX	MIN	MAX	
88	$t_{su(TCLK-H1L)}$	Setup time, TCLK external before H1 low		10		6		ns
89	$t_{h(H1L-TCLK)}$	Hold time, TCLK external after H1 low		0		0		ns
90	$t_{d(H1H-TCLK)}$	Delay time, H1 high to TCLK internal valid			9		8	ns
91	$t_{c(TCLK)}$	Cycle time, TCLK	TCLK ext	$t_{c(H)}\times2.6$		$t_{c(H)}\times2.6$		ns
			TCLK int	$t_{c(H)}\times2$	$t_{c(H)}\times2^{32}$*	$t_{c(H)}\times2$	$t_{c(H)}\times2^{32}$*	
92	$t_{w(TCLK)}$	Pulse duration, TCLK high/low	TCLK ext	$t_{c(H)}+10$		$t_{c(H)}+10$		ns
			TCLK int	$[t_{c(TCLK)}/2]-5$	$[t_{c(TCLK)}/2]+5$	$[t_{c(TCLK)}/2]-5$	$[t_{c(TCLK)}/2]+5$	

NOTE 7: Numbers 88 and 89 are applicable for a synchronous input clock. Timing parameters 91 and 92 are applicable for an asynchronous input clock.

* This parameter is not production tested.



NOTE A: $\overline{\text{HOLDA}}$ goes low in response to $\overline{\text{HOLD}}$ going low and continues to remain low until one H1 cycle after $\overline{\text{HOLD}}$ goes back high.

Figure 32. Timing for Timer Pin

Not Recommended for New Designs

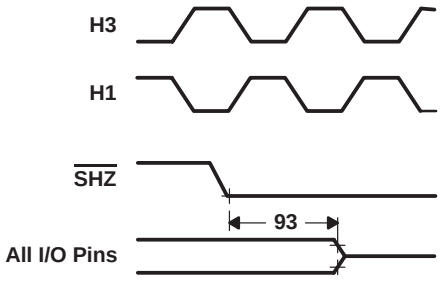
$\overline{\text{SHZ}}$ pin timing

The following table defines the timing parameter for the $\overline{\text{SHZ}}$ pin.

timing parameters for $\overline{\text{SHZ}}$ (see Figure 33)

NO.			'C31 'LC31		UNIT
			MIN	MAX	
93	$t_{dis(SHZ)}$	Disable time, $\overline{\text{SHZ}}$ low to all O, I/O pins disabled (high impedance)	0*	2P†*	ns

† P = $t_{c(CI)}$
* This parameter is not production tested.



NOTE A: Enabling $\overline{\text{SHZ}}$ destroys SMJ320C3x register and memory contents. Assert $\overline{\text{SHZ}}$ = 1 and reset the SMJ320C3x to restore it to a known condition.

Figure 33. Timing for $\overline{\text{SHZ}}$

Not Recommended for New Designs

part order information

DEVICE	TECHNOLOGY	POWER SUPPLY	OPERATING FREQUENCY	PACKAGE TYPE	PROCESSING LEVEL
5962-9205803MXA	0.6-µm CMOS	5 V ± 5%	40 MHz	Ceramic 141-pin staggered PGA	DSCC SMD
SMJ320C31GFAM40	0.6-µm CMOS	5 V ± 5%	40 MHz	Ceramic 141-pin staggered PGA	QML
SM320C31GFAM40	0.6-µm CMOS	5 V ± 5%	40 MHz	Ceramic 141-pin staggered PGA	Std
5962-9205803MYA	0.6-µm CMOS	5 V ± 5%	40 MHz	Ceramic 132-pin quad flatpack with nonconductive tie bar.	DSCC SMD
SMJ320C31HFGM40	0.6-µm CMOS	5 V ± 5%	40 MHz	Ceramic 132-lead quad flatpack with a nonconductive tie bar	QML
SM320C31HFGM40	0.6-µm CMOS	5 V ± 5%	40 MHz	Ceramic 132-lead quad flatpack with a nonconductive tie bar	Std
5962-9205803Q9A	0.72-µm CMOS	5 V ± 5%	40 MHz	C31−40 KGD (known good die)	DSCC SMD
SMJ320C31KGDM40B	0.72-µm CMOS	5 V ± 5%	40 MHz	C31−40 KGD (known good die)	QML
5962-9205804MXA	0.6-µm CMOS	5 V ± 5%	50 MHz	Ceramic 141-pin staggered PGA	DSCC SMD
SMJ320C31GFAM50	0.6-µm CMOS	5 V ± 5%	50 MHz	Ceramic 141-pin staggered PGA	QML
SM320C31GFAM50	0.6-µm CMOS	5 V ± 5%	50 MHz	Ceramic 141-pin staggered PGA	Std
5962-9205804MYA	0.6-µm CMOS	5 V ± 5%	50 MHz	Ceramic 132-pin quad flatpack with nonconductive tie bar.	DSCC SMD
SMJ320C31HFGM50	0.6-µm CMOS	5 V ± 5%	50 MHz	Ceramic 132-lead quad flatpack with nonconductive tie bar	QML
SM320C31HFGM50	0.6-µm CMOS	5 V ± 5%	50 MHz	Ceramic 132-lead quad flatpack with nonconductive tie bar	Std
5962-9205805QXA	0.6-µm CMOS	5 V ± 5%	60 MHz	Ceramic 141-pin staggered PGA	DSCC SMD
SMJ320C31GFAS60	0.6-µm CMOS	5 V ± 5%	60 MHz	Ceramic 141-pin staggered PGA	QML
SM320C31GFAS60	0.6-µm CMOS	5 V ± 5%	60 MHz	Ceramic 141-pin staggered PGA	Std
5962-9205805QYA	0.6-µm CMOS	5 V ± 5%	60 MHz	Ceramic 132-pin quad flatpack with nonconductive tie bar.	DSCC SMD
SMJ320C31HFGS60	0.6-µm CMOS	5 V ± 5%	60 MHz	Ceramic 132-lead quad flatpack with nonconductive tie bar	QML
SM320C31HFGS60	0.6-µm CMOS	5 V ± 5%	60 MHz	Ceramic 132-lead quad flatpack with nonconductive tie bar	Std
5962-9760601NXB	0.72-µm CMOS	3.3 V ± 5%	40 MHz	Plastic 132-lead good flatpack	DSCC SMD
SMQ320LC31PQM40	0.72-µm CMOS	3.3 V ± 5%	40 MHz	Plastic 132-lead good flatpack	QML
5962-9760601Q9A	0.72-µm CMOS	3.3 V ± 5%	40 MHz	LC31−40 KGD (known good die)	DSCC SMD
SMJ320LC31KGDM40B	0.72-µm CMOS	3.3 V ± 5%	40 MHz	LC31−40 KGD (known good die)	QML

Not Recommended for New Designs

part order information (continued)

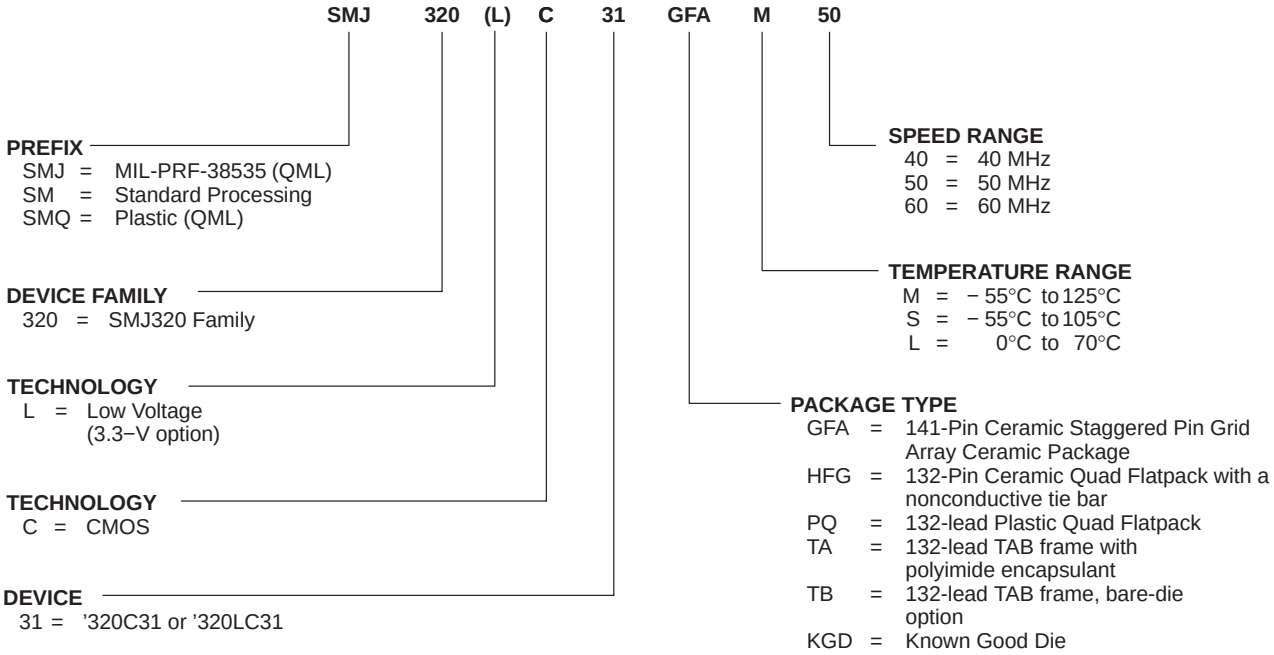


Figure 34. Device Nomenclature

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9205803MXA	NRND	Production	CPGA (GFA) | 141	21 | JEDEC TRAY (5+1)	No	Call TI	N/A for Pkg Type	-55 to 125	5962-9205803MX A SMJ320C31GFAM4 0
5962-9205803MYA	NRND	Production	CFP (HFG) | 132	10 | JEDEC TRAY (5+1)	No	Call TI	N/A for Pkg Type	-55 to 125	5962-9205803MY A SMJ320C31HFGM4 0
5962-9205804MXA	NRND	Production	CPGA (GFA) | 141	21 | JEDEC TRAY (5+1)	No	Call TI	N/A for Pkg Type	-55 to 125	5962-9205804MX A SMJ320C31GFAM5 0
5962-9205804MYA	NRND	Production	CFP (HFG) | 132	10 | JEDEC TRAY (5+1)	No	Call TI	N/A for Pkg Type	-55 to 125	5962-9205804MY A SMJ320C31HFGM5 0
5962-9205805QXA	NRND	Production	CPGA (GFA) | 141	21 | JEDEC TRAY (5+1)	No	Call TI	N/A for Pkg Type	-55 to 95	5962-9205805QX A SMJ320C31GFAS6 0
5962-9205805QYA	NRND	Production	CFP (HFG) | 132	10 | JEDEC TRAY (5+1)	No	Call TI	N/A for Pkg Type	-55 to 95	5962-9205805QY A SMJ320C31HFGS6 0
5962-9760601NXB	NRND	Production	BQFP (PQ) | 132	36 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-4-260C-72 HR	-55 to 125	5962-9760601NX B SMQ320LC31PQM4 0
SM320C31GFAM50	NRND	Production	CPGA (GFA) | 141	21 | JEDEC TRAY (5+1)	Yes	Call TI	N/A for Pkg Type	-55 to 125	SM320C31GFAM50
SM320C31HFGM40	NRND	Production	CFP (HFG) | 132	10 | null	Yes	Call TI	N/A for Pkg Type	-55 to 125	SM320C31HFGM40
SM320C31HFGM50	NRND	Production	CFP (HFG) | 132	10 | null	Yes	Call TI	N/A for Pkg Type	-55 to 125	SM320C31HFGM50
SMJ320C31GFAM40	NRND	Production	CPGA (GFA) | 141	21 | JEDEC TRAY (5+1)	No	Call TI	N/A for Pkg Type	-55 to 125	5962-9205803MX A SMJ320C31GFAM4 0

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SMJ320C31GFAM50	NRND	Production	CPGA (GFA) | 141	21 | JEDEC TRAY (5+1)	No	Call TI	N/A for Pkg Type	-55 to 125	5962-9205804MX A SMJ320C31GFAM50
SMJ320C31GFAS60	NRND	Production	CPGA (GFA) | 141	21 | JEDEC TRAY (5+1)	No	Call TI	N/A for Pkg Type	-55 to 95	5962-9205805QX A SMJ320C31GFAS60
SMJ320C31HFGM40	NRND	Production	CFP (HFG) | 132	10 | JEDEC TRAY (5+1)	No	Call TI	N/A for Pkg Type	-55 to 125	5962-9205803MY A SMJ320C31HFGM40
SMJ320C31HFGM50	NRND	Production	CFP (HFG) | 132	10 | JEDEC TRAY (5+1)	No	Call TI	N/A for Pkg Type	-55 to 125	5962-9205804MY A SMJ320C31HFGM50
SMJ320C31HFGS60	NRND	Production	CFP (HFG) | 132	10 | JEDEC TRAY (5+1)	No	Call TI	N/A for Pkg Type	-55 to 95	5962-9205805QY A SMJ320C31HFGS60
SMQ320LC31PQM40	NRND	Production	BQFP (PQ) | 132	55 | JEDEC TRAY (5+1)	-	Call TI	Call TI	-55 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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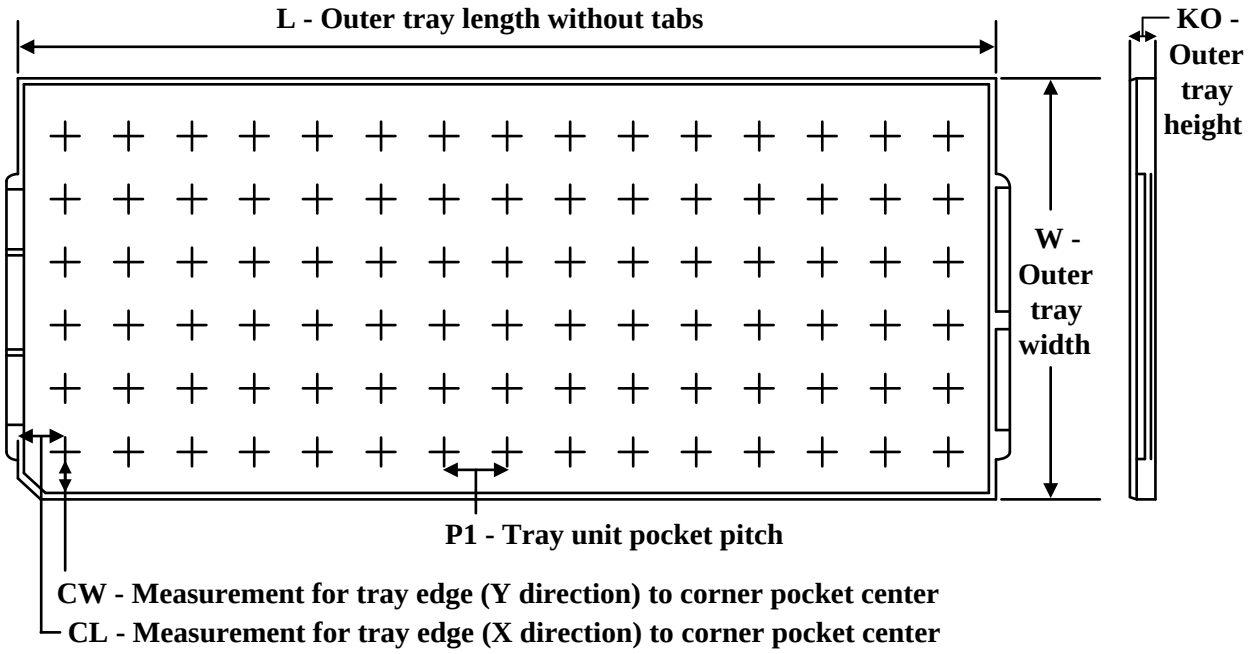
OTHER QUALIFIED VERSIONS OF SM320C31 :

- Military : SMJ320C31

NOTE: Qualified Version Definitions:

- Military - QML certified for Military and Defense Applications

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

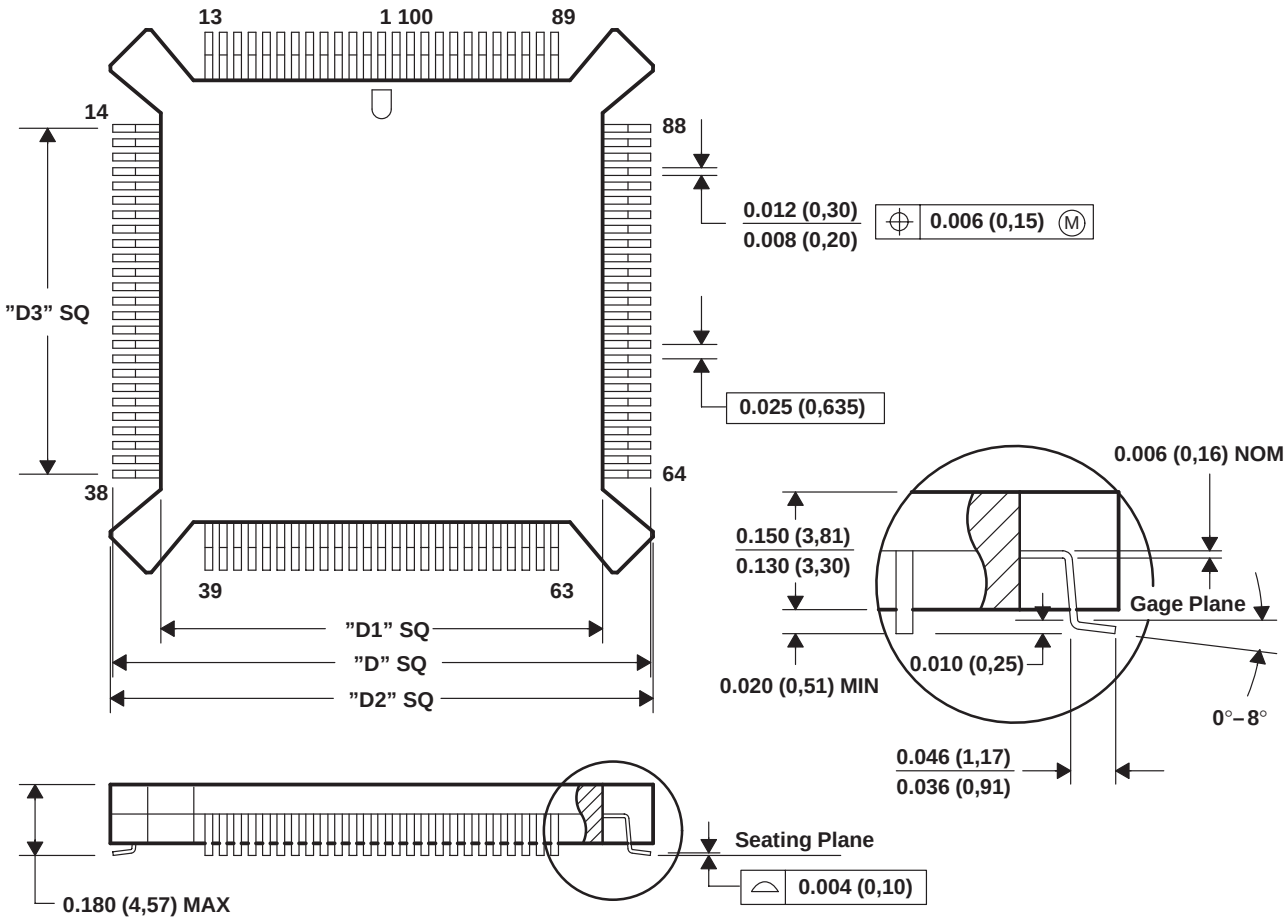
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
5962-9760601NXB	PQ	BQFP	132	36	4X9	180	315	135.9	7620	33.37	23.98	20.93

MBQF001A – NOVEMBER 1995

PQ (S-PQFP-G*)** **PLASTIC QUAD FLATPACK**

100 LEAD SHOWN

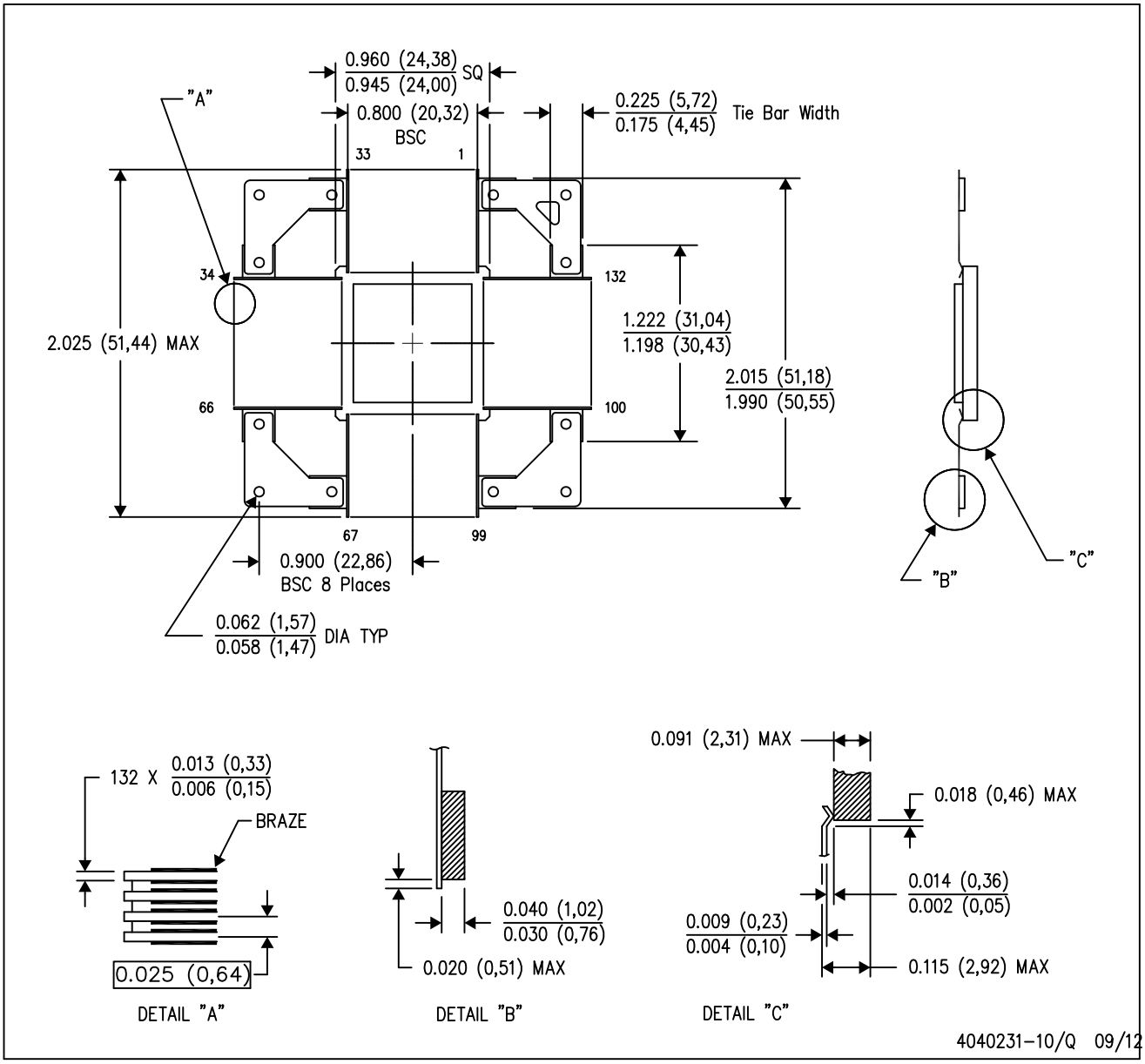


DIM \ LEADS ***		100	132
"D"	MAX	0.890 (22,61)	1.090 (27,69)
	MIN	0.870 (22,10)	1.070 (27,18)
"D1"	MAX	0.766 (19,46)	0.966 (24,54)
	MIN	0.734 (18,64)	0.934 (23,72)
"D2"	MAX	0.912 (23,16)	1.112 (28,25)
	MIN	0.888 (22,56)	1.088 (27,64)
"D3"	NOM	0.600 (15,24)	0.800 (20,32)

4040045/C 11/95

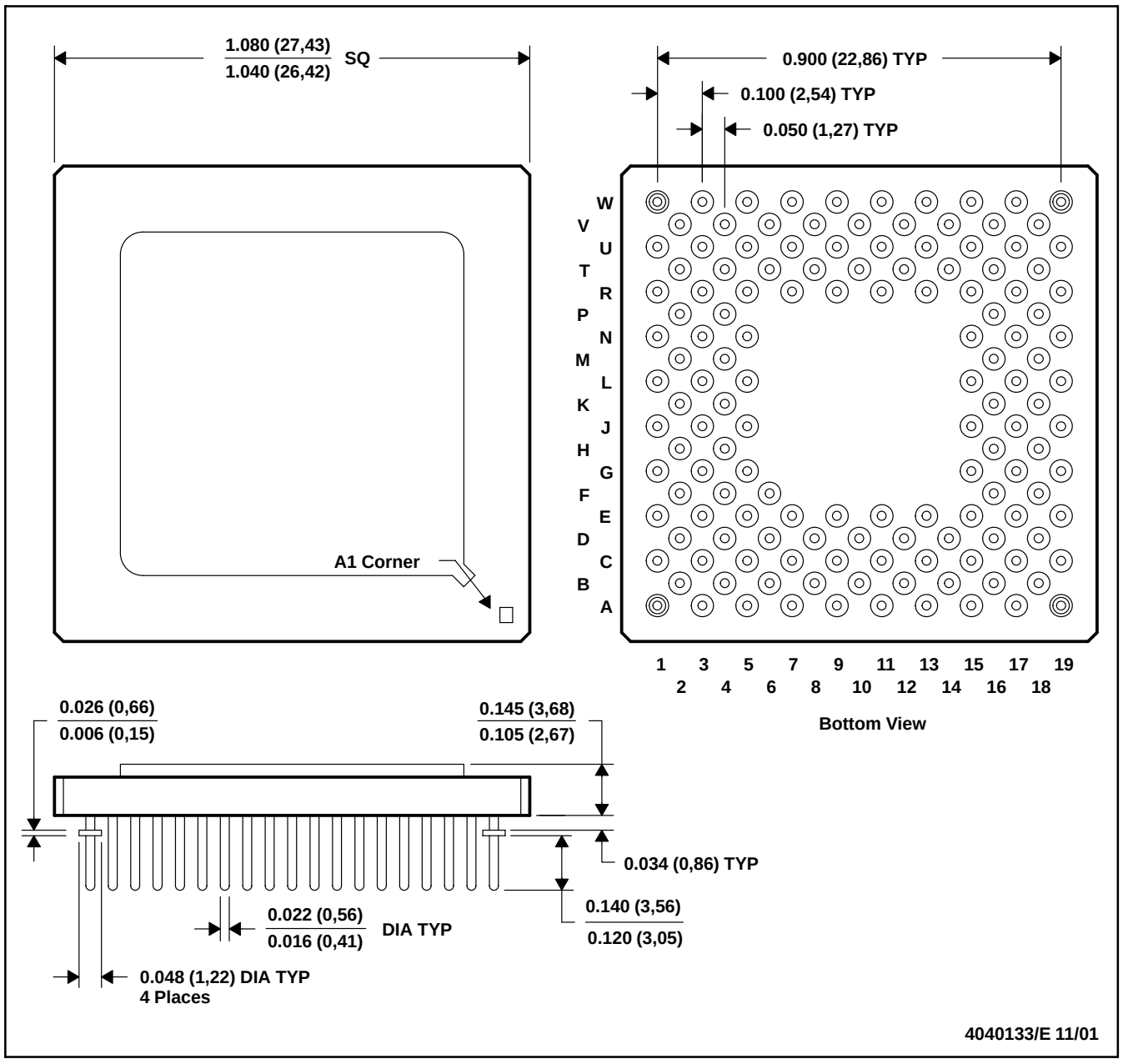
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-069

HFG (S–CQFP–F132) CERAMIC QUAD FLATPACK WITH NCTB



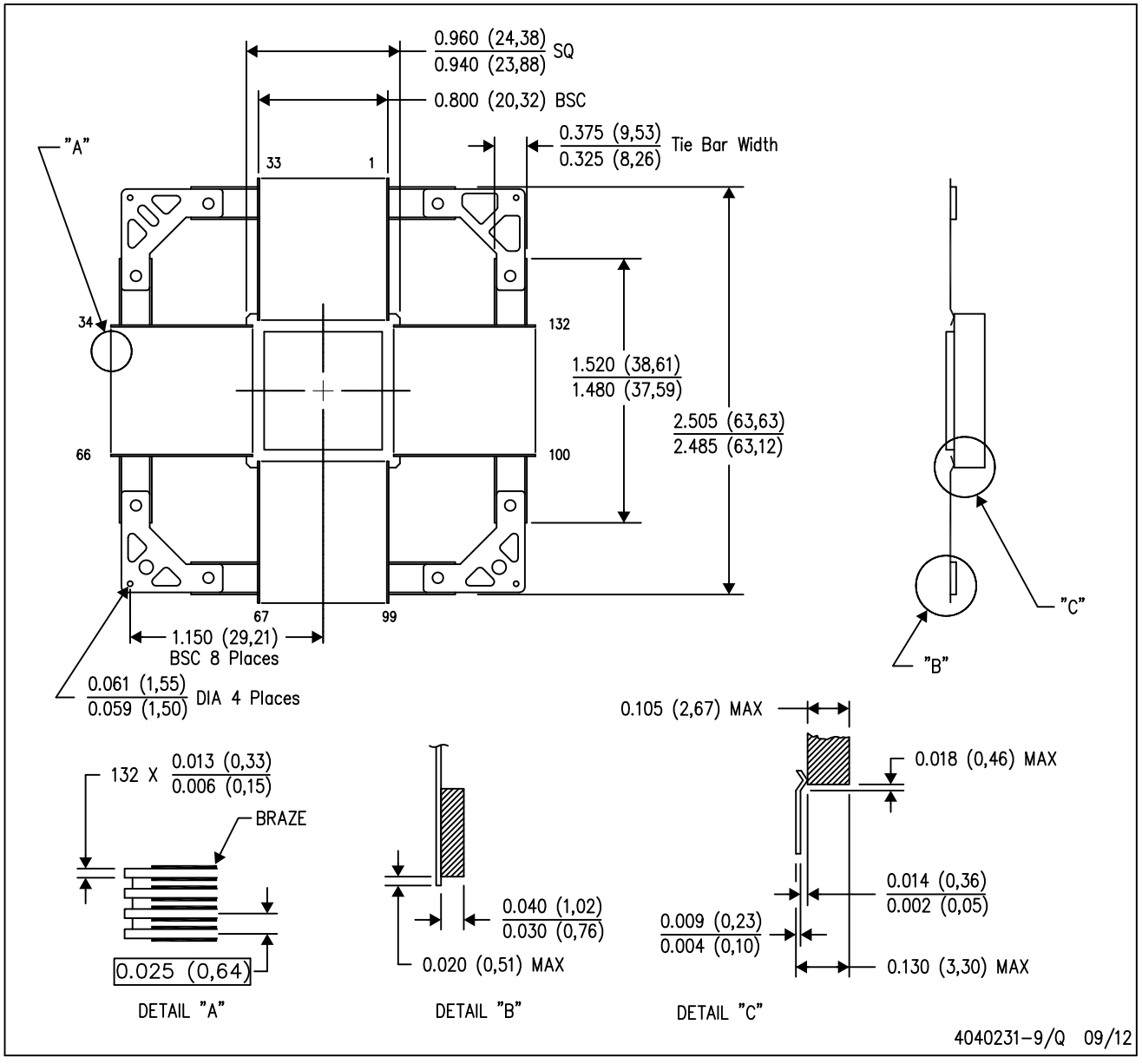
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Ceramic quad flatpack with flat leads brazed to non–conductive tie bar carrier.
D. This package is hermetically sealed with a metal lid.
E. The leads are gold plated and can be solderdipped.
F. Leads not shown for clarity purposes.

GFA (S-CPGA-P141) **CERAMIC PIN GRID ARRAY**



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Index mark can appear on top or bottom, depending on package vendor.
D. Pins are located within 0.010 (0,25) diameter of true position relative to each other at maximum material condition and within 0.030 (0,76) diameter relative to the edge of the ceramic.
E. This package can be hermetically sealed with metal lids or with ceramic lids using glass frit.
F. The pins can be gold-plated or solder-dipped.
G. Falls within JEDEC MO-128AB

HFG (S–CQFP–F132) CERAMIC QUAD FLATPACK WITH NCTB



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Ceramic quad flatpack with flat leads brazed to non–conductive tie bar carrier.
D. This package is hermetically sealed with a metal lid.
E. The leads are gold plated and can be solderdipped.
F. Leads not shown for clarity purposes.
G. Falls within JEDEC MO–113AC

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Last updated 10/2025