The SN54165 and SN74165 devices are obsolete and are no longer supplied.

SDLS062D – OCTOBER 1976 – REVISED FEBRUARY 2002

- **Complementary Outputs**
- **Direct Overriding Load (Data) Inputs**
- **Gated Clock Inputs**
- **Parallel-to-Serial Data Conversion**

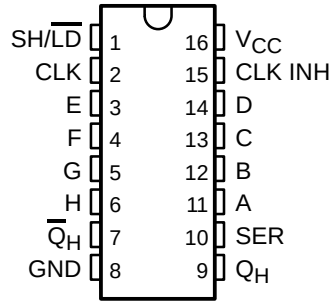
TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
’165	26 MHz	210 mW
’LS165A	35 MHz	90 mW

description

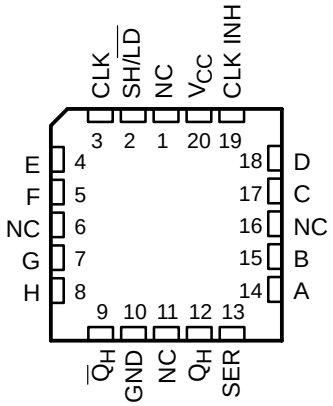
The ’165 and ’LS165A are 8-bit serial shift registers that shift the data in the direction of Q_A toward Q_H when clocked. Parallel-in access to each stage is made available by eight individual, direct data inputs that are enabled by a low level at the shift/load (SH/$\overline{LD}$) input. These registers also feature gated clock (CLK) inputs and complementary outputs from the eighth bit. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design.

Clocking is accomplished through a two-input positive-NOR gate, permitting one input to be used as a clock-inhibit function. Holding either of the clock inputs high inhibits clocking, and holding either clock input low with SH/$\overline{LD}$ high enables the other clock input. Clock inhibit (CLK INH) should be changed to the high level only while CLK is high. Parallel loading is inhibited as long as SH/$\overline{LD}$ is high. Data at the parallel inputs are loaded directly into the register while SH/$\overline{LD}$ is low, independently of the levels of CLK, CLK INH, or serial (SER) inputs.

SN54165, SN54LS165A . . . J OR W PACKAGE
SN74165 . . . N PACKAGE
SN74LS165A . . . D, N, OR NS PACKAGE
(TOP VIEW)



SN54LS165A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

The SN54165 and SN74165 devices are obsolete and are no longer supplied.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74LS165AN	SN74LS165AN
	SOIC – D	Tube	SN74LS165AD	LS165A
		Tape and reel	SN74LS165ADR	
	SOP – NS	Tape and reel	SN74LS165ANSR	74LS165A
–55°C to 125°C	CDIP – J	Tube	SN54LS165AJ	SN54LS165AJ
		Tube	SNJ54LS165AJ	SNJ54LS165AJ
	CFP – W	Tube	SNJ54LS165AW	SNJ54LS165AW
	LCCC – FK	Tube	SNJ54LS165AFK	SNJ54LS165AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

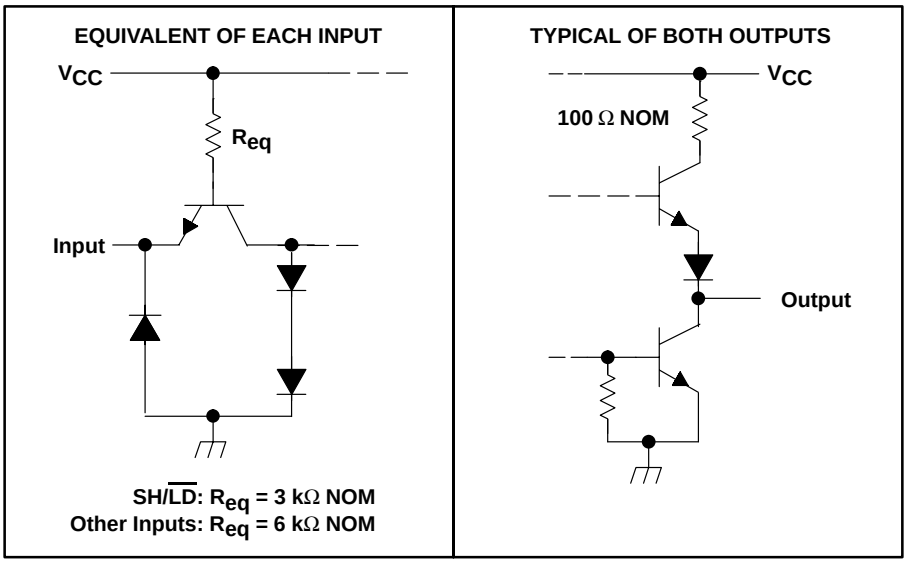
INPUTS					INTERNAL OUTPUTS		OUTPUT Q_H
SH/$\overline{LD}$	CLK INH	CLK	SER	PARALLEL A . . . H	$\overline{Q}_A$	$\overline{Q}_B$	
L	X	X	X	a . . . h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	H	X	X	X	Q_{A0}	Q_{B0}	Q_{H0}

The SN54165 and SN74165 devices are obsolete and are no longer supplied.

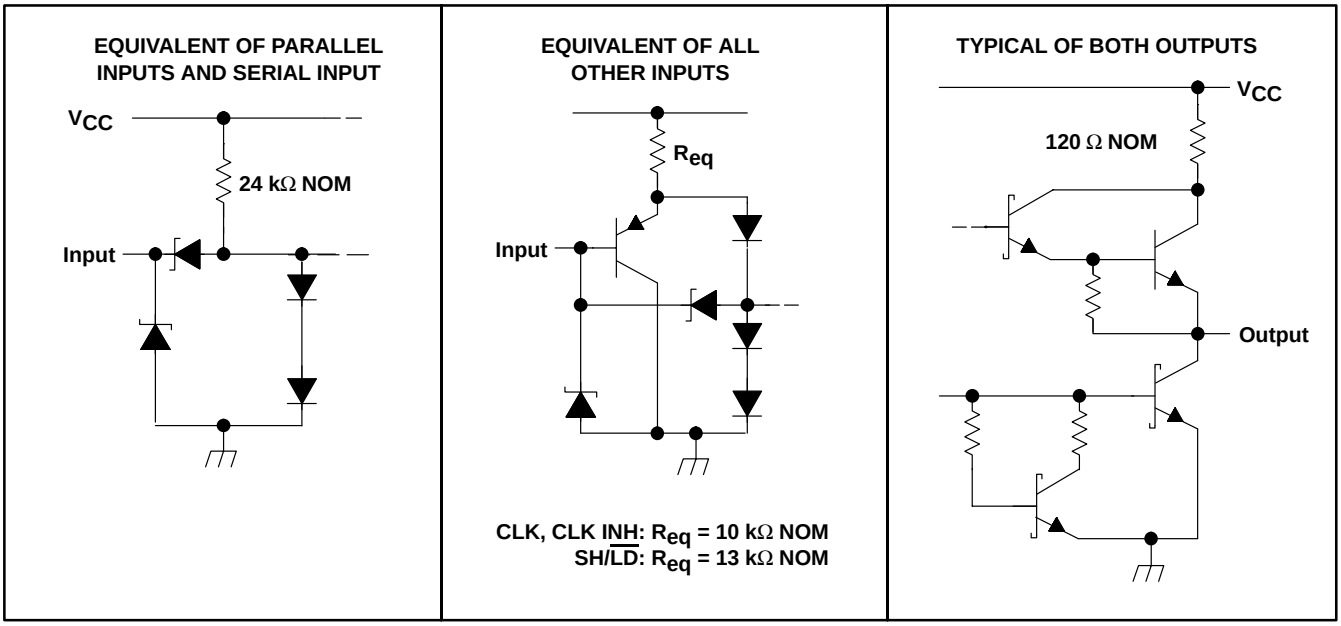
SDLS062D – OCTOBER 1976 – REVISED FEBRUARY 2002

schematics of inputs and outputs

'165

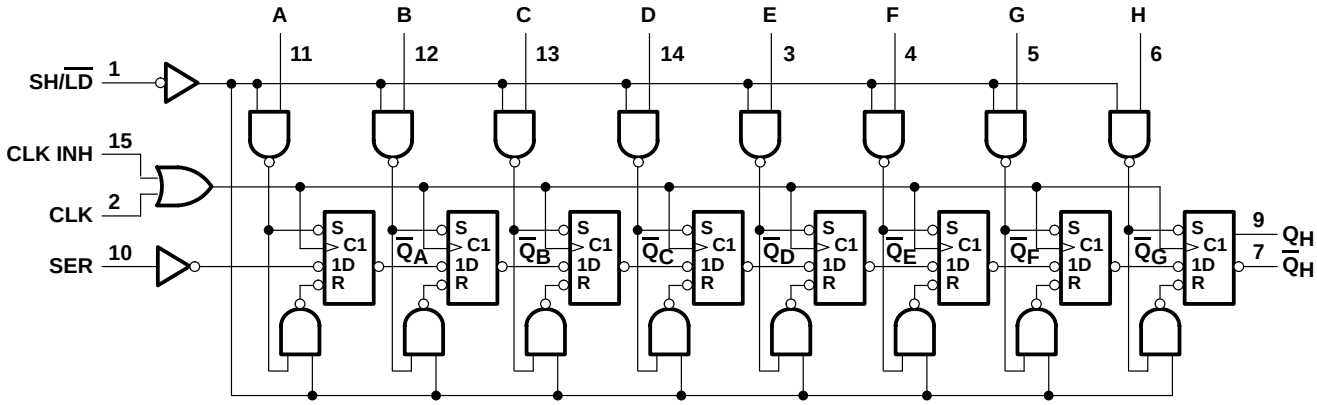


'LS165A



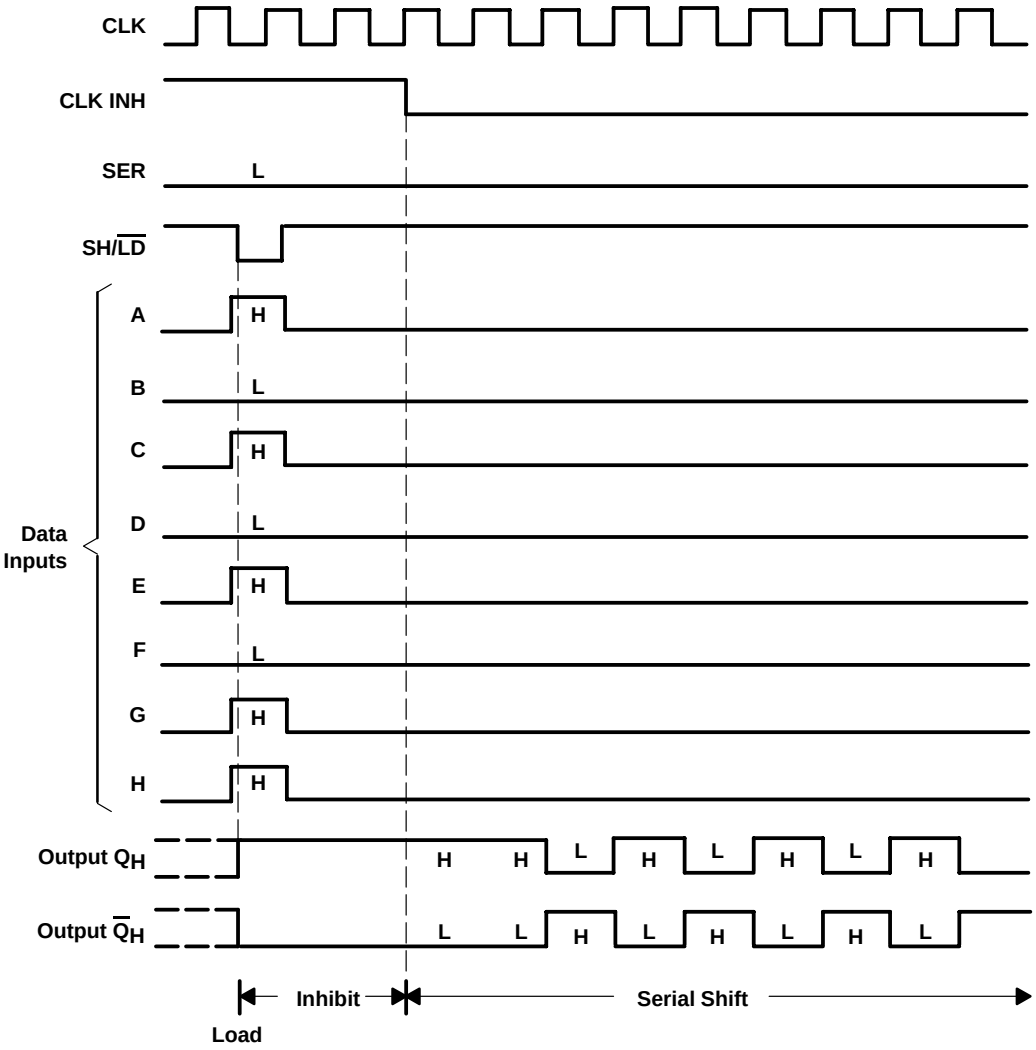
The SN54165 and SN74165 devices are obsolete and are no longer supplied.

logic diagram (positive logic)



Pin numbers shown are for D, J, N, NS, and W packages.

typical shift, load, and inhibit sequences



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, V_I: SN54165, SN74165 . . . . . 5.5 V
SN54LS165A, SN74LS165A . . . . . 7 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Package thermal impedance θ_{JA} (see Note 3): D package . . . . . 73°C/W
N package . . . . . 67°C/W
NS package . . . . . 64°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. This rating applies for the '165 to the SH/$\overline{LD}$ input in conjunction with the CLK INH input.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

		SN54165			SN74165			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current			–800			–800	μA
I_{OL}	Low-level output current			16			16	mA
f_{clock}	Clock frequency	0		20	0		20	MHz
$t_{w(clock)}$	Width of clock input pulse	25			25			ns
$t_{w(load)}$	Width of load input pulse	15			15			ns
t_{su}	Clock-enable setup time (see Figure 1)	30			30			ns
t_{su}	Parallel input setup time (see Figure 1)	10			10			ns
t_{su}	Serial input setup time (see Figure 1)	20			20			ns
t_{su}	Shift setup time (see Figure 1)	45			45			ns
t_h	Hold time at any input	0			0			ns
T_A	Operating free-air temperature	–55		125	0		70	°C

The SN54165 and SN74165 devices are obsolete and are no longer supplied.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	SN54165			SN74165			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = –12 mA			–1.5			–1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = –800 μA	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	SH/$\overline{LD}$	V_{CC} = MAX, V_I = 2.4 V			80			80	μA
		Other inputs				40			40	
I_{IL}	Low-level input current	SH/$\overline{LD}$	V_{CC} = MAX, V_I = 0.4 V			–3.2			–3.2	mA
		Other inputs				–1.6			–1.6	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	–20		–55	–18		–55	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 4		42	63		42	63	mA

NOTE 4: With the outputs open, CLK INH and CLK at 4.5 V, and a clock pulse applied to SH/$\overline{LD}$, I_{CC} is measured first with the parallel inputs at 4.5 V, then with the parallel inputs grounded.

† For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

SN54165 and SN74165 switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 1)

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}				20	26		MHz
t_{PLH}	$\overline{LD}$	Any	C_L = 15 pF, R_L = 400 Ω		21	31	ns
t_{PHL}					27	40	
t_{PLH}	CLK	Any	C_L = 15 pF, R_L = 400 Ω		16	24	ns
t_{PHL}					21	31	
t_{PLH}	H	Q_H	C_L = 15 pF, R_L = 400 Ω		11	17	ns
t_{PHL}					24	36	
t_{PLH}	H	$\overline{Q}_H$	C_L = 15 pF, R_L = 400 Ω		18	27	ns
t_{PHL}					18	27	

¶ f_{max} = maximum clock frequency, t_{PLH} = propagation delay time, low-to-high-level output, t_{PHL} = propagation delay time, high-to-low-level output

The SN54165 and SN74165 devices are obsolete and are no longer supplied.

recommended operating conditions

			SN54LS165A			SN74LS165A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				–0.4			–0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		25	0		25	MHz
$t_{w(clock)}$	Width of clock input pulse (see Figure 2)	Clock high	15			15			ns
		Clock low	25			25			
$t_{w(load)}$	Width of load input pulse	Clock high	25			25			ns
		Clock low	17			17			
t_{su}	Clock-enable setup time (see Figure 2)		30			30			ns
t_{su}	Parallel input setup time (see Figure 2)		10			10			ns
t_{su}	Serial input setup time (see Figure 2)		20			20			ns
t_{su}	Shift setup time (see Figure 2)		45			45			ns
t_h	Hold time at any input		0			0			ns
T_A	Operating free-air temperature		–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			SN54LS165A			SN74LS165A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN, I_I = –18 mA					–1.5			–1.5	V
V_{OH}	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX,		I_{OH} = –0.4 mA	2.5	3.5		2.7	3.5		V
V_{OL}	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX		I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = MAX, V_I = 7 V					0.1			0.1	mA
I_{IH}	V_{CC} = MAX, V_I = 2.7 V					20			20	µA
I_{IL}	V_{CC} = MAX, V_I = 0.4 V					–0.4			–0.4	mA
I_{OS}§	V_{CC} = MAX			–20		–100	–20		–100	mA
I_{CC}	V_{CC} = MAX, See Note 4				18	30		18	30	mA

NOTE 4. With the outputs open, CLK INH and CLK at 4.5 V, and a clock pulse applied to SH/$\overline{LD}$, I_{CC} is measured first with the parallel inputs at 4.5 V, then with the parallel inputs grounded.

† For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

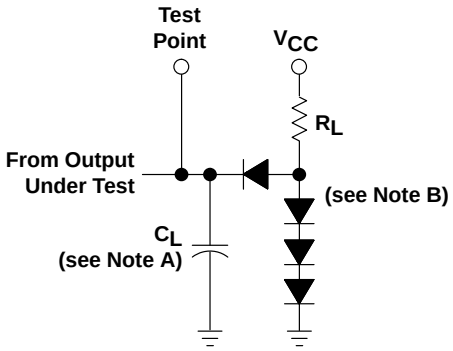
§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

SN54LS165A and SN74LS165A switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 2)

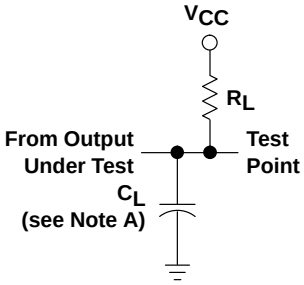
PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}				25	35		MHz
t_{PLH}	$\overline{LD}$	Any	R_L = 2 kΩ, C_L = 15 pF		21	35	ns
t_{PHL}					26	35	
t_{PLH}	CLK	Any	R_L = 2 kΩ, C_L = 15 pF		14	25	ns
t_{PHL}					16	25	
t_{PLH}	H	Q_H	R_L = 2 kΩ, C_L = 15 pF		13	25	ns
t_{PHL}					24	30	
t_{PLH}	H	$\overline{Q}_H$	R_L = 2 kΩ, C_L = 15 pF		19	30	ns
t_{PHL}					17	25	

† f_{max} = maximum clock frequency, t_{PLH} = propagation delay time, low-to-high-level output, t_{PHL} = propagation delay time, high-to-low-level output

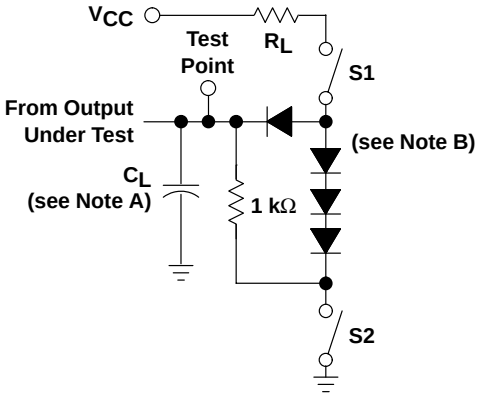
PARAMETER MEASUREMENT INFORMATION
SERIES 54/74 DEVICES



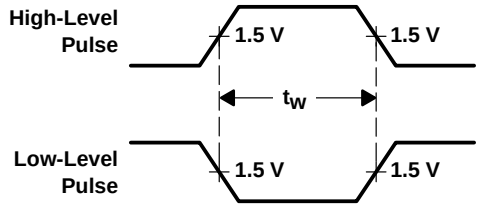
LOAD CIRCUIT FOR 2-STATE TOTEM-POLE OUTPUTS



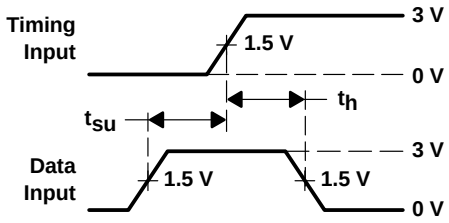
LOAD CIRCUIT FOR OPEN-COLLECTOR OUTPUTS



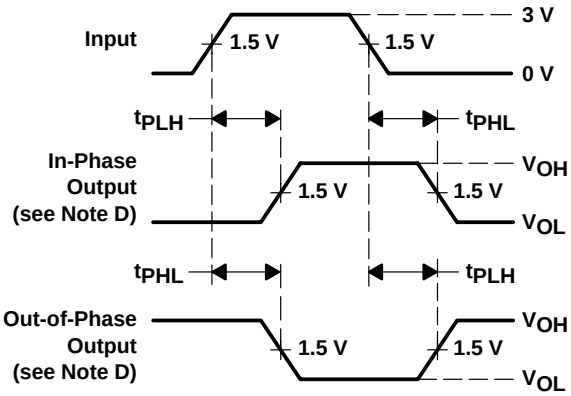
LOAD CIRCUIT FOR 3-STATE OUTPUTS



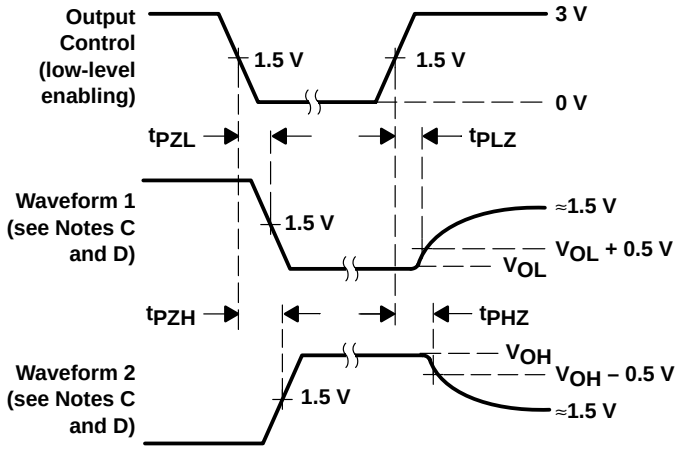
VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES

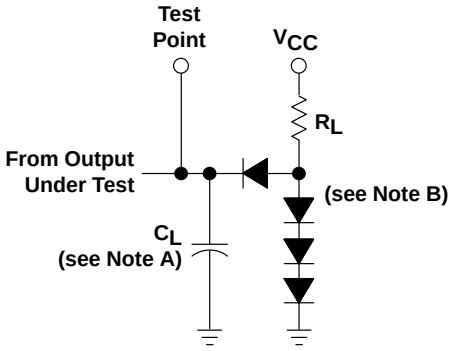


VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

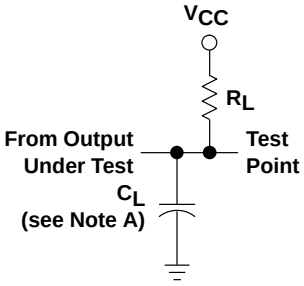
NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. S1 and S2 are closed for t_{PLH}, t_{PHL}, t_{PHZ}, and t_{PLZ}; S1 is open and S2 is closed for t_{PZH}; S1 is closed and S2 is open for t_{PZL}.
E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O \approx 50\ \Omega$; t_r and $t_f \leq 7$ ns for Series 54/74 devices and t_r and $t_f \leq 2.5$ ns for Series 54S/74S devices.
F. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

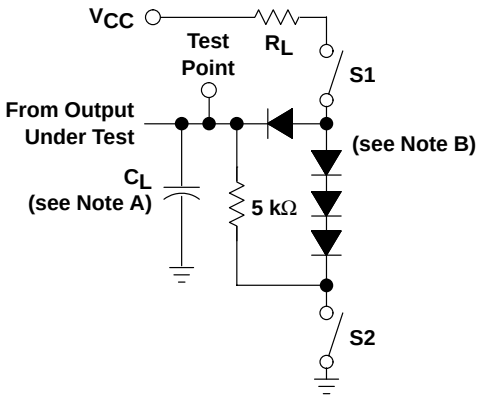
PARAMETER MEASUREMENT INFORMATION
SERIES 54LS/74LS DEVICES



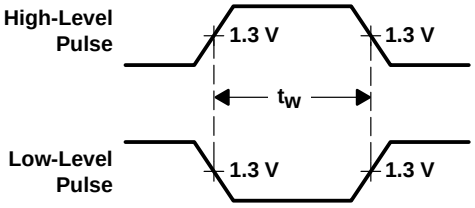
LOAD CIRCUIT FOR 2-STATE TOTEM-POLE OUTPUTS



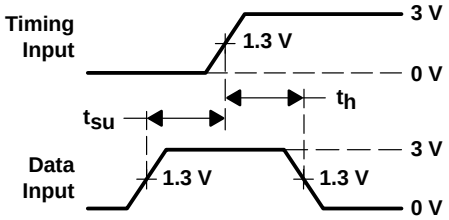
LOAD CIRCUIT FOR OPEN-COLLECTOR OUTPUTS



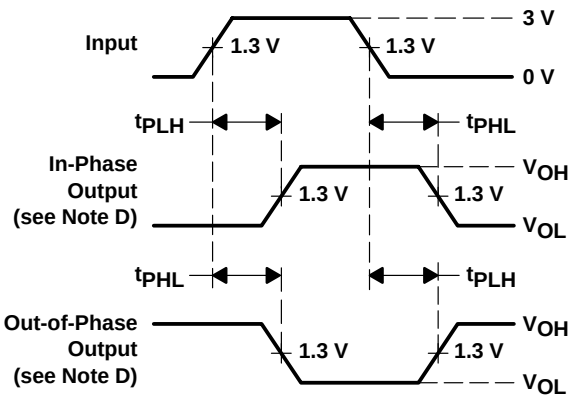
LOAD CIRCUIT FOR 3-STATE OUTPUTS



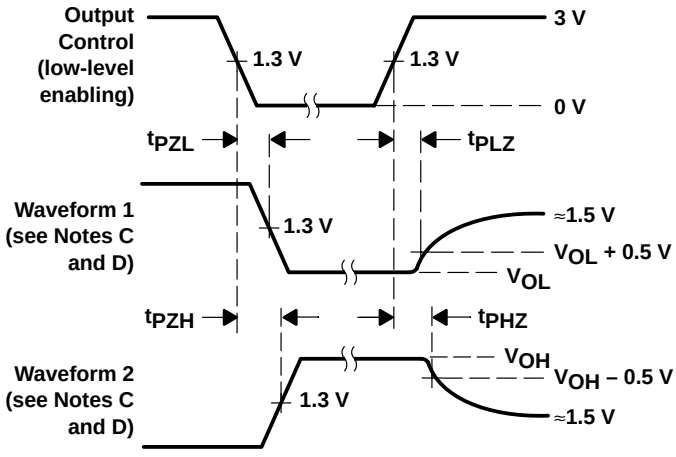
VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. S1 and S2 are closed for t_{PLH}, t_{PHL}, t_{PHZ}, and t_{PLZ}; S1 is open and S2 is closed for t_{PZH}; S1 is closed and S2 is open for t_{PZL}.
E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.
F. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O \approx 50\ \Omega$, $t_r \le 1.5$ ns, $t_f \le 2.6$ ns.
G. The outputs are measured one at a time with one input transition per measurement.

Figure 2. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-7700601VEA	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-7700601VEA SNV54LS165AJ
5962-7700601VEA.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-7700601VEA SNV54LS165AJ
5962-7700601VFA	Active	Production	CFP (W) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-7700601VFA SNV54LS165AW
5962-7700601VFA.A	Active	Production	CFP (W) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-7700601VFA SNV54LS165AW
7700601EA	NRND	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7700601EA SNJ54LS165AJ
7700601FA	Active	Production	CFP (W) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7700601FA SNJ54LS165AW
JM38510/30608B2A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 30608B2A
JM38510/30608B2A.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 30608B2A
JM38510/30608BEA	NRND	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 30608BEA
JM38510/30608BEA.A	NRND	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 30608BEA
JM38510/30608BFA	Active	Production	CFP (W) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 30608BFA
JM38510/30608BFA.A	Active	Production	CFP (W) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 30608BFA
M38510/30608B2A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 30608B2A
M38510/30608BEA	NRND	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 30608BEA
M38510/30608BFA	Active	Production	CFP (W) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 30608BFA

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN54LS165AJ	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS165AJ
SN54LS165AJ.A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS165AJ
SN74LS165AD	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	0 to 70	LS165A
SN74LS165ADR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS165A
SN74LS165ADR.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS165A
SN74LS165AN	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS165AN
SN74LS165AN.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS165AN
SN74LS165ANE4	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS165AN
SN74LS165ANSR	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS165A
SN74LS165ANSR.A	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS165A
SNJ54LS165AFK	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54LS 165AFK
SNJ54LS165AFK.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SNJ54LS 165AFK
SNJ54LS165AJ	NRND	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7700601EA SNJ54LS165AJ
SNJ54LS165AJ.A	NRND	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7700601EA SNJ54LS165AJ
SNJ54LS165AW	Active	Production	CFP (W) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7700601FA SNJ54LS165AW
SNJ54LS165AW.A	Active	Production	CFP (W) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	7700601FA SNJ54LS165AW

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54LS165A, SN54LS165A-SP, SN74LS165A :

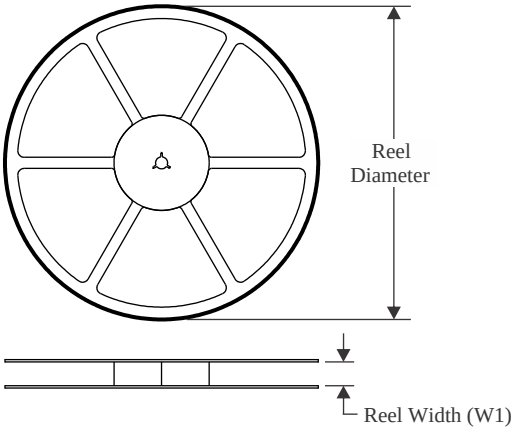
- Catalog : SN74LS165A, SN54LS165A
- Military : SN54LS165A
- Space : SN54LS165A-SP

NOTE: Qualified Version Definitions:

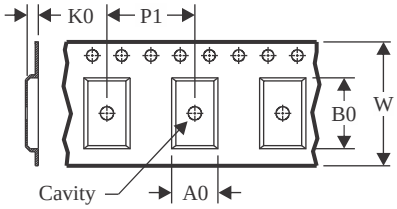
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

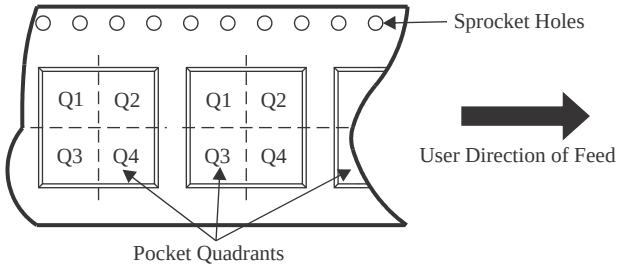


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

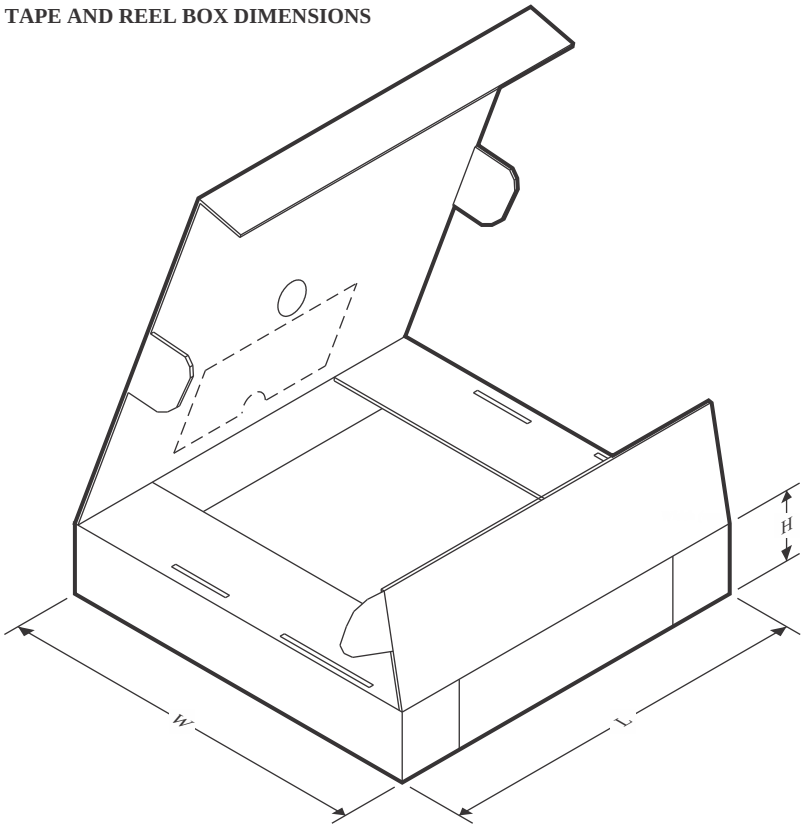
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS165ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LS165ANSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1

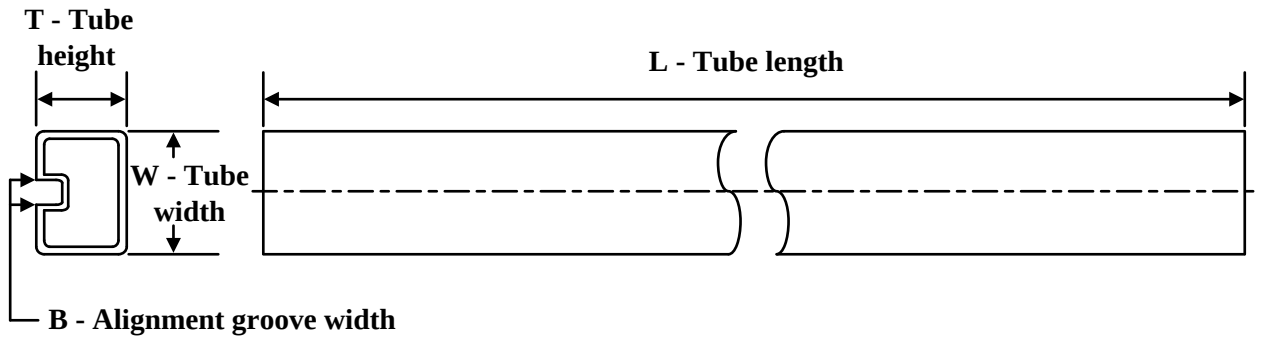
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS165ADR	SOIC	D	16	2500	353.0	353.0	32.0
SN74LS165ANSR	SOP	NS	16	2000	353.0	353.0	32.0

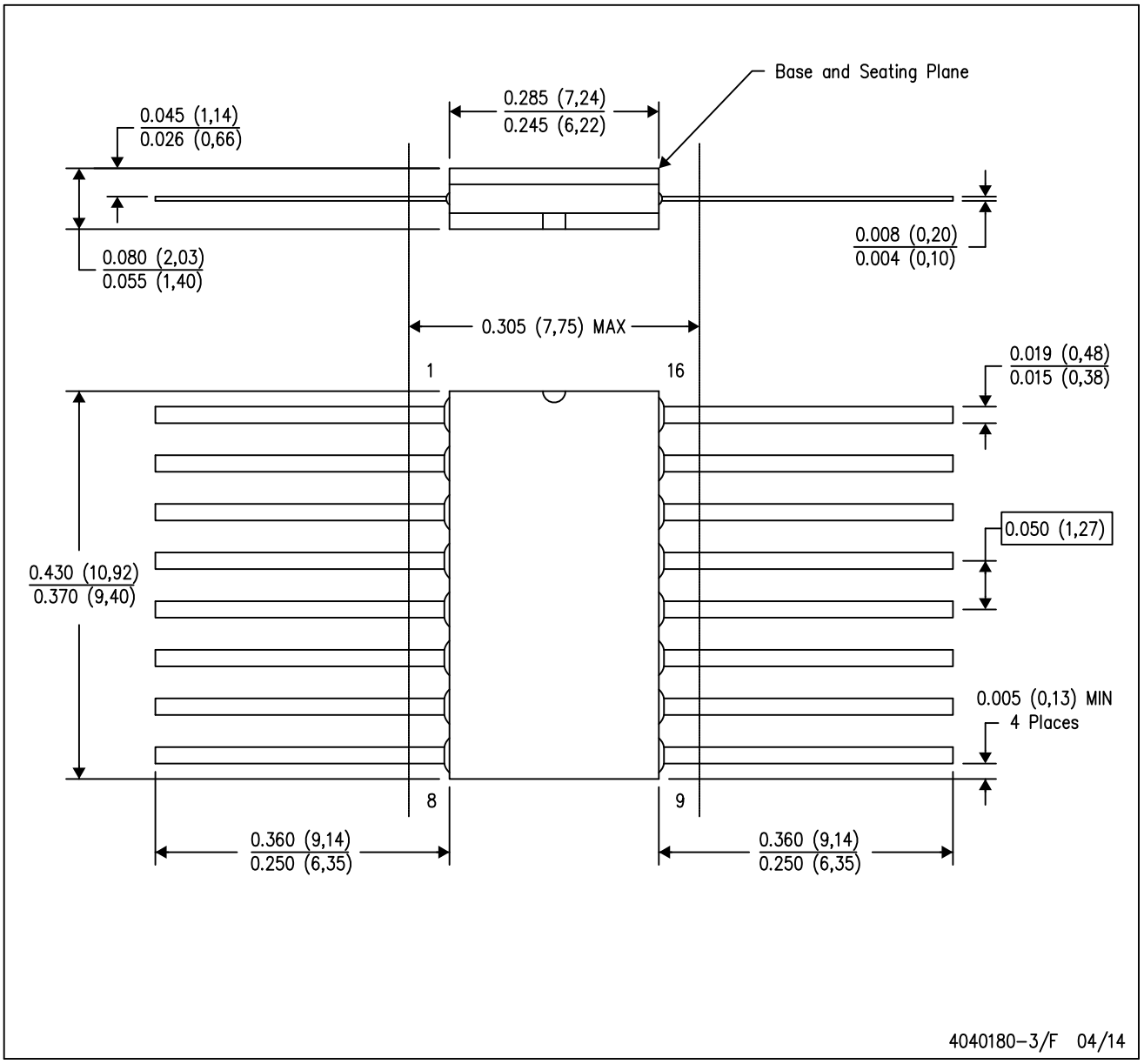
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-7700601VFA	W	CFP	16	25	506.98	26.16	6220	NA
5962-7700601VFA.A	W	CFP	16	25	506.98	26.16	6220	NA
7700601FA	W	CFP	16	25	506.98	26.16	6220	NA
JM38510/30608B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
JM38510/30608B2A.A	FK	LCCC	20	55	506.98	12.06	2030	NA
JM38510/30608BFA	W	CFP	16	25	506.98	26.16	6220	NA
JM38510/30608BFA.A	W	CFP	16	25	506.98	26.16	6220	NA
M38510/30608B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
M38510/30608BFA	W	CFP	16	25	506.98	26.16	6220	NA
SN74LS165AN	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS165AN	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS165AN.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS165AN.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS165ANE4	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS165ANE4	N	PDIP	16	25	506	13.97	11230	4.32
SNJ54LS165AFK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54LS165AFK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54LS165AW	W	CFP	16	25	506.98	26.16	6220	NA
SNJ54LS165AW.A	W	CFP	16	25	506.98	26.16	6220	NA

W (R–GDFP–F16) CERAMIC DUAL FLATPACK



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP2–F16

GENERIC PACKAGE VIEW

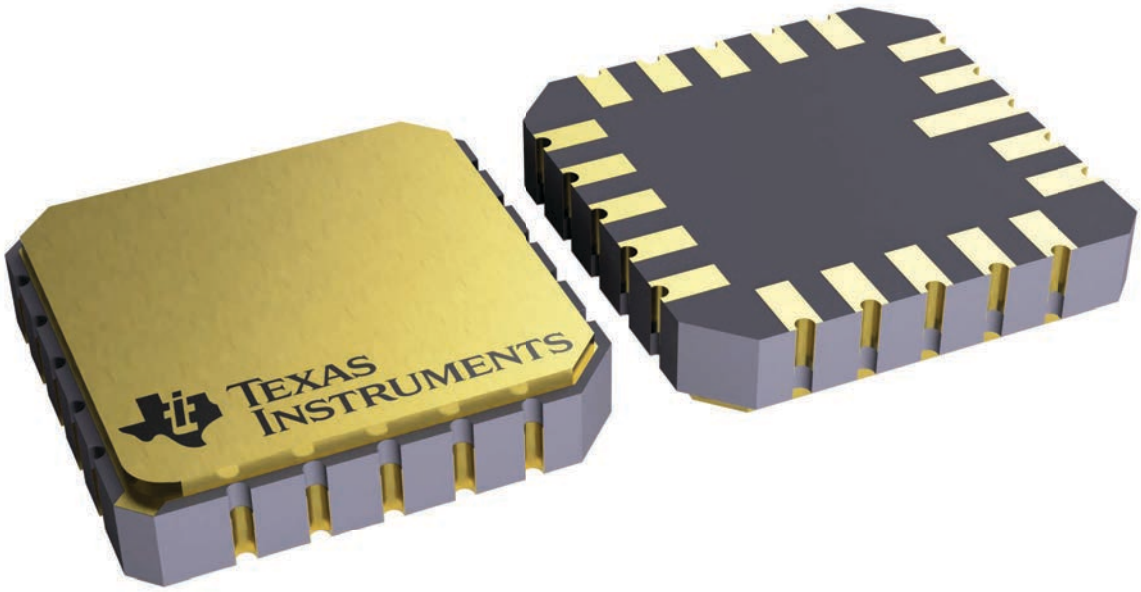
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

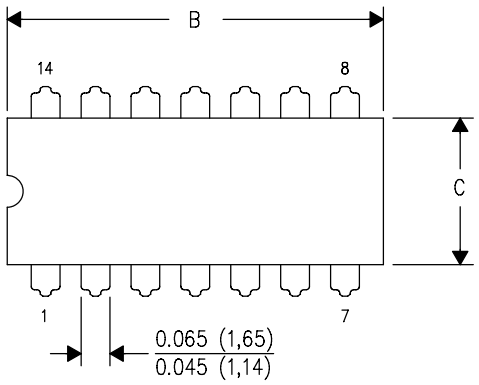


4229370VA\

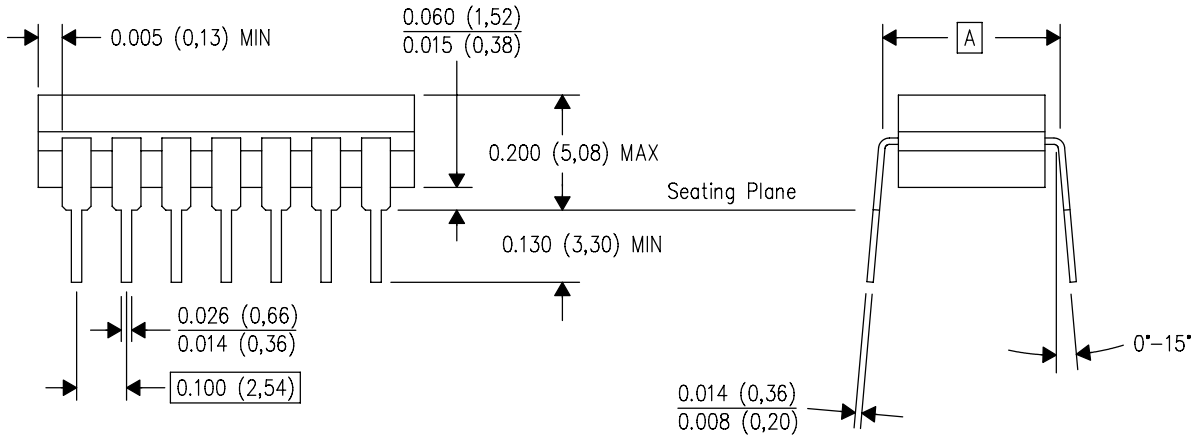
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



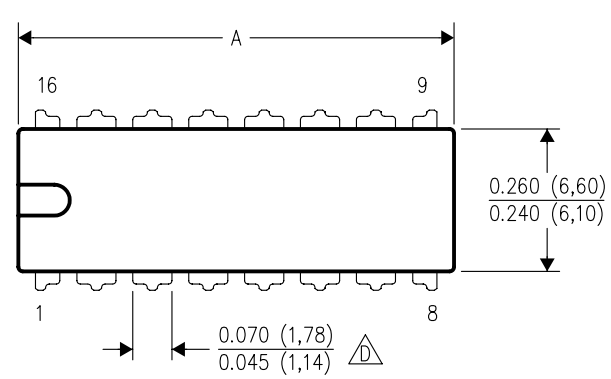
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

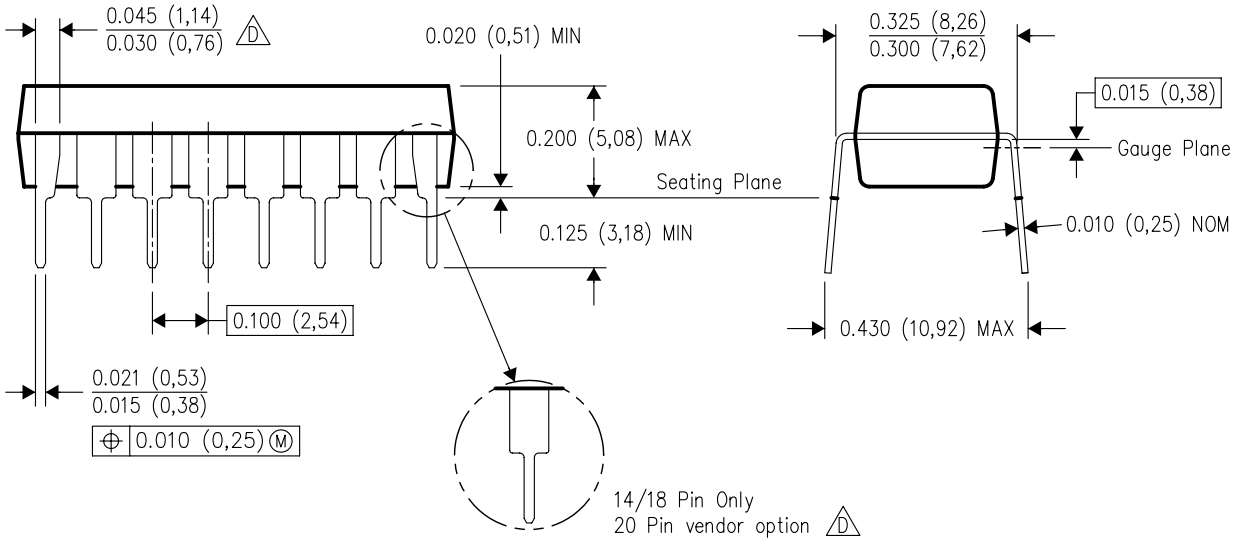
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

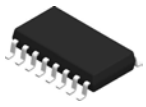


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

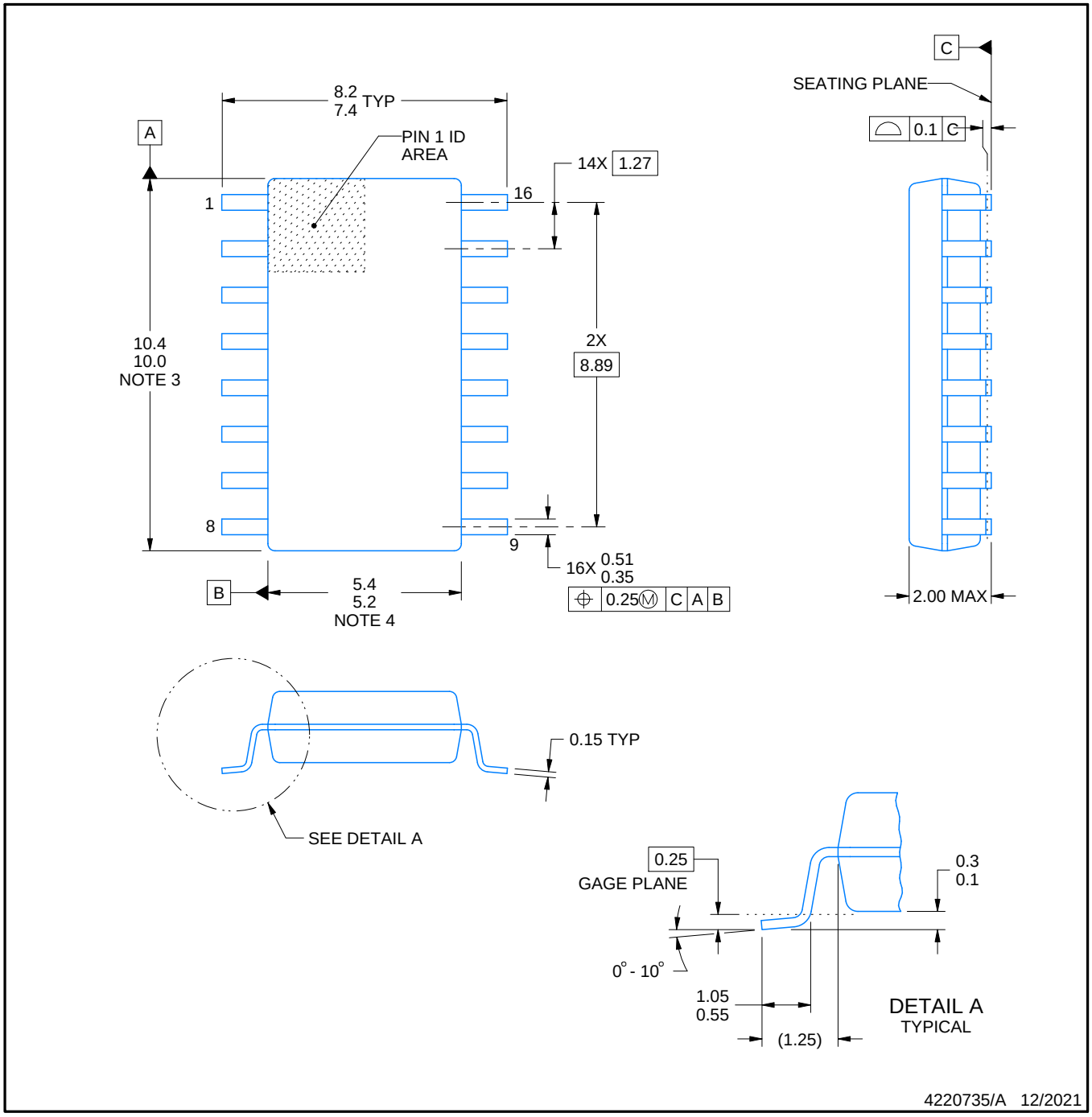


PACKAGE OUTLINE

NS0016A

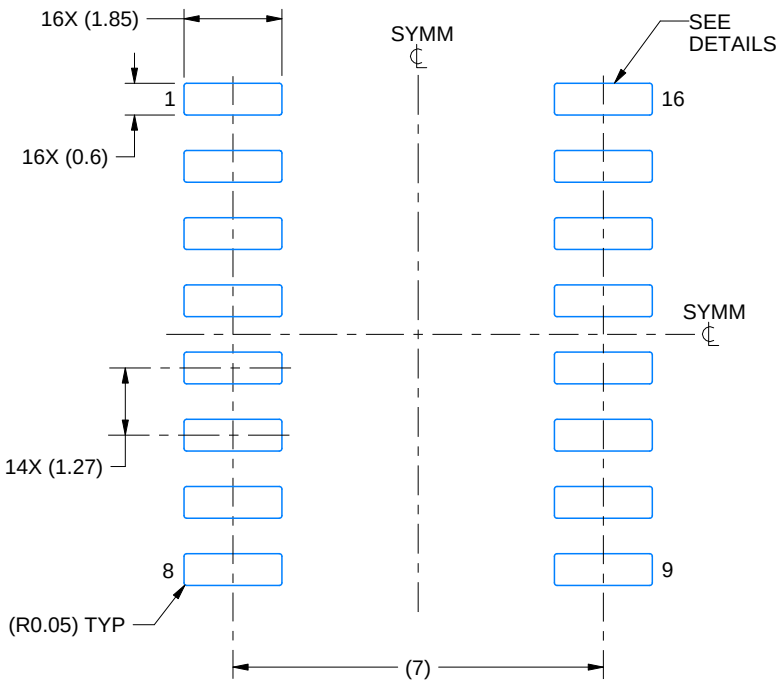
SOP - 2.00 mm max height

SOP

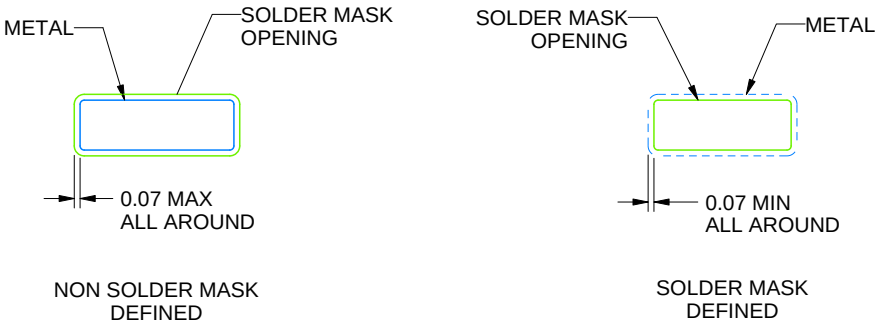


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X



NON SOLDER MASK
DEFINED

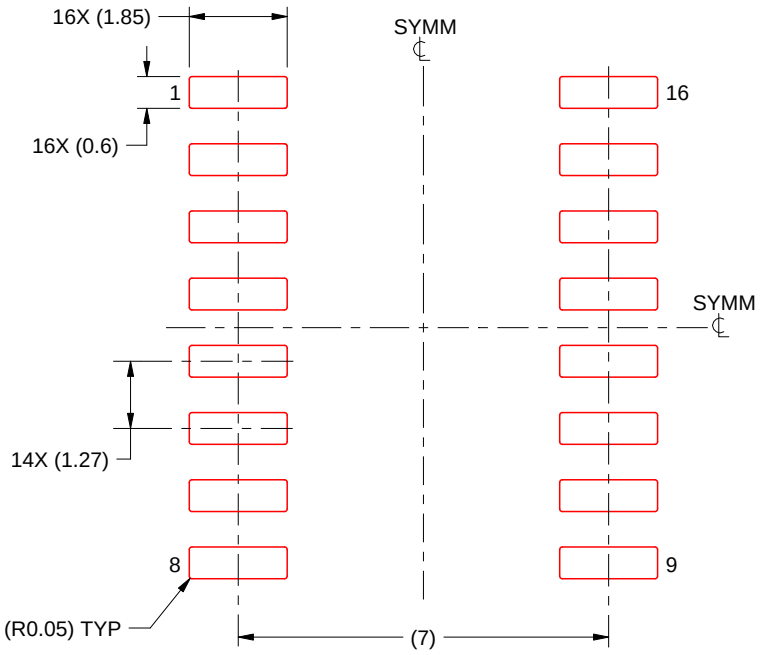
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



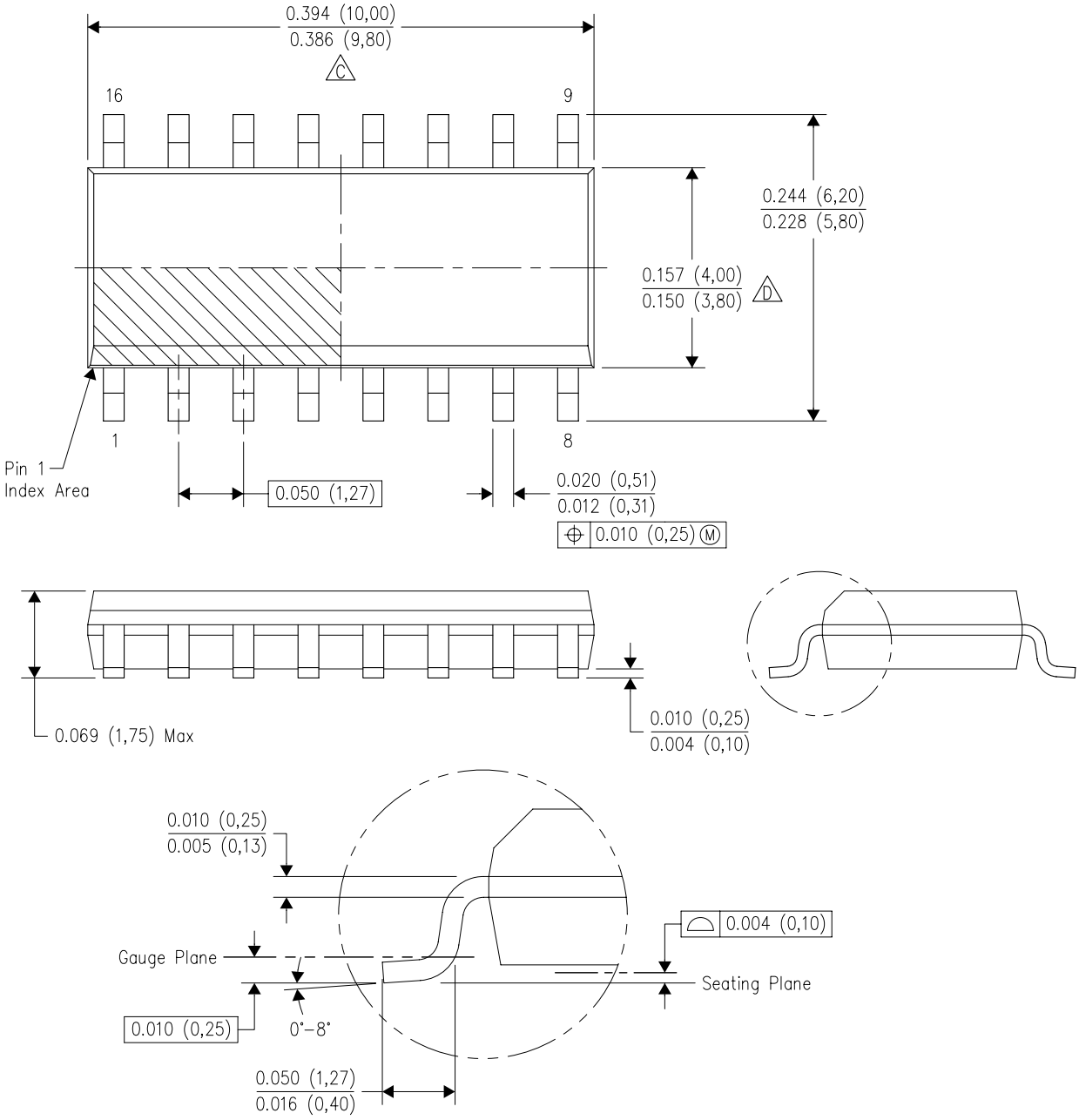
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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