

SN54LS595, SN54LS596, SN74LS595, SN74LS596 8-BIT SHIFT REGISTERS WITH OUTPUT LATCHES

SDLS006

D2634, JANUARY 1981 (REVISED MARCH 1988)

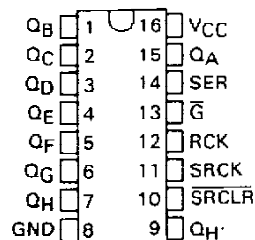
- 8-Bit Serial-In, Parallel-Out Shift Registers with Storage
- Choice of 3-State ('LS595) or Open-Collector ('LS596) Parallel Outputs
- Shift Register Has Direct Clear
- Accurate Shift Frequency: DC to 20 MHz

description

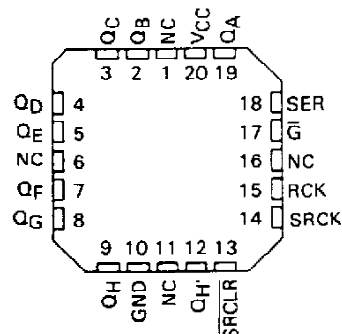
These devices each contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state ('LS595) or open-collector ('LS596) outputs. Separate clocks are provided for both the shift register and the storage register. The shift register has a direct-overriding clear, serial input, and serial output pins for cascading.

Both the shift register and storage register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the shift register state will always be one clock pulse ahead of the storage register.

SN54LS595, SN54LS596 . . . J OR W PACKAGE
SN74LS595, SN74LS596 . . . N PACKAGE
(TOP VIEW)

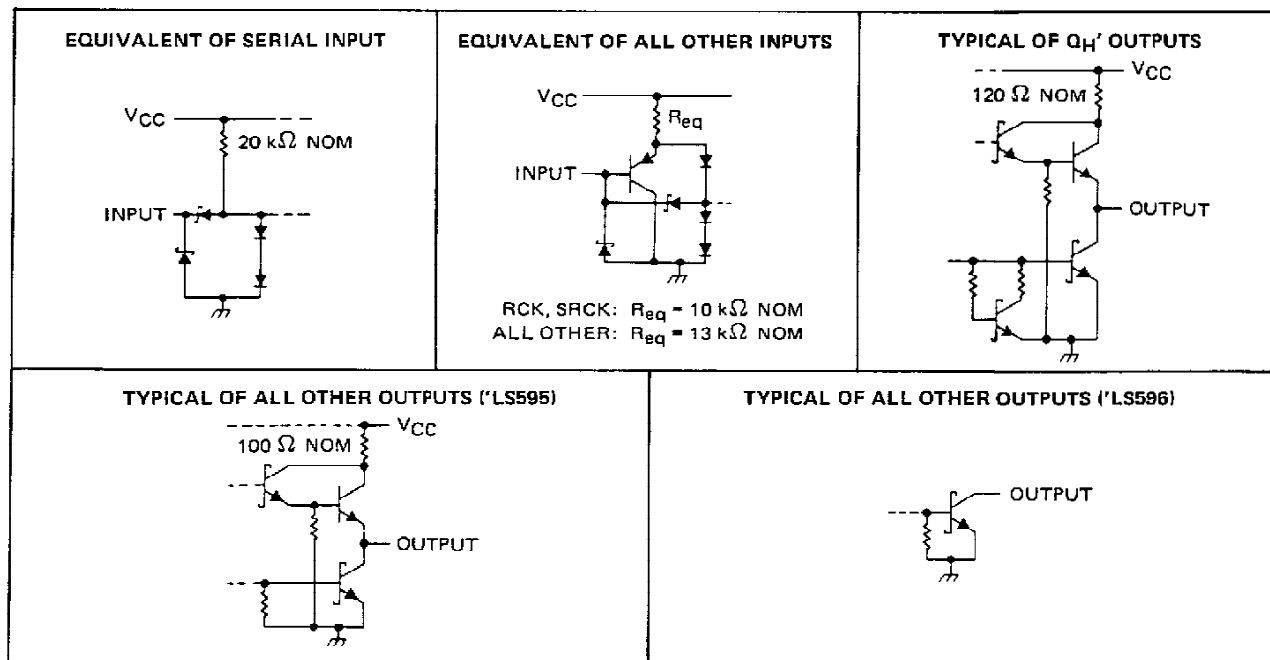


SN54LS595, SN54LS596 . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

schematics of inputs and outputs



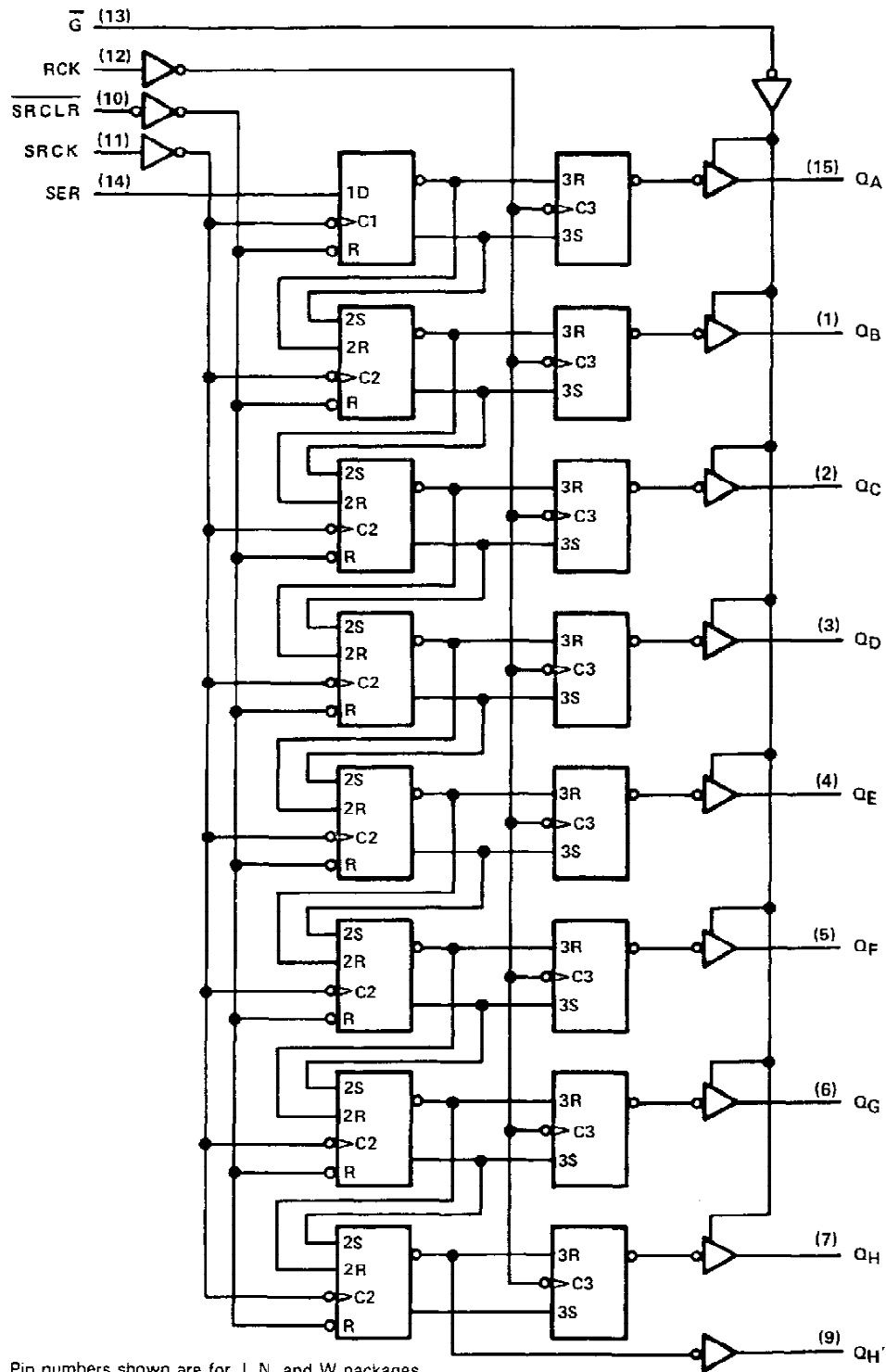
PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SN54LS595, SN54LS596, SN74LS595, SN74LS596 **8-BIT SHIFT REGISTERS WITH OUTPUT LATCHES**

logic diagram (positive logic)



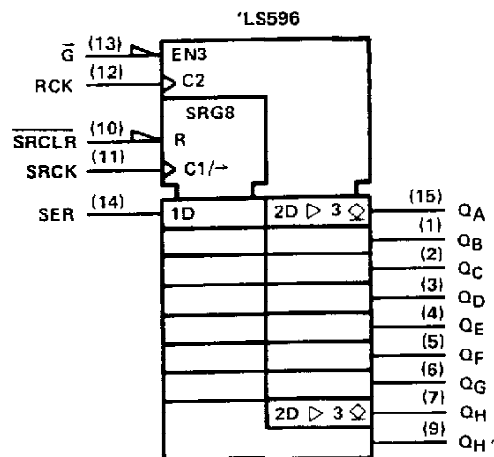
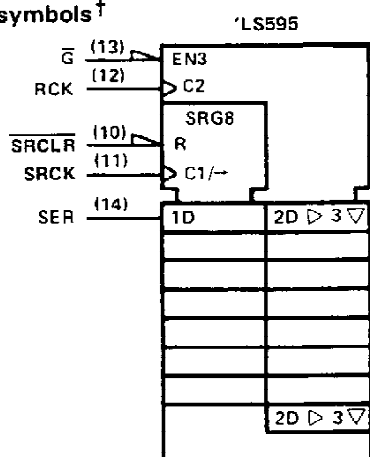
Pin numbers shown are for J, N, and W packages.

TEXAS
INSTRUMENTS

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SN54LS595, SN54LS596, SN74LS595, SN74LS596 8-BIT SHIFT REGISTERS WITH OUTPUT LATCHES

logic symbols†



†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for J, N, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS595, SN54LS596	–55°C to 125°C
SN74LS595, SN74LS596	0°C to 70°C
Storage temperature range	–65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
V_{OH}	High-level output voltage	Q_A thru Q_H , 'LS596 only		5.5			5.5	V
I_{OH}	High-level output current	Q_H'		–1			–1	mA
		Q_A thru Q_H , 'LS595 only		–1			–2.6	
I_{OL}	Low-level output current	Q_H'		8			16	mA
		Q		12			24	
f_{SRCK}	Shift clock frequency	0		20	0		20	MHz
$t_w(SRCK)$	Duration of shift clock pulse	25			25			ns
$t_w(RCK)$	Duration of register clock pulse	20			20			ns
$t_w(SRCLR)$	Duration of shift clear pulse, low level	20			20			ns
t_{SU}	Setup time	SRCLR inactive before SRCK ↑		20				ns
		SER before SRCK ↑		20				
		SRCK ↑ before RCK ↑ (see Note 2)		40			40	
		SRCLR low before RCK ↑		40			40	
t_H	Hold time	SER after SRCK ↑		0			0	ns
T_A	Operating free-air temperature	–55		125	0		70	°C

NOTE 2: This setup time ensures the register will see stable data from the shift-register outputs. The clocks may be connected together, in which case the storage register state will be one clock pulse behind the shift register.

TEXAS
INSTRUMENTS

POST OFFICE BOX 855012 • DALLAS, TEXAS 75285

SN54LS595, SN54LS596, SN74LS595, SN74LS596
8-BIT SHIFT REGISTERS WITH OUTPUT LATCHES

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS †	SN54LS*		SN74LS*		UNIT		
			MIN	TYP‡	MAX	MIN		TYP‡	MAX
V _{IK}		V _{CC} = MIN, I _I = - 18 mA			- 1.5		- 1.5	V	
V _{OH}	'LS595 Q	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX	I _{OH} = - 1 mA		2.4	3.2		V	
	I _{OH} = - 2.6 mA			2.4	3.1				
	Q _H '		I _{OH} = - 1 mA		2.4	3.2	2.4		3.2
I _{OH}	'LS596 Q	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX, V _{OH} = 5.5 V			0.1		0.1	mA	
V _{OL}	Q	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX	I _{OL} = 12 mA		0.25	0.4	0.25	0.4	V
			I _{OL} = 24 mA				0.35	0.5	
			I _{OL} = 8 mA		0.25	0.4	0.25	0.4	
	Q _H '		I _{OL} = 16 mA				0.35	0.5	
I _{OZH}	'LS595 Q	V _{CC} = MAX, V _{IH} = 2 V, V _{IL} = MAX, V _{OH} = 2.7 V			20		20	μA	
I _{OZL}	'LS595 Q	V _{CC} = MAX, V _{IH} = 2 V, V _{IL} = MAX, V _{OH} = 0.4 V			- 20		- 20	μA	
I _I		V _{CC} = MAX, V _I = 7 V			0.1		0.1	mA	
I _{IH}		V _{CC} = MAX, V _I = 2.7 V			20		20	μA	
I _{IL}	SER	V _{CC} = MAX, V _I = 0.4 V			- 0.4		- 0.4	mA	
	All others				- 0.2		- 0.2		
I _{OS} §	'LS595 Q	V _{CC} = MAX, V _O = 0 V	- 30		- 130	- 30		- 130	mA
	Q _H '		- 20		- 100	- 20		- 100	
I _{CCH}	'LS595	V _{CC} = MAX, All possible inputs grounded, All outputs open	33		50	33		50	mA
	'LS596		30		45	30		45	
I _{CCL}	'LS595		42		65	42		65	mA
	'LS596		36		55	36		55	
I _{CCZ}	'LS595		44		65	44		65	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

TEXAS
INSTRUMENTS

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SN54LS595, SN54LS596, SN74LS595, SN74LS596
8-BIT SHIFT REGISTERS WITH OUTPUT LATCHES

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS595			'LS596			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	SRCK $\uparrow$	Q_H'	$R_L = 1\text{ k}\Omega$, $C_L = 30\text{ pF}$		12	18		14	21	ns
t_{PHL}					17	25		20	30	ns
t_{PLH}	RCK $\uparrow$	Q_A thru Q_H	$R_L = 667\ \Omega$, $C_L = 45\text{ pF}$		12	18		28	42	ns
t_{PHL}					24	35		24	35	ns
t_{PZH}	$\overline{G} \downarrow$	Q_A thru Q_H			20	30				ns
t_{PZL}					25	38				ns
t_{PHZ}	$\overline{G} \uparrow$	Q_A thru Q_H	$R_L = 667\ \Omega$, $C_L = 5\text{ pF}$		20	30				ns
t_{PLZ}					25	38				ns
t_{PLH}	$\overline{G} \uparrow$	Q_A thru Q_H	$R_L = 667\ \Omega$, $C_L = 45\text{ pF}$					40	60	ns
t_{PHL}	$\overline{G} \downarrow$	Q_A thru Q_H						25	38	ns
t_{PHL}	SRCLR $\downarrow$	Q_H'	$R_L = 1\text{ k}\Omega$, $C_L = 30\text{ pF}$		24	35		24	35	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

TEXAS
INSTRUMENTS

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-8671701EA	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8671701EA SNJ54LS595J
5962-8671701FA	Active	Production	CFP (W) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8671701FA SNJ54LS595W
5962-8671701FA	Active	Production	CFP (W) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8671701FA SNJ54LS595W
SN54LS595J	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS595J
SN54LS595J	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS595J
SN54LS595J.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS595J
SN54LS595J.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54LS595J
SN74LS595D	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	0 to 70	LS595
SN74LS595D	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	0 to 70	LS595
SN74LS595DR	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS595
SN74LS595DR	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS595
SN74LS595DR.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS595
SN74LS595DR.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS595
SN74LS595N	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS595N
SN74LS595N	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS595N
SN74LS595N.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS595N
SN74LS595N.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74LS595N
SNJ54LS595J	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8671701EA SNJ54LS595J
SNJ54LS595J	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8671701EA SNJ54LS595J
SNJ54LS595J.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8671701EA SNJ54LS595J
SNJ54LS595J.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8671701EA SNJ54LS595J
SNJ54LS595W	Active	Production	CFP (W) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8671701FA SNJ54LS595W

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SNJ54LS595W	Active	Production	CFP (W) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8671701FA SNJ54LS595W
SNJ54LS595W.A	Active	Production	CFP (W) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8671701FA SNJ54LS595W
SNJ54LS595W.A	Active	Production	CFP (W) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8671701FA SNJ54LS595W

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

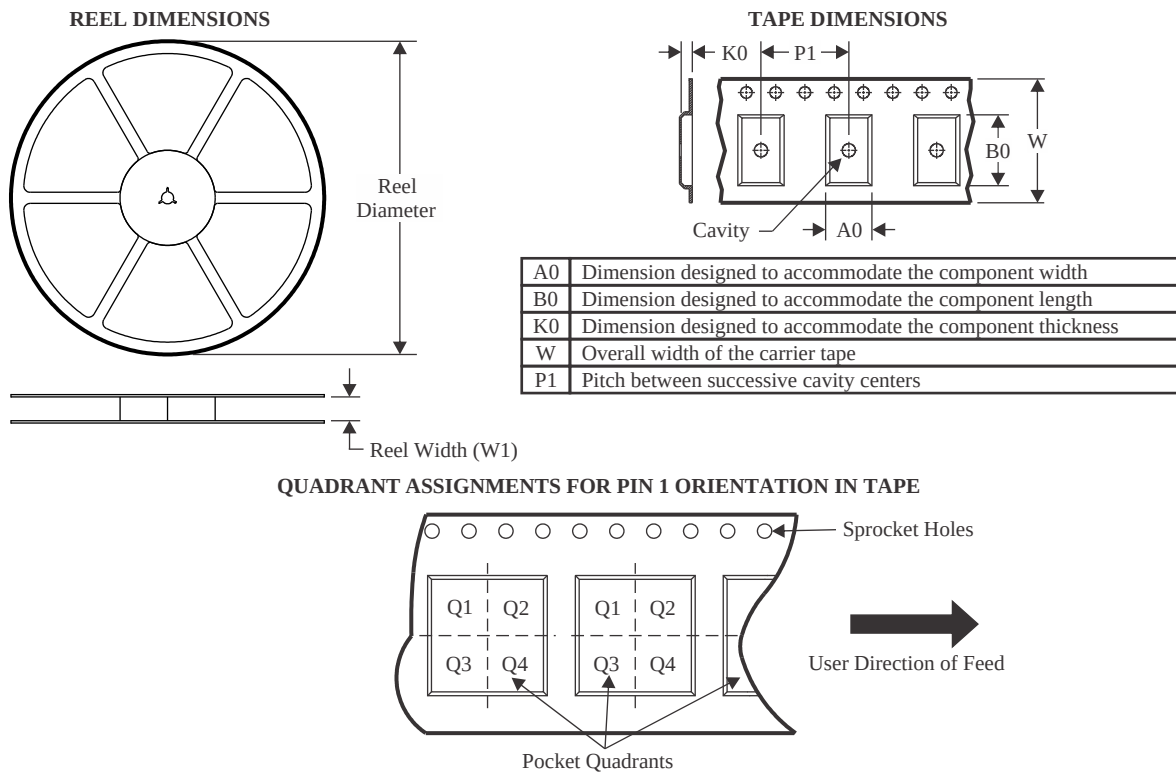
OTHER QUALIFIED VERSIONS OF SN54LS595, SN74LS595 :

- Catalog : [SN74LS595](#)
- Military : [SN54LS595](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

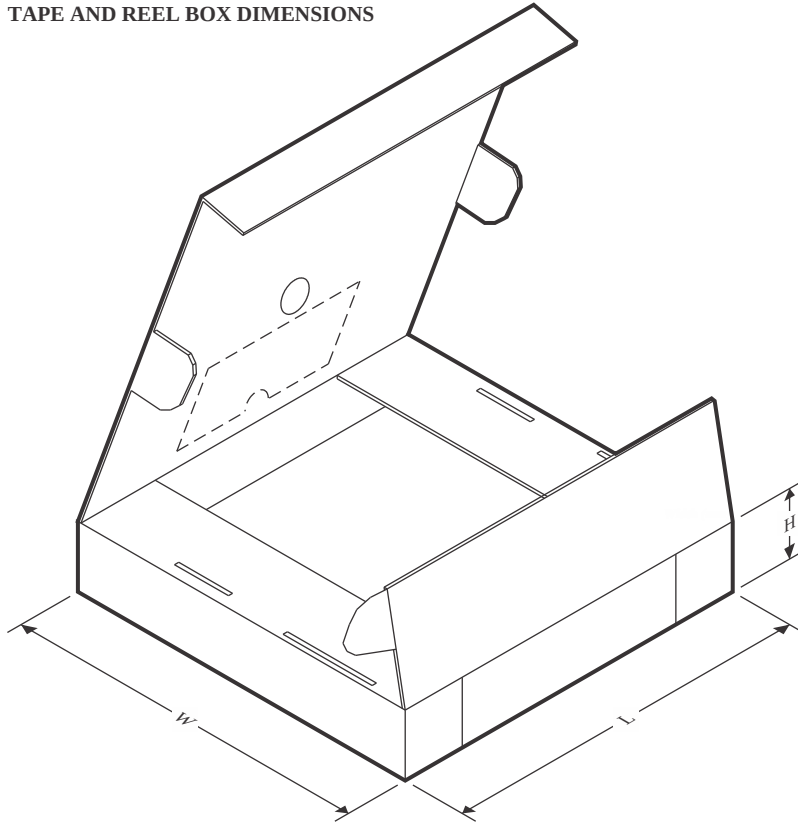
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS595DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

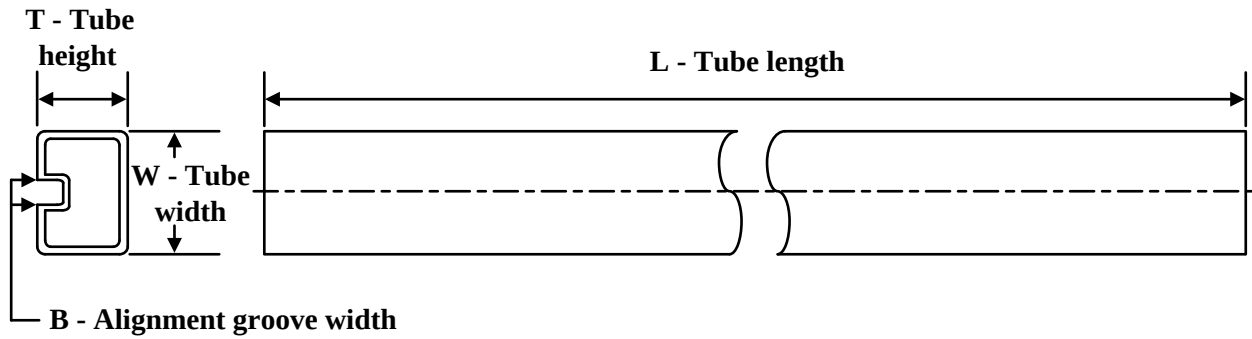
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS595DR	SOIC	D	16	2500	340.5	336.1	32.0

TUBE

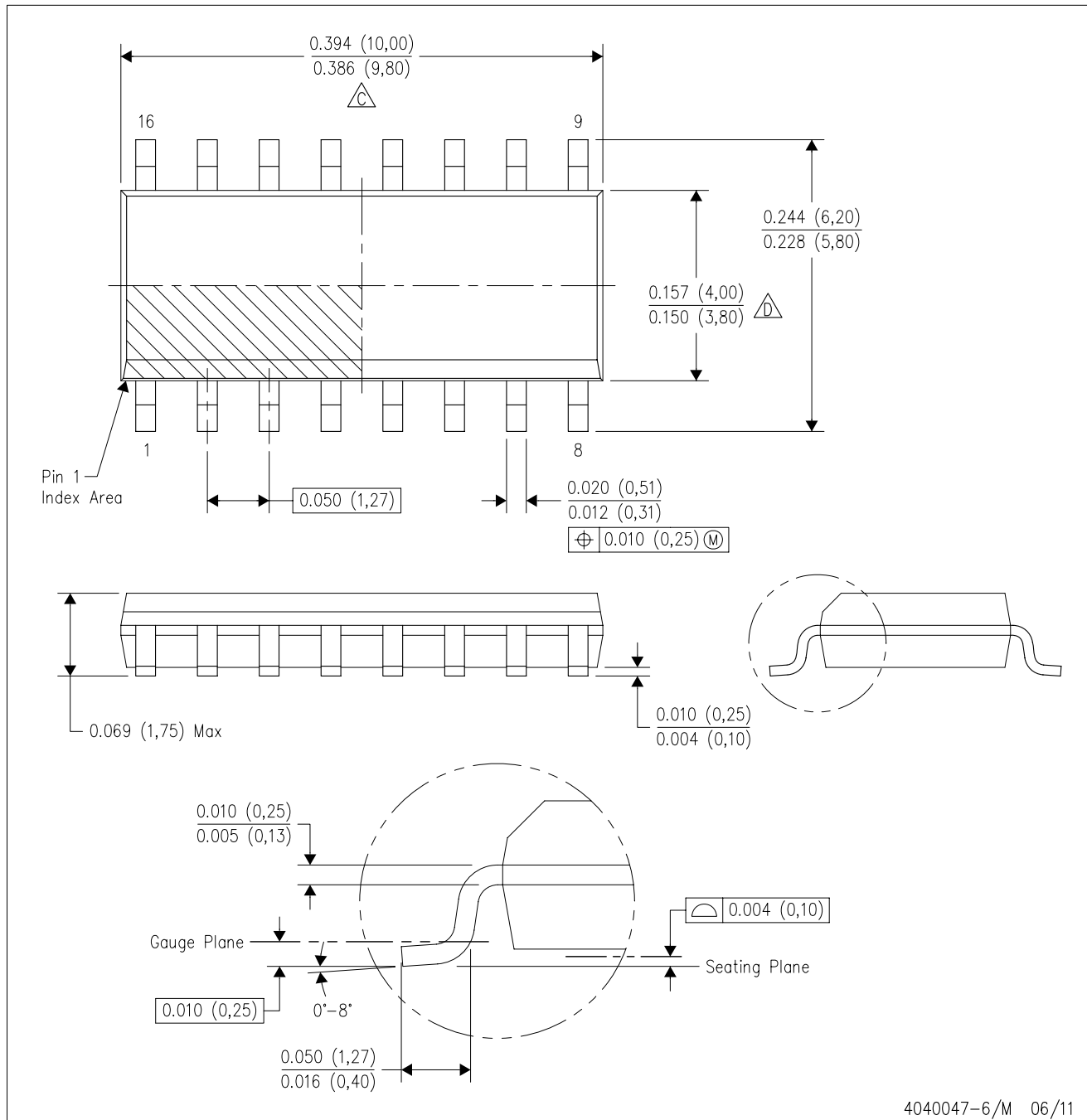


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-8671701FA	W	CFP	16	25	506.98	26.16	6220	NA
SN74LS595N	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS595N	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS595N.A	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS595N.A	N	PDIP	16	25	506	13.97	11230	4.32
SNJ54LS595W	W	CFP	16	25	506.98	26.16	6220	NA
SNJ54LS595W.A	W	CFP	16	25	506.98	26.16	6220	NA

D (R-PDSO-G16)

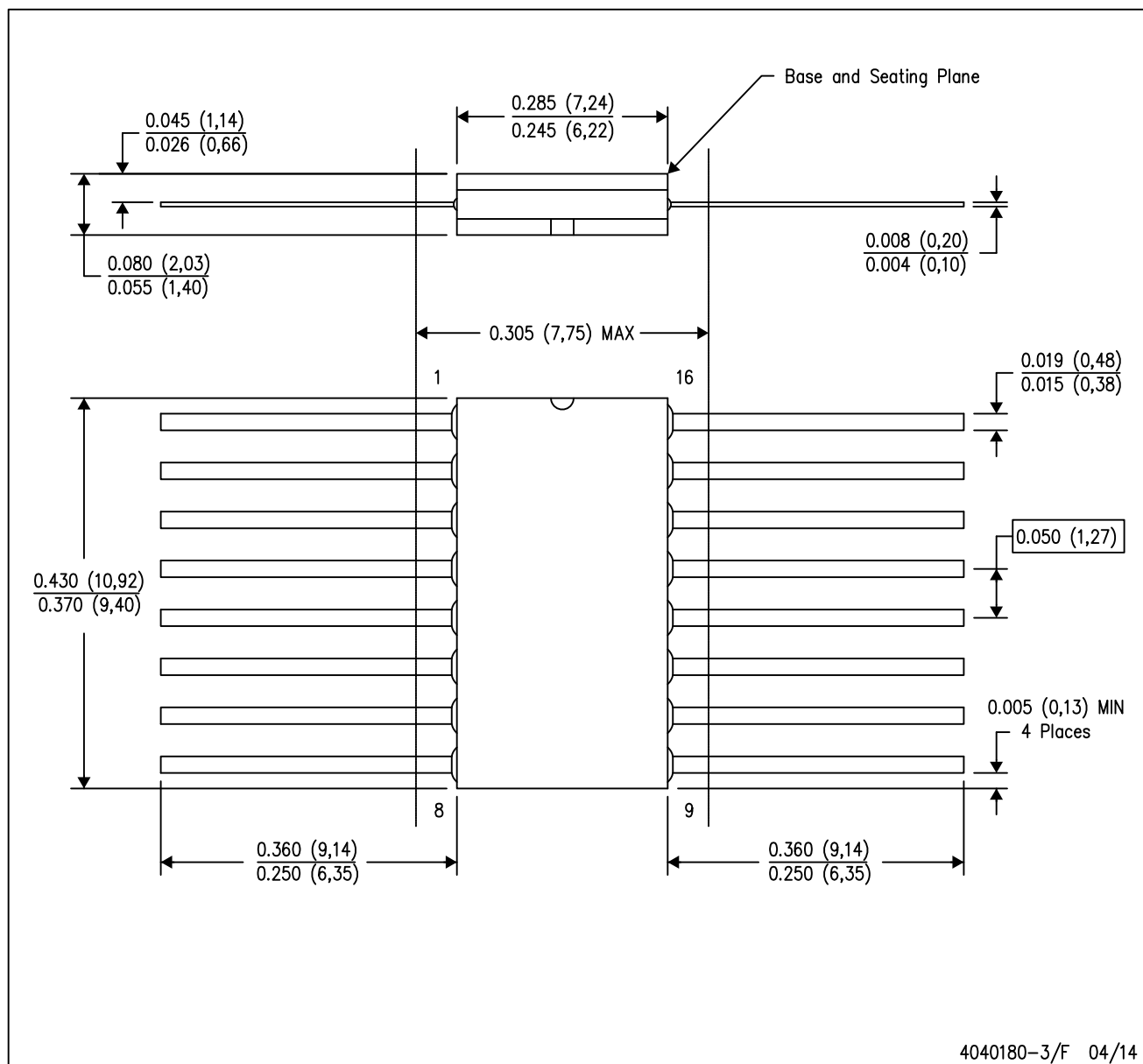
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

W (R-GDFP-F16)

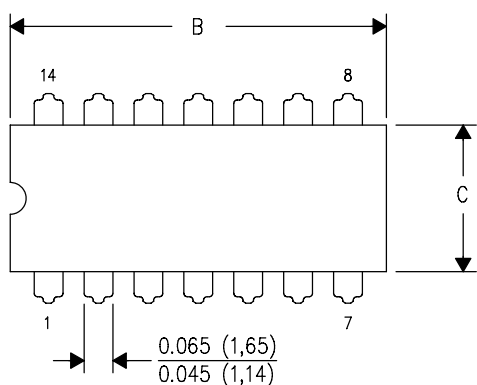
CERAMIC DUAL FLATPACK



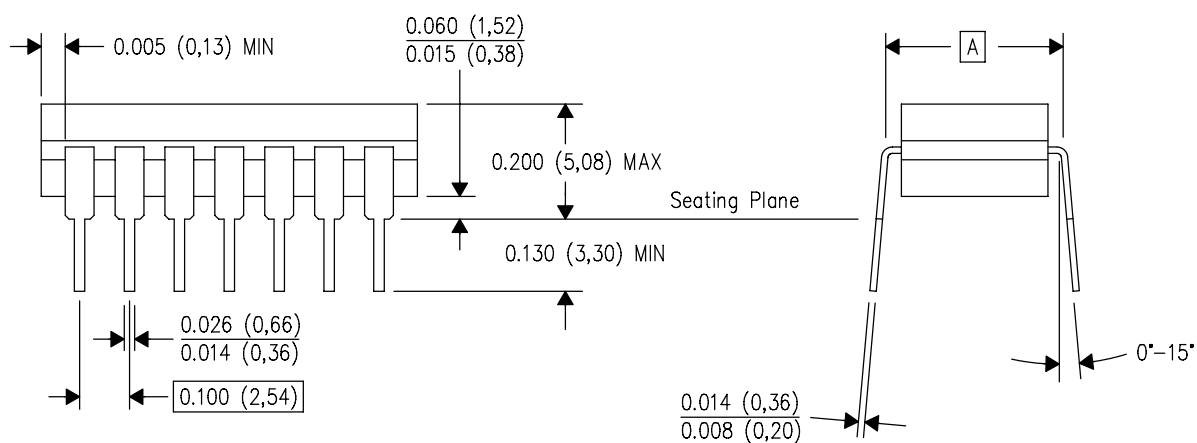
- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only.
 - Falls within MIL STD 1835 GDFP2-F16

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

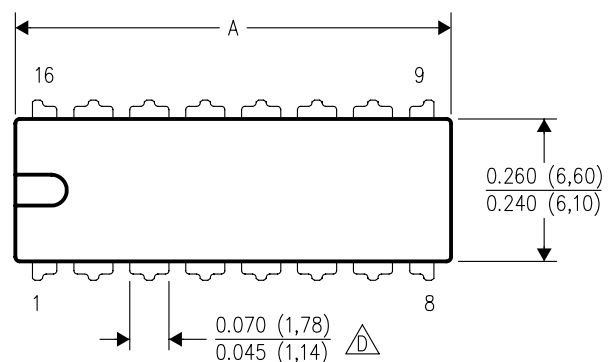
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

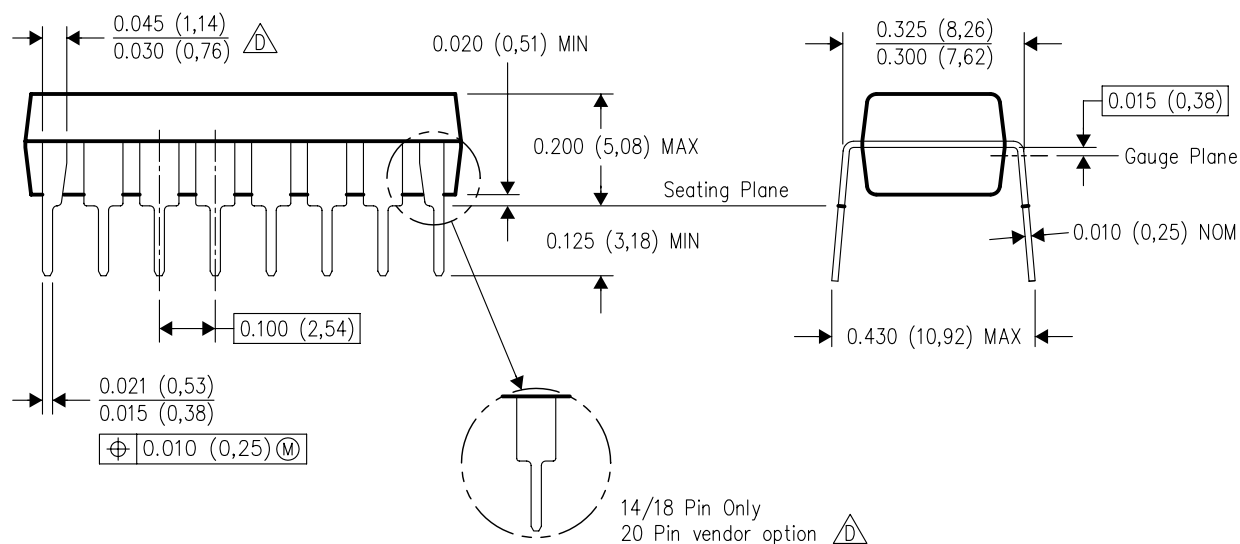
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025