

SN65LBC170, SN75LBC170 TRIPLE DIFFERENTIAL TRANSCEIVERS

SLLS459C – NOVEMBER 2000 – REVISED MARCH 2005

- Three Differential Transceivers in One Package
- Signaling Rates[†] Up to 30 Mbps
- Low Power and High Speed
- Designed for TIA/EIA-485, TIA/EIA-422, ISO 8482, and ANSI X3.277 (HVD SCSI Fast-20) Applications
- Common-Mode Bus Voltage Range –7 V to 12 V
- ESD Protection on Bus Terminals Exceeds 12 kV
- Driver Output Current up to ± 60 mA
- Thermal Shutdown Protection
- Driver Positive and Negative Current Limiting
- Power-Up, Power-Down Glitch-Free Operation
- Pin-Compatible With the SN75ALS170
- Available in Shrink Small-Outline Package

description

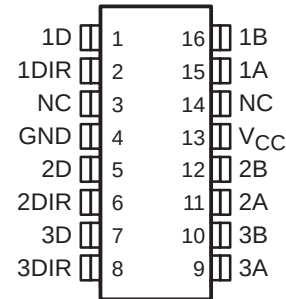
The SN65LBC170 and SN75LBC170 are monolithic integrated circuits designed for bidirectional data communication on multipoint bus-transmission lines. Potential applications include serial or parallel data transmission, cabled peripheral buses with twin axial, ribbon, or twisted-pair cabling. These devices are suitable for FAST-20 SCSI and can transmit or receive data pulses as short as 25 ns, with skew less than 3 ns.

These devices combine three 3-state differential line drivers and three differential input line receivers, all of which operate from a single 5-V power supply.

The driver differential outputs and the receiver differential inputs are connected internally to form three differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus whenever the driver is disabled or $V_{CC} = 0$. These ports feature a wide common-mode voltage range making the device suitable for party-line applications over long cable runs.

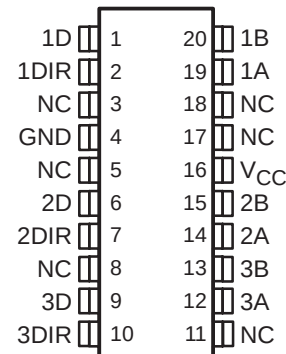
SN65LBC170DB (marked as BL170)
SN75LBC170DB (marked as BL170)

(TOP VIEW)



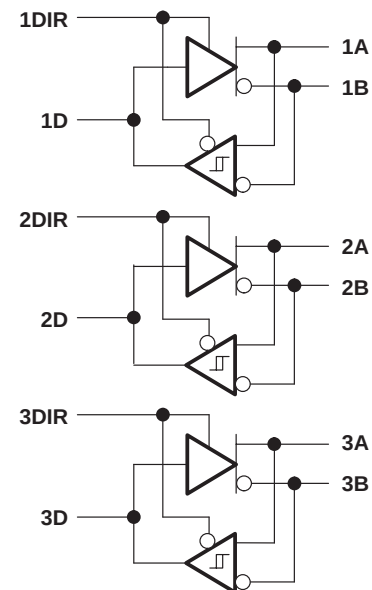
SN65LBC170DW (marked as 65LBC170)
SN75LBC170DW (marked as 75LBC170)

(TOP VIEW)



NC – No internal connection

logic diagram



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

[†]The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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SN65LBC170, SN75LBC170

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description (continued)

The driver's active-high enable and the receiver's active-low enable are tied together internally and provide a direction input for each driver/receiver pair.

The SN75LBC170 is characterized for operation over the temperature range of 0°C to 70°C. The SN65LBC170 is characterized for operation over the temperature range of -40°C to 85°C.

AVAILABLE OPTIONS†

T _A	PACKAGE	
	PLASTIC SHRINK SMALL-OUTLINE (JEDEC MO-150)	PLASTIC SMALL-OUTLINE (JEDEC MS-013)
0°C to 70°C	SN75LBC170DB	SN75LBC170DW
-40°C to 85°C	SN65LBC170DB	SN65LBC170DW

† Add R suffix for taped and reel

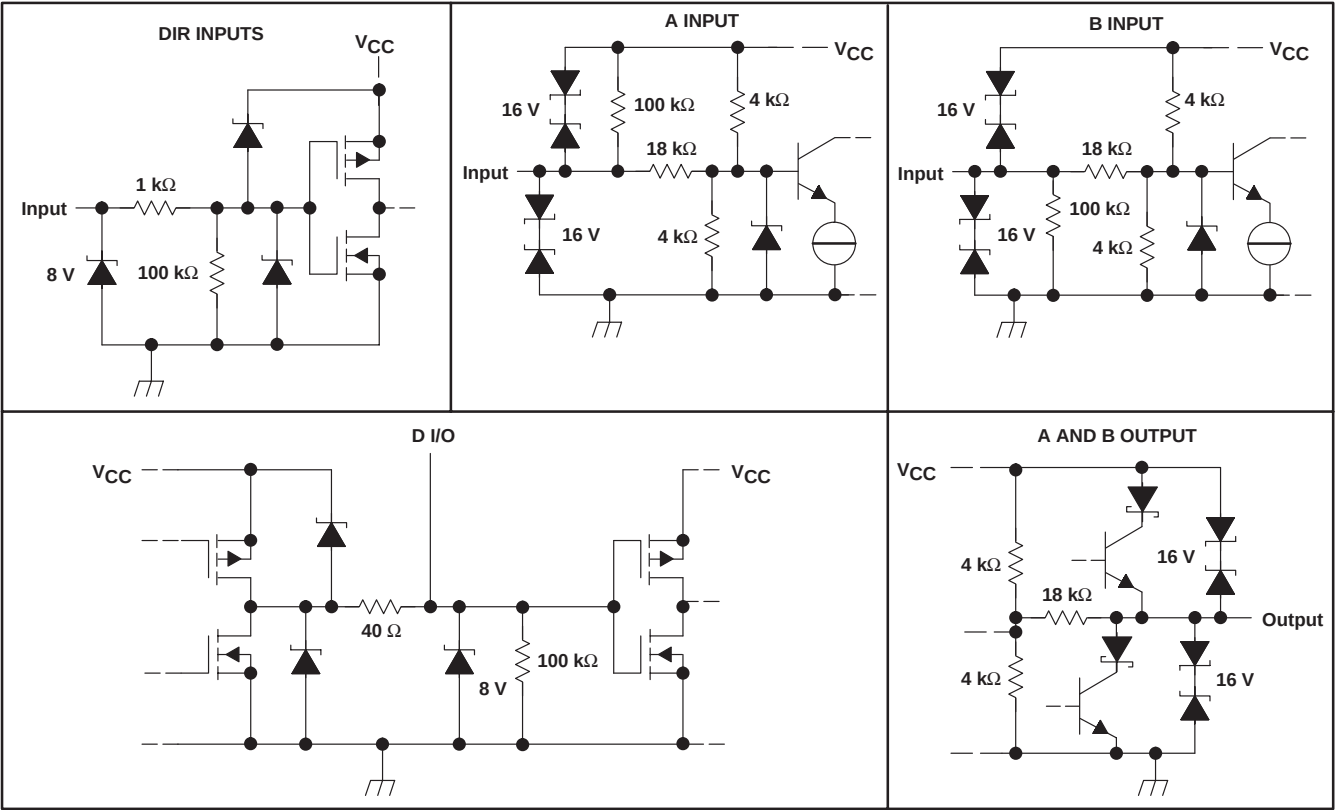
† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

Function Tables

EACH DRIVER			EACH RECEIVER		
INPUT D	ENABLE DIR	OUTPUTS	DIFFERENTIAL INPUT (V _A -V _B)	ENABLE DIR	OUTPUT D
		A B			
H	H	H L	V _{ID} ≥ 0.2 V	L	H
L	H	L H	-0.2 V < V _{ID} < 0.2 V	L	?
OPEN	H	L H	V _{ID} ≤ -0.2 V	L	L
X	L	Z Z	X	H	Z
X	OPEN	X X	OPEN	L	H

H = high level, L = low level, X = irrelevant, Z = high impedance (off), ? = indeterminate

equivalent input and output schematic diagrams



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absolute maximum ratings[†] over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	–0.3 V to 6 V
Voltage range at any bus I/O terminal (steady state)	–10 V to 15 V
Voltage input range, A and B, (transient pulse through 100 Ω , see Figure 12)	–30 V to 30 V
Voltage range at any D or DIR terminal	–0.5 V to $V_{CC} + 0.5$ V
Receiver output current, I_O	± 10 mA
Electrostatic discharge: Human body model (A, B, GND) (see Note 2)	12 kV
All pins	5 kV
Charged-device model (all pins) (see Note 3)	1 kV
Continuous total power dissipation	See Power Dissipation Rating Table

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
2. Tested in accordance with JEDEC Standard 22, Test Method A114–A.
3. Tested in accordance with JEDEC Standard 22, Test Method C101.

POWER DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR [‡] ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
DB	995 mW	8.0 mW/ $^\circ\text{C}$	635 mW	515 mW
DW	1480 mW	11.8 mW/ $^\circ\text{C}$	950 mW	770 mW

[‡] This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V _{CC}		4.75	5	5.25	V
Voltage at any bus I/O terminal	A, B	−7		12	V
High-level input voltage, V _{IH}	D, DIR	2	V _{CC}		V
Low-level input voltage, V _{IL}		0	0.8		
Differential input voltage, V _{ID}	A with respect to B	−12		12	V
Output current	Driver	−60		60	mA
	Receiver	−8		8	
Operating free-air temperature, T _A	SN75LBC170	0		70	°C
	SN65LBC170	−40		85	



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DRIVER SECTION

electrical characteristics over recommended operating conditions

PARAMETER			TEST CONDITIONS		MIN	TYP [†]	MAX	UNIT
V _{IK}	Input clamp voltage	D and DIR	I _I = 18 mA		-1.5	-0.7		V
V _O	Open-circuit output voltage (single-ended)		A or B, No load		0		V _{CC}	V
V _{OD(SS)}	Steady-state differential output voltage magnitude [‡]		No load		3.8	4.3	V _{CC}	V
			R _L = 54 Ω, See Figure 1		1	1.6	2.4	
			With common-mode loading, See Figure 2		1	1.6	2.4	
ΔV _{OD}	Change in differential output voltage magnitude, V _{OD(H)} – V _{OD(L)}		R _L = 54 Ω, C _L = 50 pF	See Figure 1	-0.2		0.2	V
V _{OC(SS)}	Steady-state common-mode output voltage				2		2.4	
ΔV _{OC(SS)}	Change in steady-state common-mode output voltage (V _{OC(H)} – V _{OC(L)})						-0.2	
I _I	Input current		D, DIR		-100		100	μA
I _O	Output current with power off		V _{CC} = 0 V, V _O = -7 V to 12 V		-700		900	μA
I _{OS}	Short-circuit output current		V _O = -7 V to 12 V, See Figure 7		-250		250	mA
I _{CC}	Supply current (driver enabled)		D at 0 V or V _{CC} , DIR at V _{CC} , No load		14		20	mA

[†] All typical values are at V_{CC} = 5 V and T_A = 25°C.

[‡] The minimum V_{OD} may not fully comply with TIA/EIA-485-A at operating temperatures below 0°C. System designers should take the possibly lower output signal into account in determining the maximum signal-transmission distance.

switching characteristics over recommended operating conditions

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
t _{PLH}	Differential output propagation delay, low-to-high		R _L = 54 Ω, C _L = 50 pF, See Figure 3		4	8.5	12	ns
t _{PHL}	Differential output propagation delay, high-to-low				4	8.5	11	
t _r	Differential output rise time				3	7.5	11	
t _f	Differential output fall time				3	7.5	11	
t _{sk(p)}	Pulse skew (t _{PLH} - t _{PHL})						2	
t _{sk(o)}	Output skew [§]						1.5	
t _{sk(pp)}	Part-to-part skew [¶]						2	
t _{PLH}	Differential output propagation delay, low-to-high		See Figure 4, (HVD SCSI double-terminated load)		3	7	10	ns
t _{PHL}	Differential output propagation delay, high-to-low				3	7.5	10	
t _r	Differential output rise time				3	7.5	12	
t _f	Differential output fall time				3	7.5	12	
t _{sk(p)}	Pulse skew (t _{PLH} - t _{PHL})						3	
t _{sk(o)}	Output skew [§]						1.5	
t _{sk(pp)}	Part-to-part skew [¶]						2.5	
t _{pZH}	Output enable time to high level		See Figure 5			15	25	ns
t _{pHZ}	Output disable time from high level					18	25	
t _{pZL}	Output enable time to low level		See Figure 6			10	25	ns
t _{pLZ}	Output disable time from low level					17	25	

[§] Output skew (t_{sk(o)}) is the magnitude of the time delay difference between the outputs of a single device with all of the inputs connected together.

[¶] Part-to-part skew (t_{sk(pp)}) is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same input signals, the same supply voltages, at the same temperature, and have identical packages and test circuits.

RECEIVER SECTION

electrical characteristics over recommended operating conditions

PARAMETER	TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT
V _{IT+} Positive-going differential input voltage threshold	See Figure 8			0.2	V
V _{IT-} Negative-going differential input voltage threshold		-0.2			
V _{hys} Hysteresis voltage (V _{IT+} - V _{IT-})			40		mV
V _{OH} High-level output voltage	V _{ID} = 200 mV, I _{OH} = -8 mA, See Figure 8	4	4.7	V _{CC}	V
V _{OL} Low-level output voltage	V _{ID} = -200 mV, I _{OL} = -8 mA, See Figure 8	0	0.2	0.4	
I _I Line input current	Other input = 0 V	V _I = 12 V		0.9	mA
		V _I = -7 V		-0.7	
R _I Input resistance	A, B	12			kΩ
I _{CC} Supply current (receiver enabled)	A, B, D, and DIR open			16	mA

[†] All typical values are at V_{CC} = 5 V and T_A = 25°C.

switching characteristics over recommended operating conditions

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH} Propagation delay time, low-to-high level output	See Figure 9	7		16	ns
t _{PHL} Propagation delay time, high-to-low level output		7		16	ns
t _r Receiver output rise time			1.3	3	ns
t _f Receiver output fall time			1.3	3	ns
t _{PZH} Receiver output enable time to high level	See Figure 10		26	40	ns
t _{PHZ} Receiver output disable time from high level				40	
t _{PZL} Receiver output enable time to low level	See Figure 11		29	40	ns
t _{PLZ} Receiver output enable time to high level				40	
t _{sk(p)} Pulse skew (t _{PLH} - t _{PHL})				2	ns
t _{sk(o)} Output skew [‡]				1.5	ns
t _{sk(pp)} Part-to-part skew [§]				3	ns

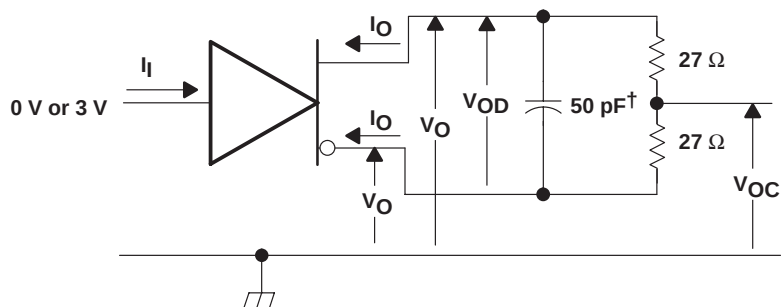
[‡] Output skew (t_{sk(o)}) is the magnitude of the time delay difference between the outputs of a single device with all of the inputs connected together.

[§] Part-to-part skew (t_{sk(pp)}) is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same input signals, the same supply voltages, at the same temperature, and have identical packages and test circuits.

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PARAMETER MEASUREMENT INFORMATION



† Includes probe and jig capacitance

Figure 1. Driver Test Circuit, V_{OD} and V_{OC} Without Common-Mode Loading

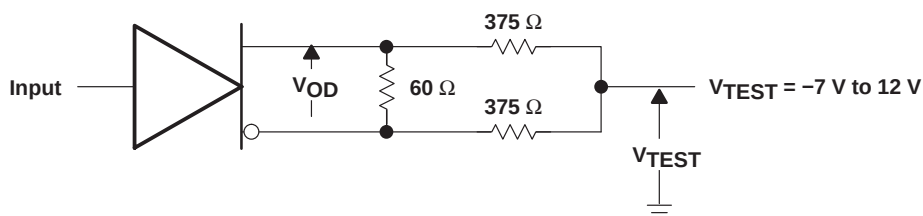
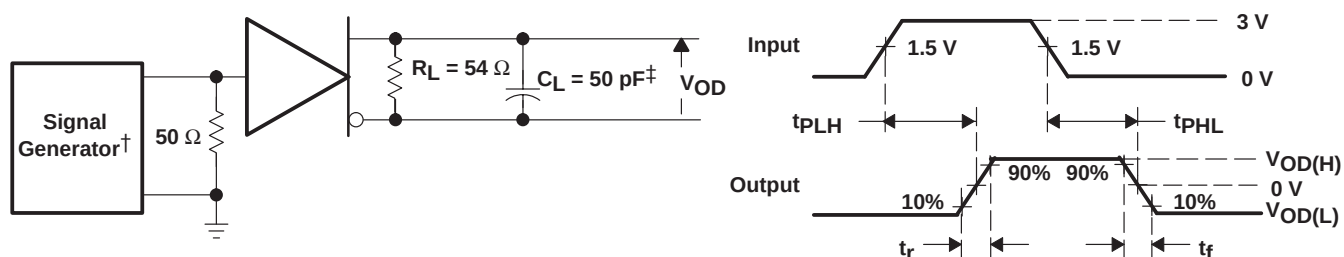


Figure 2. Driver Test Circuit, V_{OD} With Common-Mode Loading

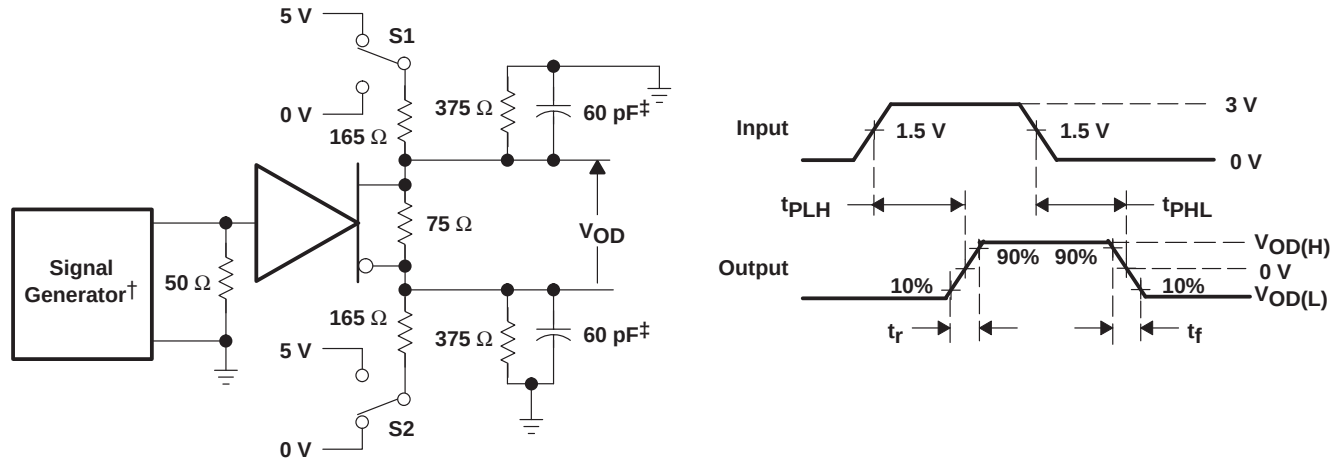


† PRR = 1 MHz, 50% Duty Cycle, $t_r < 6$ ns, $t_f < 6$ ns, $Z_0 = 50 \Omega$

‡ Includes probe and jig capacitance

Figure 3. Driver Switching Test Circuit and Waveforms, 485-Loading

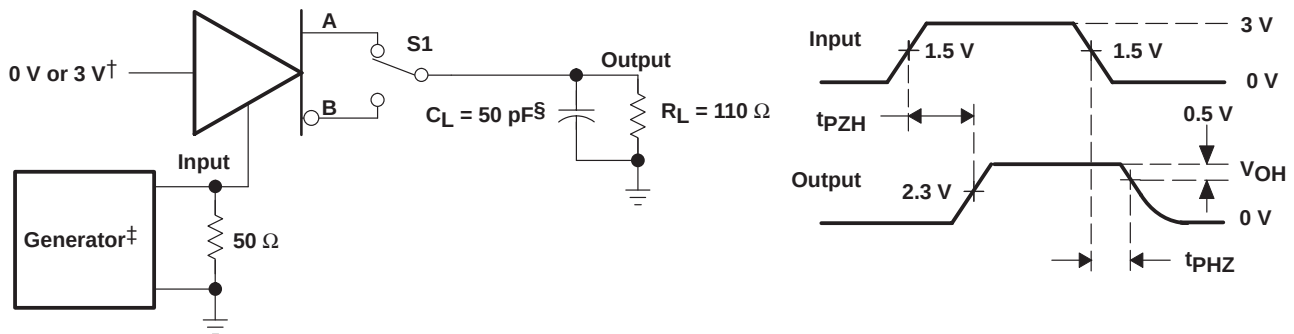
PARAMETER MEASUREMENT INFORMATION



† PRR = 1 MHz, 50% Duty Cycle, t_r < 6 ns, t_f < 6 ns, Z₀ = 50 Ω

‡ Includes probe and jig capacitance

Figure 4. Driver Switching Test Circuit and Waveforms, HVD SCSI-Loading (double terminated)

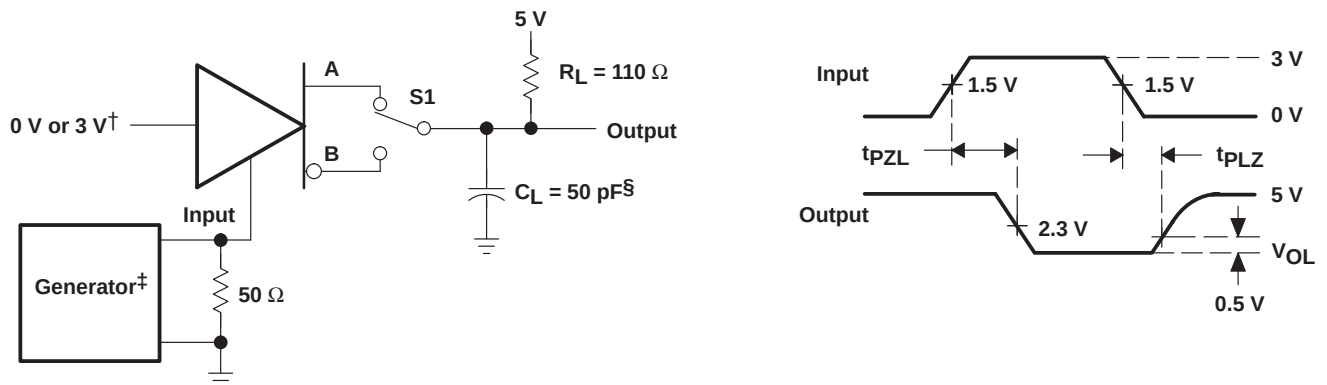


† 3 V if testing A output, 0 V if testing B output

‡ PRR = 1 MHz, 50% Duty Cycle, t_r < 6 ns, t_f < 6 ns, Z₀ = 50 Ω

§ Includes probe and jig capacitance

Figure 5. Driver Enable/Disable Test, High Output



† 0 V if testing A output, 3 V if testing B output

‡ PRR = 1 MHz, 50% Duty Cycle, t_r < 6 ns, t_f < 6 ns, Z₀ = 50 Ω

§ Includes probe and jig capacitance

Figure 6. Driver Enable/Disable Test, Low Output

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PARAMETER MEASUREMENT INFORMATION

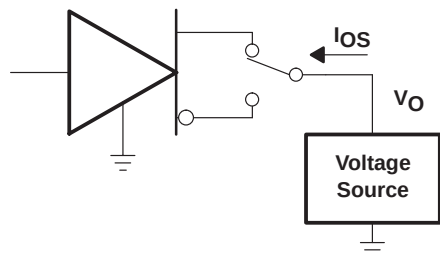


Figure 7. Driver Short-Circuit Test

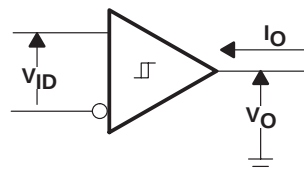
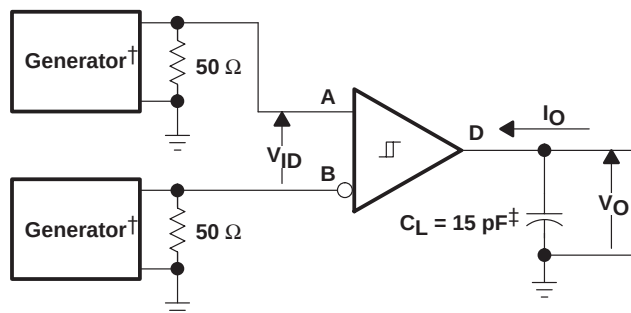
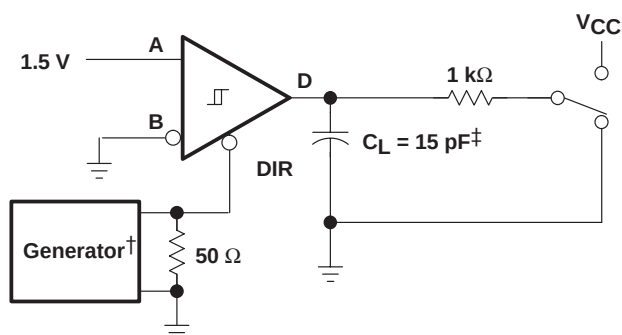


Figure 8. Receiver DC Parameters



† PRR = 1 MHz, 50% Duty Cycle, $t_r < 6$ ns, $t_f < 6$ ns, $Z_0 = 50 \Omega$
‡ Includes probe and jig capacitance

Figure 9. Receiver Switching Test Circuit and Waveforms



† PRR = 1 MHz, 50% Duty Cycle, $t_r < 6$ ns, $t_f < 6$ ns, $Z_0 = 50 \Omega$
‡ Includes probe and jig capacitance

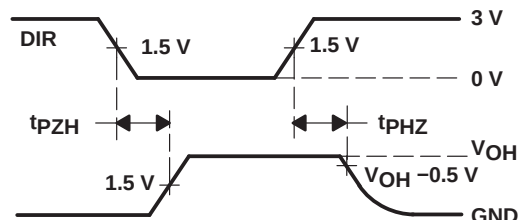
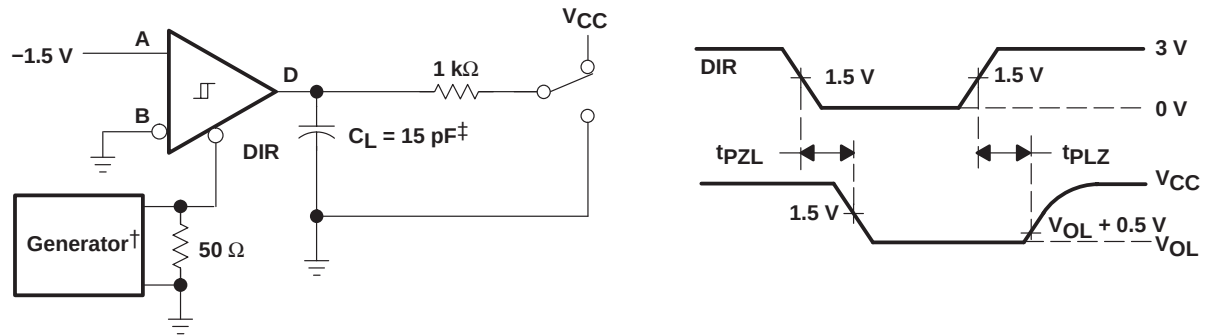


Figure 10. Receiver Enable/Disable Test, High Output

PARAMETER MEASUREMENT INFORMATION



† PRR = 1 MHz, 50% Duty Cycle, $t_r < 6$ ns, $t_f < 6$ ns, $Z_0 = 50 \Omega$

‡ Includes probe and jig capacitance

Figure 11. Receiver Enable/Disable Test, Low Output

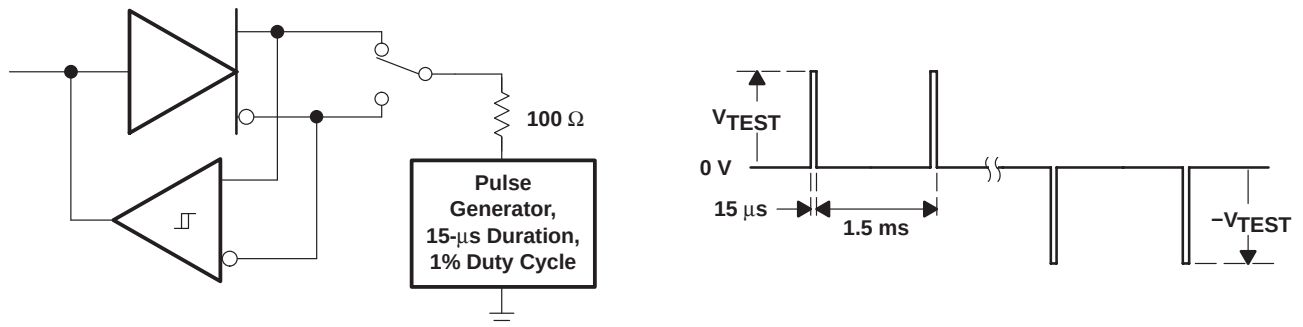


Figure 12. Test Circuit and Waveform, Transient Over Voltage Test

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TYPICAL CHARACTERISTICS

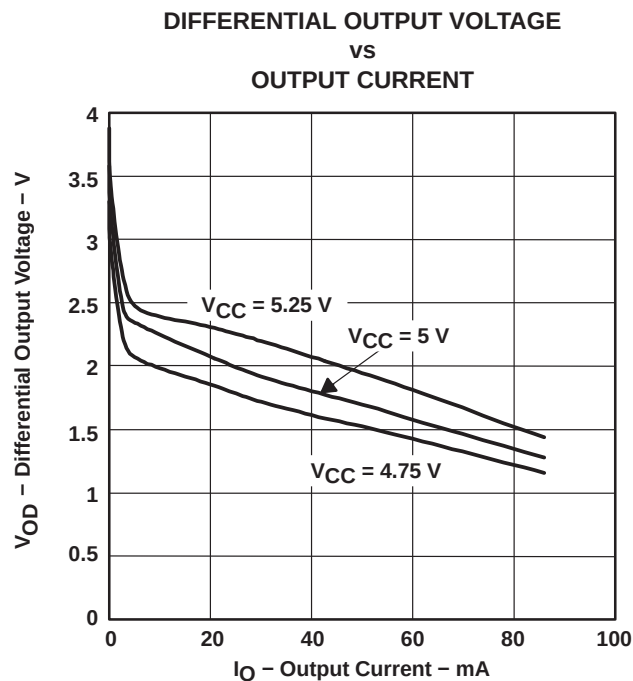


Figure 13

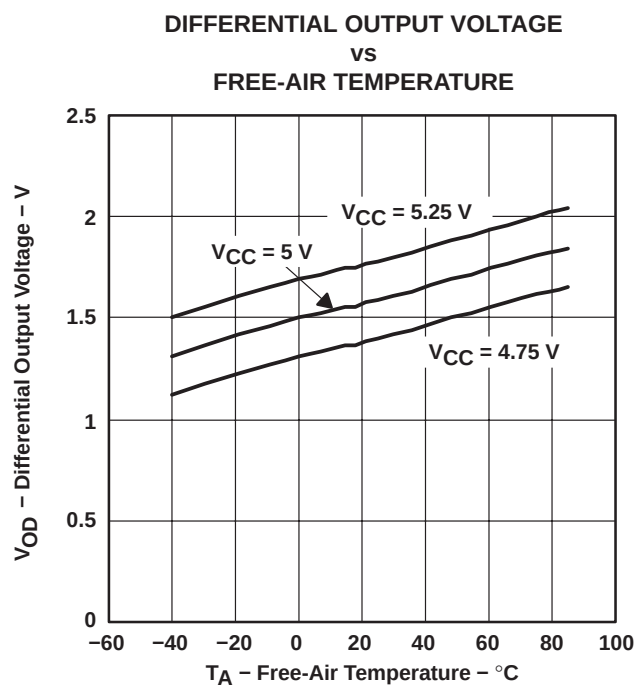


Figure 14

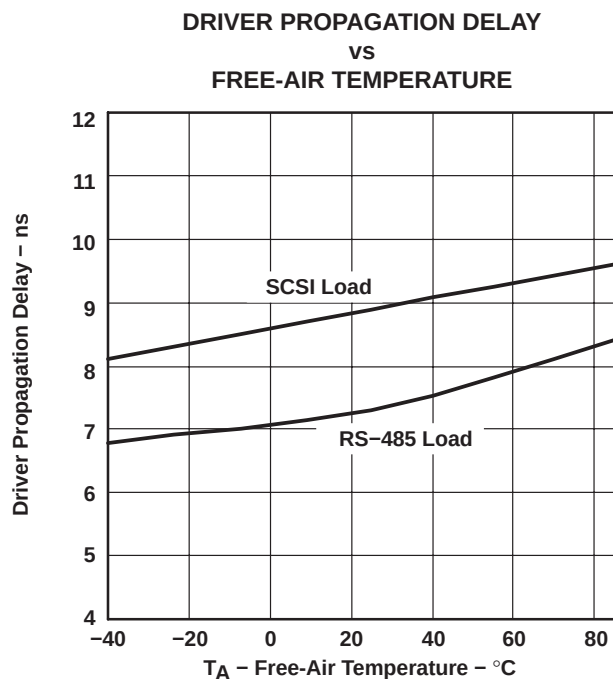


Figure 15

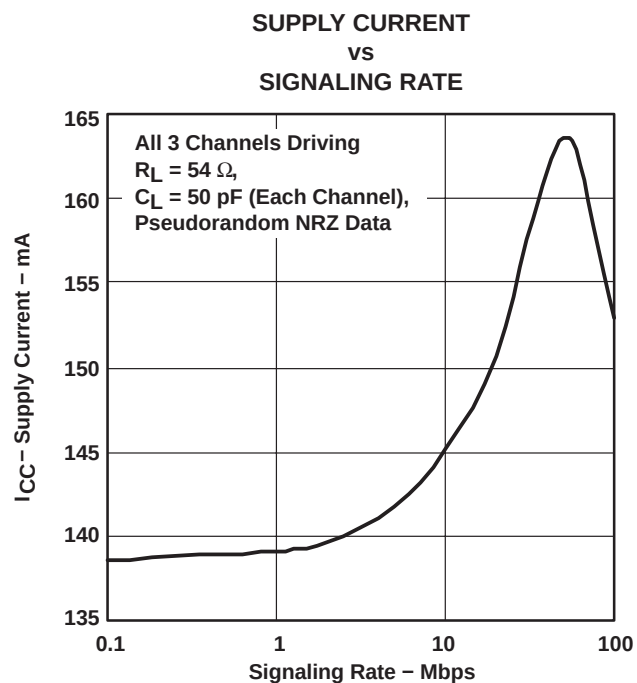


Figure 16

TYPICAL CHARACTERISTICS

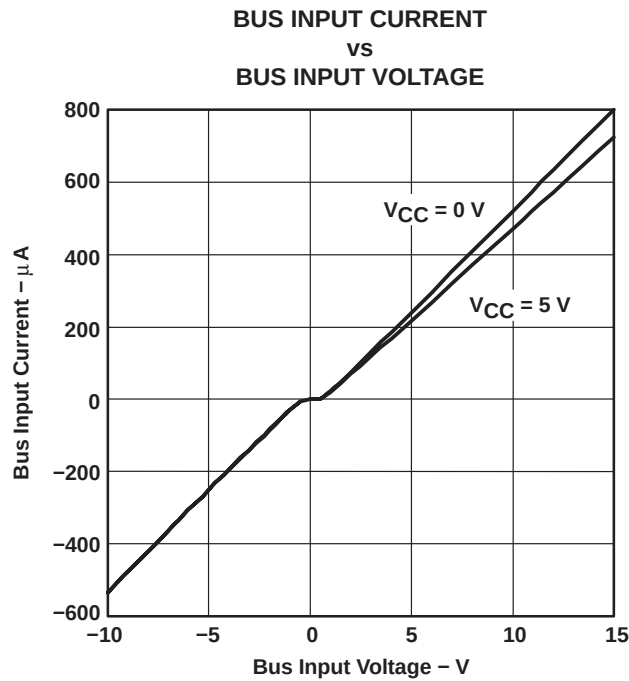


Figure 17

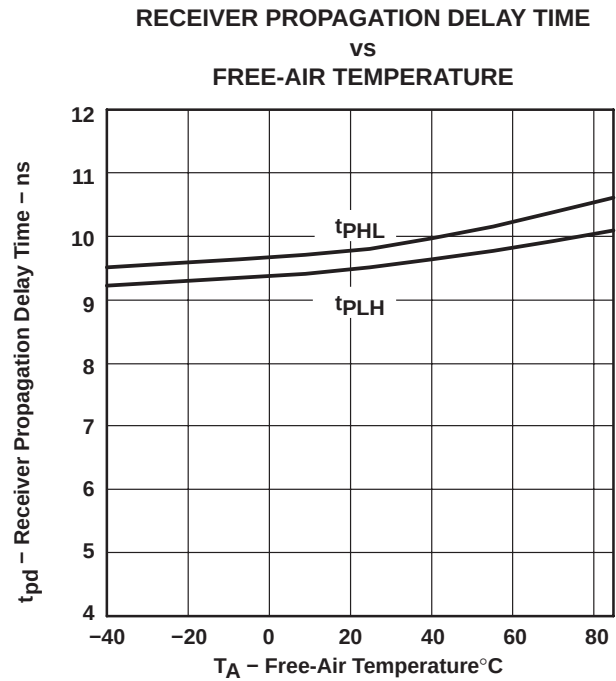


Figure 18

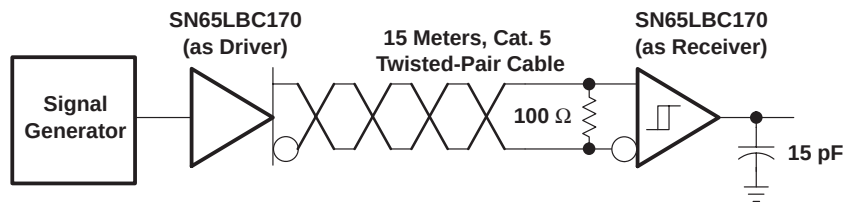


Figure 19. Circuit Diagram for Signaling Characteristics

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TYPICAL CHARACTERISTICS

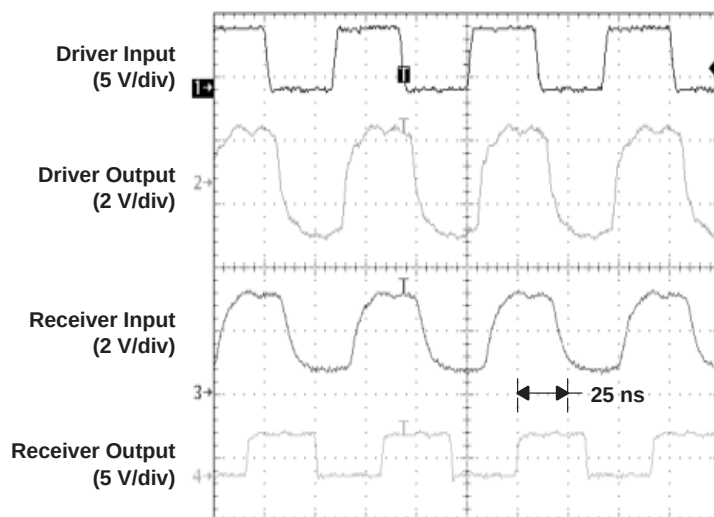


Figure 20. Signal Waveforms at 30 Mbps

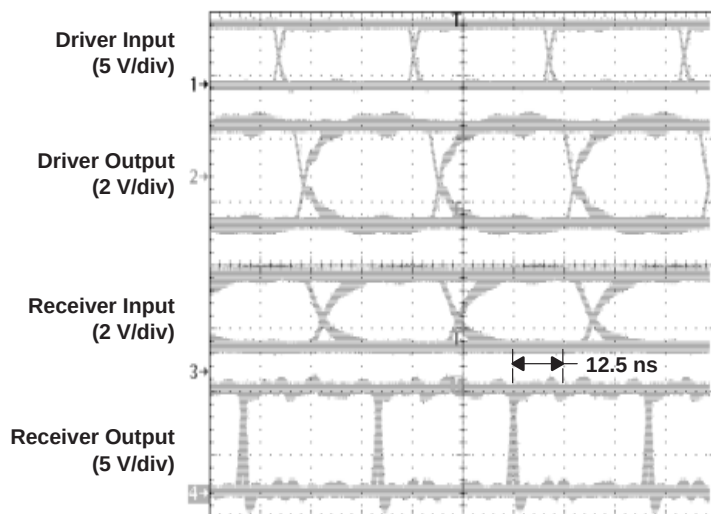


Figure 21. Eye Patterns, Pseudorandom Data at 30 Mbps

TYPICAL CHARACTERISTICS

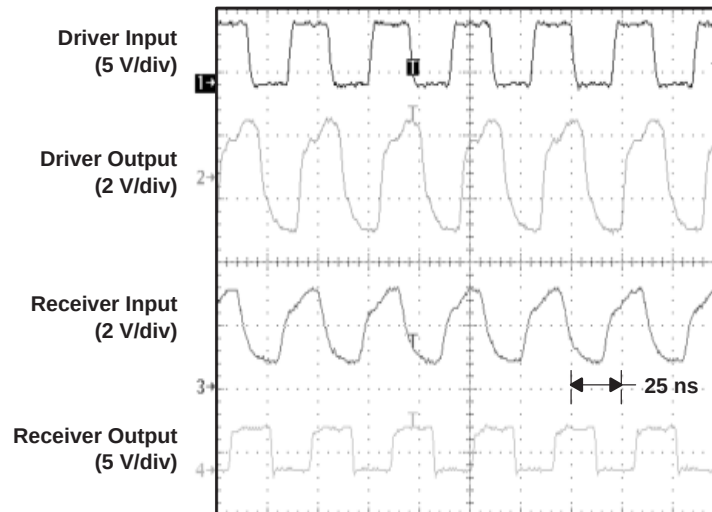


Figure 22. Signal Waveforms at 50 Mbps

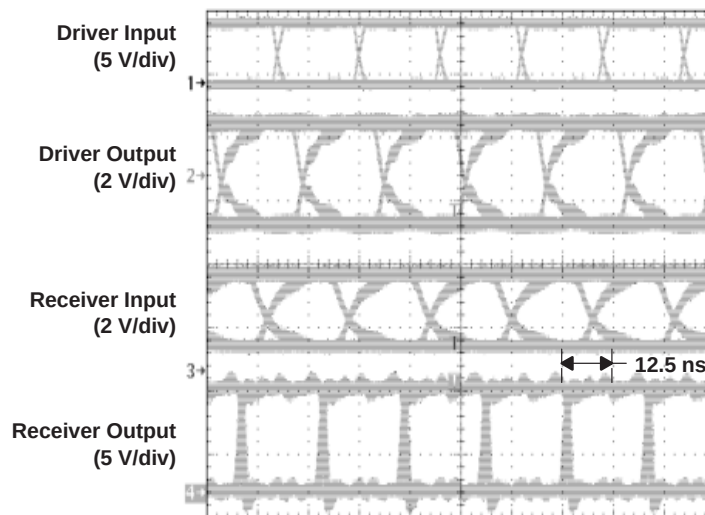


Figure 23. Eye Patterns, Pseudorandom Data at 50 Mbps

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65LBC170DB	Active	Production	SSOP (DB) 16	80 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BL170
SN65LBC170DB.A	Active	Production	SSOP (DB) 16	80 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BL170
SN65LBC170DW	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65LBC170
SN65LBC170DW.A	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65LBC170
SN75LBC170DB	Active	Production	SSOP (DB) 16	80 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LB170
SN75LBC170DB.A	Active	Production	SSOP (DB) 16	80 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LB170
SN75LBC170DBR	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LB170
SN75LBC170DBR.A	Active	Production	SSOP (DB) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	LB170

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

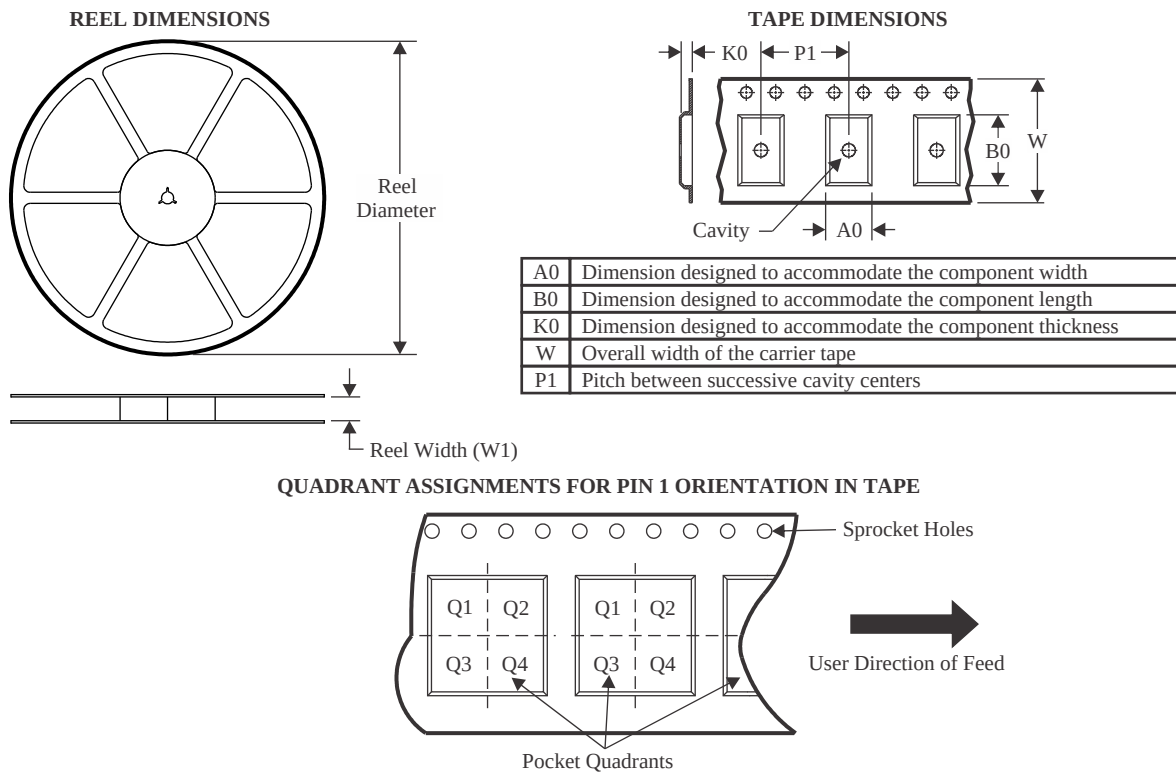
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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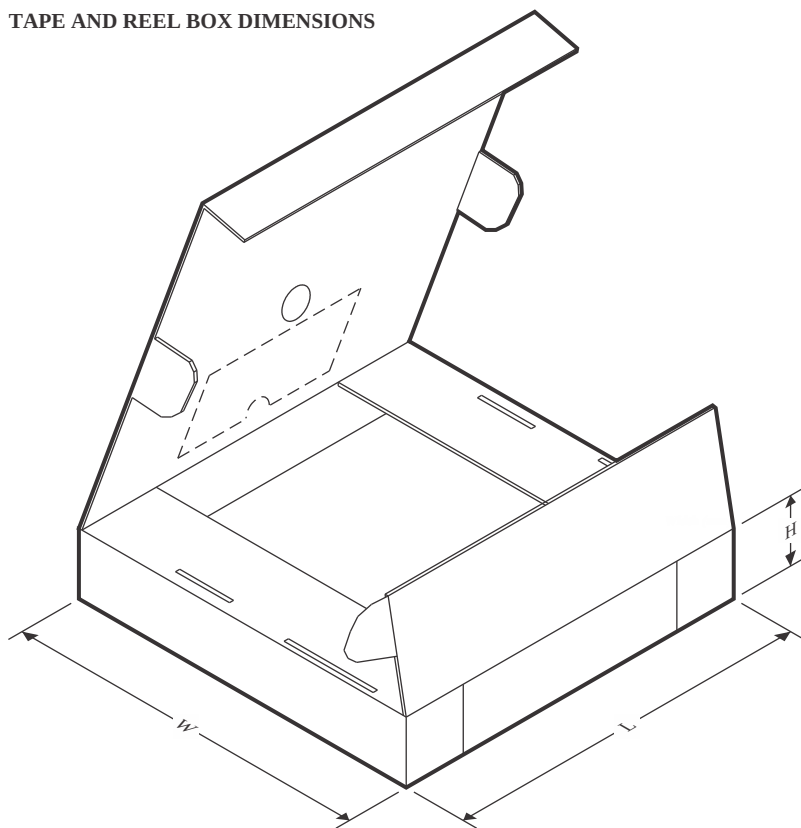
TAPE AND REEL INFORMATION



*All dimensions are nominal

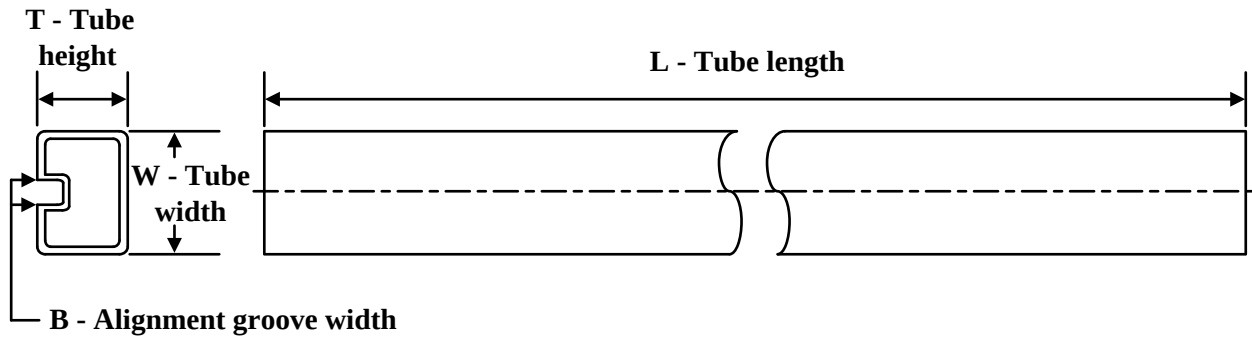
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75LBC170DBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



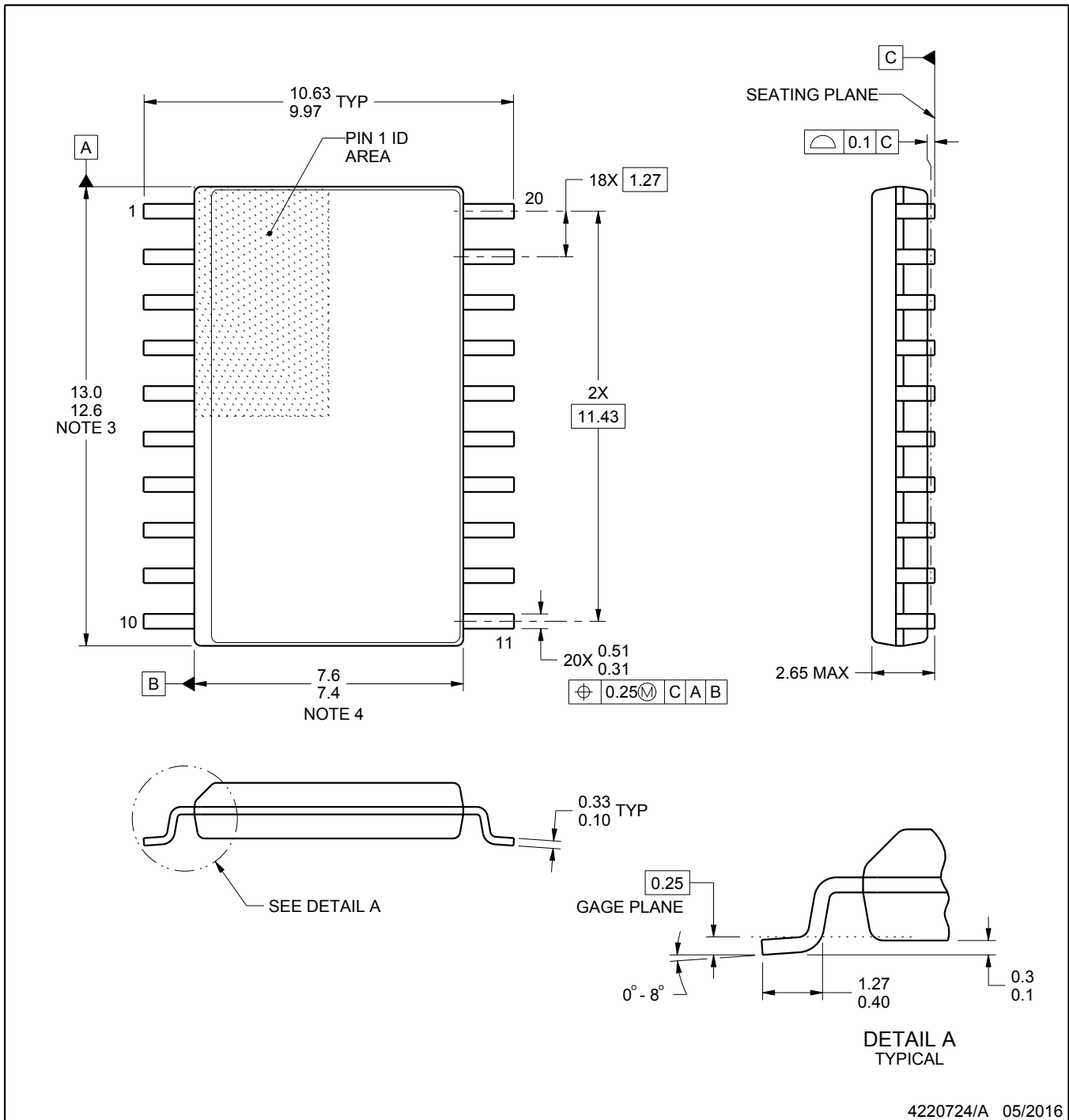
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75LBC170DBR	SSOP	DB	16	2000	353.0	353.0	32.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN65LBC170DB	DB	SSOP	16	80	530	10.5	4000	4.1
SN65LBC170DB.A	DB	SSOP	16	80	530	10.5	4000	4.1
SN65LBC170DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN65LBC170DW.A	DW	SOIC	20	25	507	12.83	5080	6.6
SN75LBC170DB	DB	SSOP	16	80	530	10.5	4000	4.1
SN75LBC170DB.A	DB	SSOP	16	80	530	10.5	4000	4.1



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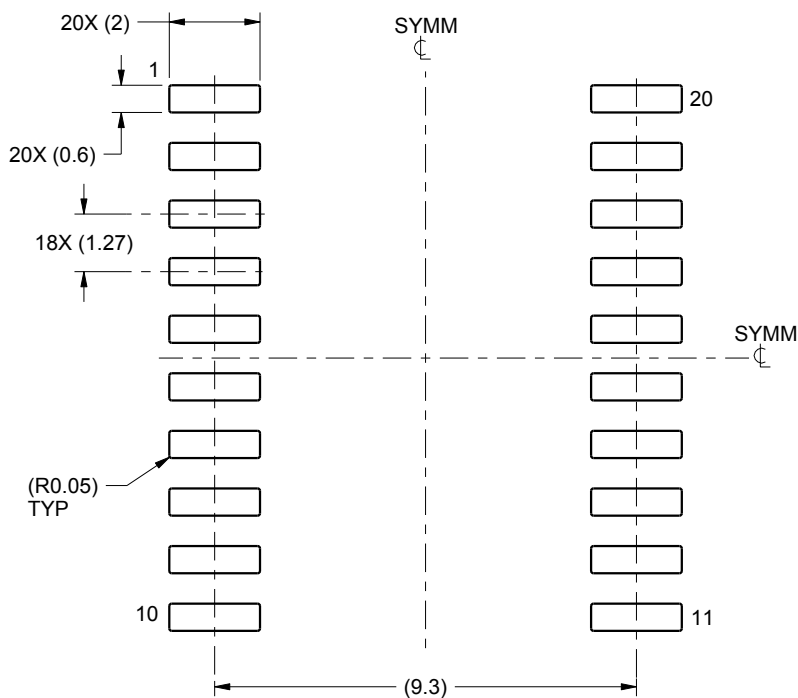
NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

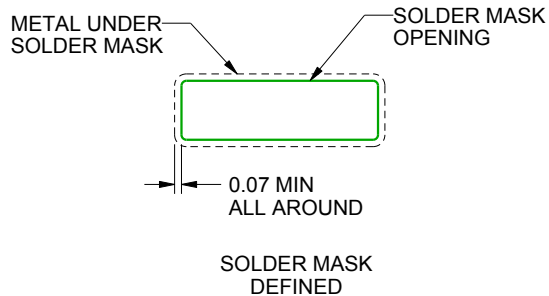
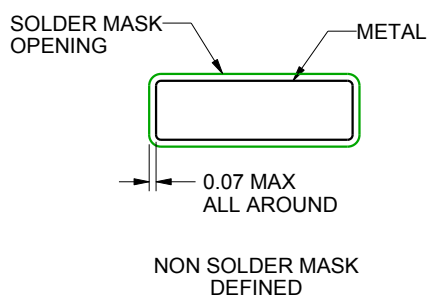
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

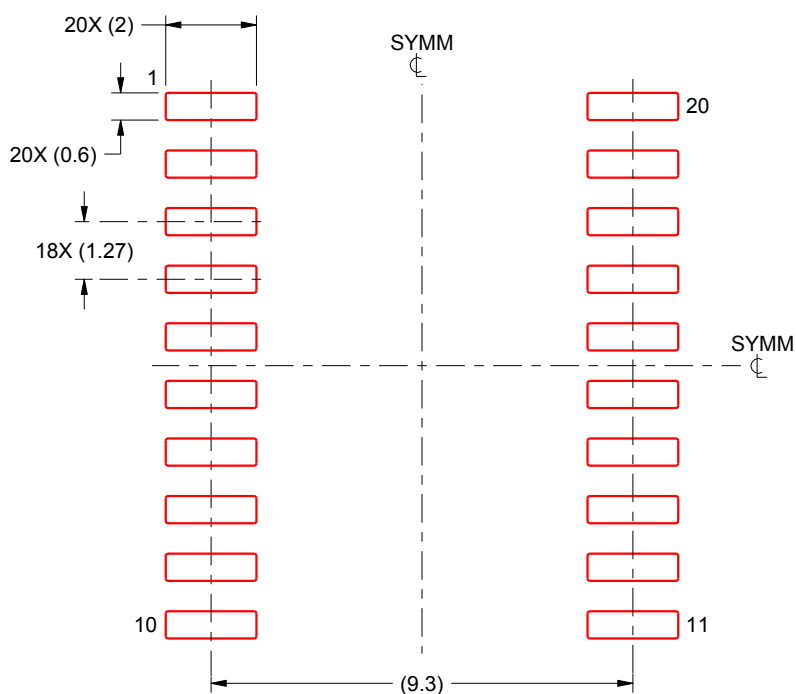
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC

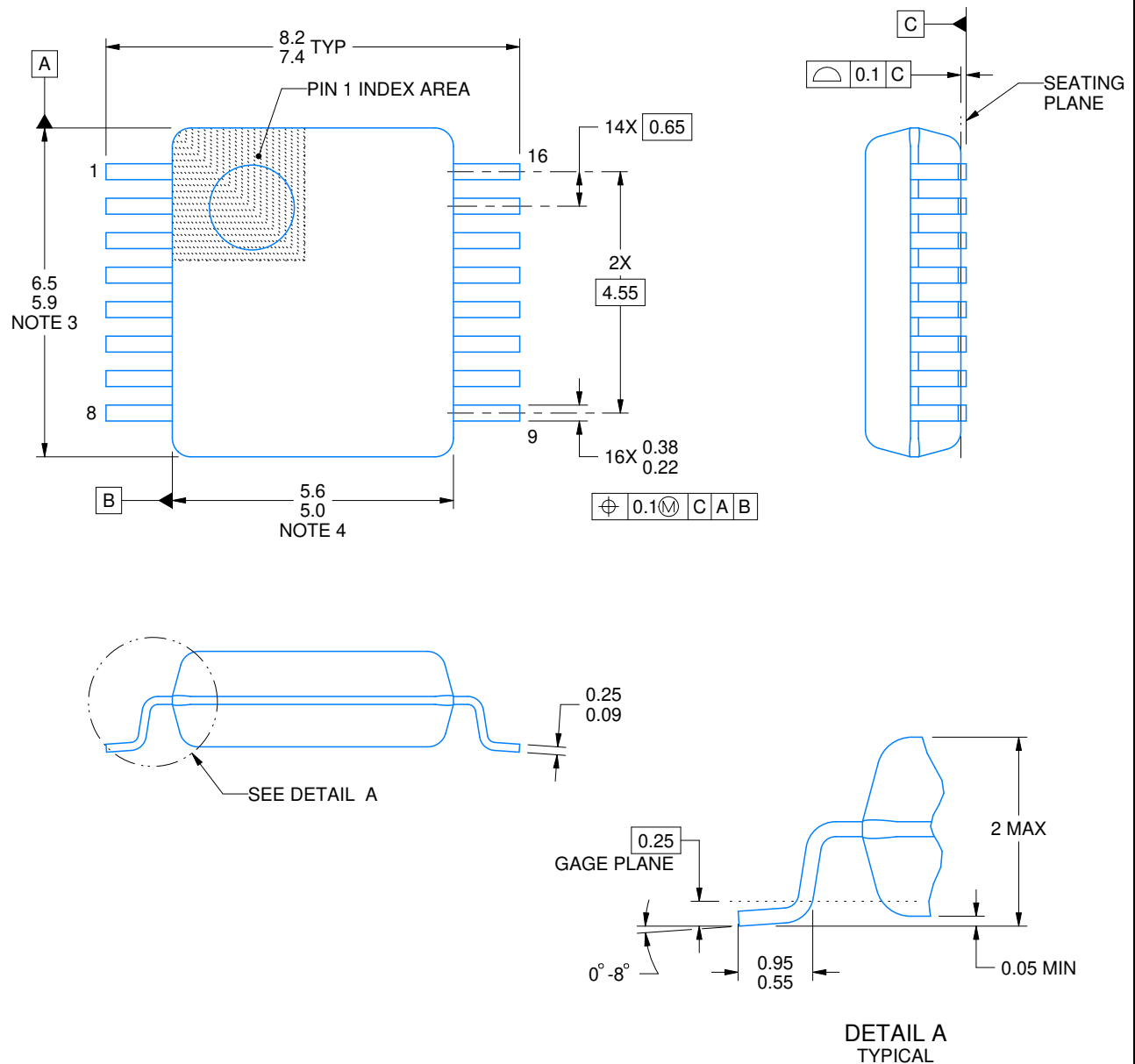


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



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NOTES:

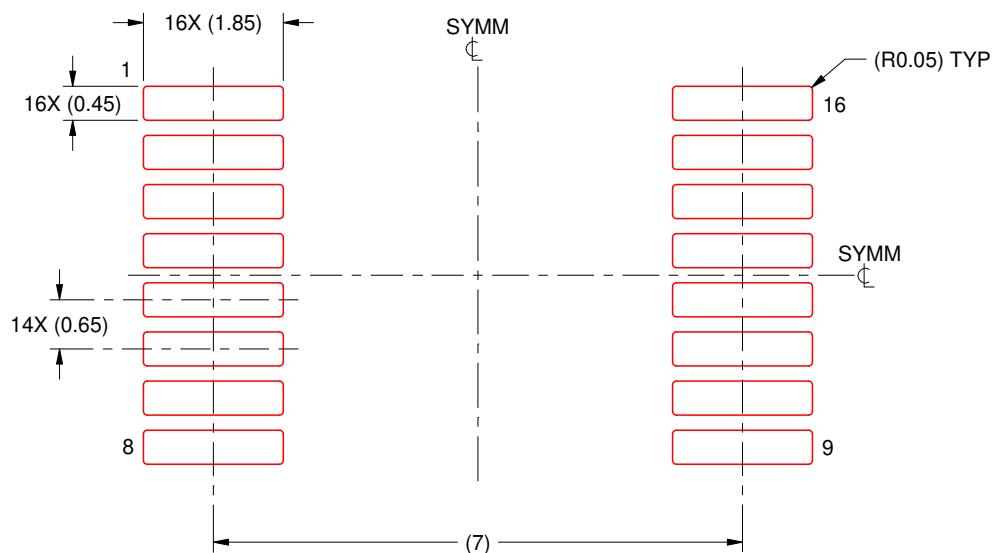
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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