SN65LVDSxxx High-Speed Differential Line Drivers and Receivers

1 Features

- Meets or Exceeds the Requirements of ANSI TIA/EIA-644-1995 Standard
- Full-Duplex Signaling Rates up to 150 Mbps (See Table 1)
- Bus-Pin ESD Exceeds 12 kV
- Operates From a Single 3.3-V Supply
- Low-Voltage Differential Signaling With Typical Output Voltages of 350 mV and a 100-Ω Load
- Propagation Delay Times
  - Driver: 1.7 ns Typical
  - Receiver: 3.7 ns Typical
- Power Dissipation at 200 MHz
  - Driver: 25 mW Typical
  - Receiver: 60 mW Typical
- LVTTL Input Levels Are 5-V Tolerant
- Receiver Maintains High Input Impedance With V_{CC} < 1.5 V
- Receiver Has Open-Circuit Fail Safe

2 Applications

- Wireless Infrastructure
- Telecom Infrastructure
- Printer

3 Description

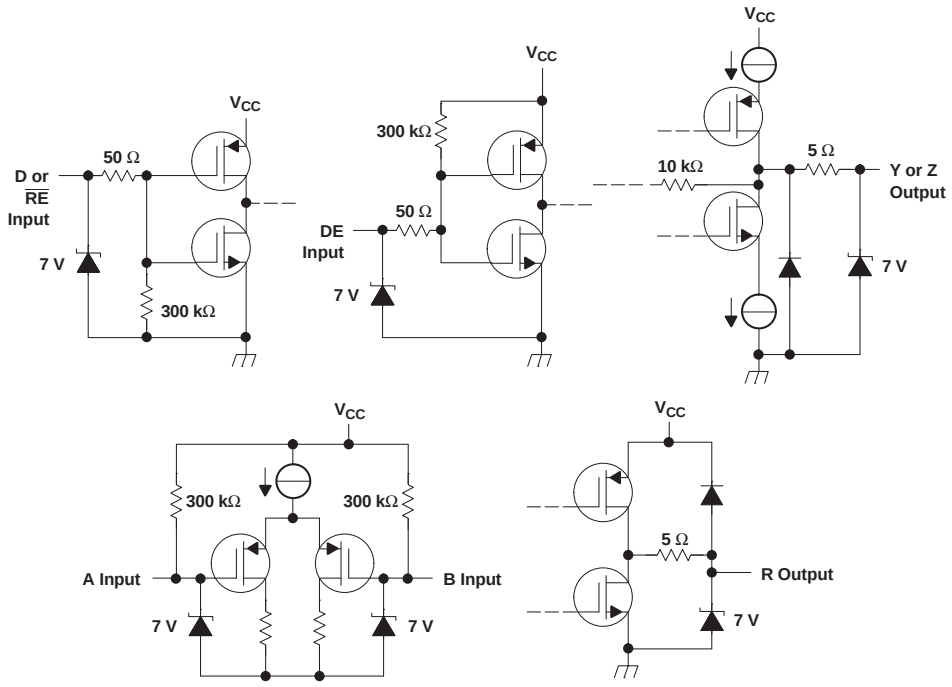
The SN65LVDS179, SN65LVDS180, SN65LVDS050, and SN65LVDS051 devices are differential line drivers and receivers that use low-voltage differential signaling (LVDS) to achieve signaling rates as high as 400 Mbps (see Table 1). The TIA/EIA-644 standard-compliant electrical interface provides a minimum differential output voltage magnitude of 247 mV into a 100-Ω load and receipt of 100-mV signals with up to 1 V of ground potential difference between a transmitter and receiver.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN65LVDS179	SOIC (8)	4.90 mm × 3.91 mm
	VSSOP (8)	3.00 mm × 3.00 mm
SN65LVDS180	SOIC (14)	8.65 mm × 3.91 mm
	TSSOP (14)	5.00 mm × 4.40 mm
SN65LVDS050	SOIC (16)	9.90 mm × 3.91 mm
	TSSOP (16)	5.00 mm × 4.40 mm
SN65LVDS051	SOIC (16)	9.90 mm × 3.91 mm
	TSSOP (16)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Equivalent Input and Output Schematic Diagrams



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Changes from Revision Q (December 2014) to Revision R **Page**

- Changed pin A in the *Pin Functions: SN65LVDS179* From: "non-inverting output" To: "non-inverting input" ... 5
- Changed pin B in the *Pin Functions: SN65LVDS179* From: "inverting output" To: "inverting input" ... 5

Changes from Revision P (April 2009) to Revision Q **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

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5 Description (Continued)

These devices offer various driver, receiver, and enabling combinations in industry-standard footprints. Because these devices are intended for use in simplex or distributed simplex bus structures, the driver enable function does not put the differential outputs into a high-impedance state but rather disconnects the input and reduces the quiescent power used by the device. For these functions with a high-impedance driver output, see the SN65LVDM series of devices. All devices are characterized for operation from –40°C to 85°C.

6 Device Options

PACKAGE		
SMALL OUTLINE (D)	SMALL OUTLINE (DGK)	SMALL OUTLINE (PW)
SN65LVDS050D	—	SN65LVDS050PW
SN65LVDS051D	—	SN65LVDS051PW
SN65LVDS179D	SN65LVDS179DGK	—
SN65LVDS180D	—	SN65LVDS180PW

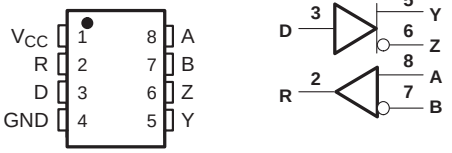
Table 1. Maximum Recommended Operating Speeds

PART NUMBER	ALL BUFFERS ACTIVE	RX BUFFER ONLY	TX BUFFER ONLY
SN65LVDS179	150 Mbps	150 Mbps	400 Mbps
SN65LVDS180	150 Mbps	150 Mbps	400 Mbps
SN65LVDS050	100 Mbps	100 Mbps	400 Mbps
SN65LVDS051	100 Mbps	100 Mbps	400 Mbps

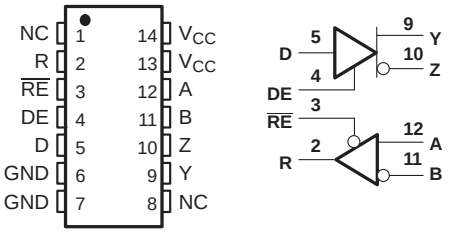
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7 Pin Configuration and Functions

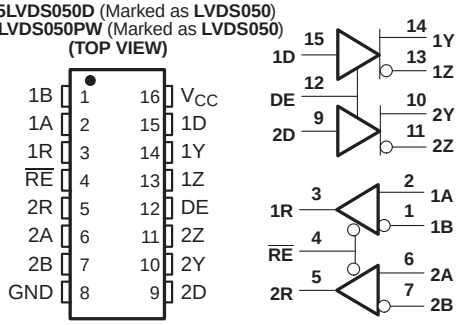
SN65LVDS179D (Marked as **DL179** or **LVD179**)
SN65LVDS179DGK (Marked as **S79**)
(TOP VIEW)



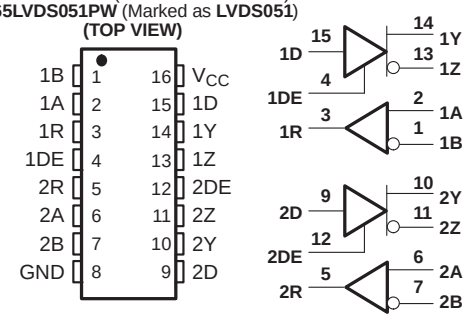
SN65LVDS180D (Marked as **LVDS180**)
SN65LVDS180PW (Marked as **LVDS180**)
(TOP VIEW)



SN65LVDS050D (Marked as **LVDS050**)
SN65LVDS050PW (Marked as **LVDS050**)
(TOP VIEW)



SN65LVDS051D (Marked as **LVDS051**)
SN65LVDS051PW (Marked as **LVDS051**)
(TOP VIEW)



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Pin Functions: SN65LVDS179

PIN		I/O	DESCRIPTION
NAME	NUMBER		
V_{CC}	1	–	Supply voltage
GND	4	–	Ground
D	3	I	LVTTL input signal
Y	5	O	Differential (LVDS) non-inverting output
Z	6	O	Differential (LVDS) inverting output
R	2	O	LVTTL output signal
A	8	I	Differential (LVDS) non-inverting input
B	7	I	Differential (LVDS) inverting input

Pin Functions: SN65LVDS180

PIN		I/O	DESCRIPTION
NAME	NUMBER		
V_{CC}	13, 14	–	Supply voltage
GND	6, 7	–	Ground
D	5	I	LVTTL input signal
Y	9	O	Differential (LVDS) non-inverting output
Z	10	O	Differential (LVDS) inverting output
R	2	O	LVTTL output signal
A	12	I	Differential (LVDS) non-inverting input
B	11	I	Differential (LVDS) inverting input
DE	4	I	Driver enable
RE/	3	I	Receiver enable
NC	1, 8	–	No connection

Pin Functions: SN65LVDS050

PIN		I/O	DESCRIPTION
NAME	NUMBER		
V_{CC}	16	–	Supply voltage
GND	8	–	Ground
1D	15	I	LVTTL input signal
1Y	14	O	Differential (LVDS) non-inverting output
1Z	13	O	Differential (LVDS) inverting output
2D	9	I	LVTTL input signal
2Y	10	O	Differential (LVDS) non-inverting output
2Z	11	O	Differential (LVDS) inverting output
1R	3	O	LVTTL output signal
1A	2	I	Differential (LVDS) non-inverting input
1B	1	I	Differential (LVDS) inverting input
2R	5	O	LVTTL output signal
2A	6	I	Differential (LVDS) non-inverting input
2B	7	I	Differential (LVDS) inverting input
DE	12	I	Driver enable
RE/	4	I	Receiver enable

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Pin Functions: SN65LVDS051

PIN		I/O	DESCRIPTION
NAME	NUMBER		
V_{CC}	16	–	Supply voltage
GND	8	–	Ground
1D	15	I	LVTTL input signal
1Y	14	O	Differential (LVDS) non-inverting output
1Z	13	O	Differential (LVDS) inverting output
2D	9	I	LVTTL input signal
2Y	10	O	Differential (LVDS) non-inverting output
2Z	11	O	Differential (LVDS) inverting output
1R	3	O	LVTTL output signal
1A	2	I	Differential (LVDS) non-inverting input
1B	1	I	Differential (LVDS) inverting input
2R	5	O	LVTTL output signal
2A	6	I	Differential (LVDS) non-inverting input
2B	7	I	Differential (LVDS) inverting input
1DE	4	I	Driver 1 enable
2DE	12	I	Driver 2 enable

8 Specifications

8.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}(2)	Supply voltage range		–0.5	4	V
	Voltage range:	D, R, DE, $\overline{RE}$	–0.5	6	V
		Y, Z, A, and B	–0.5	4	V
$\|V_{OD}\|$	Differential output voltage			1	V
	Continuous power dissipation		See *Thermal Information*		
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages are with respect to network ground terminal.

8.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Y, Z, A, B , and GND (see (1))	Class 3, A	±12000	V
			Class 3, B	±600	V
		All	Class 3, A	±7000	V
			Class 3, B	±500	V
	Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds			250	°C

(1) Tested in accordance with MIL-STD-883C Method 3015.7.

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8.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
$\|V_{ID}\|$	Magnitude of differential input voltage	0.05		0.6	V
$\|V_{OD}(dis)\|$	Magnitude of differential output voltage with disabled driver			520	mV
V_{OY} or V_{OZ}	Driver output voltage	0		2.4	V
V_{IC}	Common-mode input voltage (see Figure 14)			V_{CC} – 0.8	V
T_A	Operating free-air temperature	–40		85	°C

8.4 Thermal Information

THERMAL METRIC(1)	SN65LVDS179		SN65LVDS180		SN65LVDS050, SN65LVDS051		UNIT
	D	DGK	D	PW	D	PW	
	8 PINS		14 PINS		16 PINS		
Power Rating: $T_A \leq 25°C$	635	424	987	736	1110	839	mW
Derating Factor Above $T_A = 25°C$(2)	5.1	3.4	7.9	5.9	8.9	6.7	mW/°C
Power Rating: $T_A = 85°C$	330	220	513	383	577	437	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no airflow.

8.5 Device Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
I_{CC} Supply current	SN65LVDS179	No receiver load, driver R_L = 100 Ω		9	12	mA
	SN65LVDS180	Driver and receiver enabled, no receiver load, driver R_L = 100 Ω		9	12	mA
		Driver enabled, receiver disabled, R_L = 100 Ω		5	7	
		Driver disabled, receiver enabled, no load		1.5	2	
		Disabled		0.5	1	
	SN65LVDS050	Drivers and receivers enabled, no receiver loads, driver R_L = 100 Ω		12	20	mA
		Drivers enabled, receivers disabled, R_L = 100 Ω		10	16	
		Drivers disabled, receivers enabled, no loads		3	6	
		Disabled		0.5	1	
	SN65LVDS051	Drivers enabled, no receiver loads, driver R_L = 100 Ω		12	20	mA
		Drivers disabled, no loads		3	6	

(1) All typical values are at 25°C and with a 3.3-V supply.

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8.6 Driver Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\|V_{OD}\|$	Differential output voltage magnitude		R_L = 100 Ω, See Figure 11 and Figure 12	247	340	454	mV
$\Delta\|V_{OD}\|$	Change in differential output voltage magnitude between logic states			–50		50	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage		See Figure 12	1.125	1.2	1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states			–50		50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage				50	150	mV
I_{IH}	High-level input current	DE	V_{IH} = 5 V		–0.5	–20	µA
		D			2	20	
I_{IL}	Low-level input current	DE	V_{IL} = 0.8 V		–0.5	–10	µA
		D			2	10	
I_{OS}	Short-circuit output current		V_{OY} or V_{OZ} = 0 V		3	10	mA
			V_{OD} = 0 V		3	10	
$I_{O(OFF)}$	Off-state output current		DE = 0 V V_{OY} = V_{OZ} = 0 V	–1		1	µA
			DE = V_{CC} V_{OY} = V_{OZ} = 0 V V_{CC} < 1.5 V				
C_{IN}	Input capacitance				3		pF

8.7 Receiver Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going differential input voltage threshold	See Figure 14 and Table 2			100	mV
$V_{IT–}$	Negative-going differential input voltage threshold		–100			
V_{OH}	High-level output voltage	I_{OH} = –8 mA	2.4			V
		I_{OH} = –4 mA	2.8			
V_{OL}	Low-level output voltage	I_{OL} = 8 mA			0.4	V
I_I	Input current (A or B input)	V_I = 0 V	–2	–11	–20	µA
		V_I = 2.4 V	–1.2	–3		
$I_{I(OFF)}$	Power-off input current (A or B input)	V_{CC} = 0 V			±20	µA
I_{IH}	High-level input current (enables)	V_{IH} = 5 V			±10	µA
I_{IL}	Low-level input current (enables)	V_{IL} = 0.8 V			±10	µA
I_{OZ}	High-impedance output current	V_O = 0 or 5 V			±10	µA
C_I	Input capacitance			5		pF

(1) All typical values are at 25°C and with a 3.3-V supply.

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8.8 Driver Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 100 Ω, C_L = 10 pF, See Figure 11		1.7	2.7	ns
t_{PHL}	Propagation delay time, high-to-low-level output			1.7	2.7	ns
t_r	Differential output signal rise time			0.8	1	ns
t_f	Differential output signal fall time			0.8	1	ns
$t_{sk(p)}$	Pulse skew ($\|t_{pHL} - t_{pLH}\|$)(2)			300		ps
$t_{sk(o)}$	Channel-to-channel output skew(3)			150		ps
t_{en}	Enable time	See Figure 13		4.3	10	ns
t_{dis}	Disable time			3.1	10	ns

(1) All typical values are at 25°C and with a 3.3-V supply.
(2) $t_{sk(p)}$ is the magnitude of the time difference between the high-to-low and low-to-high propagation delay times at an output.
(3) $t_{sk(o)}$ is the magnitude of the time difference between the outputs of a single device with all of their inputs connected together.

8.9 Receiver Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 10 pF, See Figure 15		3.7	4.5	ns
t_{PHL}	Propagation delay time, high-to-low-level output			3.7	4.5	ns
$t_{sk(p)}$	Pulse skew ($\|t_{pHL} - t_{pLH}\|$)(2)			0.3		ns
t_r	Output signal rise time			0.7	1.5	ns
t_f	Output signal fall time			0.9	1.5	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	See Figure 16		2.5		ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output			2.5		ns
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output			7		ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output			4		ns

(1) All typical values are at 25°C and with a 3.3-V supply.
(2) $t_{sk(p)}$ is the magnitude of the time difference between the high-to-low and low-to-high propagation delay times at an output.

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8.10 Typical Characteristics

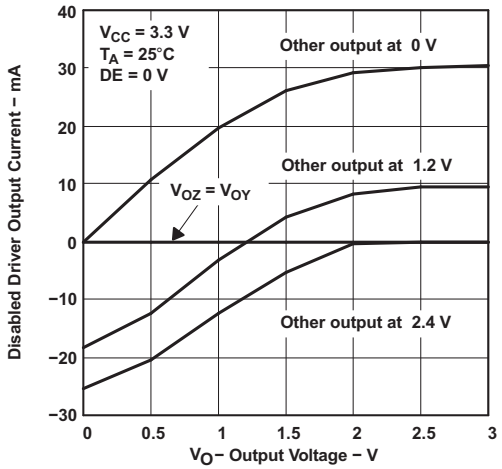


Figure 1. Disabled Driver Output Current vs Output Voltage

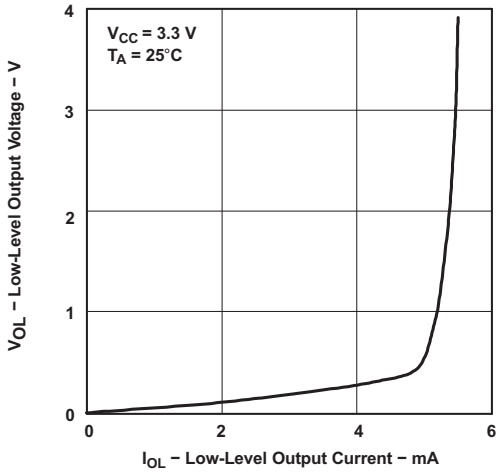


Figure 2. Driver Low-Level Output Voltage vs Low-Level Output Current

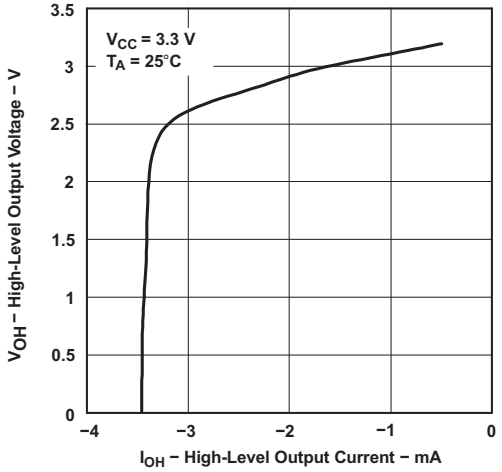


Figure 3. Driver High-Level Output Voltage vs High-Level Output Current

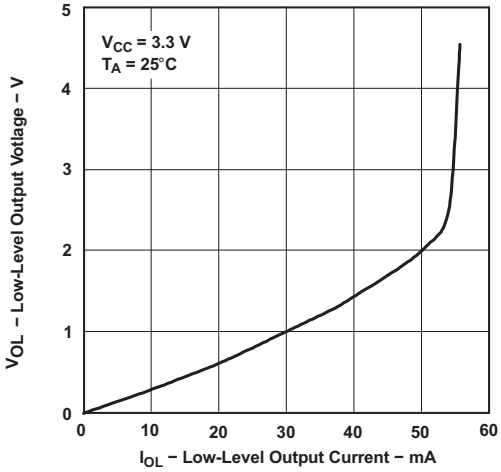


Figure 4. Receiver Low-Level Output Voltage vs Low-Level Output Current

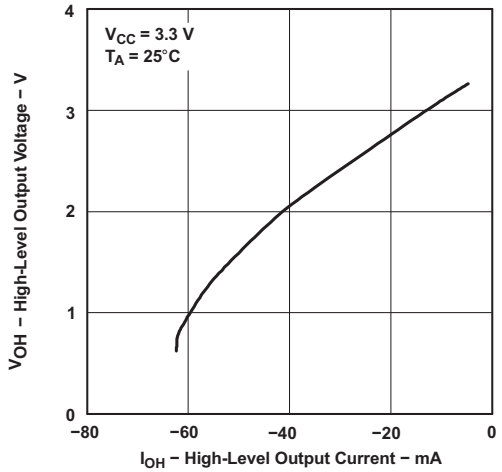


Figure 5. Receiver High-Level Output Voltage vs High-Level Output Current

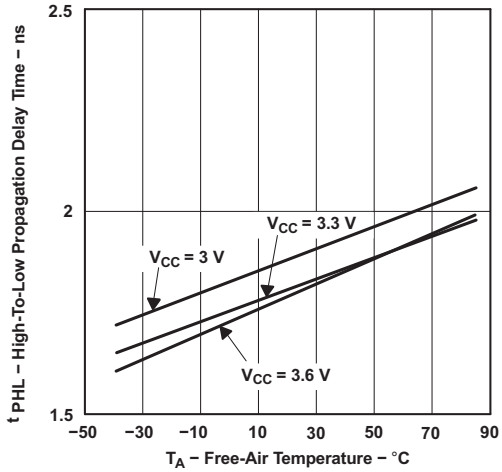


Figure 6. Driver High-to-Low Level Propagation Delay Time vs Free-Air Temperature

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Typical Characteristics (continued)

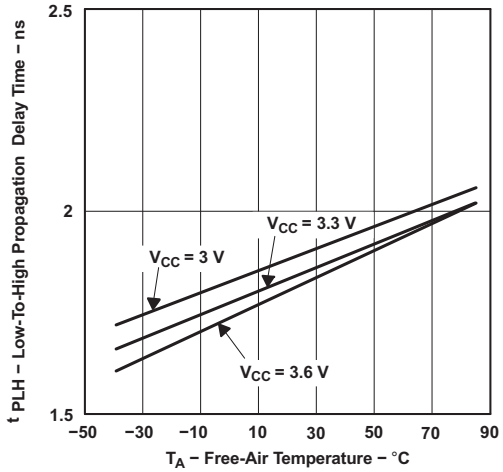


Figure 7. Driver Low-to-High Level Propagation Delay Time vs Free-Air Temperature

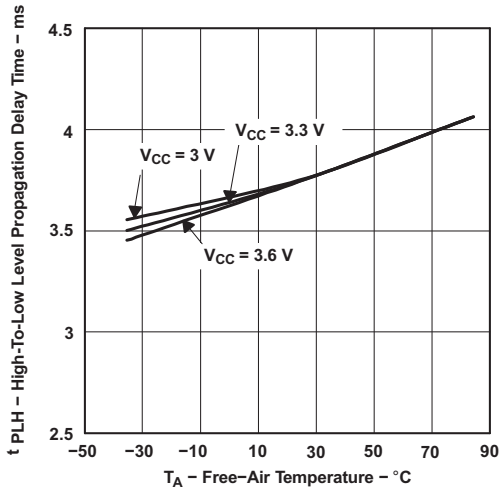


Figure 8. Receiver High-to-Low Level Propagation Delay Time vs Free-Air Temperature

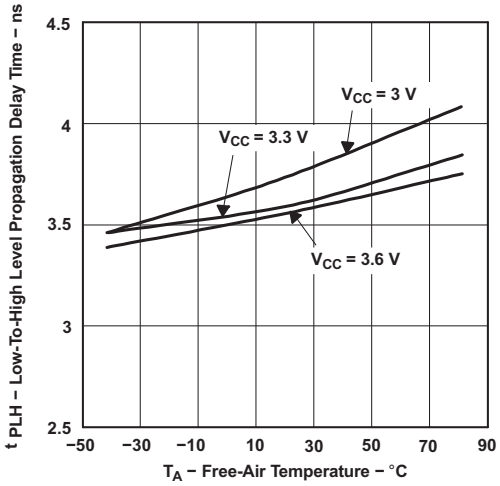


Figure 9. Receiver Low-to-High Level Propagation Delay Time vs Free-Air Temperature

9 Parameter Measurement Information

9.1 Driver

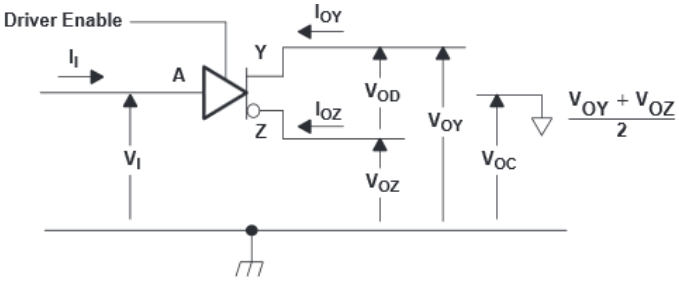
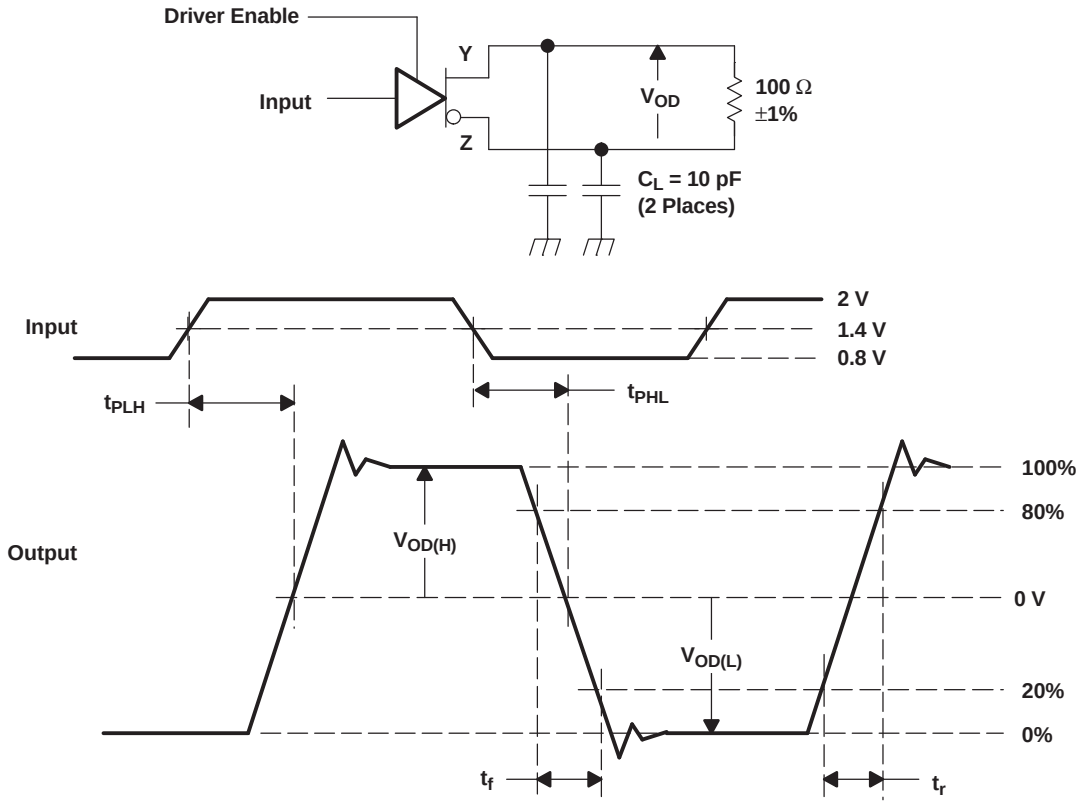


Figure 10. Driver Voltage and Current Definitions

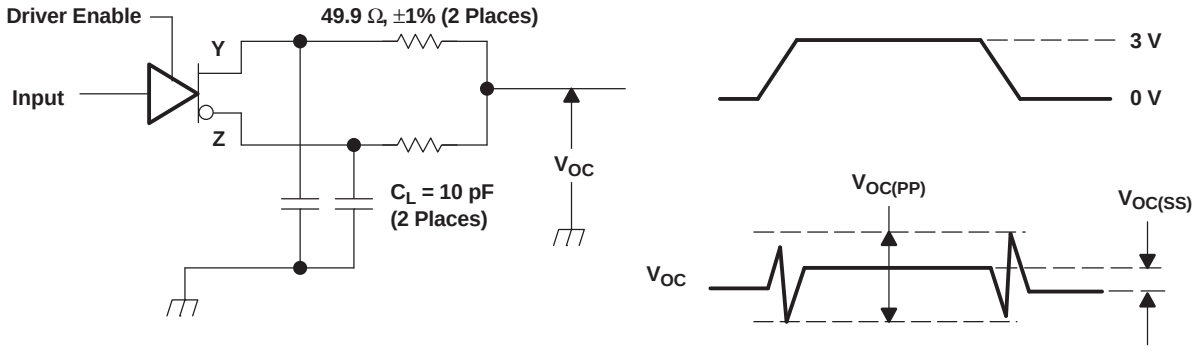


A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns. C_L includes instrumentation and fixture capacitance within 0.06 mm of the device under test.

Figure 11. Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal

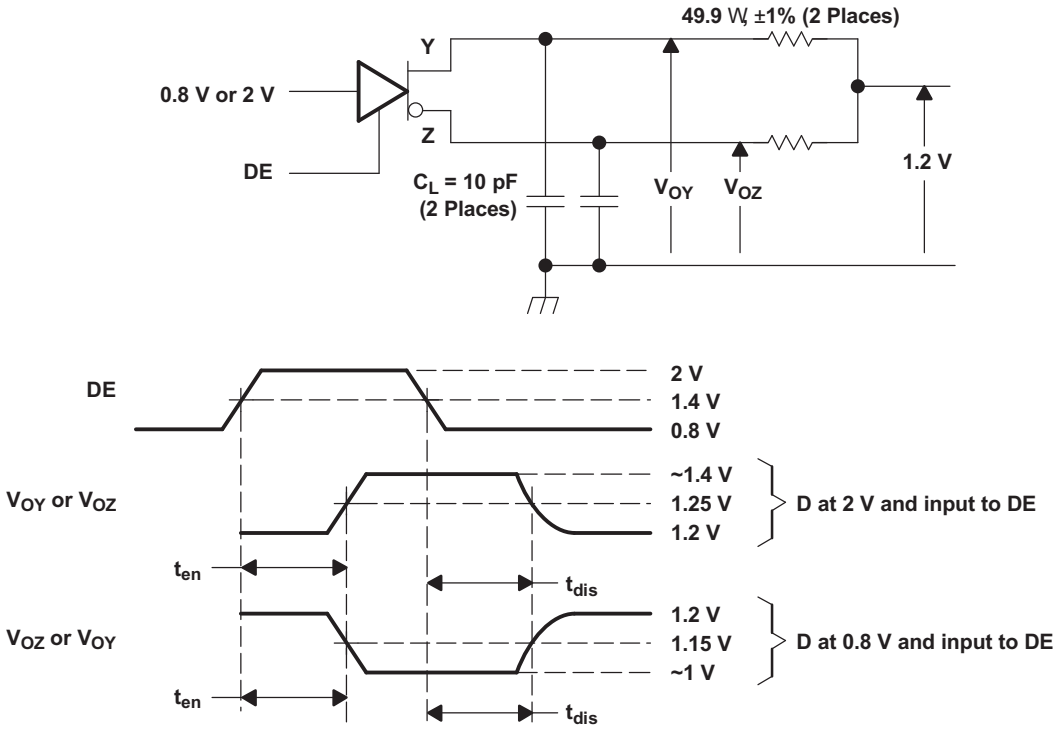
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Driver (continued)



A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns. C_L includes instrumentation and fixture capacitance within 0.06 mm of the device under test. The measurement of $V_{OC(PP)}$ is made on test equipment with a –3-dB bandwidth of at least 300 MHz.

Figure 12. Test Circuit and Definitions for the Driver Common-Mode Output Voltage



A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0.06 mm of the device under test.

Figure 13. Enable or Disable Time Circuit and Definitions

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9.2 Receiver

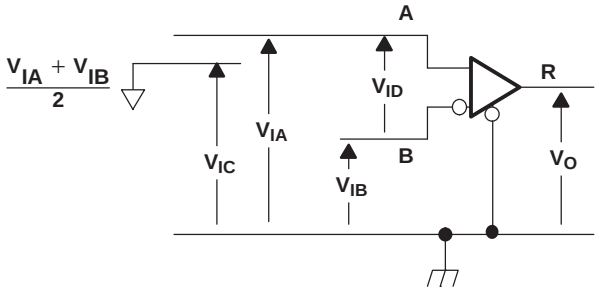
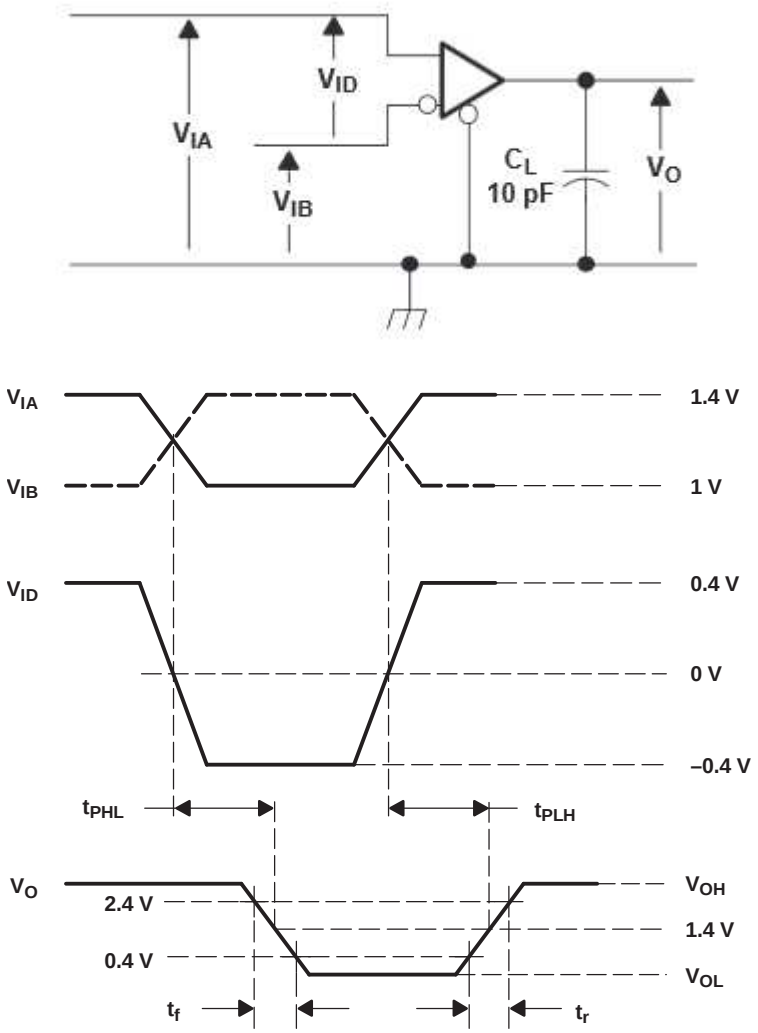


Figure 14. Receiver Voltage Definitions

Table 2. Receiver Minimum And Maximum Input Threshold Test Voltages

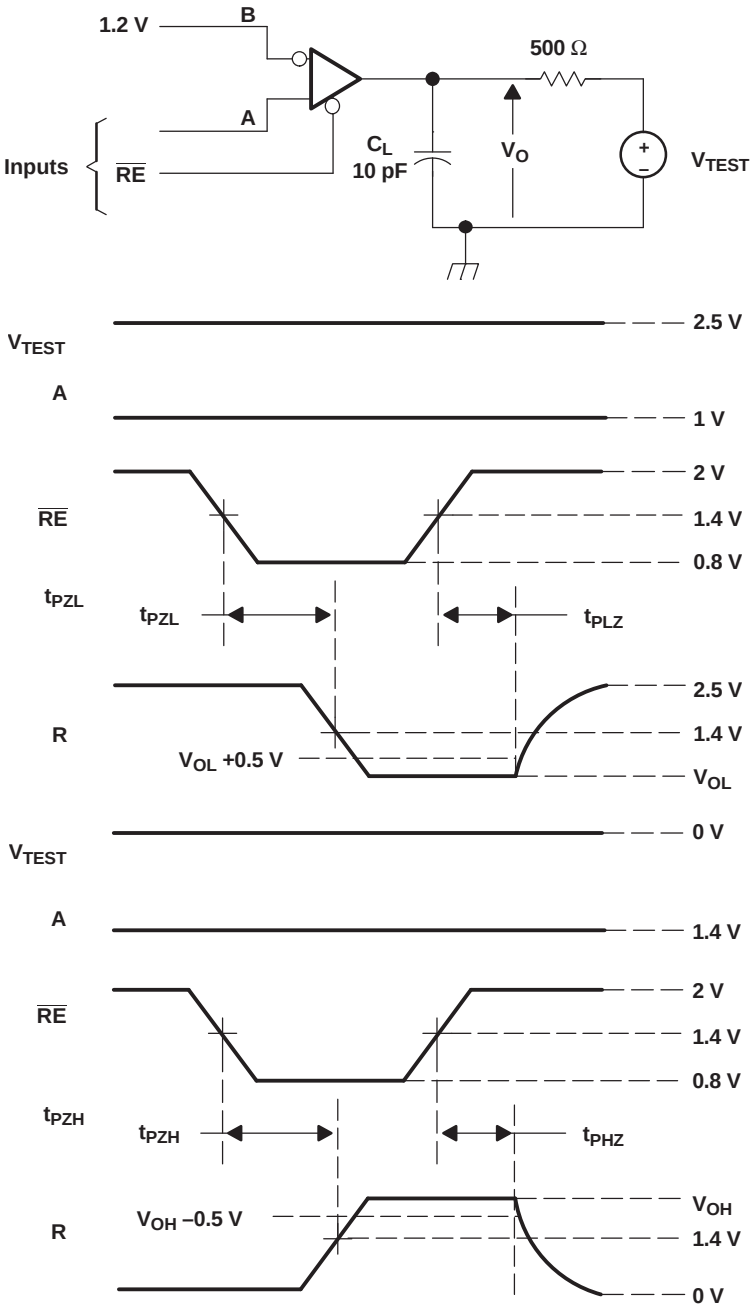
APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE
V_{IA} (V)	V_{IB} (V)	V_{ID} (mV)	V_{IC} (V)
1.25	1.15	100	1.2
1.15	1.25	–100	1.2
2.4	2.3	100	2.35
2.3	2.4	–100	2.35
0.1	0	100	0.05
0	0.1	–100	0.05
1.5	0.9	600	1.2
0.9	1.5	–600	1.2
2.4	1.8	600	2.1
1.8	2.4	–600	2.1
0.6	0	600	0.3
0	0.6	–600	0.3

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A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns. C_L includes instrumentation and fixture capacitance within 0.06 m of the device under test.

Figure 15. Timing Test Circuit and Waveforms



A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0.06 m of the device under test.

Figure 16. Enable or Disable Time Test Circuit and Waveforms

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10 Detailed Description

10.1 Overview

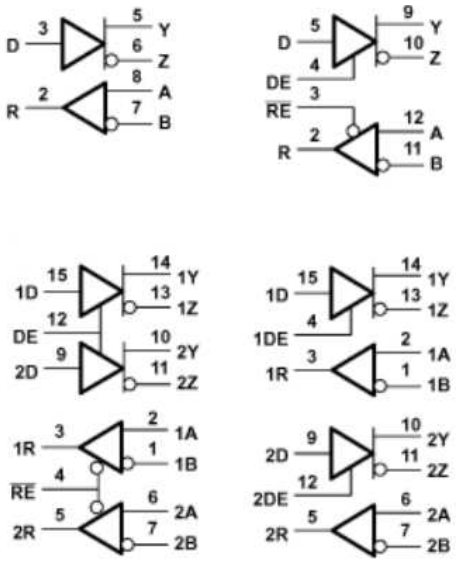
The SN65LVDSxxx devices are single- and dual-channel LVDS line drivers and receivers. They operate from a single supply that is nominally 3.3 V, but can be as low as 3.0 V and as high as 3.6 V.

The input signal to the drivers is an LVTTL signal. The output of the drivers is a differential signal complying with the LVDS standard (TIA/EIA-644). The driver differential output signal operates with a signal level of 340 mV, nominally, at a common-mode voltage of 1.2 V. This low differential output voltage results in a low emitted radiated energy, which is dependent on the signal slew rate. The differential nature of the output provides immunity to common-mode coupled signals that the driven signal may experience.

The SN65LVDSxxx devices are intended to drive a 100-Ω transmission line. This transmission line may be a printed-circuit board (PCB) or cabled interconnect. With transmission lines, the optimum signal quality and power delivery is reached when the transmission line is terminated with a load equal to the characteristic impedance of the interconnect. Likewise, the driven 100-Ω transmission line should be terminated with a matched resistance.

The SN65LVDSxxx devices also include LVDS line receivers. The input signal to the receivers is a differential LVDS signal. The output of the device is an LVTTL digital signal. This LVDS receivers require ±50 mV of input signal to determine the correct state of the received signal. Compliant LVDS receivers can accept input signals with a common-mode range between 0.025 V and 2.375 V. As the common-mode output voltage of an LVDS driver is 1.2 V, the SN65LVDSxxx receivers correctly determine the line state when operated with a 1-V ground shift between driver and receiver.

10.2 Functional Block Diagram



10.3 Feature Description

10.3.1 Driver Offset

An LVDS-compliant driver is required to maintain the common-mode output voltage at 1.2 V (±75 mV). The SN65LVDSxxx drivers incorporate sense circuitry and a control loop to source common-mode current and keep the output signal within specified values. Further, the device maintains the output common-mode voltage at this set point over the full 3.0-V to 3.6-V supply range.

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Feature Description (continued)

10.3.2 5-V Input Tolerance

5-V and 3.3-V TTL logic standards share the same input high-voltage and input low-voltage thresholds, namely 2.0 V and 0.8 V, respectively. Although the maximum supply voltage for the SN65LVDSxxx is 3.6 V, the driver can operate and meet all performance requirements when the input signals are as high as 5 V. This allows operation with 3.3-V TTL as well as 5-V TTL logic. 3.3-V CMOS and 5-V CMOS inputs are also allowable, although one should ensure that the duty-cycle distortion that will result from the TTL (ground-referenced) thresholds are acceptable.

10.3.3 NC Pins

NC (not connected) pins are pins where the die is not physically connected to the lead frame or package. For optimum thermal performance, a good rule of thumb is to ground the NC pins at the board level.

10.3.4 Driver Equivalent Schematics

The SN65LVDSxxx equivalent input and output schematic diagrams are shown in Figure 17. The driver input is represented by a CMOS inverter stage with a 7-V Zener diode. The input stage is high-impedance, and includes an internal pulldown to ground. If the driver input is left open, the driver input provides a low-level signal to the rest of the driver circuitry, resulting in a low-level signal at the driver output pins. The Zener diode provides ESD protection. The driver output stage is a differential pair, one half of which is shown in Figure 17. Like the input stage, the driver output includes Zener diodes for ESD protection. The schematic shows an output stage that includes a set of current sources (nominally 3.5 mA) that are connected to the output load circuit based upon the input stage signal. To the first order, the SN65LVDSxxx output stage acts a constant-current source.

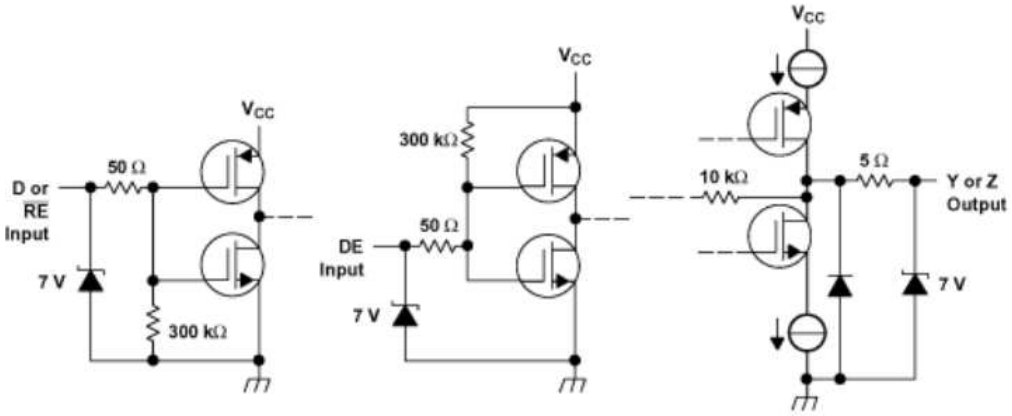


Figure 17. Equivalent Input and Output Schematic Diagrams

10.3.5 Receiver Features

10.3.5.1 Receiver Output States

When the receiver differential input signal is greater than 50 mV, the receiver output is high, and when the differential input voltage is below –50 mV, the receiver output is low. When the input voltage is between these thresholds (for example, between –50 mV and +50 mV), the receiver output is indeterminate. It may be high or low. A special case occurs when the input to the receiver is open-circuited, which is covered in *Receiver Open-Circuit Fail-Safe*. When the receiver is disabled, the receiver outputs will be high-impedance.

10.3.5.2 Receiver Open-Circuit Fail-Safe

One of the most common problems with differential signaling applications is how the system responds when no differential voltage is present on the signal pair. The LVDS receiver is like most differential line receivers in that its output logic state can be indeterminate when the differential input voltage is between –100 mV and 100 mV and within its recommended input common-mode voltage range. However, the SN65LVDSxxx receiver is different in how it handles the open-input circuit situation.

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Feature Description (continued)

Open circuit means that there is little or no input current to the receiver from the data line itself. This could be when the driver is in a high-impedance state or the cable is disconnected. When this occurs, the LVDS receiver pulls each line of the signal to V_{CC} through 300-kΩ resistors as shown in Figure 18. The fail-safe feature uses an AND gate with input voltage thresholds at about 2.3 V to detect this condition and force the output to a high level.

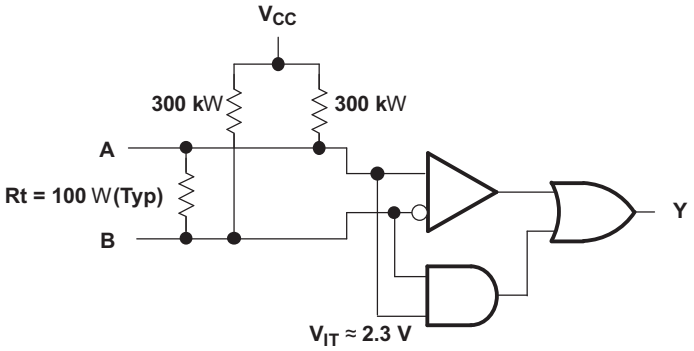


Figure 18. Open-Circuit Fail Safe of the LVDS Receiver

It is only under these conditions that the output of the receiver is valid with less than a 100-mV differential input voltage magnitude. The presence of the termination resistor, Rt does not affect the fail-safe function as long as it is connected as shown in Figure 18. Other termination circuits may allow a dc current to ground that could defeat the pullup currents from the receiver and the fail-safe feature.

10.3.5.3 Receiver Power-On Reset

The SN65LVDSxxx receivers include power-on reset circuitry. When the supply voltage drops below 1.5 V (or is turning on and has not yet reached 1.5 V), power-on reset circuitry sets the receiver input pins to a high-impedance state.

10.3.5.4 Common-Mode Range vs Supply Voltage

The SN65LVDSxxx receivers operate over an input common-mode range from $V_{ID}/2$ V to $(2.4 – V_{ID}/2)$ V. Hence, if the input signal is a minimum differential voltage of 50 mV, common-mode values in the range of 0.025 V to 2.375 V are supported.

10.3.5.5 General Purpose Comparator

While the SN65LVDSxxx are LVDS standard-compliant receivers, their utility and applications extend to a wider range of signals. As long as the input signals are within the required differential and common-mode voltage ranges mentioned above, the receiver output will be a faithful representation of the input signal.

10.3.5.6 Receiver Equivalent Schematics

The SN65LVDSxxx receiver equivalent input and output schematic diagrams are shown in Figure 19. The receiver input is a high-impedance differential pair. 7-V Zener diodes are included on each input to provide ESD protection. The receiver output structure shown is a CMOS inverter with an additional Zener diode, again for ESD protection.

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Feature Description (continued)

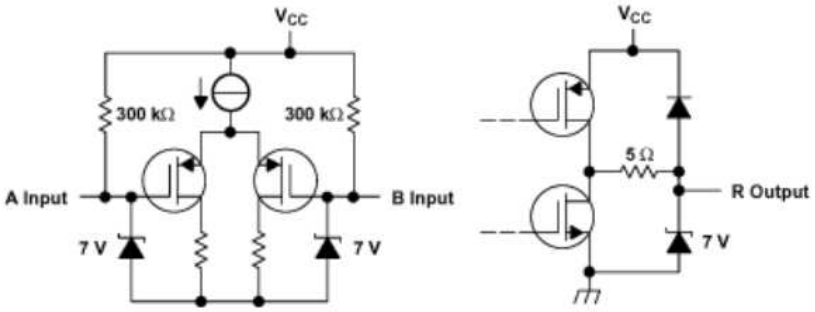


Figure 19. Equivalent Input and Output Schematic Diagrams

10.4 Device Functional Modes

10.4.1 Function Tables

Table 3. SN65LVDS179 Receiver

INPUTS	OUTPUT(1)
$V_{ID} = V_A - V_B$	R
$V_{ID} \geq 100$ mV	H
-100 mV $< V_{ID} < 100$ mV	?
$V_{ID} \leq -100$ mV	L
Open	H

(1) H = high level, L = low level, ? = indeterminate

Table 4. SN65LVDS179 Driver(1)

INPUT	OUTPUTS	
D	Y	Z
L	L	H
H	H	L
Open	L	H

(1) H = high level, L = low level

Table 5. SN65LVDS180, SN65LVDS050, and SN65LVDS051 Receivers(1)

INPUTS		OUTPUT
$V_{ID} = V_A - V_B$	$\overline{RE}$	R
$V_{ID} \geq 100$ mV	L	H
-100 mV $< V_{ID} < 100$ mV	L	?
$V_{ID} \leq -100$ mV	L	L
Open	L	H
X	H	Z

(1) H = high level, L = low level, Z = high-impedance, X = don't care, ? = indeterminate

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Table 6. SN65LVDS180, SN65LVDS050, and SN65LVDS051 Drivers(1)

INPUTS		OUTPUTS	
D	DE	Y	Z
L	H	L	H
H	H	H	L
Open	H	L	H
X	L	Off	Off

(1) H = high level, L = low level, Z = high-impedance, X = don't care, Off = no output

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11 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

11.1 Application Information

The SNx5LVDSxx are LVDS drivers and receivers. These devices are generally used as building blocks for high-speed, point-to-point, data transmission where ground differences are less than 1 V. LVDS drivers and receivers provide high-speed signaling rates that are often implemented with ECL class devices without the ECL power and dual-supply requirements.

11.2 Typical Application

The most basic application for LVDS buffers, as found in this data sheet, is for point-to-point communications of digital data, as shown in Figure 20.

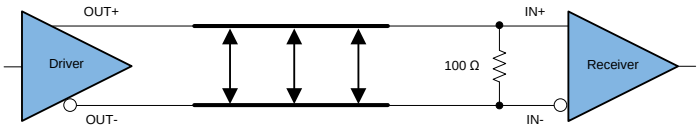


Figure 20. Point-to-Point Topology

A point-to-point communications channel has a single transmitter (driver) and a single receiver. This communications topology is often referred to as simplex. In Figure 20 the driver receives a single-ended input signal and the receiver outputs a single-ended recovered signal. The LVDS driver converts the single-ended input to a differential signal for transmission over a balanced interconnecting media of 100-Ω characteristic impedance. The conversion from a single-ended signal to an LVDS signal retains the digital data payload while translating to a signal whose features are more appropriate for communication over extended distances or in a noisy environment.

11.2.1 Design Requirements

DESIGN PARAMETERS	EXAMPLE VALUE
Driver Supply Voltage (V_{CCD})	3.0 to 3.6 V
Driver Input Voltage	0.8 to 3.3 V
Driver Signaling Rate	DC to 100 Mbps
Interconnect Characteristic Impedance	100 Ω
Termination Resistance	100 Ω
Number of Receiver Nodes	1
Receiver Supply Voltage (V_{CCR})	3.0 to 3.6 V
Receiver Input Voltage	0 to 2.4 V
Receiver Signaling Rate	DC to 100 Mbps
Ground shift between driver and receiver	±1 V

11.2.2 Detailed Design Procedure

11.2.2.1 Equipment

- Hewlett Packard HP6624A DC power supply
- Tektronix TDS7404 Real Time Scope
- Agilent ParBERT E4832A

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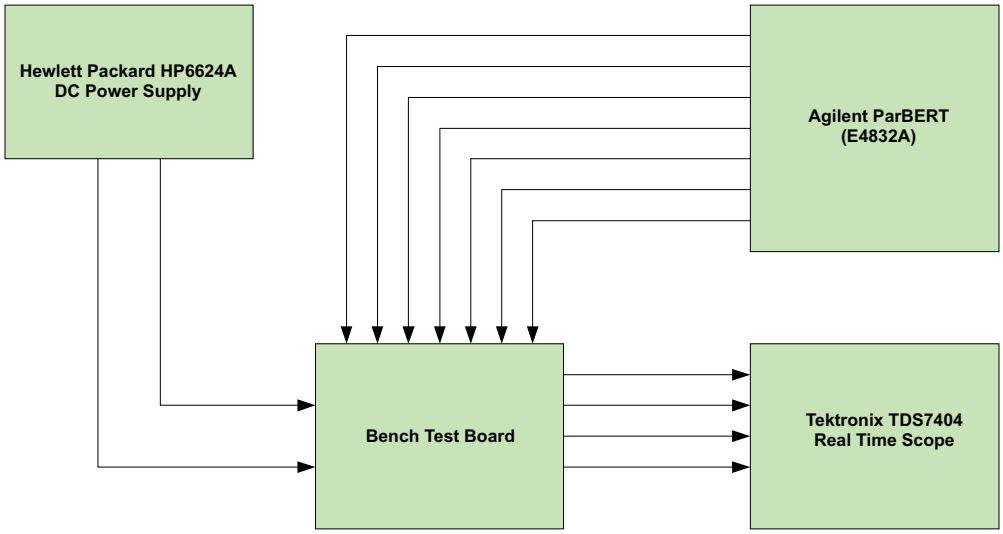


Figure 21. Equipment Setup

11.2.2.2 Driver Supply Voltage

An LVDS driver is operated from a single supply. The device can support operation with a supply as low as 3 V and as high as 3.6 V. The differential output voltage is nominally 340 mV over the complete output range. The minimum output voltage stays within the specified LVDS limits (247 mV to 454 mV) for the complete 3-V to 3.6-V supply range.

11.2.2.3 Driver Bypass Capacitance

Bypass capacitors play a key role in power distribution circuitry. Specifically, they create low-impedance paths between power and ground. At low frequencies, a good digital power supply offers very-low-impedance paths between its terminals. However, as higher frequency currents propagate through power traces, the source is quite often incapable of maintaining a low-impedance path to ground. Bypass capacitors are used to address this shortcoming. Usually, large bypass capacitors (10 to 1000 µF) at the board-level do a good job up into the kHz range. Due to their size and length of their leads, they tend to have large inductance values at the switching frequencies of modern digital circuitry. To solve this problem, one should resort to the use of smaller capacitors (nF to µF range) installed locally next to the integrated circuit.

Multilayer ceramic chip or surface-mount capacitors (size 0603 or 0805) minimize lead inductances of bypass capacitors in high-speed environments, because their lead inductance is about 1 nH. For comparison purposes, a typical capacitor with leads has a lead inductance around 5 nH.

The value of the bypass capacitors used locally with LVDS chips can be determined by the following formula according to Johnson(1), equations 8.18 to 8.21. A conservative rise time of 200 ps and a worst-case change in supply current of 1 A covers the whole range of LVDS devices offered by Texas Instruments. In this example, the maximum power supply noise tolerated is 200 mV; however, this figure varies depending on the noise budget available in your design. (1)

$$C_{chip} = \left(\frac{\Delta I_{Maximum\ Step\ Change\ Supply\ Current}}{\Delta V_{Maximum\ Power\ Supply\ Noise}} \right) \times T_{Rise\ Time} \quad (1)$$

$$C_{LVDS} = \left(\frac{1A}{0.2V} \right) \times 200\ ps = 0.001\ \mu F \quad (2)$$

The following example lowers lead inductance and covers intermediate frequencies between the board-level capacitor (>10 µF) and the value of capacitance found above (0.001 µF). You should place the smallest value of capacitance as close as possible to the chip.

(1) Howard Johnson & Martin Graham.1993. High Speed Digital Design – A Handbook of Black Magic. Prentice Hall PRT. ISBN number 013395724.

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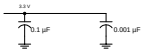


Figure 22. Recommended LVDS Bypass Capacitor Layout

11.2.2.4 Driver Output Voltage

The LVDS driver output is a 1.2-V common-mode voltage, with a nominal differential output signal of 340 mV. This 340 mV is the absolute value of the differential swing (V_{OD} = $|V^+ – V^–|$). The peak-to-peak differential voltage is twice this value, or 680 mV.

11.2.2.5 Interconnecting Media

The physical communication channel between the driver and the receiver may be any balanced paired metal conductors meeting the requirements of the LVDS standard, the key points which will be included here. This media may be a twisted pair, twinax, flat ribbon cable, or PCB traces.

The nominal characteristic impedance of the interconnect should be between 100 Ω and 120 Ω with variation no more than 10% (90 Ω to 132 Ω).

11.2.2.6 PCB Transmission Lines

As per SNLA187, Figure 23 depicts several transmission line structures commonly used in printed-circuit boards (PCBs). Each structure consists of a signal line and a return path with uniform cross-section along its length. A microstrip is a signal trace on the top (or bottom) layer, separated by a dielectric layer from its return path in a ground or power plane. A stripline is a signal trace in the inner layer, with a dielectric layer in between a ground plane above and below the signal trace. The dimensions of the structure along with the dielectric material properties determine the characteristic impedance of the transmission line (also called controlled-impedance transmission line).

When two signal lines are placed close by, they form a pair of coupled transmission lines. Figure 23 shows examples of edge-coupled microstrips, and edge-coupled or broad-side-coupled striplines. When excited by differential signals, the coupled transmission line is referred to as a differential pair. The characteristic impedance of each line is called odd-mode impedance. The sum of the odd-mode impedances of each line is the differential impedance of the differential pair. In addition to the trace dimensions and dielectric material properties, the spacing between the two traces determines the mutual coupling and impacts the differential impedance. When the two lines are immediately adjacent; for example, S is less than 2W, the differential pair is called a tightly-coupled differential pair. To maintain constant differential impedance along the length, it is important to keep the trace width and spacing uniform along the length, as well as maintain good symmetry between the two lines.

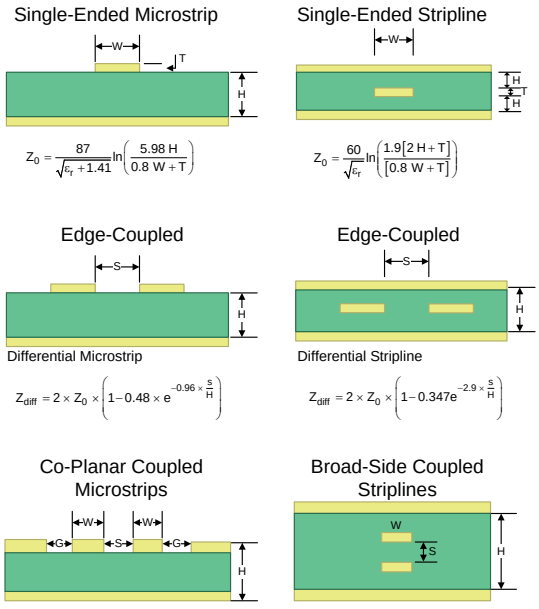


Figure 23. Controlled-Impedance Transmission Lines

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11.2.2.7 Termination Resistor

An LVDS communication channel employs a current source driving a transmission line which is terminated with a resistive load. This load serves to convert the transmitted current into a voltage at the receiver input. To ensure incident wave switching (which is necessary to operate the channel at the highest signaling rate), the termination resistance should be matched to the characteristic impedance of the transmission line. The designer should ensure that the termination resistance is within 10% of the nominal media characteristic impedance. If the transmission line is targeted for 100-Ω impedance, the termination resistance should be between 90 and 110 Ω.

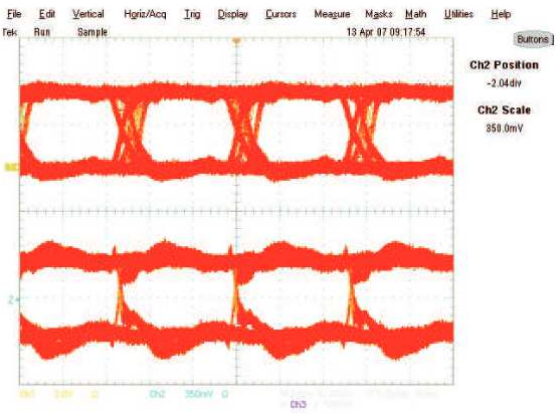
The line termination resistance should be located as close as possible to the receiver, thereby minimizing the stub length from the resistor to the receiver. The limiting case would be to incorporate the termination resistor into the receiver, which is exactly what is offered with the TI ‘LVDT receivers.

While we talk in this section about point-to-point communications, a word of caution is useful when a multidrop topology is used. In such topologies, line termination resistors are to be located only at the end(s) of the transmission line. In such an environment, LVDS receivers could be used for loads branching off the main bus, with an LVDT receiver used only at the bus end.

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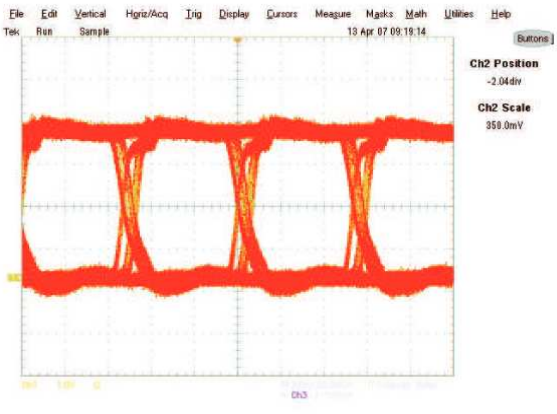
11.2.3 Application Curves

Unless otherwise specified: T = 25°C; V_{CC} = 3.6 V; PRBS = $2^{23} - 1$



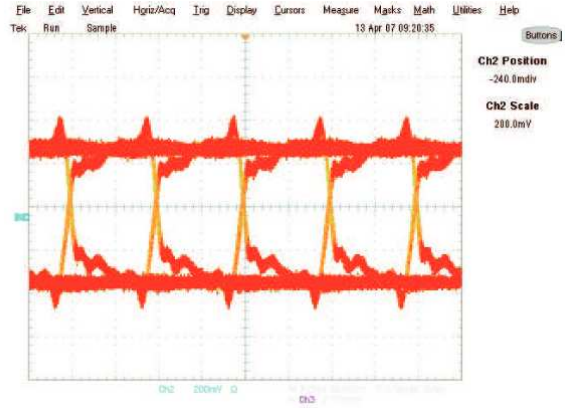
Tx + Rx running at 150 Mbps; Channel 1: R, Channel 2: Y-Z

Figure 24. Typical Eye Pattern SN65LVDS179: Tx + Rx



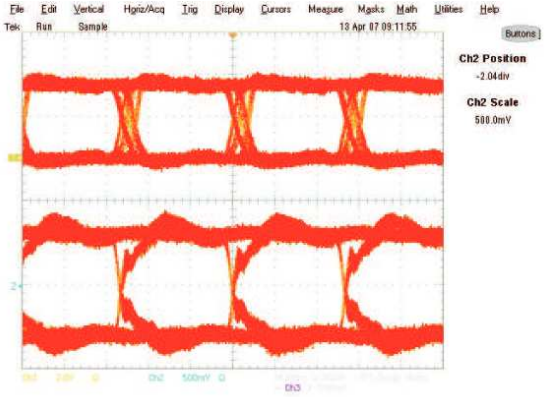
Rx only running at 150 Mbps; Channel 1: R

Figure 25. Typical Eye Pattern SN65LVDS179: Rx



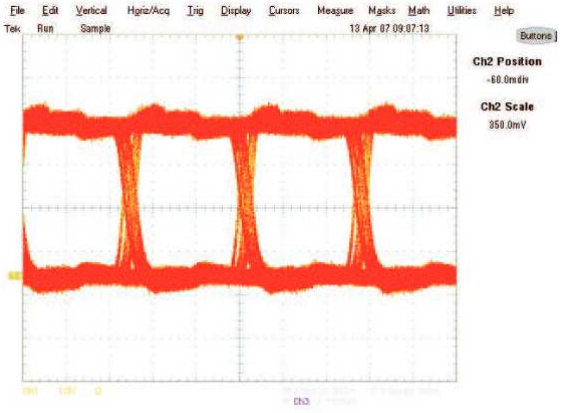
Tx only running at 400 Mbps; Channel 1: Y-Z

Figure 26. Typical Eye Pattern SN65LVDS179: Tx



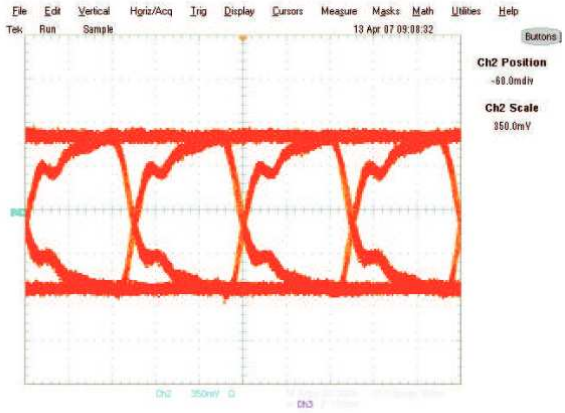
Tx + Rx running at 150 Mbps; Channel 1: R, Channel 2: Y-Z

Figure 27. Typical Eye Pattern SN65LVDS180: Tx + Rx



Rx only running at 150 Mbps; Channel 1: R

Figure 28. Typical Eye Pattern SN65LVDS180: Rx

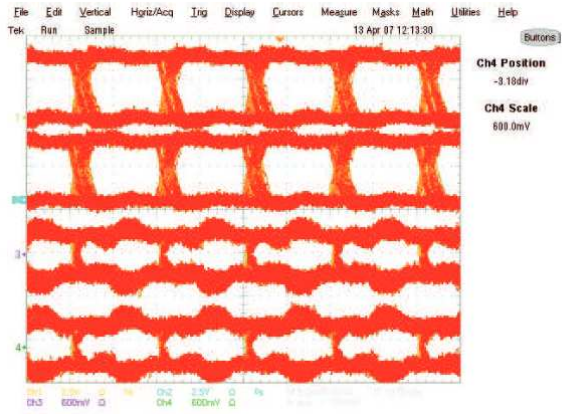


Tx only running at 400 Mbps; Channel 1: Y-Z

Figure 29. Typical Eye Pattern SN65LVDS180: Tx

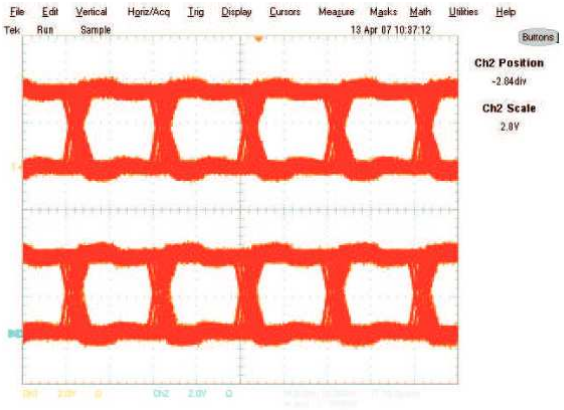
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Unless otherwise specified: T = 25°C; V_{CC} = 3.6 V; PRBS = $2^{23} - 1$



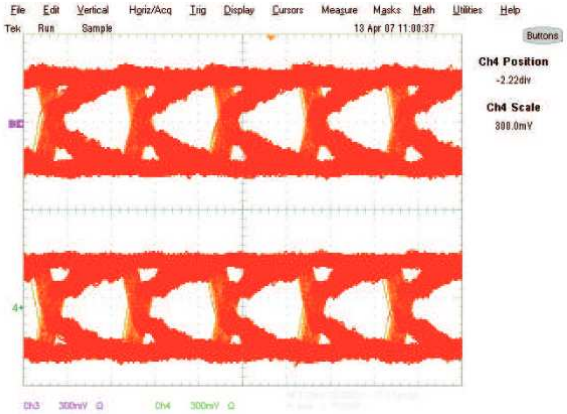
All buffers running at 100 Mbps; Channel 1: R, Channel 2: 2R, Channel 3: 1Y-1Z, Channel 4: 2Y-2Z

Figure 30. Typical Eye Pattern SN65LVDS050: All Buffers



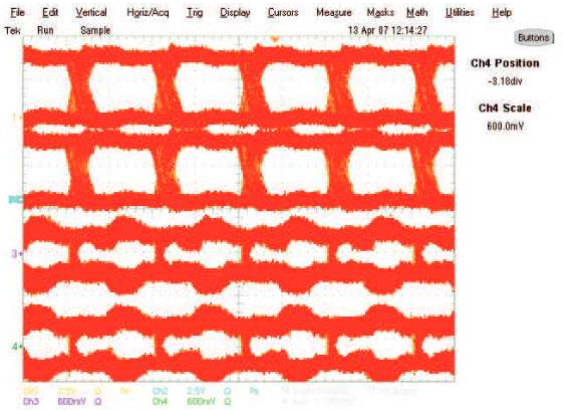
Rx buffers only running at 100 Mbps; Channel 1: R, Channel 2: 2R

Figure 31. Typical Eye Pattern SN65LVDS050: Rx Buffers



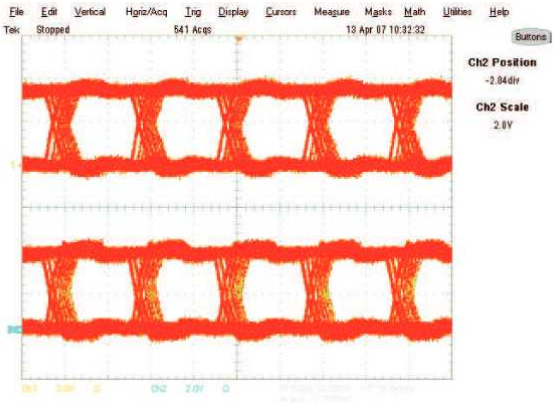
Tx buffers only running at 400 Mbps; Channel 3: 1Y-1Z, Channel 4: 2Y-2Z

Figure 32. Typical Eye Pattern SN65LVDS050: Tx Buffers



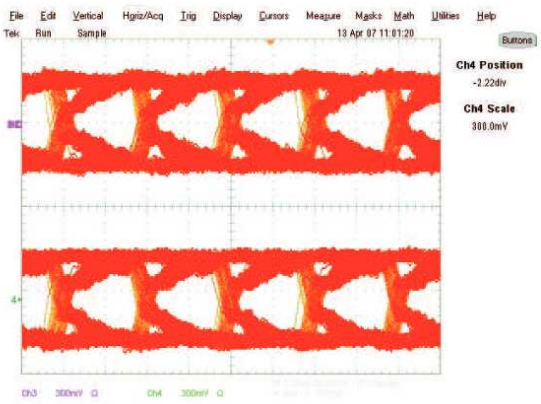
All buffers running at 100 Mbps; Channel 1: R, Channel 2: 2R, Channel 3: 1Y-1Z, Channel 4: 2Y-2Z

Figure 33. Typical Eye Pattern SN65LVDS051: All Buffers



Rx buffers only running at 100 Mbps; Channel 1: R, Channel 2: 2R

Figure 34. Typical Eye Pattern SN65LVDS051: Rx Buffers



Tx buffers only running at 400 Mbps; Channel 3: 1Y-1Z, Channel 4: 2Y-2Z

Figure 35. Typical Eye Pattern SN65LVDS051: Tx Buffers

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12 Power Supply Recommendations

The LVDS driver and receivers in this data sheet are designed to operate from a single power supply. Both drivers and receivers operate with supply voltages in the range of 3.0 V to 3.6 V. In a typical application, a driver and a receiver may be on separate boards, or even separate equipment. In these cases, separate supplies would be used at each location. The expected ground potential difference between the driver power supply and the receiver power supply would be less than |±1 V|. Board level and local device level bypass capacitance should be used and are covered in *Driver Bypass Capacitance*.

13 Layout

13.1 Layout Guidelines

13.1.1 Microstrip vs. Stripline Topologies

As per SLLD009, printed-circuit boards usually offer designers two transmission line options: Microstrip and stripline. Microstrips are traces on the outer layer of a PCB, as shown in Figure 36.

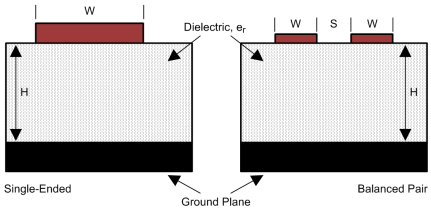


Figure 36. Microstrip Topology

On the other hand, striplines are traces between two ground planes. Striplines are less prone to emissions and susceptibility problems because the reference planes effectively shield the embedded traces. However, from the standpoint of high-speed transmission, juxtaposing two planes creates additional capacitance. TI recommends routing LVDS signals on microstrip transmission lines, if possible. The PCB traces allow designers to specify the necessary tolerances for Z_O based on the overall noise budget and reflection allowances. Footnotes 1(1), 2(2), and 3(3) provide formulas for Z_O and t_{PD} for differential and single-ended traces. (1) (2) (3)

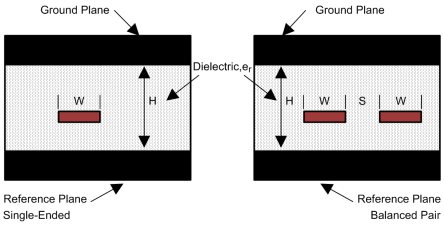


Figure 37. Stripline Topology

13.1.2 Dielectric Type and Board Construction

The speeds at which signals travel across the board dictates the choice of dielectric. FR-4, or equivalent, usually provides adequate performance for use with LVDS signals. If rise or fall times of TTL/CMOS signals are less than 500 ps, empirical results indicate that a material with a dielectric constant near 3.4, such as Rogers™ 4350 or Nelco N4000-13 is better suited. Once the designer chooses the dielectric, there are several parameters pertaining to the board construction that can affect performance. The following set of guidelines were developed experimentally through several designs involving LVDS devices:

- Copper weight: 15 g or 1/2 oz start, plated to 30 g or 1 oz
- All exposed circuitry should be solder-plated (60/40) to 7.62 µm or 0.0003 in (minimum).

(1) Howard Johnson & Martin Graham.1993. High Speed Digital Design – A Handbook of Black Magic. Prentice Hall PRT. ISBN number 013395724.
(2) Mark I. Montrose. 1996. Printed Circuit Board Design Techniques for EMC Compliance. IEEE Press. ISBN number 0780311310.
(3) Clyde F. Coombs, Jr. Ed, Printed Circuits Handbook, McGraw Hill, ISBN number 0070127549.

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Layout Guidelines (continued)

- Copper plating should be 25.4 µm or 0.001 in (minimum) in plated-through-holes.
- Solder mask over bare copper with solder hot-air leveling

13.1.3 Recommended Stack Layout

Following the choice of dielectrics and design specifications, you should decide how many levels to use in the stack. To reduce the TTL/CMOS to LVDS crosstalk, it is a good practice to have at least two separate signal planes as shown in Figure 38.

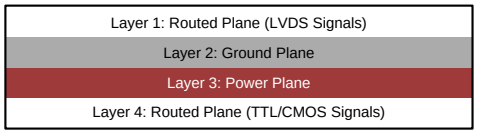


Figure 38. Four-Layer PCB Board

NOTE

The separation between layers 2 and 3 should be 127 µm (0.005 in). By keeping the power and ground planes tightly coupled, the increased capacitance acts as a bypass for transients.

One of the most common stack configurations is the six-layer board, as shown in Figure 39.

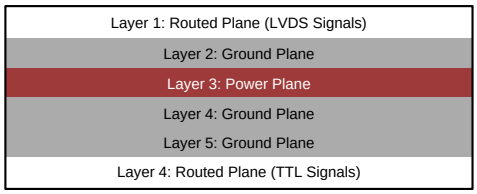


Figure 39. Six-Layer PCB Board

In this particular configuration, it is possible to isolate each signal layer from the power plane by at least one ground plane. The result is improved signal integrity; however, fabrication is more expensive. Using the 6-layer board is preferable, because it offers the layout designer more flexibility in varying the distance between signal layers and referenced planes, in addition to ensuring reference to a ground plane for signal layers 1 and 6.

13.1.4 Separation Between Traces

The separation between traces depends on several factors; however, the amount of coupling that can be tolerated usually dictates the actual separation. Low-noise coupling requires close coupling between the differential pair of an LVDS link to benefit from the electromagnetic field cancellation. The traces should be 100-Ω differential and thus coupled in the manner that best fits this requirement. In addition, differential pairs should have the same electrical length to ensure that they are balanced, thus minimizing problems with skew and signal reflection.

In the case of two adjacent single-ended traces, one should use the 3-W rule, which stipulates that the distance between two traces should be greater than two times the width of a single trace, or three times its width measured from trace center to trace center. This increased separation effectively reduces the potential for crosstalk. The same rule should be applied to the separation between adjacent LVDS differential pairs, whether the traces are edge-coupled or broad-side-coupled.

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Layout Guidelines (continued)

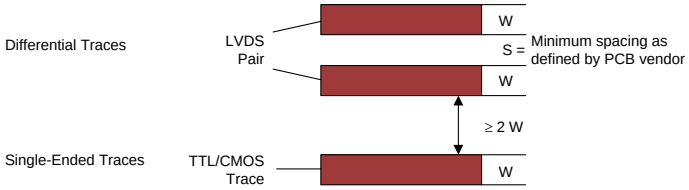


Figure 40. 3-W Rule for Single-Ended and Differential Traces (Top View)

You should exercise caution when using autorouters, because they do not always account for all factors affecting crosstalk and signal reflection. For instance, it is best to avoid sharp 90° turns to prevent discontinuities in the signal path. Using successive 45° turns tends to minimize reflections.

13.1.5 Crosstalk and Ground Bounce Minimization

To reduce crosstalk, it is important to provide a return path to high-frequency currents that is as close as possible to its originating trace. A ground plane usually achieves this. Because the returning currents always choose the path of lowest inductance, they are most likely to return directly under the original trace, thus minimizing crosstalk. Lowering the area of the current loop lowers the potential for crosstalk. Traces kept as short as possible with an uninterrupted ground plane running beneath them emit the minimum amount of electromagnetic field strength. Discontinuities in the ground plane increase the return path inductance and should be avoided.

13.2 Layout Example

At least two or three times the width of an individual trace should separate single-ended traces and differential pairs to minimize the potential for crosstalk. Single-ended traces that run in parallel for less than the wavelength of the rise or fall times usually have negligible crosstalk. Increase the spacing between signal paths for long parallel runs to reduce crosstalk. Boards with limited real estate can benefit from the staggered trace layout, as shown in Figure 41.

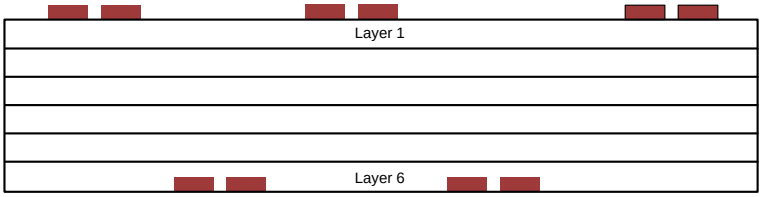


Figure 41. Staggered Trace Layout

This configuration lays out alternating signal traces on different layers; thus, the horizontal separation between traces can be less than 2 or 3 times the width of individual traces. To ensure continuity in the ground signal path, TI recommends having an adjacent ground via for every signal via, as shown in Figure 42. Note that vias create additional capacitance. For example, a typical via has a lumped capacitance effect of 1/2 pF to 1 pF in FR4.

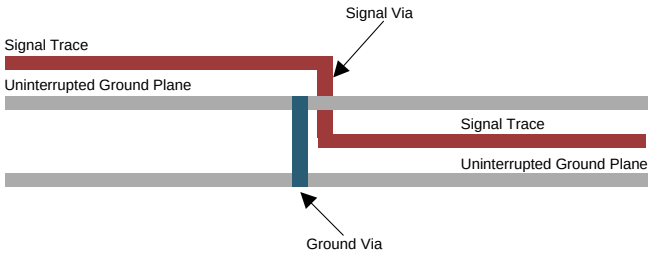


Figure 42. Ground Via Location (Side View)

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Layout Example (continued)

Short and low-impedance connection of the device ground pins to the PCB ground plane reduces ground bounce. Holes and cutouts in the ground planes can adversely affect current return paths if they create discontinuities that increase returning current loop areas.

To minimize EMI problems, TI recommends avoiding discontinuities below a trace (for example, holes, slits, and so on) and keeping traces as short as possible. Zoning the board wisely by placing all similar functions in the same area, as opposed to mixing them together, helps reduce susceptibility issues.

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14 Device and Documentation Support

14.1 Device Support

14.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

14.1.2 Other LVDS Products

For other products and application notes in the LVDS and LVDM product families visit our Web site at http://www.ti.com/sc/datatran.

14.2 Documentation Support

14.2.1 Related Information

IBIS modeling is available for this device. Contact the local TI sales office or the TI Web site at www.ti.com for more information.

For more application guidelines, see the following documents:

- *Low-Voltage Differential Signaling Design Notes* (SLLA014)
- *Interface Circuits for TIA/EIA-644* (LVDS) (SLLA038)
- *Reducing EMI With LVDS* (SLLA030)
- *Slew Rate Control of LVDS Circuits* (SLLA034)
- *Using an LVDS Receiver With RS-422 Data* (SLLA031)
- *Evaluating the LVDS EVM* (SLLA033)

14.3 Related Links

Table 7 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 7. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN65LVDS179	Click here	Click here	Click here	Click here	Click here
SN65LVDS180	Click here	Click here	Click here	Click here	Click here
SN65LVDS050	Click here	Click here	Click here	Click here	Click here
SN65LVDS051	Click here	Click here	Click here	Click here	Click here

14.4 Trademarks

Rogers is a trademark of Rogers Corporation.
All other trademarks are the property of their respective owners.

14.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

14.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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15 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65LVDS050D	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS050
SN65LVDS050D.B	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS050
SN65LVDS050DG4	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS050
SN65LVDS050DR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS050
SN65LVDS050DR.B	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS050
SN65LVDS050PW	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-	LVDS050
SN65LVDS050PW.B	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS050
SN65LVDS050PWG4	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS050
SN65LVDS050PWG4.B	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS050
SN65LVDS050PWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	LVDS050
SN65LVDS050PWR.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS050
SN65LVDS051D	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS051
SN65LVDS051D.B	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS051
SN65LVDS051DR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS051
SN65LVDS051DR.B	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS051
SN65LVDS051PW	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS051
SN65LVDS051PW.B	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS051
SN65LVDS051PWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS051
SN65LVDS051PWR.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS051
SN65LVDS179D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DL179
SN65LVDS179D.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DL179
SN65LVDS179DGK	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	S79
SN65LVDS179DGK.B	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	S79
SN65LVDS179DGKG4	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	S79
SN65LVDS179DGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	S79
SN65LVDS179DGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	S79
SN65LVDS179DGKRG4	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	S79
SN65LVDS179DGKRG4.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	S79
SN65LVDS179DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DL179

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65LVDS179DR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DL179
SN65LVDS179DRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DL179
SN65LVDS179DRG4.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DL179
SN65LVDS180D	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS180
SN65LVDS180D.B	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS180
SN65LVDS180DG4	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS180
SN65LVDS180DR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS180
SN65LVDS180DR.B	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS180
SN65LVDS180DRG4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS180
SN65LVDS180PW	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS180
SN65LVDS180PW.B	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS180
SN65LVDS180PWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS180
SN65LVDS180PWR.B	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS180
SN65LVDS180PWRG4	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS180

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN65LVDS050, SN65LVDS051, SN65LVDS179, SN65LVDS180 :

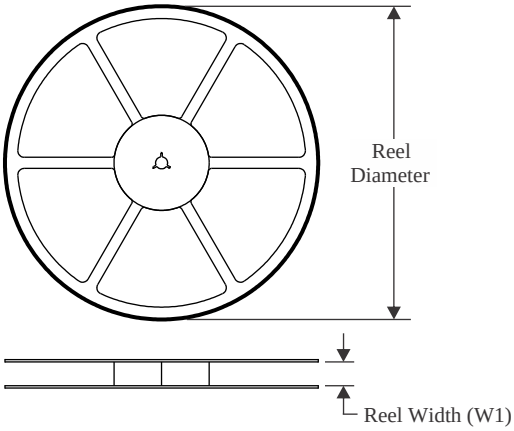
- Automotive : SN65LVDS050-Q1, SN65LVDS051-Q1, SN65LVDS180-Q1
- Enhanced Product : SN65LVDS179-EP

NOTE: Qualified Version Definitions:

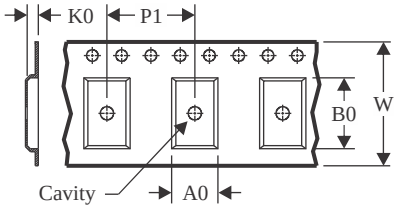
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

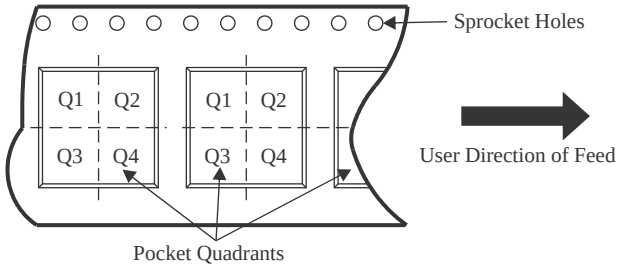


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

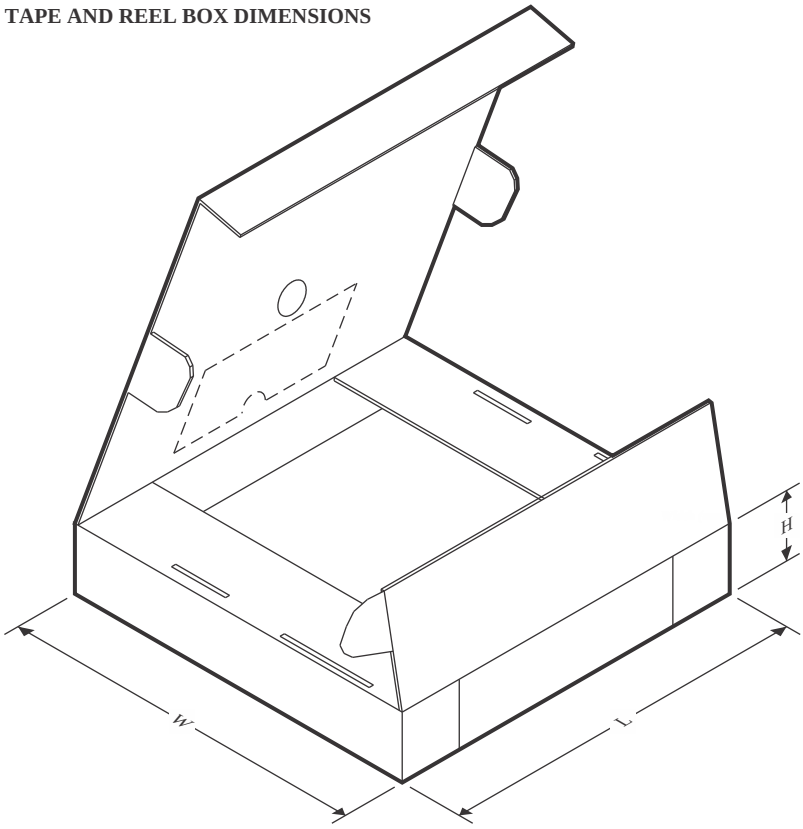
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDS050DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN65LVDS050PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN65LVDS051DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN65LVDS051PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN65LVDS179DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65LVDS179DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65LVDS179DGKRG4	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65LVDS179DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65LVDS179DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65LVDS180DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN65LVDS180PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

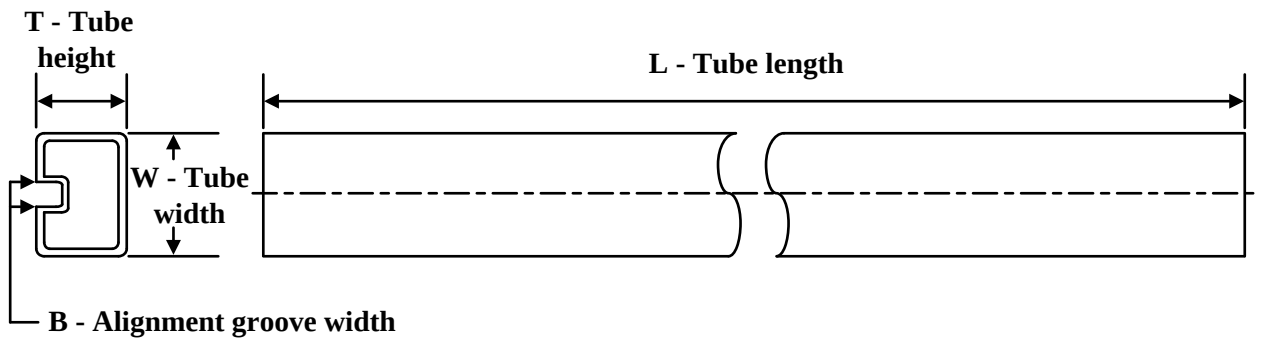
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVDS050DR	SOIC	D	16	2500	350.0	350.0	43.0
SN65LVDS050PWR	TSSOP	PW	16	2000	350.0	350.0	43.0
SN65LVDS051DR	SOIC	D	16	2500	350.0	350.0	43.0
SN65LVDS051PWR	TSSOP	PW	16	2000	350.0	350.0	43.0
SN65LVDS179DGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
SN65LVDS179DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
SN65LVDS179DGKRG4	VSSOP	DGK	8	2500	353.0	353.0	32.0
SN65LVDS179DR	SOIC	D	8	2500	353.0	353.0	32.0
SN65LVDS179DRG4	SOIC	D	8	2500	353.0	353.0	32.0
SN65LVDS180DR	SOIC	D	14	2500	350.0	350.0	43.0
SN65LVDS180PWR	TSSOP	PW	14	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

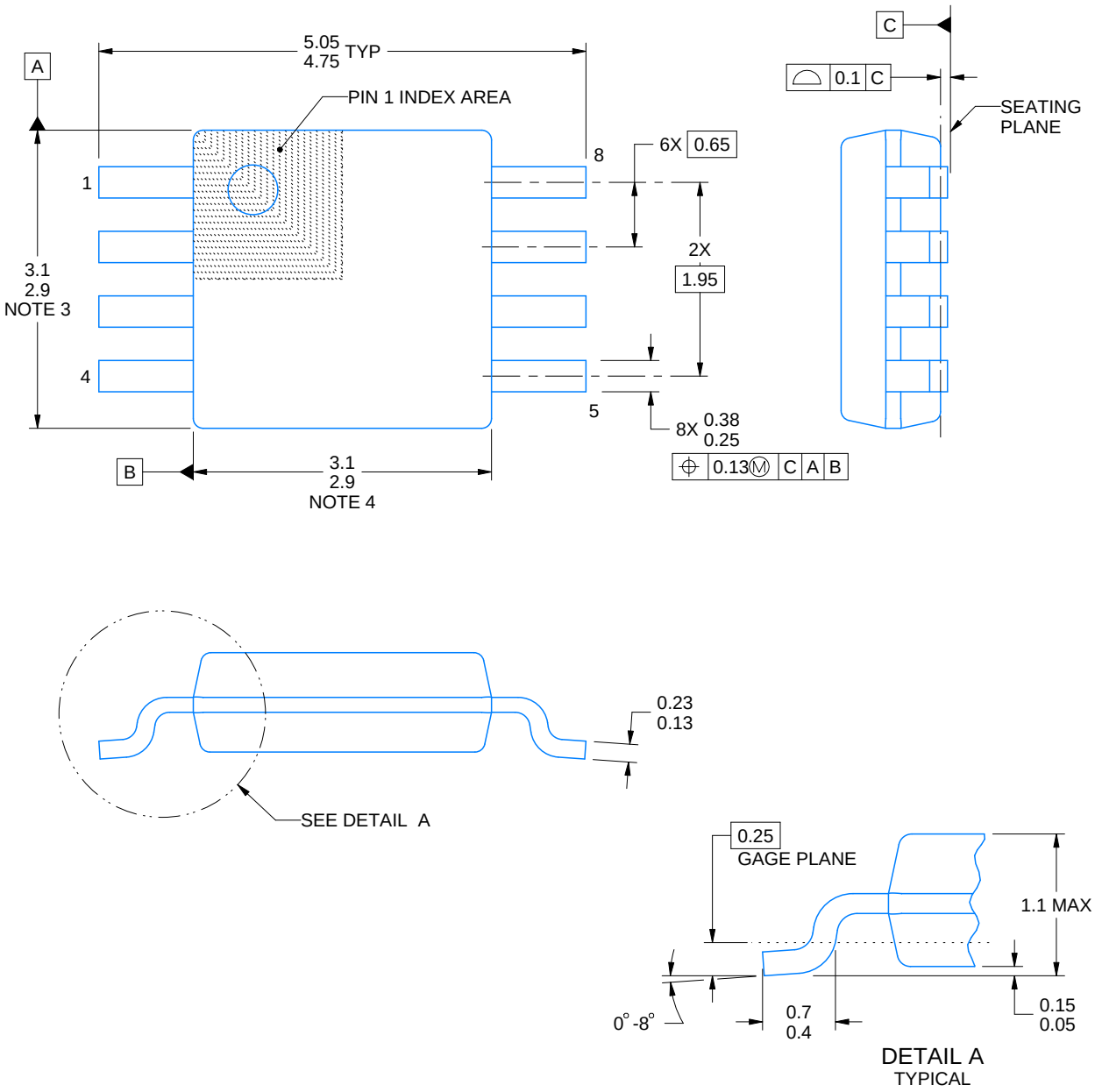
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65LVDS050D	D	SOIC	16	40	505.46	6.76	3810	4
SN65LVDS050D.B	D	SOIC	16	40	505.46	6.76	3810	4
SN65LVDS050DG4	D	SOIC	16	40	505.46	6.76	3810	4
SN65LVDS050PW	PW	TSSOP	16	90	530	10.2	3600	3.5
SN65LVDS050PW.B	PW	TSSOP	16	90	530	10.2	3600	3.5
SN65LVDS050PWG4	PW	TSSOP	16	90	530	10.2	3600	3.5
SN65LVDS050PWG4.B	PW	TSSOP	16	90	530	10.2	3600	3.5
SN65LVDS051D	D	SOIC	16	40	505.46	6.76	3810	4
SN65LVDS051D.B	D	SOIC	16	40	505.46	6.76	3810	4
SN65LVDS051PW	PW	TSSOP	16	90	530	10.2	3600	3.5
SN65LVDS051PW.B	PW	TSSOP	16	90	530	10.2	3600	3.5
SN65LVDS179D	D	SOIC	8	75	505.46	6.76	3810	4
SN65LVDS179D	D	SOIC	8	75	507	8	3940	4.32
SN65LVDS179D.B	D	SOIC	8	75	505.46	6.76	3810	4
SN65LVDS179D.B	D	SOIC	8	75	507	8	3940	4.32
SN65LVDS180D	D	SOIC	14	50	505.46	6.76	3810	4
SN65LVDS180D.B	D	SOIC	14	50	505.46	6.76	3810	4
SN65LVDS180DG4	D	SOIC	14	50	505.46	6.76	3810	4
SN65LVDS180PW	PW	TSSOP	14	90	530	10.2	3600	3.5
SN65LVDS180PW.B	PW	TSSOP	14	90	530	10.2	3600	3.5

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

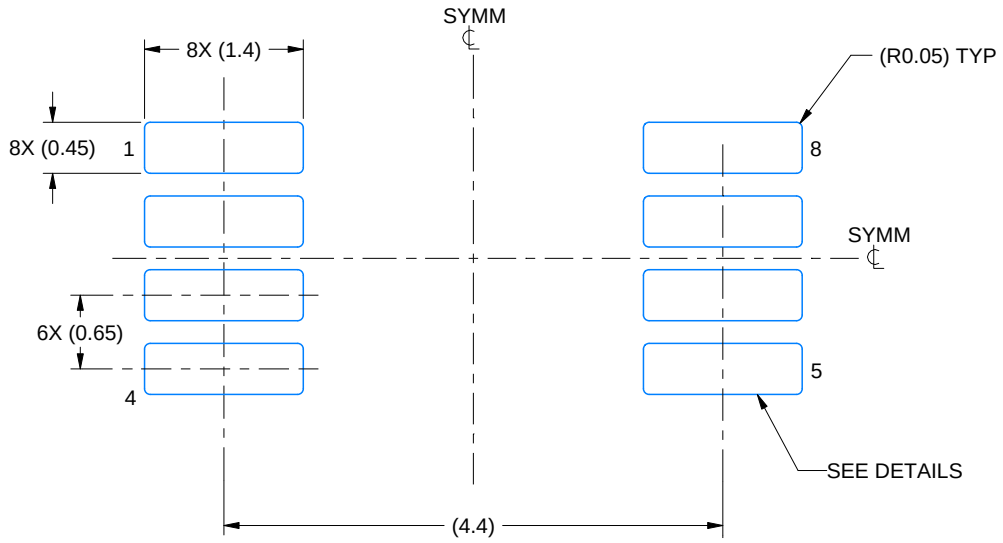
SMALL OUTLINE PACKAGE



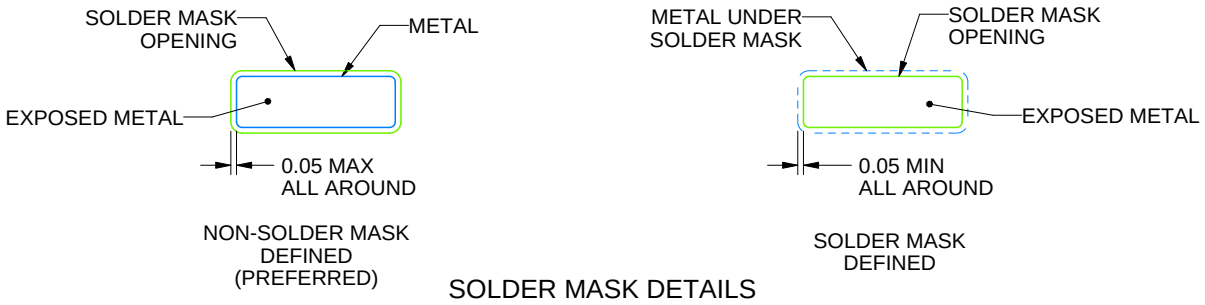
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

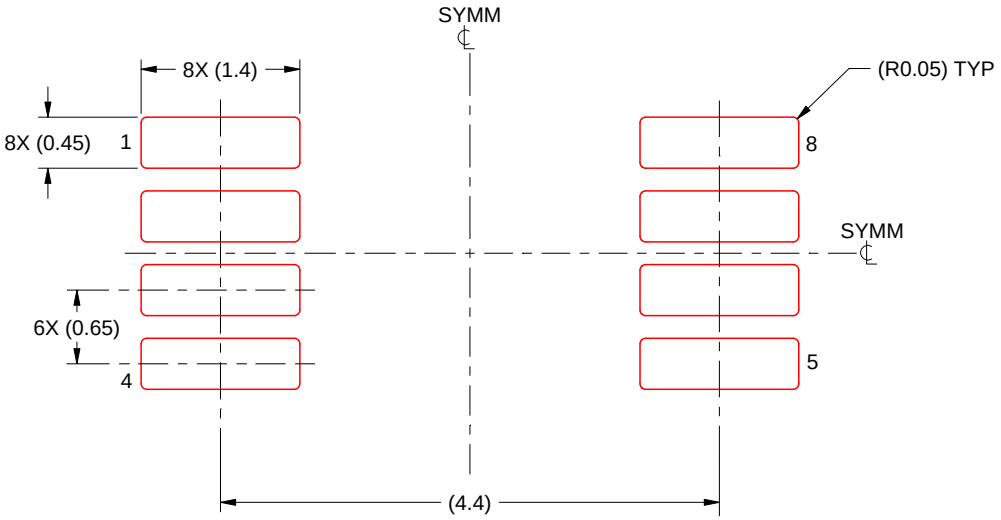


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

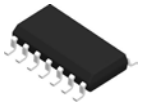


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

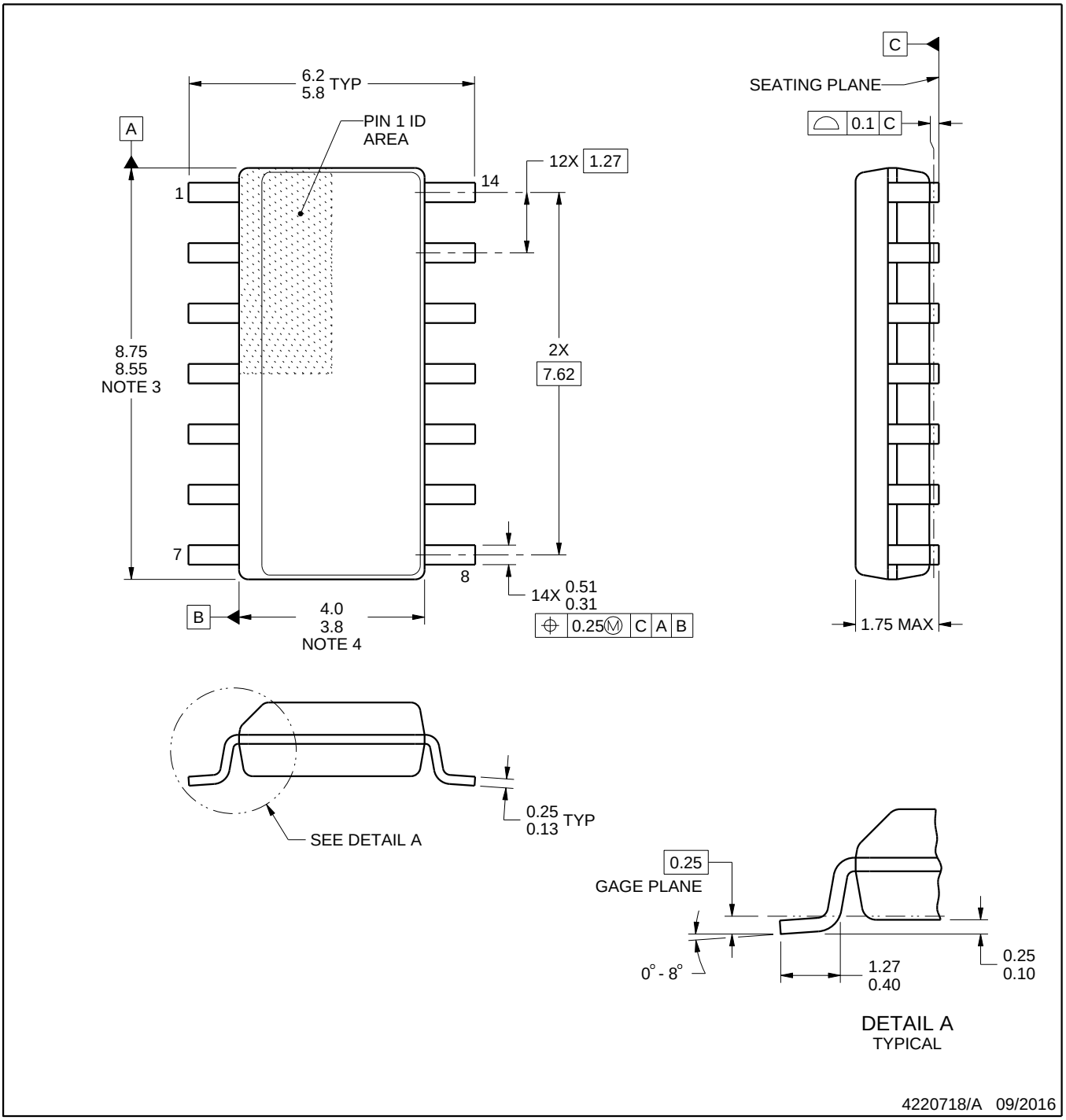


PACKAGE OUTLINE

D0014A

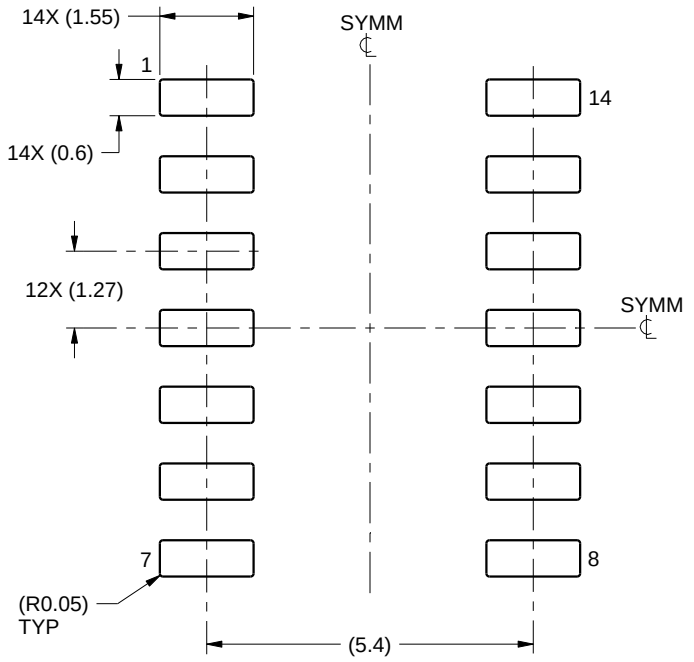
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

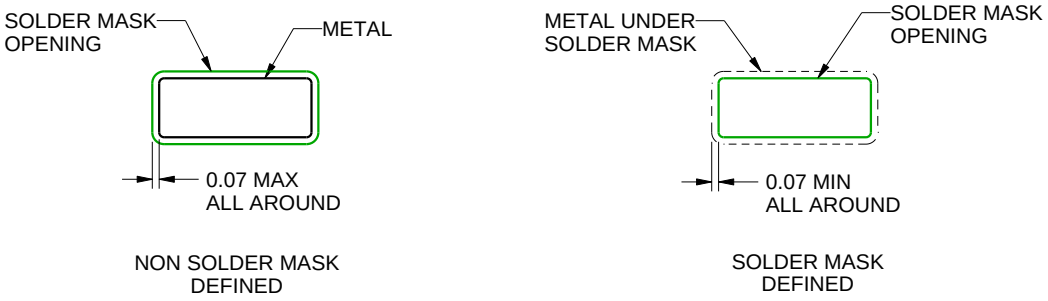


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

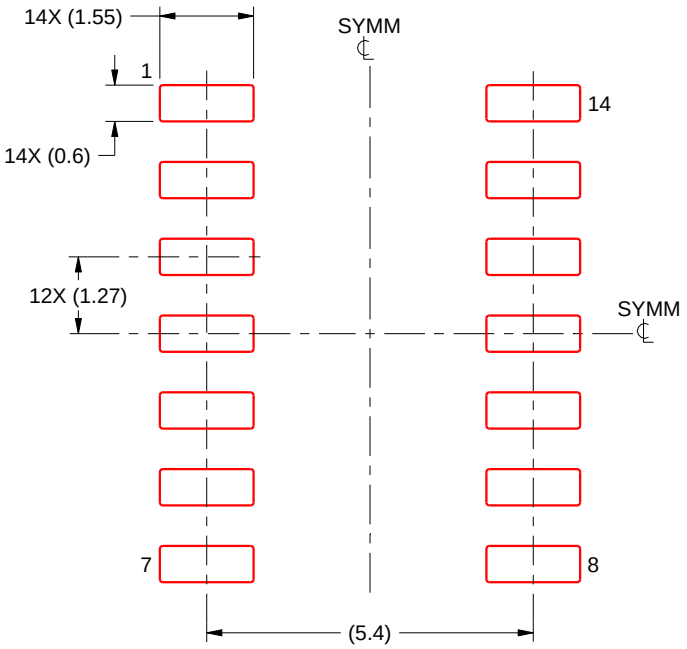
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



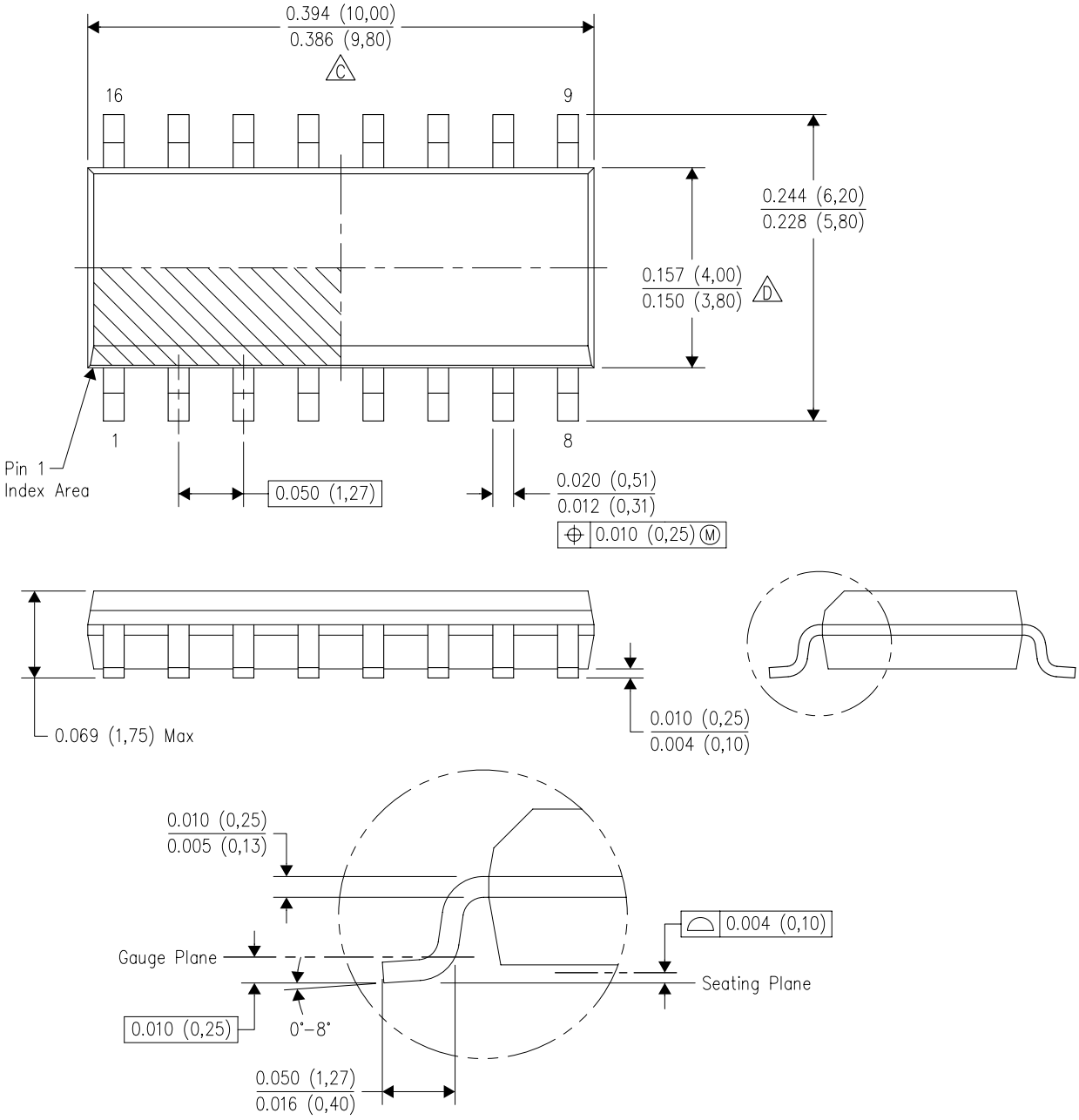
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



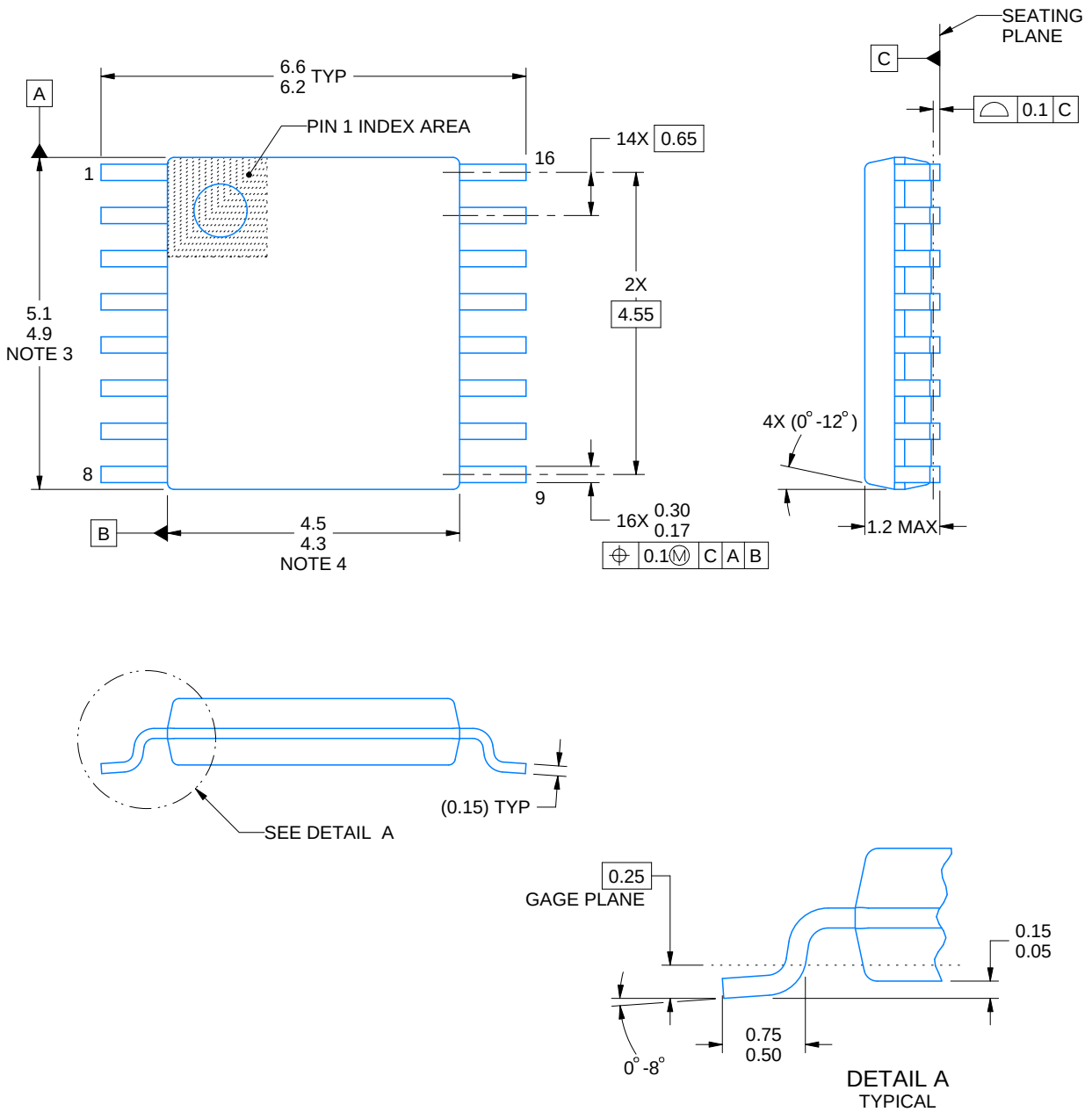
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

PACKAGE OUTLINE

PW0016A

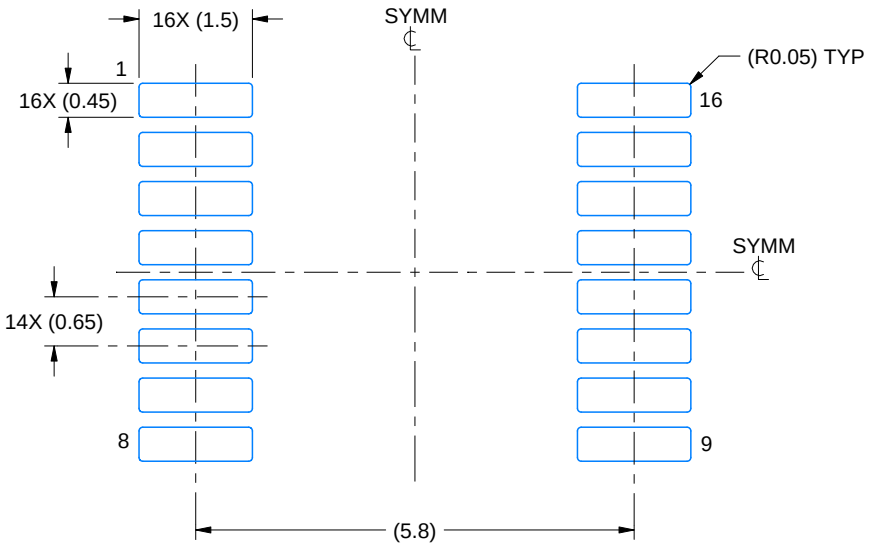
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

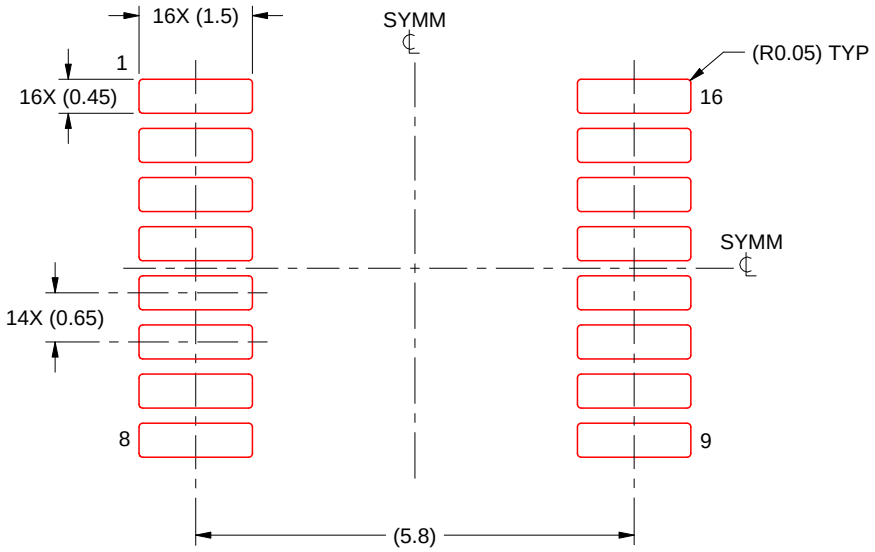


SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

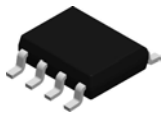


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

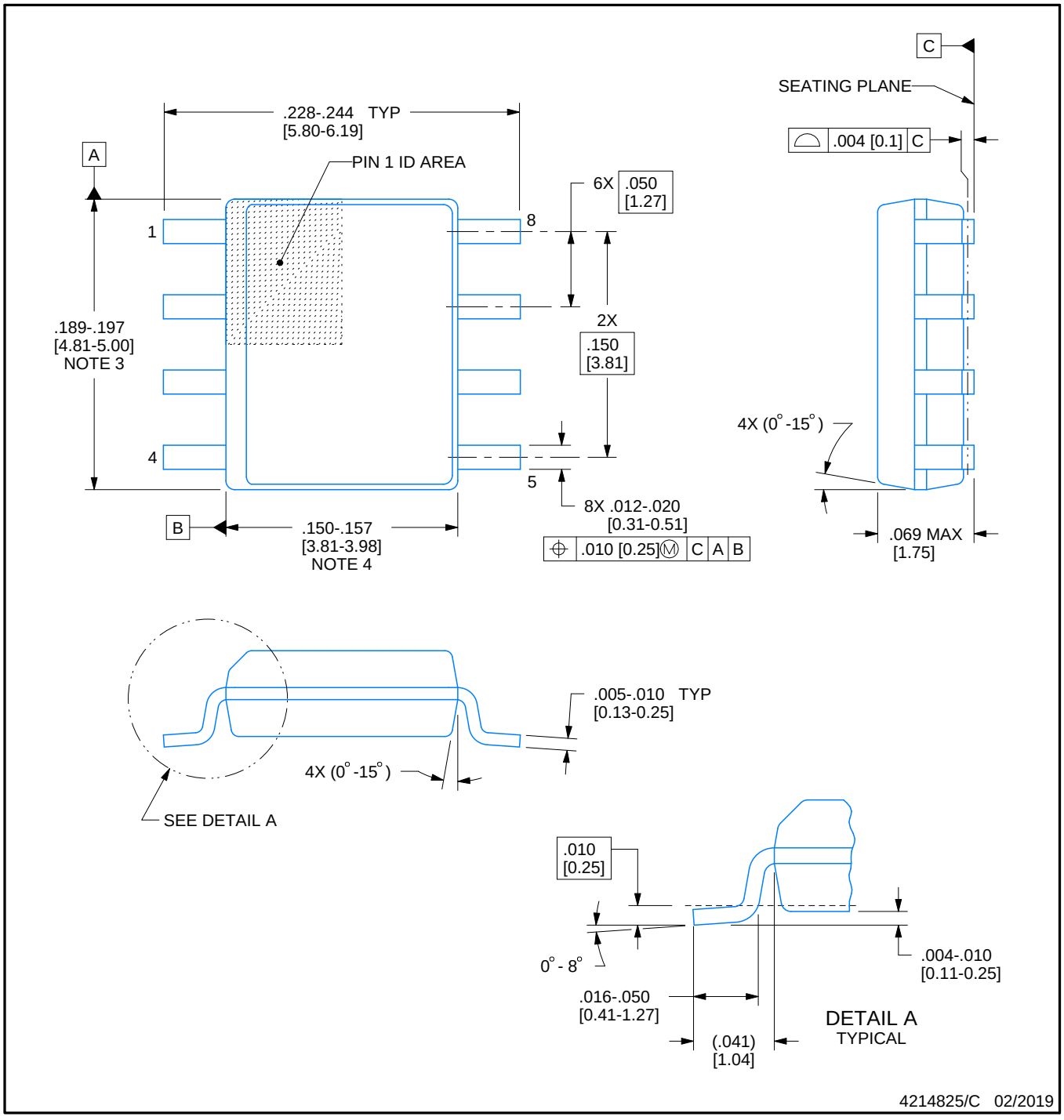


PACKAGE OUTLINE

D0008A

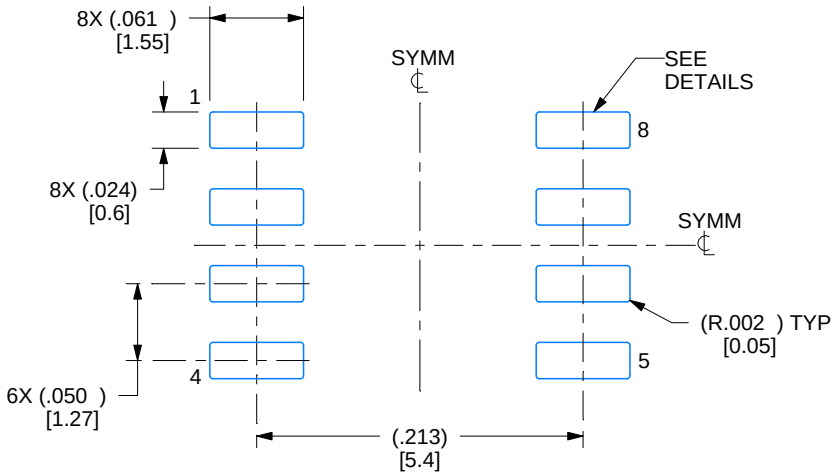
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

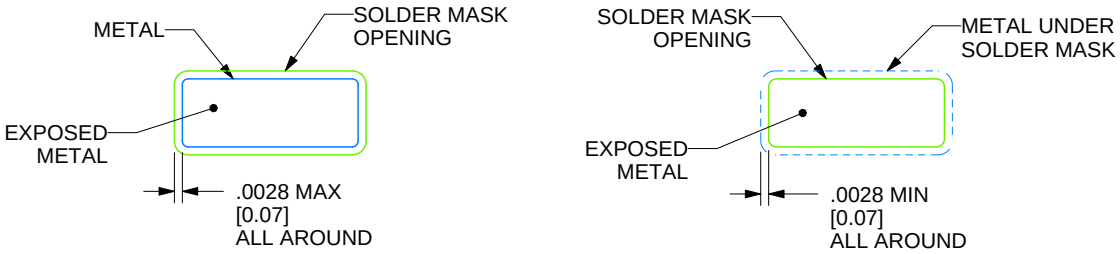


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

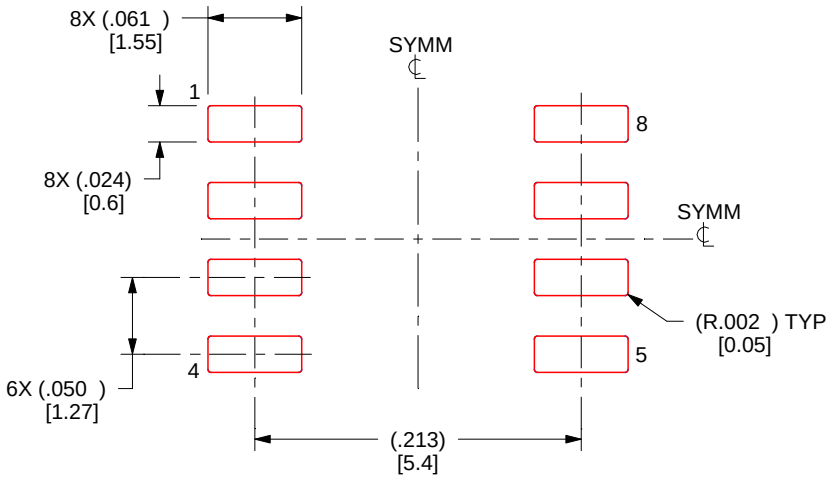
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

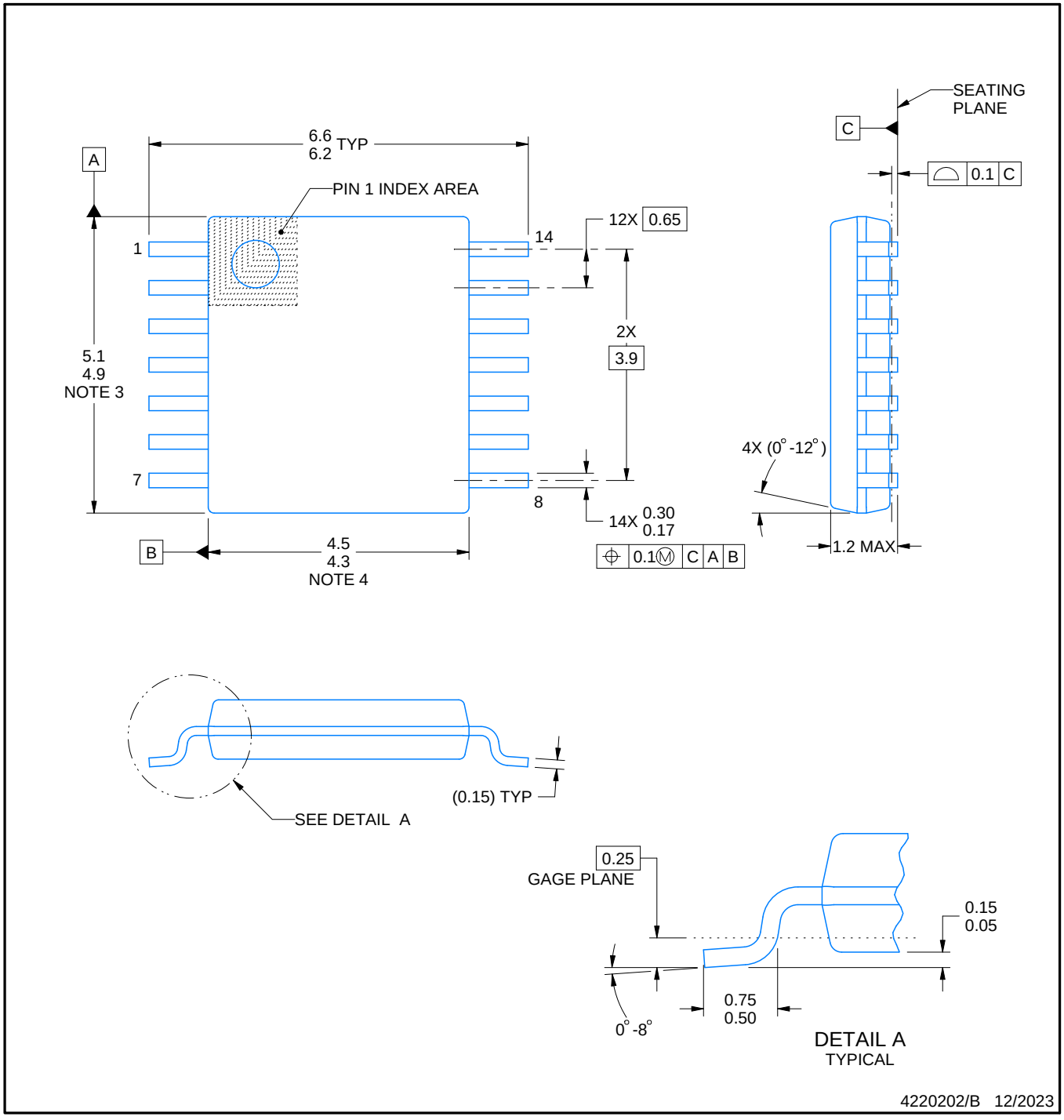
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0014A

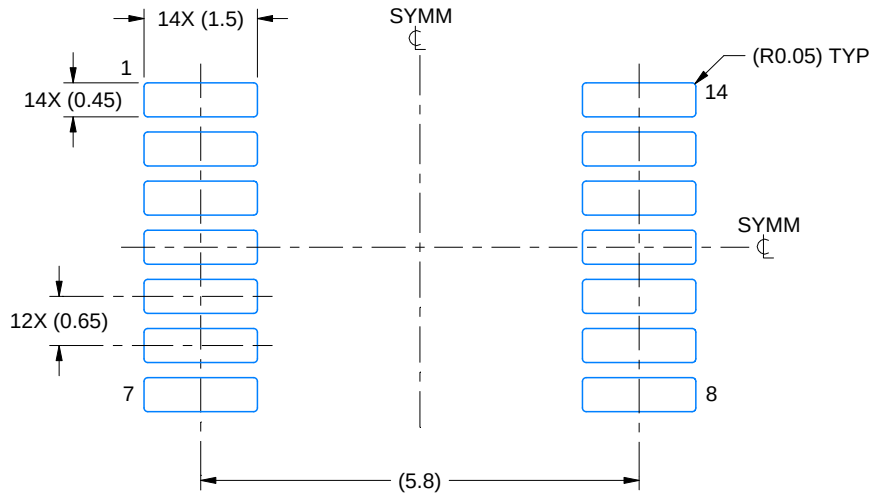
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

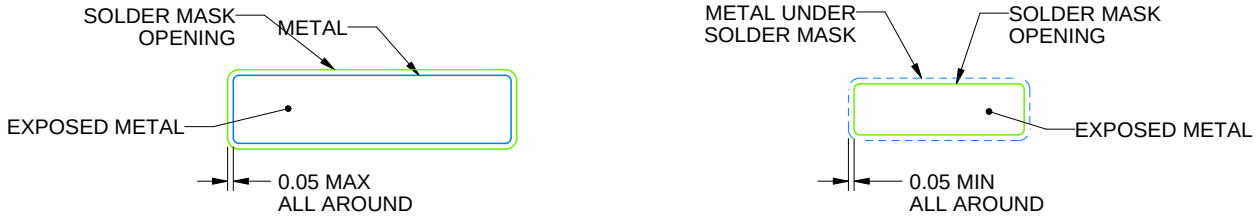


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

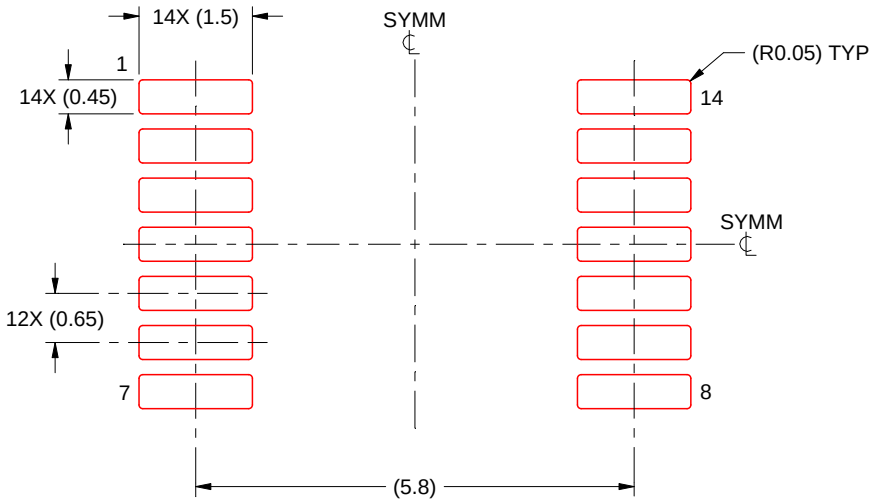


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025