TEXAS INSTRUMENTS

SN65LVDS104, SN65LVDS105

SLLS396G – SEPTEMBER 1999 – REVISED DECEMBER 2015

SN65LVDS10x 4-Port LVDS and 4-Port TTL-to-LVDS Repeaters

1 Features

- Receiver and Drivers Meet or Exceed the Requirements of ANSI EIA/TIA-644 Standard
  - SN65LVDS105 Receives Low-Voltage TTL (LVTTL) Levels
  - SN65LVDS104 Receives Differential Input Levels, ±100 mV
- Typical Data Signaling Rates to 400 Mbps or Clock Frequencies to 400 MHz
- Operates From a Single 3.3-V Supply
- Low-Voltage Differential Signaling With Typical Output Voltage of 350 mV and a 100-Ω Load
- Propagation Delay Time
  - SN65LVDS105 – 2.2 ns (Typ)
  - SN65LVDS104 – 3.1 ns (Typ)
- LVTTL Levels Are 5-V Tolerant
- Electrically Compatible With LVDS, PECL, LVPECL, LVTTL, LVCMOS, GTL, BTL, CTT, SSTL, or HSTL Outputs With External Networks
- Driver Outputs Are High-Impedance When Disabled or With V_{CC} <1.5 V
- Bus-Pin ESD Protection Exceeds 16 kV
- SOIC and TSSOP Packaging

2 Applications

- Clock Distribution
- Wireless Base Stations
- Network Routers

3 Description

The SN65LVDS10x are a differential line receiver and a LVTTL input (respectively) connected to four differential line drivers that implement the electrical characteristics of low-voltage differential signaling (LVDS). LVDS, as specified in EIA/TIA-644 is a data signaling technique that offers low-power, low-noise coupling, and switching speeds to transmit data at relatively long distances. (Note: The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other system characteristics.)

The intended application of this device and signaling technique is for point-to-point baseband data transmission over controlled impedance media of approximately 100 Ω. The transmission media may be printed-circuit board traces, backplanes, or cables. Having the drivers integrated into the same substrate, along with the low pulse skew of balanced signaling, allows extremely precise timing alignment of the signals repeated from the input. This is particularly advantageous in distribution or expansion of signals such as clock or serial data stream.

The SN65LVDS10x are characterized for operation from –40°C to 85°C.

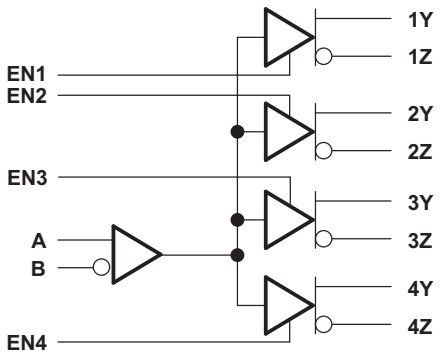
The SN65LVDS10x are members of a family of LVDS repeaters. A brief overview of the family is provided in the *Selection Guide to LVDS Repeaters* section.

Device Information[1]

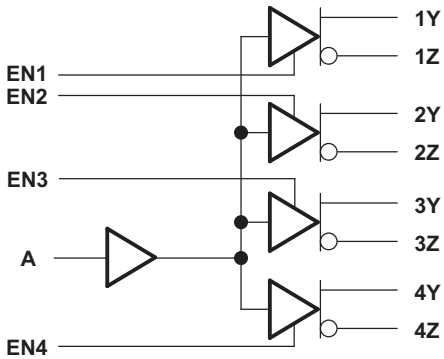
PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN65LVDS104, SN65LVDS105	SOIC (16)	9.90 mm × 3.91 mm
	TSSOP (16)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

SN65LVDS104 Logic Diagram (Positive Logic)



SN65LVDS105 Logic Diagram (Positive Logic)



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (January 2005) to Revision G	Page
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

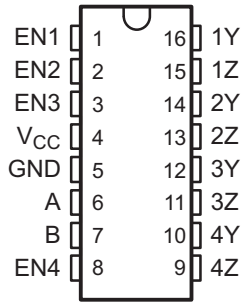
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5 Selection Guide to LVDS Repeaters

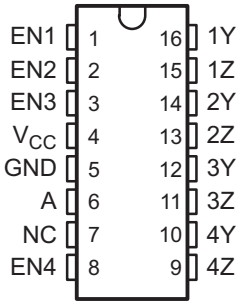
DEVICE	NO. INPUTS	NO. OUTPUTS	PACKAGE	COMMENT
SN65LVDS22	2 LVDS	2 LVDS	16-pin D	Dual multiplexed LVDS repeater
SN65LVDS104	1 LVDS	4 LVDS	16-pin D	4-Port LVDS repeater
SN65LVDS105	1 LVTTL	4 LVDS	16-pin D	4-Port TTL-to-LVDS repeater
SN65LVDS108	1 LVDS	8 LVDS	38-pin DBT	8-Port LVDS repeater
SN65LVDS109	2 LVDS	8 LVDS	38-pin DBT	Dual 4-port LVDS repeater
SN65LVDS116	1 LVDS	16 LVDS	64-pin DGG	16-Port LVDS repeater
SN65LVDS117	2 LVDS	16 LVDS	64-pin DGG	Dual 8-port LVDS repeater

6 Pin Configuration and Functions

SN65LVDS104 D or PW Package
16-Pin SOIC or TSSOP
Top View



SN65LVDS105 D or PW Package
16-Pin SOIC or TSSOP
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	SN65LVDS104	SN65LVDS105		
A	6	6	I	LVDS input, positive (LVDS104) or LVTTL input, (LVDS105)
B	7	—	I	LVDS input, negative
EN1	1	1	I	Enable, channel 1
EN2	2	2	I	Enable, channel 2
EN3	3	3	I	Enable, channel 3
EN4	8	8	I	Enable, channel 4
GND	5	5	—	Ground
NC	—	7	—	No connect
V_{CC}	4	4	—	Supply voltage
1Y	16	16	O	LVDS output, positive, channel 1
1Z	15	15	O	LVDS output, negative, channel 1
2Y	14	14	O	LVDS output, positive, channel 2
2Z	13	13	O	LVDS output, negative, channel 2
3Y	12	12	O	LVDS output, positive, channel 3
3Z	11	11	O	LVDS output, negative, channel 3
4Y	10	10	O	LVDS output, positive, channel 4
4Z	9	9	O	LVDS output, negative, channel 4

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply voltage, V_{CC} (2)		–0.5	4	V
Voltage	Enables, A (SN65LVDS105)	–0.5	6	V
	A, B, Y or Z	–0.5	4	V
Continuous power dissipation		See *Dissipation Ratings*		
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds		260		°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

7.2 ESD Ratings—JEDEC

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±12000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 ESD Ratings—MIL-STD

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Tested in accordance with MIL-STD-883C Method 3015.7; A, B, Y, Z, and GND pins	Class 3, A	16000	V
			Class 3, B	400	

7.4 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I or V_{IC}	Voltage at any bus terminal (separately or common-mode)	0		V_{CC}–0.8	
T_A	Operating free-air temperature	–40		85	°C

7.5 Thermal Information

THERMAL METRIC (1)		SN65LVDS104, SN65LVDS105		UNIT
		D (SOIC)	PW (TSSOP)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	74.4	101.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	35.1	29.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	32	47.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6	1.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	31.7	46.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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7.6 SN65LVDS104 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going differential input voltage threshold	See Figure 13 and Table 1			100	mV
V_{IT-}	Negative-going differential input voltage threshold	See Figure 13 and Table 1	–100			
$\|V_{OD}\|$	Differential output voltage magnitude	R_L = 100 Ω, V_{ID} = ± 100 mV, See Figure 13 and Figure 14	247	340	454	mV
$\Delta\|V_{OD}\|$	Change in differential output voltage magnitude between logic states	R_L = 100 Ω, V_{ID} = ± 100 mV, See Figure 13 and Figure 14	–50		50	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 15	1.125		1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states	See Figure 15	–50		50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage	See Figure 15		25	150	mV
I_{CC}	Supply current	Enabled, R_L = 100 Ω		23	35	mA
		Disabled		3	8	
I_I	Input current (A or B inputs)	V_I = 0 V	–2	–11	–20	µA
		V_I = 2.4 V	–1.2	–3		
$I_{I(OFF)}$	Power-off Input current	V_{CC} = 1.5 V, V_I = 2.4 V			20	µA
I_{IH}	High-level input current (enables)	V_{IH} = 2 V			20	µA
I_{IL}	Low-level input current (enables)	V_{IL} = 0.8 V			10	µA
I_{OS}	Short-circuit output current	V_{OY} or V_{OZ} = 0 V			±10	mA
		V_{OD} = 0 V			±10	
I_{OZ}	High-impedance output current	V_O = 0 V or 2.4 V			±1	µA
$I_{O(OFF)}$	Power-off output current	V_{CC} = 1.5 V, V_O = 2.4 V			±1	µA
C_{IN}	Input capacitance (A or B inputs)	V_I = 0.4 sin (4E6πt) + 0.5 V		3		pF
C_O	Output capacitance (Y or Z outputs)	V_I = 0.4 sin (4E6πt) + 0.5 V, Disabled		9.4		pF

(1) All typical values are at 25°C and with a 3.3-V supply.

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7.7 SN65LVDS105 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$\|V_{OD}\|$	Differential output voltage magnitude	R_L = 100 Ω, V_{ID} = ±100 mV, See Figure 18 and Figure 19	247	340	454	mV
$\Delta\|V_{OD}\|$	Change in differential output voltage magnitude between logic states	R_L = 100 Ω, V_{ID} = ±100 mV, See Figure 18 and Figure 19	–50		50	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 20	1.125		1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states	See Figure 20	–50		50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage	See Figure 20		25	150	mV
I_{CC}	Supply current	Enabled, R_L = 100 Ω		23	35	mA
		Disabled		0.7	6.4	
I_{IH}	High-level input current	V_{IH} = 2 V			20	µA
I_{IL}	Low-level input current	V_{IL} = 0.8 V			10	µA
I_{OS}	Short-circuit output current	V_{OY} or V_{OZ} = 0 V			±10	mA
		V_{OD} = 0 V			±10	
I_{OZ}	High-impedance output current	V_O = 0 V or 2.4 V			±1	µA
$I_{O(OFF)}$	Power-off output current	V_{CC} = 1.5 V, V_O = 2.4 V		0.3	±1	µA
C_{IN}	Input capacitance	V_I = 0.4 sin (4E6πt) + 0.5 V		5		pF
C_O	Output capacitance (Y or Z outputs)	V_I = 0.4 sin (4E6πt) + 0.5 V, Disabled		9.4		pF

(1) All typical values are at 25°C and with a 3.3-V supply.

7.8 SN65LVDS104 Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 100 Ω, C_L = 10 pF, See Figure 16	2.4	3.2	4.2	ns
t_{PHL}	Propagation delay time, high-to-low-level output	R_L = 100 Ω, C_L = 10 pF, See Figure 16	2.2	3.1	4.2	ns
t_r	Differential output signal rise time	R_L = 100 Ω, C_L = 10 pF, See Figure 16	0.3	0.8	1.2	ns
t_f	Differential output signal fall time	R_L = 100 Ω, C_L = 10 pF, See Figure 16	0.3	0.8	1.2	ns
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)	R_L = 100 Ω, C_L = 10 pF, See Figure 16		150	500	ps
$t_{sk(o)}$	Channel-to-channel output skew(2)	R_L = 100 Ω, C_L = 10 pF, See Figure 16		20	100	ps
$t_{sk(pp)}$	Part-to-part skew(3)				1.5	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	See Figure 17		7.2	15	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output	See Figure 17		8.4	15	ns
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output	See Figure 17		3.6	15	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output	See Figure 17		6	15	ns

(1) All typical values are at 25°C and with a 3.3-V supply.
(2) $t_{sk(o)}$ is the magnitude of the time difference between the t_{PLH} or t_{PHL} of all drivers of a single device with all of their inputs connected together.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

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7.9 SN65LVDS105 Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 100 Ω, C_L = 10 pF, See Figure 21	1.7	2.2	3	ns
t_{PHL}	Propagation delay time, high-to-low-level output	R_L = 100 Ω, C_L = 10 pF, See Figure 21	1.4	2.3	3.5	ns
t_r	Differential output signal rise time	R_L = 100 Ω, C_L = 10 pF, See Figure 21	0.3	0.8	1.2	ns
t_f	Differential output signal fall time	R_L = 100 Ω, C_L = 10 pF, See Figure 21	0.3	0.8	1.2	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)	R_L = 100 Ω, C_L = 10 pF, See Figure 21		150	500	ps
$t_{sk(o)}$	Channel-to-channel output skew(2)	R_L = 100 Ω, C_L = 10 pF, See Figure 21		20	100	ps
$t_{sk(pp)}$	Part-to-part skew(3)				1.5	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	See Figure 22		7.2	15	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output	See Figure 22		8.4	15	ns
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output	See Figure 22		3.6	15	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output	See Figure 22		6	15	ns

(1) All typical values are at 25°C and with a 3.3-V supply.
(2) $t_{sk(o)}$ is the magnitude of the time difference between the t_{PLH} or t_{PHL} of all drivers of a single device with all of their inputs connected together.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

7.10 Dissipation Ratings

PACKAGE	$T_A \leq$ 25°C POWER RATING	OPERATING FACTOR(1) ABOVE T_A = 25°C	T_A = 85°C POWER RATING
D	950 mW	7.6 mW/°C	494 mW
PW	774 mW	6.2 mW/°C	402 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted (low-k) and with no air flow.

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7.11 Typical Characteristics

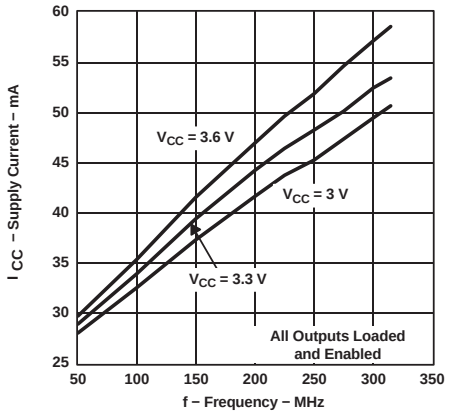


Figure 1. SN65LVDS104 Supply Current vs Frequency

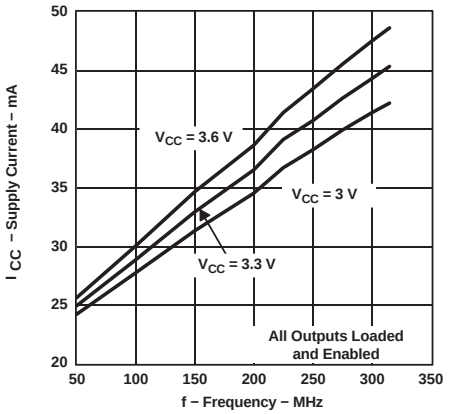


Figure 2. SN65LVDS105 Supply Current vs Frequency

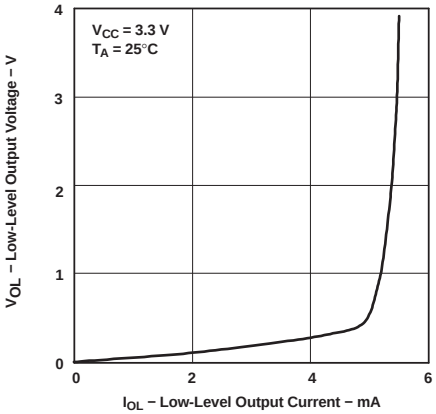


Figure 3. Driver Low-Level Output Voltage vs Low-Level Output Current

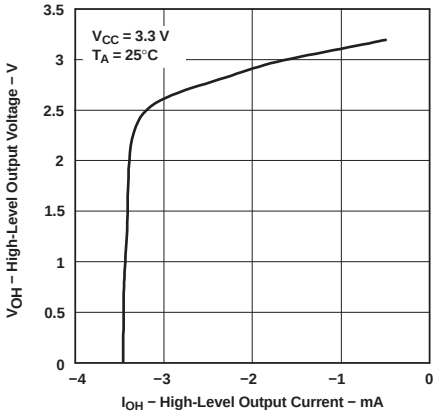


Figure 4. Driver High-Level Output Voltage vs High-Level Output Current

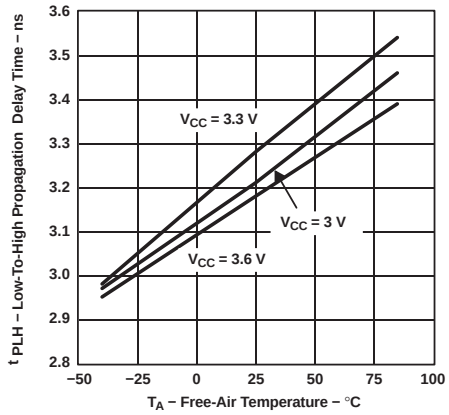


Figure 5. SN65LVDS104 Low-to-High Propagation Delay Time vs Free-Air Temperature

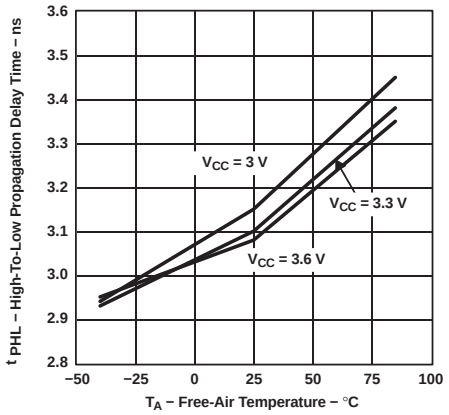


Figure 6. SN65LVDS104 High-to-Low Propagation Delay Time vs Free-Air Temperature

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Typical Characteristics (continued)

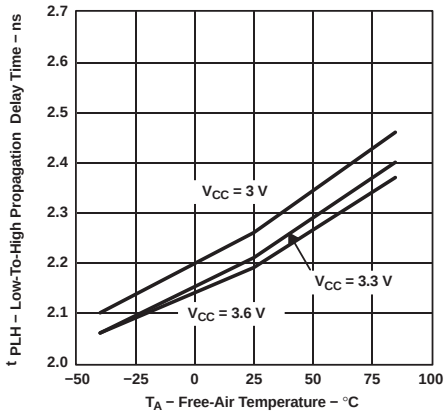


Figure 7. SN65LVDS105 Low-to-High Propagation Delay Time vs Free-Air Temperature

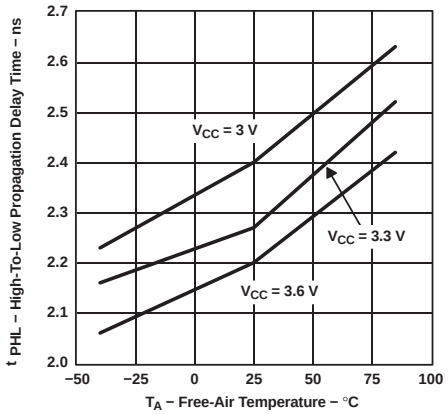
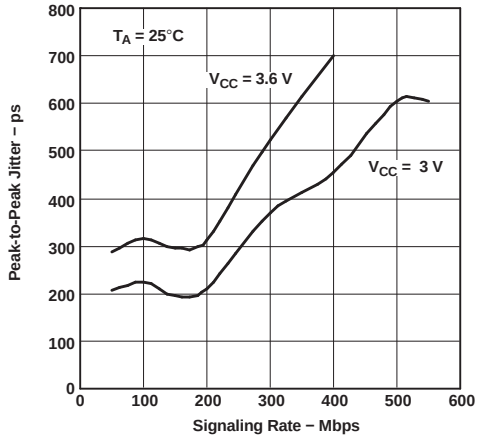
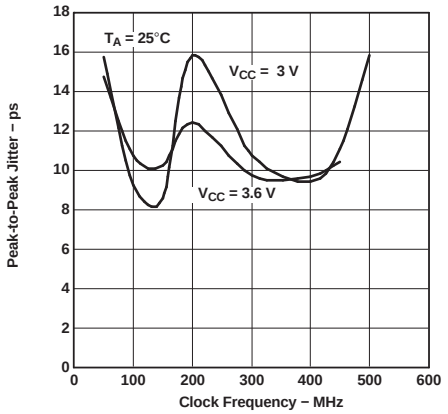


Figure 8. SN65LVDS105 High-to-Low Propagation Delay Time vs Free-Air Temperature



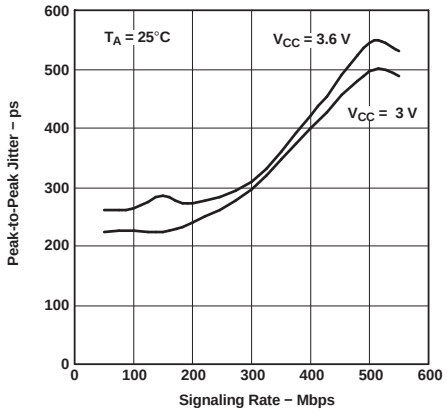
Input: 2^{15} PRBS with peak-to-peak jitter <115 ps at 100 Mbps. Test board adds about 70 ps p-p jitter. All outputs enabled and loaded with differential 100-Ω loads, worst-case output, supply decoupled with 0.1-µF ceramic 0603-style capacitors 1 cm from the device.

Figure 9. SN65LVDS104 P-P Eye-Pattern Jitter vs PRBS Signaling Rate



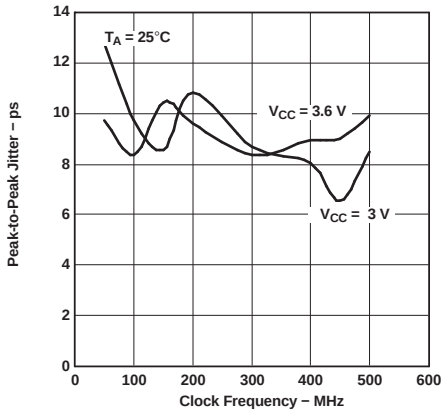
Input: 50% duty cycle square wave with period jitter < 9 ps at 100 MHz. Test board adds about 5 ps p-p jitter. All outputs enabled and loaded with differential 100-Ω loads, worst-case output, supply decoupled with 0.1-µF and 0.001-µF ceramic 0603-style capacitors 1 cm from the device.

Figure 10. SN65LVDS104 P-P Period Jitter vs Clock Frequency



Input: 2^{15} PRBS with peak-to-peak Jitter < 147 ps at 100 Mbps, Test board adds about 43 ps p-p jitter. All outputs enabled and loaded with differential 100-Ω loads, worst-case output, supply decoupled with 0.1-µF and 0.001-µF ceramic 0603-style capacitors 1 cm from the device.

Figure 11. SN65LVDS105 P-P Eye-Pattern Jitter vs PRBS Signaling Rate



Input: 50% duty cycle square wave with period jitter < 10 ps at 100 MHz. Test board adds about 5 ps p-p jitter. All outputs enabled and loaded with differential 100-Ω loads, worst-case output, supply decoupled with 0.1-µF and 0.001-µF ceramic 0603-style capacitors 1 cm from the device.

Figure 12. SN65LVDS105 P-P Period Jitter vs Clock Frequency

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8 Parameter Measurement Information

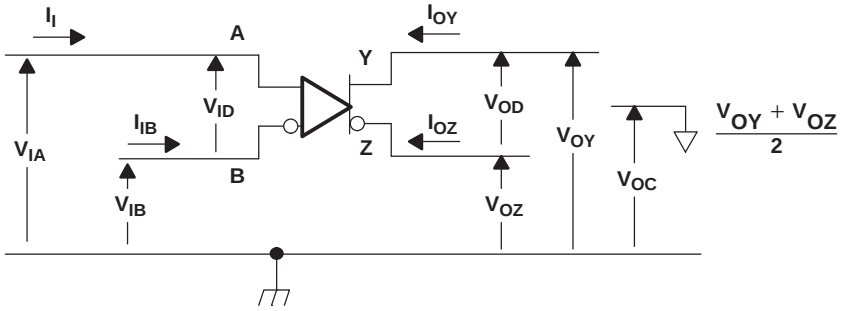


Figure 13. SN65LVDS104 Voltage and Current Definitions

Table 1. SN65LVDS104 Minimum and Maximum Input Threshold Test Voltages

APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE
V_{IA}	V_{IB}	V_{ID}	V_{IC}
1.25 V	1.15 V	100 mV	1.2 V
1.15 V	1.25 V	–100 mV	1.2 V
2.4 V	2.3 V	100 mV	2.35 V
2.3 V	2.4 V	–100 mV	2.35 V
0.1 V	0 V	100 mV	0.05 V
0 V	0.1 V	–100 mV	0.05 V
1.5 V	0.9 V	600 mV	1.2 V
0.9 V	1.5 V	–600 mV	1.2 V
2.4 V	1.8 V	600 mV	2.1 V
1.8 V	2.4 V	–600 mV	2.1 V
0.6 V	0 V	600 mV	0.3 V
0 V	0.6 V	–600 mV	0.3 V

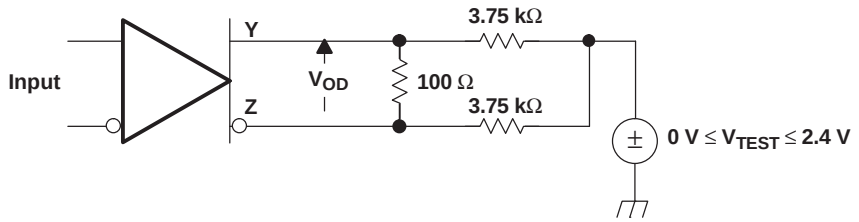
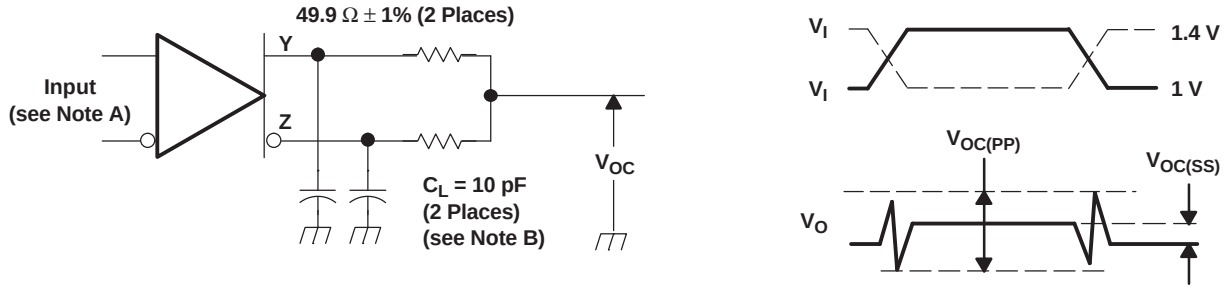


Figure 14. SN65LVDS104 V_{OD} Test Circuit

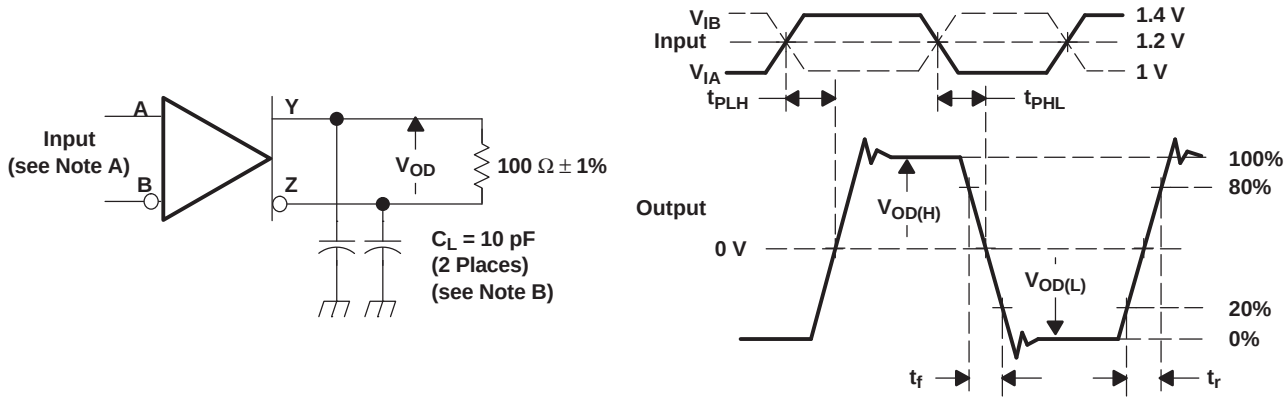
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A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, Pulse Repetition Rate (PRR) = 0.5 Mpps, and pulse width = 500 ± 10 ns.

B. C_L includes instrumentation and fixture capacitance within 0.06 m of the device under test. The measurement of $V_{OC(PP)}$ is made on test equipment with a –3 dB bandwidth of at least 300 MHz.

Figure 15. SN65LVDS104 Test Circuit and Definitions for the Driver Common-Mode Output Voltage

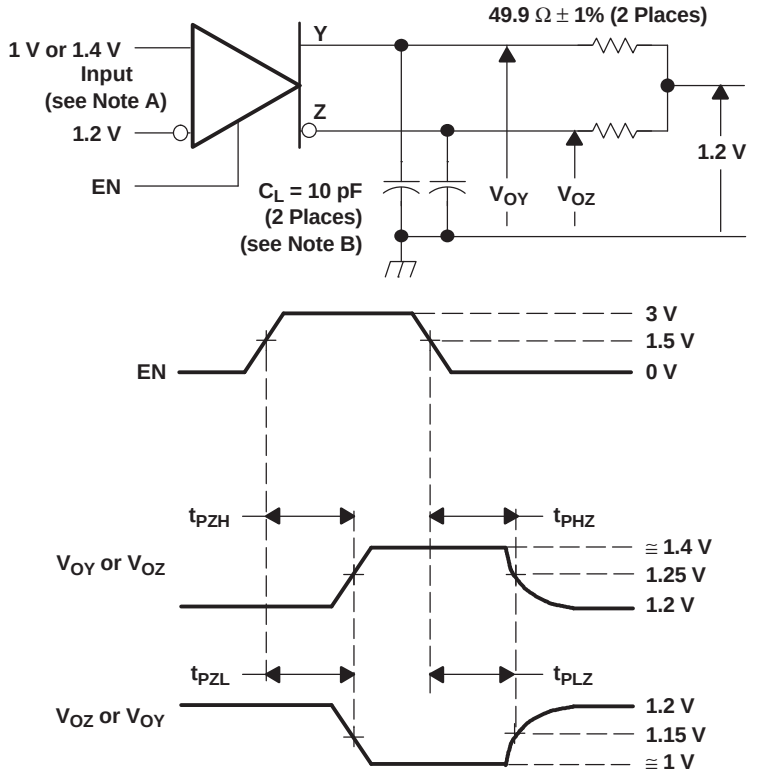


A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, Pulse Repetition Rate (PRR) = 50 Mpps, and pulse width = 10 ± 0.2 ns.

B. C_L includes instrumentation and fixture capacitance within 0.06 m of the device under test.

Figure 16. SN65LVDS104 Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal

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A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq$ 1 ns, Pulse Repetition Rate (PRR) = 0.5 Mpps, and pulse width = 500 ± 10 ns.

B. C_L includes instrumentation and fixture capacitance within 0.06 m of the device under test.

Figure 17. SN65LVDS104 Enable and Disable Time Circuit and Definitions

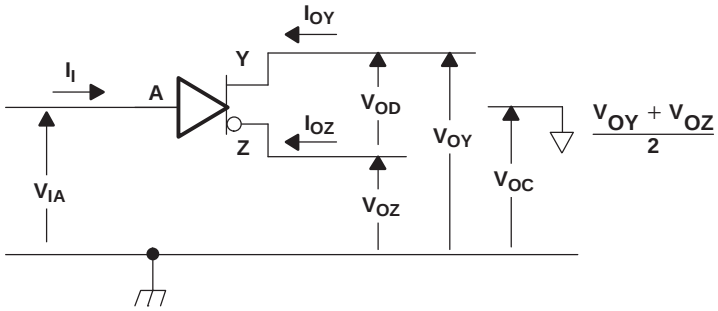


Figure 18. SN65LVDS105 Voltage and Current Definitions

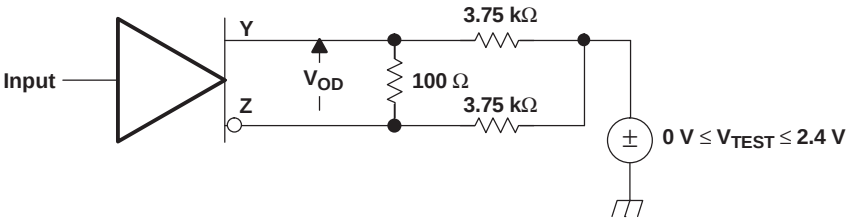
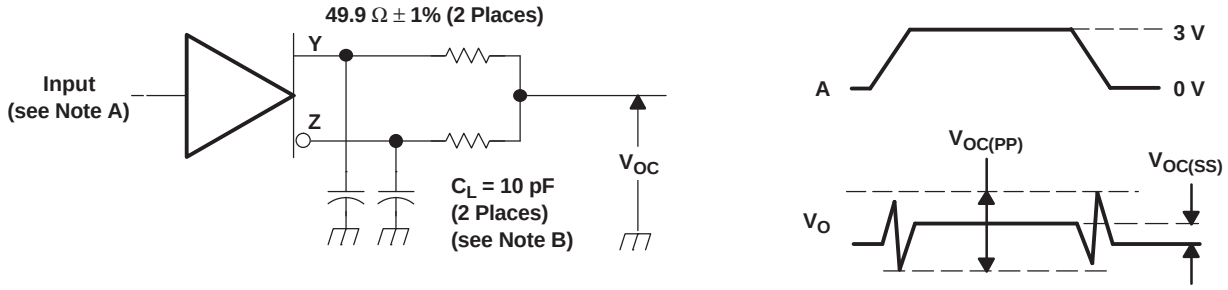


Figure 19. SN65LVDS105 VOD Test Circuit

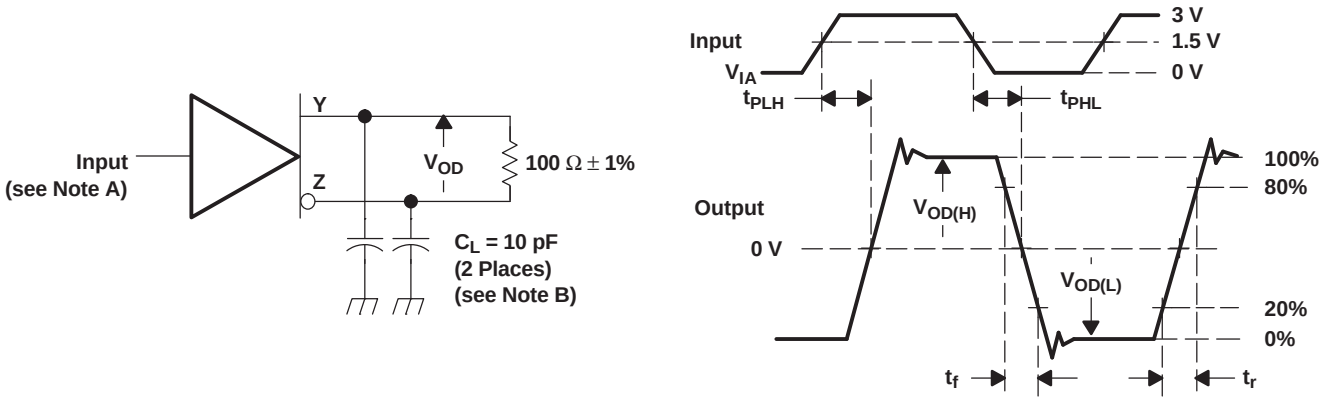
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A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f≤ 1 ns, Pulse Repetition Rate (PRR) = 0.5 Mpps, and pulse width = 500 ± 10 ns.

B. C_L includes instrumentation and fixture capacitance within 0.06 m of the device under test. The measurement of $V_{OC(PP)}$ is made on test equipment with a -3 dB bandwidth of at least 300 MHz.

Figure 20. SN65LVDS105 Test Circuit and Definitions for the Driver Common-Mode Output Voltage

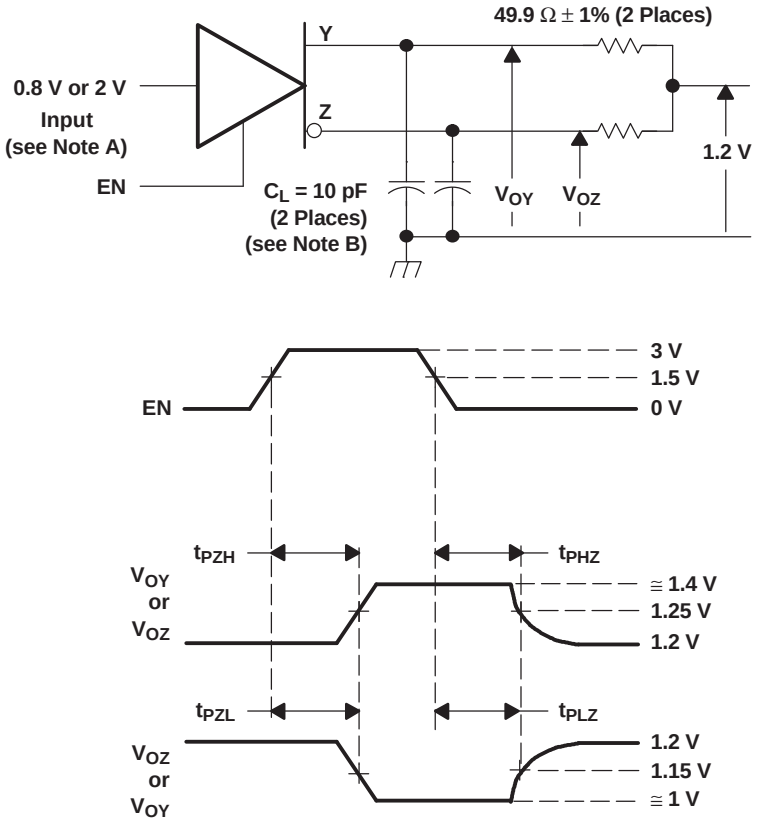


A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f≤ 1 ns, Pulse Repetition Rate (PRR) = 50 Mpps, and pulse width = 10 ± 0.2 ns.

B. C_L includes instrumentation and fixture capacitance within 0.06 m of the device under test.

Figure 21. SN65LVDS105 Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal

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A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f≤ 1 ns, Pulse Repetition Rate (PRR) = 0.5 Mpps, and pulse width = 500 ± 10 ns.

B. C_L includes instrumentation and fixture capacitance within 0.06 m of the device under test.

Figure 22. SN65LVDS105 Enable and Disable Time Circuit and Definitions

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9 Detailed Description

9.1 Overview

The SN65LVDS10x are a differential line receiver and a LVTTL input, respectively, connected to four differential signaling (LVDS) line drivers. These devices operate from a single 3.3-V supply. The input signal to the SN65LVDS104 is a differential LVDS signal; this device requires ±100 mV of input signal to determine the correct state of the received signal. The input signal to the SN65LVDS105 is an LVTTL signal. The outputs of both devices are four differential signals complying with the LVDS standard (TIA/EIA-644). The differential output signal operates with a signal level of 350 mV, nominally, at a common-mode voltage of 1.2 V. The intended application of this device and signaling technique is for point-to-point baseband data transmission over controlled impedance media of approximately 100 Ω. The transmission media may be printed-circuit board traces, backplanes, or cables. Having the drivers integrated into the same substrate, along with the low pulse skew of balanced signaling, allows extremely precise timing alignment of the signals repeated from the input. This is particularly advantageous in distribution or expansion of signals such as clock or serial data stream.

9.2 Functional Block Diagram

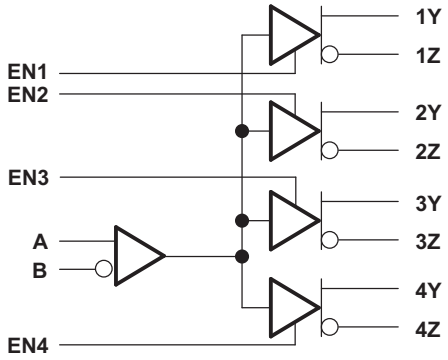


Figure 23. Example of Functional Block Diagram (SN65LVDS104)

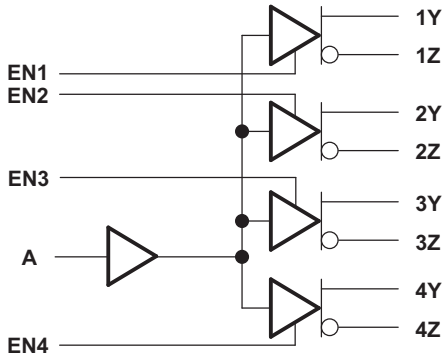


Figure 24. Example of Functional Block Diagram (SN65LVDS105)

9.3 Feature Description

9.3.1 Fail Safe

A common problem with differential signaling applications is how the system responds when no differential voltage is present on the signal pair. The LVDS receiver is like most differential line receivers, in that its output logic state can be indeterminate when the differential input voltage is between –100 mV and 100 mV and within its recommended input common-mode voltage range. However, TI LVDS receivers handles the open-input circuit situation differently.

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Feature Description (continued)

Open-circuit means that there is little or no input current to the receiver from the data line itself. This could be when the driver is in a high-impedance state or the cable is disconnected. When this occurs, the LVDS receiver pulls each line of the signal pair to near VCC through 300-kΩ resistors as shown in Figure 25. The fail-safe feature uses an AND gate with input voltage thresholds at about 2.3 V to detect this condition and force the output to a high-level regardless of the differential input voltage.

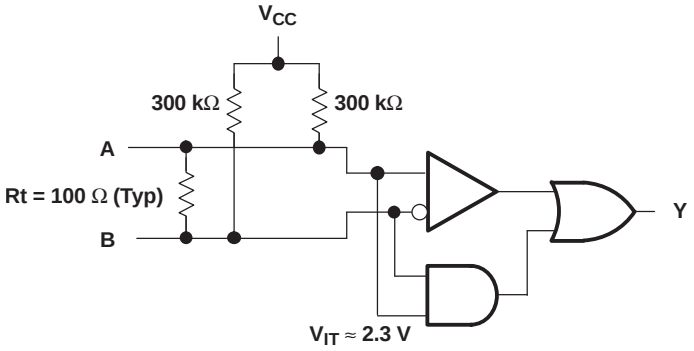


Figure 25. Open-Circuit Fail Safe of the LVDS Receiver

It is only under these conditions that the output of the receiver will be valid with less than a 100 mV differential input voltage magnitude. The presence of the termination resistor, Rt, does not affect the fail-safe function as long as it is connected as shown in Figure 25. Other termination circuits may allow a dc current to ground that could defeat the pullup currents from the receiver and the fail-safe feature.

9.4 Device Functional Modes

Table 2 lists the function tables for the SN65LVDS104 and 105 devices.

Table 2. Function Tables(1)

SN65LVDS104				SN65LVDS105			
INPUT		OUTPUT		INPUT		OUTPUT	
$V_{ID} = V_A - V_B$	xEN	xY	xZ	A	ENx	xY	xZ
X	X	Z	Z	L	H	L	H
X	L	Z	Z	H	H	H	L
$V_{ID} \geq 100$ mV	H	H	L	Open	H	L	H
–100 mV < V_{ID} < 100 mV	H	?	?	X	L	Z	Z
$V_{ID} \leq$ –100 mV	H	L	H	X	X	Z	Z

(1) H = high level, L = low level, Z = high impedance, ? = indeterminate, X = don't care

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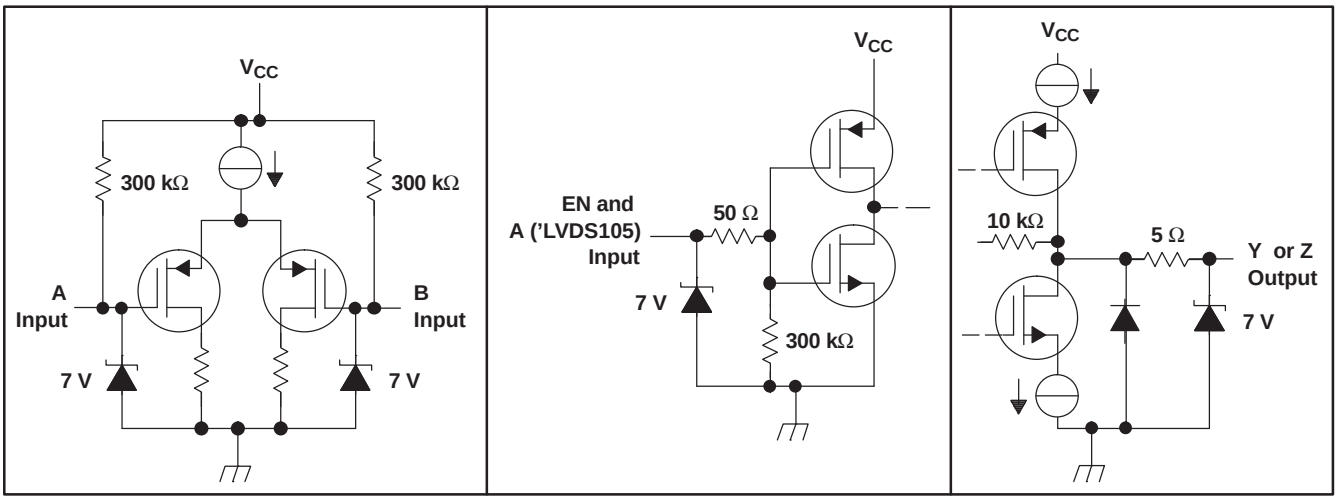


Figure 26. Equivalent Input and Output Schematic Diagrams

9.4.1 Input Level Translation

An LVDS receiver can be used to receive various other types of logic signals. Figure 27 through Figure 36 show the termination circuits for SSTL, HSTL, GTL, BTL, LVPECL, PECL, CMOS, and TTL.

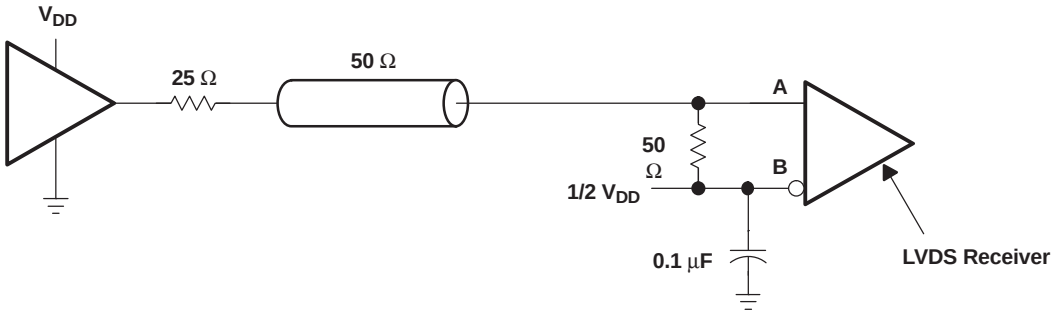


Figure 27. Sub-Series Terminated (SSTL) or High-Speed Transceiver Logic (HSTL)

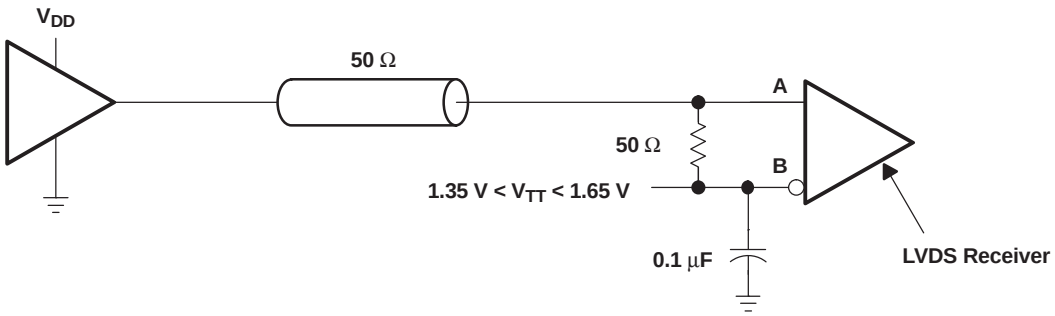


Figure 28. Center Tap Termination

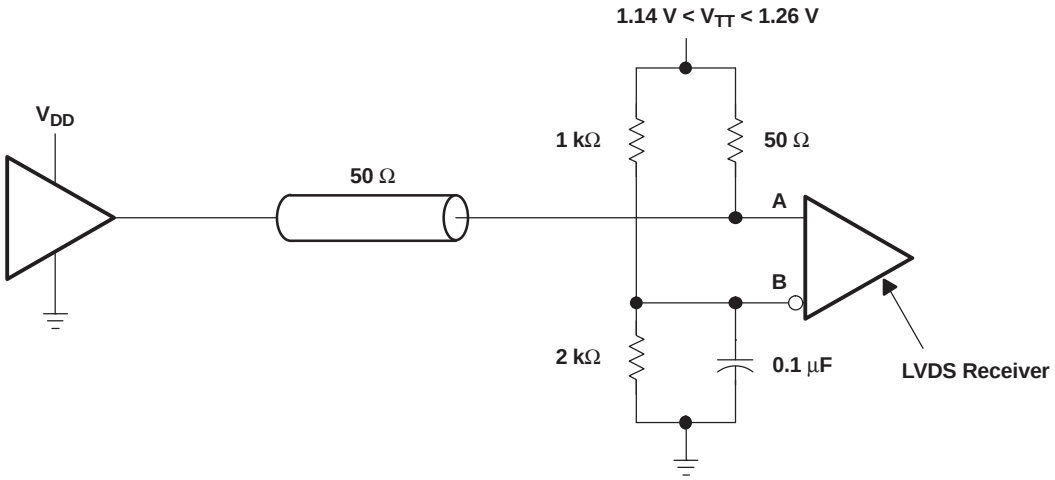


Figure 29. Gunning Transceiver Logic (GTL)

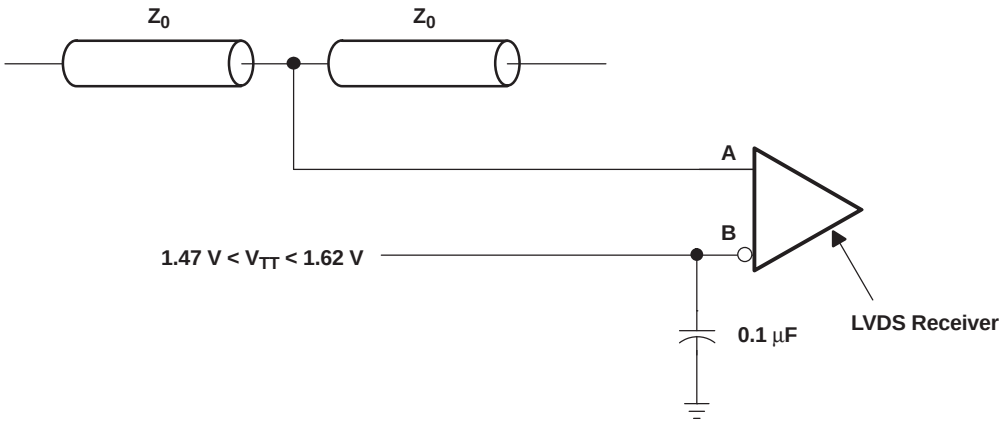


Figure 30. Backplane Transceiver

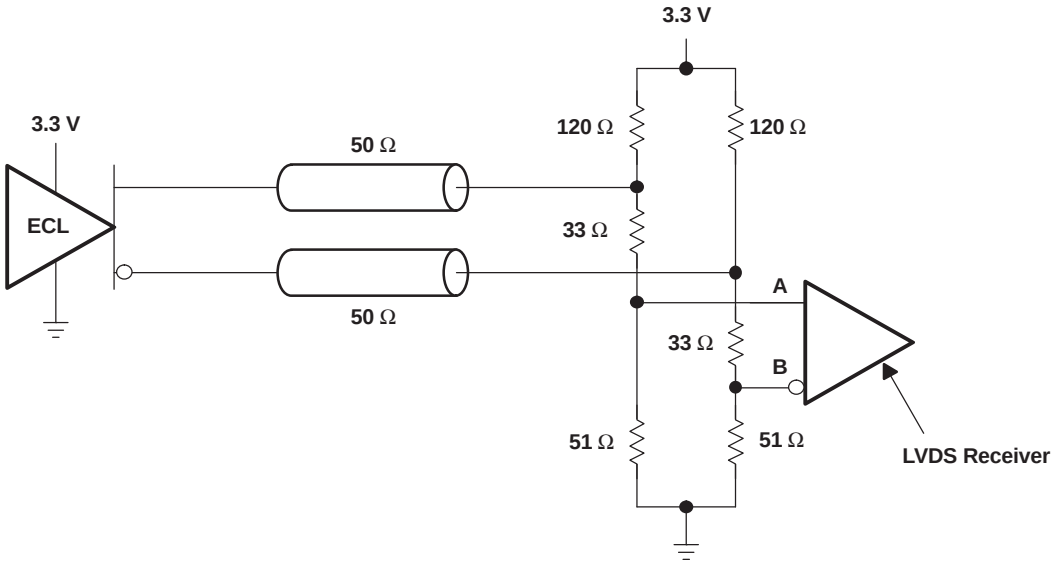


Figure 31. Low-Voltage Positive Emitter-Coupled Logic (LVPECL)

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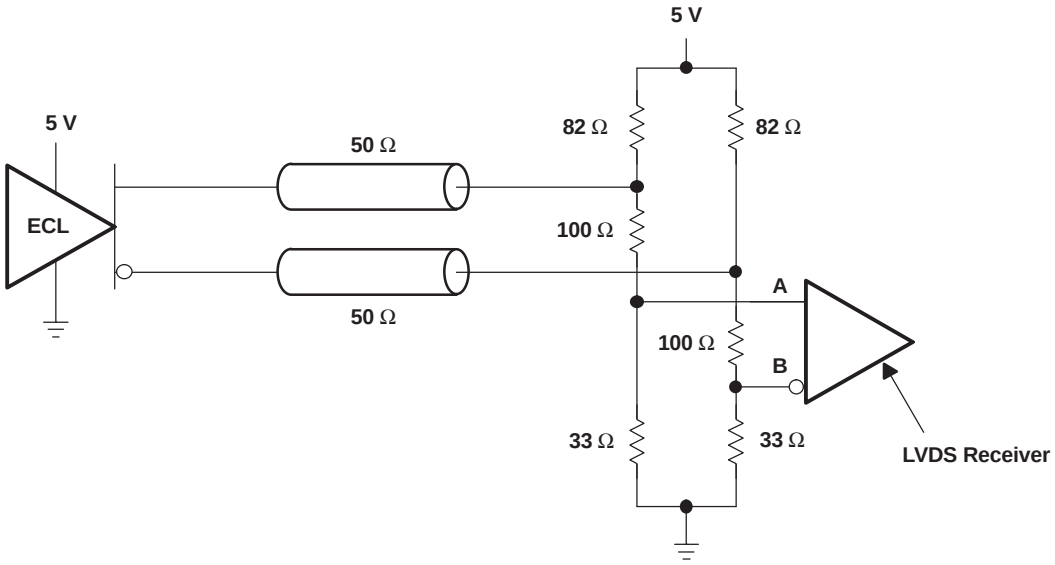


Figure 32. Positive Emitter-Coupled Logic (PECL)

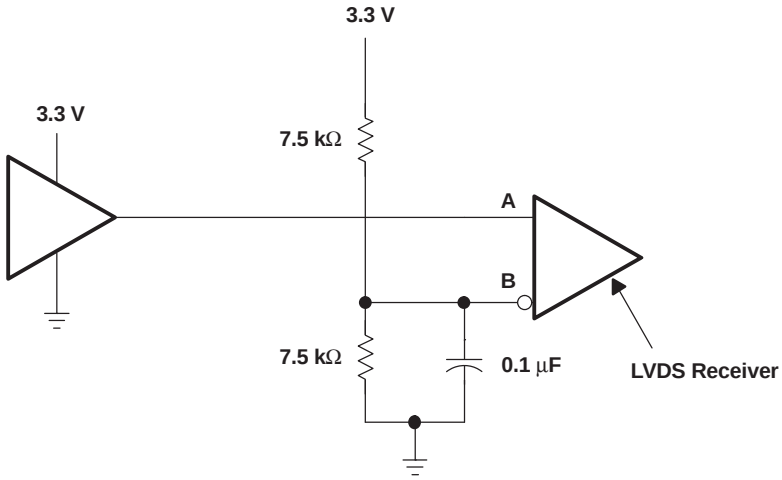


Figure 33. 3.3-V CMOS

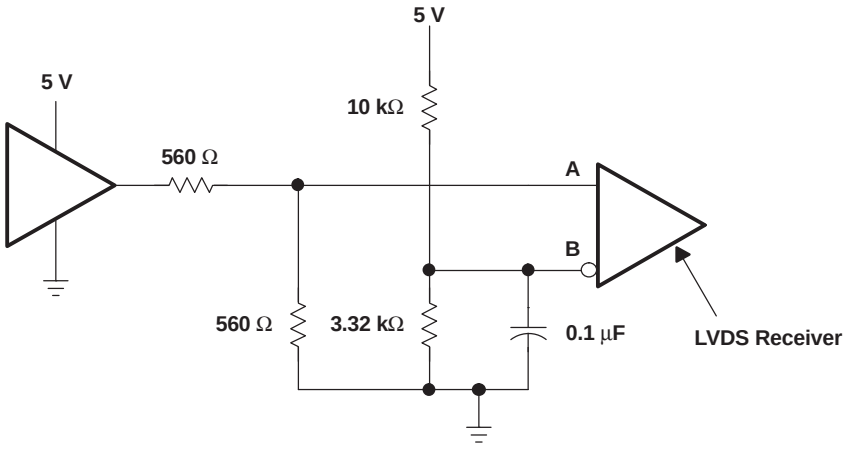


Figure 34. 5-V CMOS

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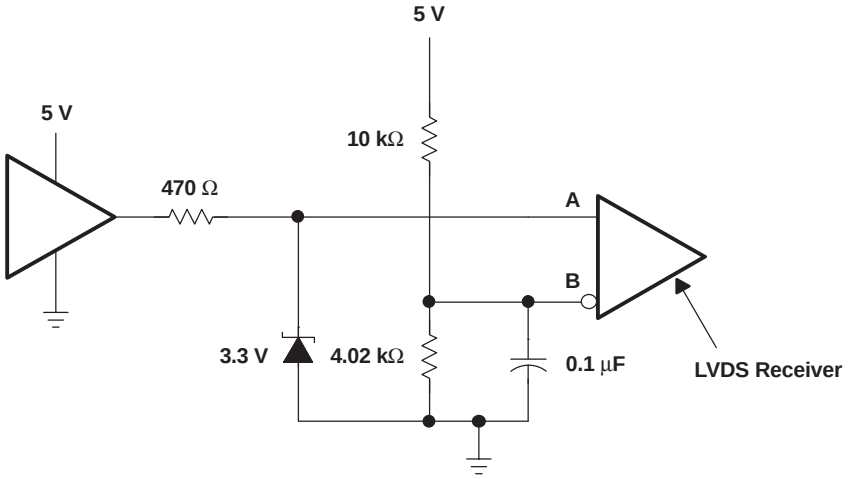


Figure 35. 5-V TTL

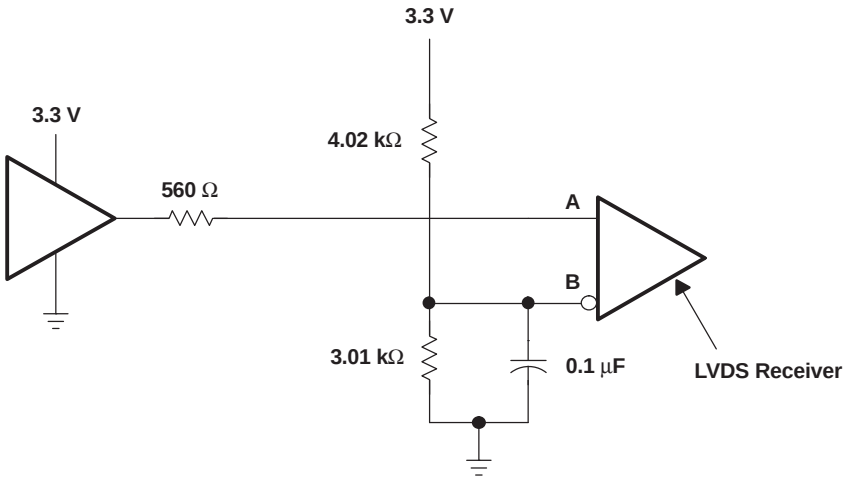


Figure 36. LVTTL

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10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The SN65LVDS049 is a dual LVDS driver-receiver pair. The functionality of these devices is simple, yet extremely flexible, leading to their use in designs ranging from wireless base stations to desktop computers. The varied class of potential applications share features and applications discussed in the paragraphs below.

10.2 Typical Application

10.2.1 Point-to-Point Communications

The most basic application for LVDS buffers, as found in this data sheet, is for point-to-point communications of digital data, as shown in Figure 37.

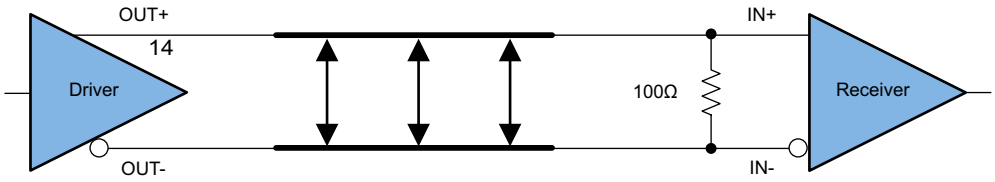


Figure 37. Point-to-Point Topology

A point-to-point communications channel has a single transmitter (driver) and a single receiver. This communications topology is often referred to as simplex. In Figure 37 the driver receives a single-ended input signal and the receiver outputs a single-ended recovered signal. The LVDS driver converts the single-ended input to a differential signal for transmission over a balanced interconnecting media of 100-Ω characteristic impedance. The conversion from a single-ended signal to an LVDS signal retains the digital data payload while translating to a signal whose features are more appropriate for communication over extended distances or in a noisy environment.

10.2.2 Design Requirements

For this design example, use the parameters listed in Table 3.

Table 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Driver supply voltage (V_{CCD})	3 to 3.6 V
Driver input voltage	0.8 to V_{CCD}V
Driver signaling rate	DC to 400 Mbps
Interconnect characteristic impedance	100 Ω
Termination resistance	100 Ω
Receiver supply voltage (V_{CCR})	3 to 3.6 V
Number of receiver nodes	1
Receiver input voltage	0 to V_{CCR} – 0.8 V
Ground shift between driver and receiver	±1

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Typical Application (continued)

10.2.3 Detailed Design Procedure

10.2.3.1 Bypass Capacitance

Bypass capacitors play a key role in power distribution circuitry. At low frequencies, power supply offers very low-impedance paths between the terminals. However, as higher frequency currents propagate through power traces, the source is quite often incapable of maintaining a low-impedance path to ground. Bypass capacitors are used to address this shortcoming. Usually, large bypass capacitors (10 µF to 1000 µF) at the board level do a good job into the kHz range. Due to their size and length of their leads, large capacitors tend to have large inductance values at the switching frequencies. To solve this problem, smaller capacitors must be (nF to µF range) installed locally next to the integrated circuit.

Multilayer ceramic chip or surface-mount capacitors (size 0603 or 0805) minimize lead inductances of bypass capacitors in high-speed environments, because their lead inductance is about 1 nH. For comparison purposes, a typical capacitor with leads has a lead inductance of approximately 5 nH.

The value of the bypass capacitors used locally with LVDS chips can be determined by the following formula according to Johnson, equations 8.18 to 8.21. A conservative rise time of 4 ns and a worst-case change in supply current of 100 mA covers the whole range of LVDS devices offered by TI. In this example, the maximum power supply noise tolerated is 100 mV. However, this figure varies depending on the noise budget available in your design.

$$C_{chip} = \left(\frac{\Delta I_{\text{Maximum Step Change Supply Current}}}{\Delta V_{\text{Maximum Power Supply Noise}}} \right) \times T_{\text{Rise Time}} \quad (1)$$

$$C_{LVDS} = \left(\frac{100\ \text{mA}}{0.1\ \text{V}} \right) \times 4\ \text{ns} = 0.004\ \mu\text{F} \quad (2)$$

The following example, Figure 38, lowers lead inductance and covers intermediate frequencies between the board-level capacitor (>10 µF) and the value of capacitance found in Equation 2 (0.004 µF). You must place the smallest value of capacitance as close as possible to the chip.

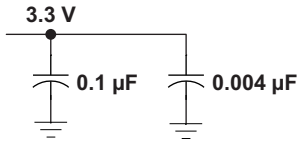


Figure 38. Recommended LVDS Bypass Capacitor Layout

10.2.3.2 Driver Supply Voltage

The device can support operation with a supply as low as 3 V and as high as 3.6 V. As shown in the *SN65LVDS104 Electrical Characteristics* and *SN65LVDS105 Electrical Characteristics*, the differential output voltage is nominally 350 mV over the complete output range. The minimum output voltage stays within the specified LVDS limits (247 mV to 454 mV) for a 3.3-V supply.

10.2.3.3 Driver Input Voltage

The driver will operate with a decision threshold of approximately 1.4 V for LVTTL input signals.

10.2.3.4 Driver Output Voltage

The SN65LVDS049 driver output is a 1.2-V common-mode voltage, with a nominal differential output signal of 350 mV. This 350 mV is the absolute value of the differential swing (VOD = |V+ – V–|). The peak-to-peak differential voltage is twice this value, or 700 mV.

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Typical Application (continued)

10.2.3.5 Interconnecting Media

The physical communication channel between the driver and the receiver may be any balanced paired metal conductors meeting the requirements of the LVDS standard. This media may be a twisted-pair, twinax, flat ribbon cable, or PCB traces. The nominal characteristic impedance of the interconnect must be from 100 Ω to 120 Ω with variation no more than 10% (90 Ω to 132 Ω).

10.2.3.6 PCB Transmission Lines

As per SNLA187, Figure 39 depicts several transmission line structures commonly used in PCBs. Each structure consists of a signal line and a return path with uniform cross-section along its length. A microstrip is a signal trace on the top (or bottom) layer, separated by a dielectric layer from its return path in a ground or power plane. A stripline is a signal trace in the inner layer, with a dielectric layer in between a ground plane above and below the signal trace. The dimensions of the structure along with the dielectric material properties determine the characteristic impedance of the transmission line (also called controlled-impedance transmission line).

When two signal lines are placed near one another, they form a pair of coupled transmission lines. Figure 39 shows examples of edge-coupled microstrips, and edge-coupled or broad-side-coupled striplines. When excited by differential signals, the coupled transmission line is referred to as a differential pair. The characteristic impedance of each line is called odd-mode impedance. The sum of the odd-mode impedances of each line is the differential impedance of the differential pair. In addition to the trace dimensions and dielectric material properties, the spacing between the two traces determines the mutual coupling and impacts the differential impedance. When the two lines are immediately adjacent; for example, if S is less than 2×W, the differential pair is called a tightly-coupled differential pair. To maintain constant differential impedance along the length, it is important to keep the trace width and spacing uniform along the length, as well as maintain good symmetry between the two lines.

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Typical Application (continued)

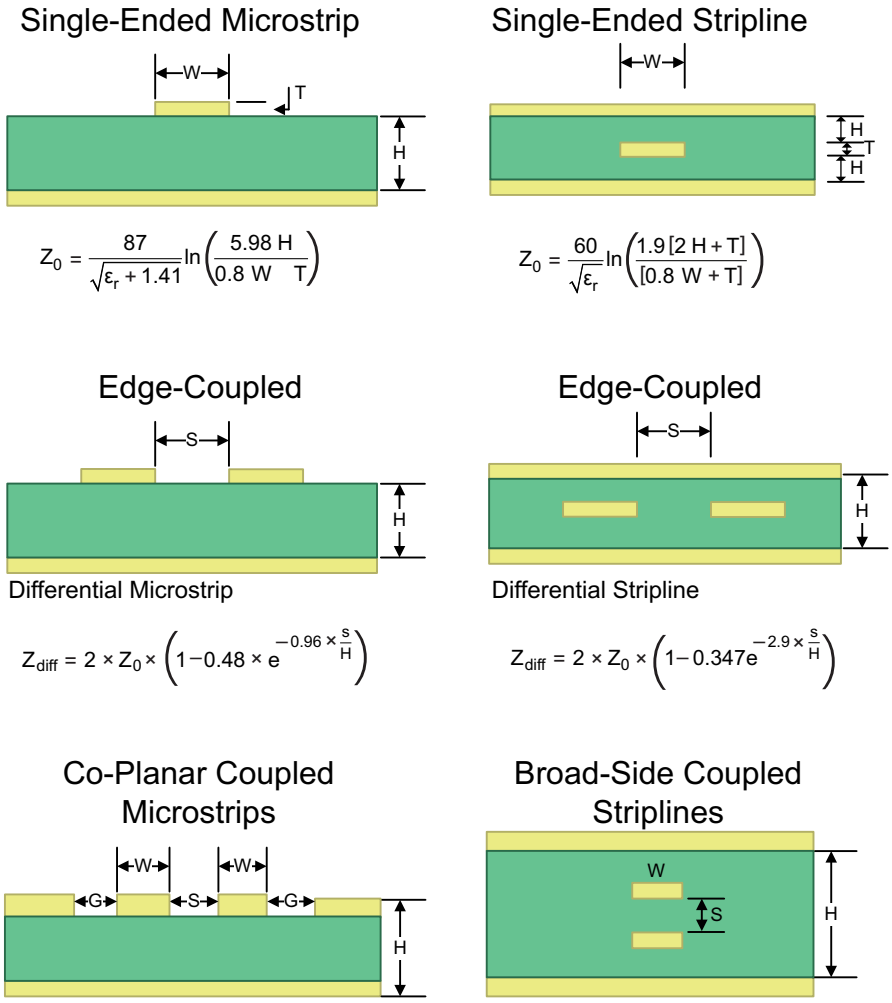


Figure 39. Controlled-Impedance Transmission Lines

10.2.3.7 Termination Resistor

As shown earlier in Figure 37, an LVDS communication channel employs a current source driving a transmission line which is terminated with a resistive load. This load serves to convert the transmitted current into a voltage at the receiver input. To ensure good signal integrity, the termination resistance must be matched to the characteristic impedance of the transmission line. The designer must ensure that the termination resistance is within 10% of the nominal media characteristic impedance. If the transmission line is targeted for 100-Ω impedance, the termination resistance must be from 90 Ω to 110 Ω.

The line termination resistance must be located as close as possible to the receiver, thereby minimizing the stub length from the resistor to the receiver.

When a multidrop topology is used, line termination resistors are typically placed at the end (or ends) of the transmission line.

10.2.3.8 Receiver Supply Voltage

The receiver can support operation with a supply as low as 3 V and as high as 3.6 V.

10.2.3.9 Receiver Input Common-Mode Range

Receiver supports common-mode values in the range of 0.05 V to 2.35 V. This is assuming 100 mV differential signal and a 3.3 V supply.

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Typical Application (continued)

The driver has an output common-mode range of 1.2 V. Using the receiver discussed here, we see that valid operation of the communication link will occur when the ground difference between transmitter and receiver is within approximately ±1 V. The use of differential signaling in LVDS allows operation in an environment where the combination of ground difference and common-mode noise result in a common-mode difference between transmitter and receiver of 1 V. This 1-V potential difference hints at the intended application of LVDS circuits.

Standards such as RS-485 support potential differences of almost 10 V, allowing for communication over distances of greater than 1 km. The intended application of LVDS devices is more moderate distances, such as those from chip to chip on a board, board to board in a rack, or from rack to nearby rack. When the 1-V potential difference is not adequate, yet the high-speed and low-voltage features of LVDS are still needed, the designer can choose from either M-LVDS devices available from TI, or from LVDS devices with extended common-mode ranges, such as the SN65LVDS33.

10.2.3.10 Receiver Input Signal

The LVDS receivers herein comply with the LVDS standard and correctly determine the bus state when the differential input voltage is greater than 100 mV (HI output) or less than –100 mV (LO output).

10.2.3.11 Receiver Output Signal

Receiver outputs comply with LVTTL output voltage standards when the supply voltage is within the range of 3 V to 3.6 V.

10.2.4 Application Curve

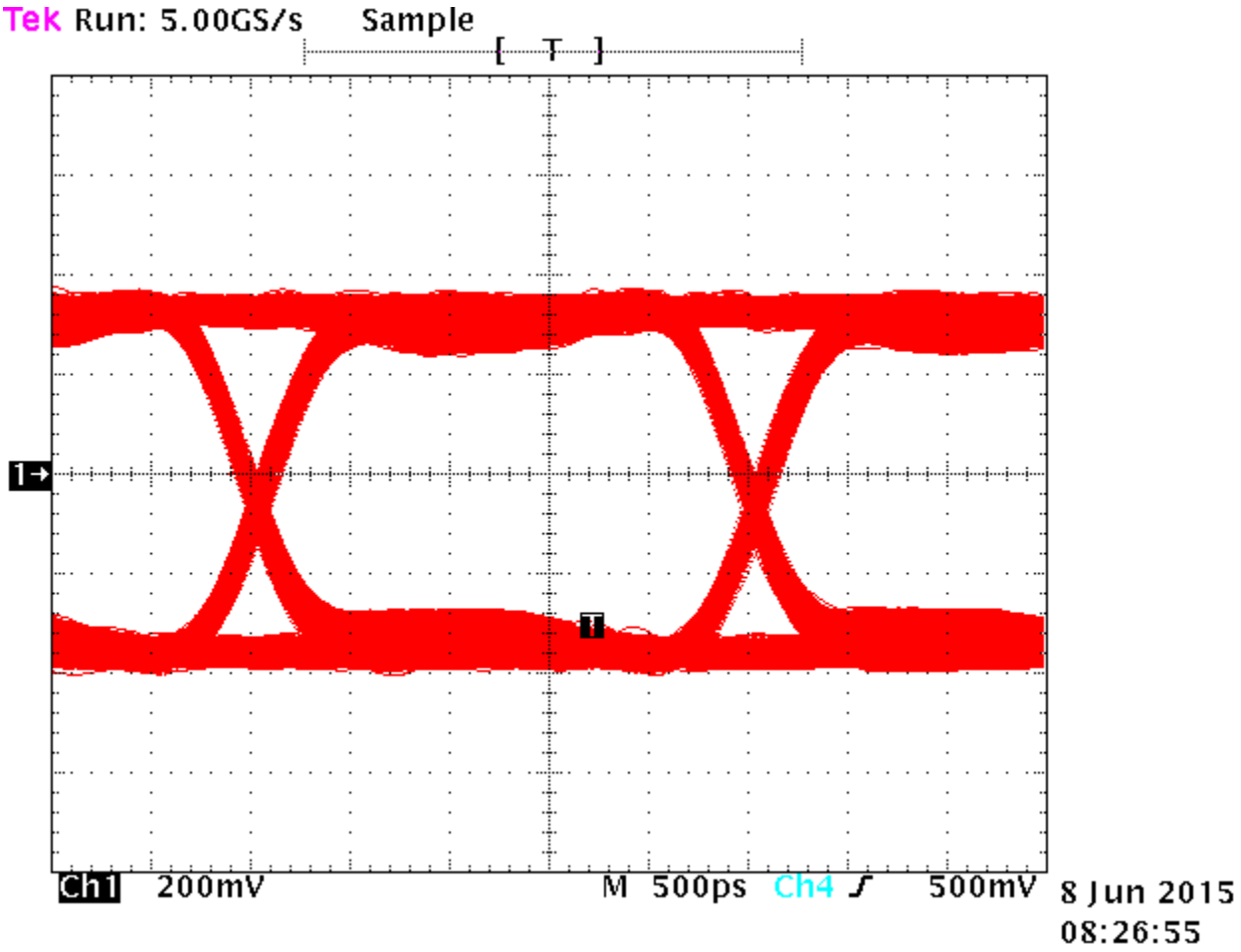


Figure 40. Typical Driver Output Eye Pattern in Point-to-Point System

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10.3 Multidrop Communications

A second common application of LVDS buffers is a multidrop topology. In a multidrop configuration, a single driver and a shared bus are present, along with two or more receivers (with a maximum permissible number of 32 receivers). Figure 41 shows an example of a multidrop system.

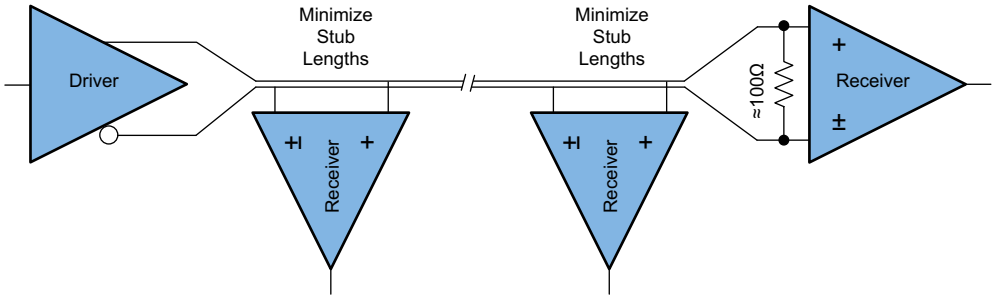


Figure 41. Multidrop Topology

10.3.1 Design Requirements

For this design example, use the parameters listed in Table 4

Table 4. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
Driver supply voltage (V_{CCD})	3 to 3.6 V
Driver input voltage	0.8 to V_{CCD} V
Driver signaling rate	DC to 400 Mbps
Interconnect characteristic impedance	100 Ω
Termination resistance	100 Ω
Number of receiver nodes	2 to 32
Receiver supply voltage (V_{CCR})	3 to 3.6 V
Receiver input voltage	0 to $_{VCCR}$ – 0.8 V
Receiver signaling rate	DC to 400 Mbps
Ground shift between driver and receiver	±1 V

10.3.2 Detailed Design Procedure

10.3.2.1 Interconnecting Media

The interconnect in a multidrop system differs considerably from a point-to-point system. While point-to-point interconnects are straightforward, and well understood, the bus type architecture encountered with multidrop systems requires more careful attention. We will use Figure 41 to explore these details.

The most basic multidrop system would include a single driver, located at a bus origin, with multiple receiver nodes branching off the main line, and a final receiver at the end of the transmission line, co-located with a bus termination resistor. While this would be the most basic multidrop system, it has several considerations not yet explored.

The location of the transmitter at one bus end allows the design concerns to be simplified, but this comes at the cost of flexibility. With a transmitter located at the origin, a single bus termination at the far-end is required. The far-end termination absorbs the incident traveling wave. The flexibility lost with this arrangement is thus: if the single transmitter needed to be relocated on the bus, at any location other than the origin, we would be faced with a bus with one open-circuited end, and one properly terminated end. Locating the transmitter say in the middle of the bus may be desired to reduce (by ½) the maximum flight time from the transmitter to receiver.

Another new feature in Figure 41 is clear in that every node branching off the main line results in stubs. The stubs must be minimized in any case, but have the unintended effect of locally changing the loaded impedance of the bus.

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To a good approximation, the characteristic transmission line impedance of an unloaded multipoint or multidrop bus is defined by √L/C, where L is the inductance per unit length and C is the capacitance per unit length. As capacitance is added to the bus in the form of devices and interconnections, the bus characteristic impedance is lowered. This may result in signal reflections from the impedance mismatch between the unloaded and loaded segments of the bus.

If the number of loads is constant and can be distributed evenly along the line, reflections can be reduced by changing the bus termination resistors to match the loaded characteristic impedance. Normally, the number of loads are not constant or distributed evenly and the reflections resulting from any mismatching must be accounted for in the noise budget.

11 Power Supply Recommendations

11.1 Coupling Capacitor Recommendations

To minimize the power supply noise floor, provide good decoupling near the SN65LVDS10x power pins. It is recommended to place one 0.01-µF ceramic capacitor at each power pin, and two 0.1-µF ceramic capacitors on each power node. The distance between the device and capacitors must be minimized to reduce loop inductance and provide optimal noise filtering. Placing the capacitor underneath the device on the bottom of the PCB is often a good choice. A 100-pF ceramic capacitor can be put at each power pin to optimize the EMI performance.

12 Layout

12.1 Layout Guidelines

12.1.1 Microstrip vs. Stripline Topologies

As per SLLD009, printed-circuit boards usually offer designers two transmission line options: microstrip and stripline. Microstrips are traces on the outer layer of a PCB, as shown in Figure 42.

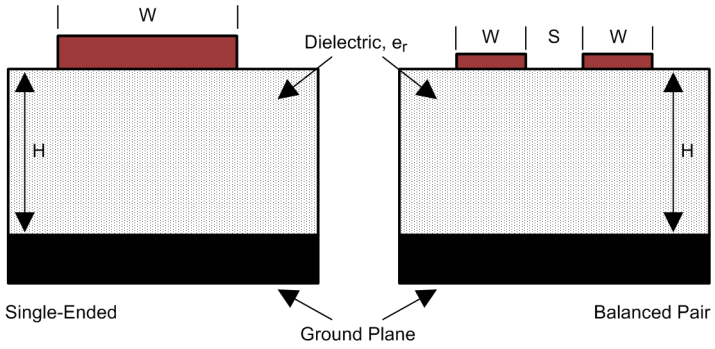


Figure 42. Microstrip Topology

On the other hand, striplines are traces between two ground planes. Striplines are less prone to emissions and susceptibility problems because the reference planes effectively shield the embedded traces. However, from the standpoint of high-speed transmission, juxtaposing two planes creates additional capacitance. TI recommends routing LVDS signals on microstrip transmission lines, if possible. The PCB traces allow designers to specify the necessary tolerances for ZO based on the overall noise budget and reflection allowances. Footnotes (1), (2)and (3)provide formulas for ZO and tPD for differential and single-ended traces.

(1) Howard Johnson & Martin Graham.1993. High Speed Digital Design – A Handbook of Black Magic. Prentice Hall PRT. ISBN number 013395724.
(2) Mark I. Montrose. 1996. Printed Circuit Board Design Techniques for EMC Compliance. IEEE Press. ISBN number 0780311310.
(3) Clyde F. Coombs, Jr. Ed, Printed Circuits Handbook, McGraw Hill, ISBN number 0070127549.

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Layout Guidelines (continued)

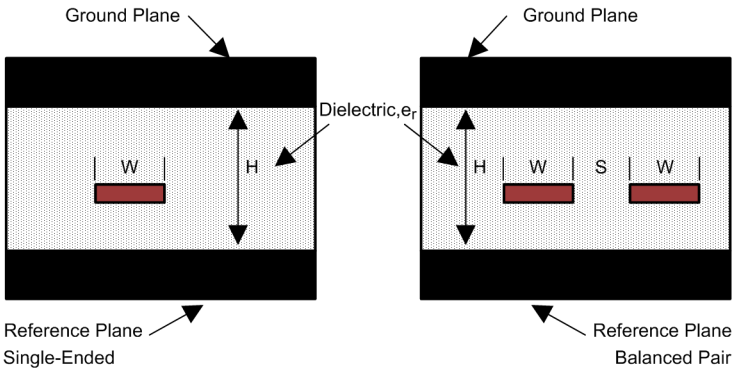


Figure 43. Stripline Topology

12.1.2 Dielectric Type and Board Construction

The speeds at which signals travel across the board dictates the choice of dielectric. FR-4, or equivalent, usually provides adequate performance for use with LVDS signals. If rise or fall times of TTL/CMOS signals are less than 500 ps, empirical results indicate that a material with a dielectric constant near 3.4, such as Rogers™ 4350 or Nelco N4000-13 is better suited. Once the designer chooses the dielectric, there are several parameters pertaining to the board construction that can affect performance. The following set of guidelines were developed experimentally through several designs involving LVDS devices:

- Copper weight: 15 g or 1/2 oz start, plated to 30 g or 1 oz
- All exposed circuitry must be solder-plated (60/40) to 7.62 µm or 0.0003 in. (minimum)
- Copper must must be 25.4 µm or 0.001 in. (minimum)

12.1.3 Recommended Stack Layout

Following the choice of dielectrics and design specifications, you must decide how many levels to use in the stack. To reduce the TTL/CMOS to LVDS crosstalk, it is a good practice to have at least two separate signal planes as shown in Figure 44.

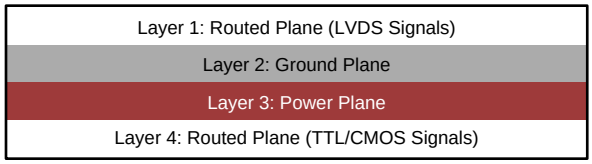


Figure 44. Four-Layer PCB Board

NOTE

The separation between layers 2 and three should be 127 µm (0.005 in). By keeping the power and ground planes tightly coupled, the increased capacitance acta as a bypass for transients.

One of the most common stack configurations is the six-layer board as shown in Figure 45

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Layout Guidelines (continued)

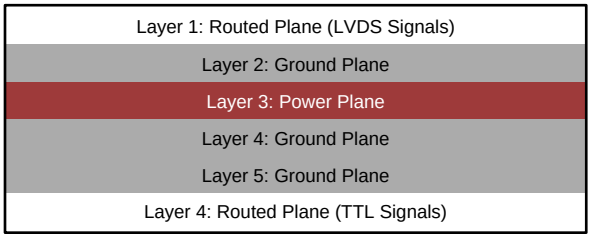


Figure 45. Six-Layer PCB Board

In this particular configuration, it is possible to isolate each signal layer from the power plane by at least one ground plane. The result is improved signal integrity; however, fabrication is more expensive. Using the 6-layer board is preferable, because it offers the layout designer more flexibility in varying the distance between signal layers and referenced planes, in addition to ensuring reference to a ground plane for signal layers 1 and 6.

12.1.4 Separation Between Traces

The separation between traces depends on several factors. However, the amount of coupling that can be tolerated usually dictates the actual separation. Low noise coupling requires close coupling between the differential pair of an LVDS link to benefit from the electromagnetic field cancellation. The traces must be 100-Ω differential and thus coupled in the manner that best fits this requirement. In addition, differential pairs must have the same electrical length to ensure that they are balanced, thus minimizing problems with skew and signal reflection.

In the case of two adjacent single-ended traces, one must use the 3-W rule, which stipulates that the distance between two traces must be greater than two times the width of a single trace, or three times its width measured from trace center to trace center. This increased separation effectively reduces the potential for crosstalk. The same rule must be applied to the separation between adjacent LVDS differential pairs, whether the traces are edge-coupled or broad-side-coupled.

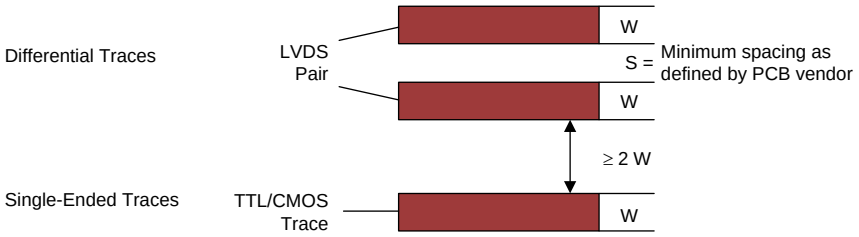


Figure 46. 3-W Rule for Single-Ended and Differential Traces (Top View)

You must exercise caution when using autorouters, because they do not always account for all factors affecting crosstalk and signal reflection. For instance, it is best to avoid sharp 90° turns to prevent discontinuities in the signal path. Using successive 45° turns tends to minimize reflections.

12.1.5 Crosstalk and Ground Bounce Minimization

To reduce crosstalk, it is important to provide a return path to high-frequency currents that is as close as possible to its originating trace. A ground plane usually achieves this. Because the returning currents always choose the path of lowest inductance, they are most likely to return directly under the original trace, thus minimizing crosstalk. Lowering the area of the current loop lowers the potential for crosstalk. Traces kept as short as possible with an uninterrupted ground plane running beneath them emit the minimum amount of electromagnetic field strength. Discontinuities in the ground plane increase the return path inductance and must be avoided.

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Layout Guidelines (continued)

12.1.6 Decoupling

Each power or ground lead of a high-speed device must be connected to the PCB through a low inductance path. For best results, one or more vias are used to connect a power or ground pin to the nearby plane. Ideally, via placement is immediately adjacent to the pin to avoid adding trace inductance. Placing a power plane closer to the top of the board reduces the effective via length and its associated inductance.

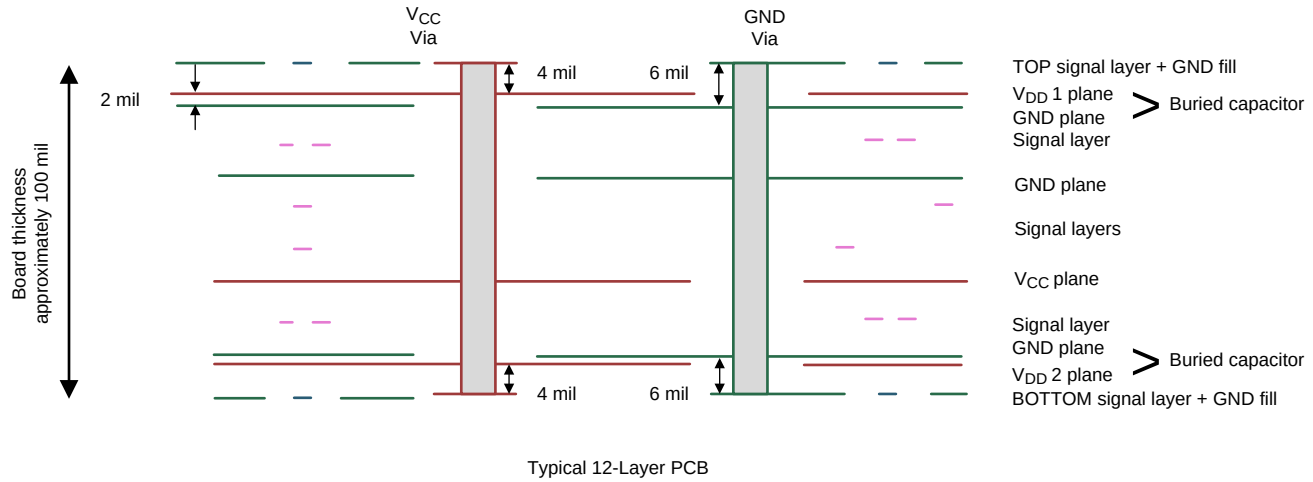


Figure 47. Low Inductance, High-Capacitance Power Connection

Bypass capacitors must be placed close to VDD pins. They can be placed conveniently near the corners or underneath the package to minimize the loop area. This extends the useful frequency range of the added capacitance. Small-physical-size capacitors, such as 0402 or even 0201, or X7R surface-mount capacitors must be used to minimize body inductance of capacitors. Each bypass capacitor is connected to the power and ground plane through vias tangent to the pads of the capacitor as shown in Figure 48(a).

An X7R surface-mount capacitor of size 0402 has about 0.5 nH of body inductance. At frequencies above 30 MHz or so, X7R capacitors behave as low-impedance inductors. To extend the operating frequency range to a few hundred MHz, an array of different capacitor values like 100 pF, 1 nF, 0.03 µF, and 0.1 µF are commonly used in parallel. The most effective bypass capacitor can be built using sandwiched layers of power and ground at a separation of 2 to 3 mils. With a 2-mil FR4 dielectric, there is approximately 500 pF per square inch of PCB. Refer back to Figure 5-1 for some examples. Many high-speed devices provide a low-inductance GND connection on the backside of the package. This center dap must be connected to a ground plane through an array of vias. The via array reduces the effective inductance to ground and enhances the thermal performance of the small Surface Mount Technology (SMT) package. Placing vias around the perimeter of the dap connection ensures proper heat spreading and the lowest possible die temperature. Placing high-performance devices on opposing sides of the PCB using two GND planes (as shown in Figure 46) creates multiple paths for heat transfer. Often thermal PCB issues are the result of one device adding heat to another, resulting in a very high local temperature. Multiple paths for heat transfer minimize this possibility. In many cases the GND dap that is so important for heat dissipation makes the optimal decoupling layout impossible to achieve due to insufficient padto- dap spacing as shown in Figure 48(b). When this occurs, placing the decoupling capacitor on the backside of the board keeps the extra inductance to a minimum. It is important to place the VDD via as close to the device pin as possible while still allowing for sufficient solder mask coverage. If the via is left open, solder may flow from the pad and into the via barrel. This will result in a poor solder connection.

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Layout Guidelines (continued)



Figure 48. Typical Decoupling Capacitor Layouts

12.2 Layout Example

At least two or three times the width of an individual trace must separate single-ended traces and differential pairs to minimize the potential for crosstalk. Single-ended traces that run in parallel for less than the wavelength of the rise or fall times usually have negligible crosstalk. Increase the spacing between signal paths for long parallel runs to reduce crosstalk. Boards with limited real estate can benefit from the staggered trace layout, as shown in Figure 49.

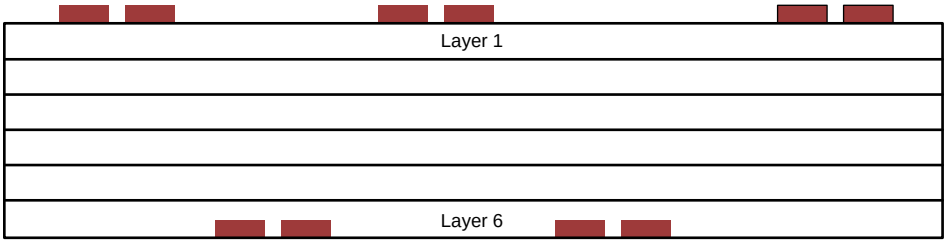


Figure 49. Staggered Trace Layout

This configuration lays out alternating signal traces on different layers; thus, the horizontal separation between traces can be less than 2 or 3 times the width of individual traces. To ensure continuity in the ground signal path, TI recommends having an adjacent ground via for every signal via, as shown in Figure 50. Note that vias create additional capacitance. For example, a typical via has a lumped capacitance effect of 1/2 pF to 1 pF in FR4.

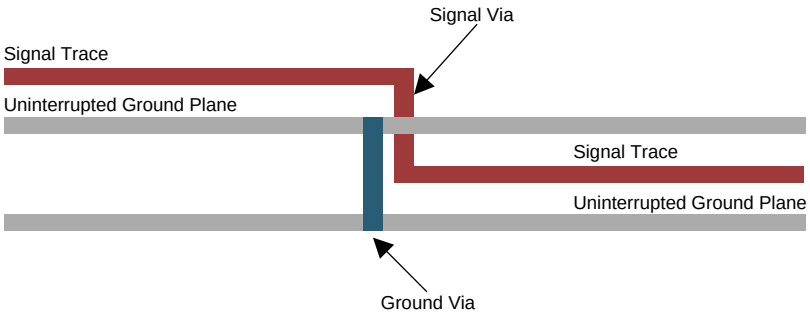


Figure 50. Ground Via Location

Short and low-impedance connection of the device ground pins to the PCB ground plane reduces ground bounce. Holes and cutouts in the ground planes can adversely affect current return paths if they create discontinuities that increase returning current loop areas.

To minimize EMI problems, TI recommends avoiding discontinuities below a trace (for example, holes, slits, and so on) and keeping traces as short as possible. Zoning the board wisely by placing all similar functions in the same area, as opposed to mixing them together, helps reduce susceptibility issues.

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13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 5. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN65LVDS104	Click here	Click here	Click here	Click here	Click here
SN65LVDS105	Click here	Click here	Click here	Click here	Click here

13.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65LVDS104D	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS104
SN65LVDS104D.B	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS104
SN65LVDS104DG4	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS104
SN65LVDS104DR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS104
SN65LVDS104DR.B	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS104
SN65LVDS104PW	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS104
SN65LVDS104PW.B	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS104
SN65LVDS104PWG4	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS104
SN65LVDS104PWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS104
SN65LVDS104PWR.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS104
SN65LVDS104PWRG4	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS104
SN65LVDS105D	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS105
SN65LVDS105D.B	Active	Production	SOIC (D) | 16	40 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS105
SN65LVDS105DR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS105
SN65LVDS105DR.B	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS105
SN65LVDS105PW	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS105
SN65LVDS105PW.B	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS105
SN65LVDS105PWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS105
SN65LVDS105PWR.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS105
SN65LVDS105PWRG4	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS105

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

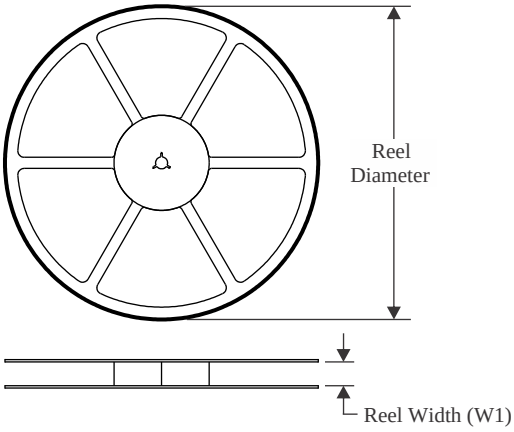
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

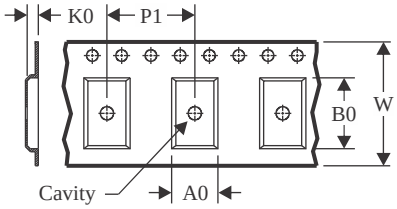
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

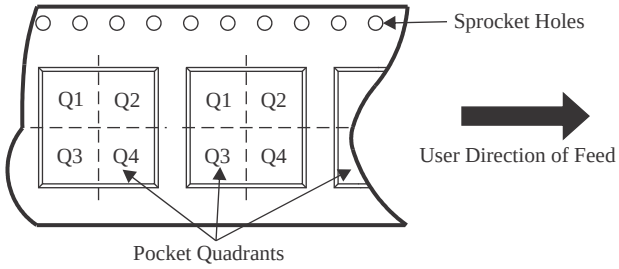


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

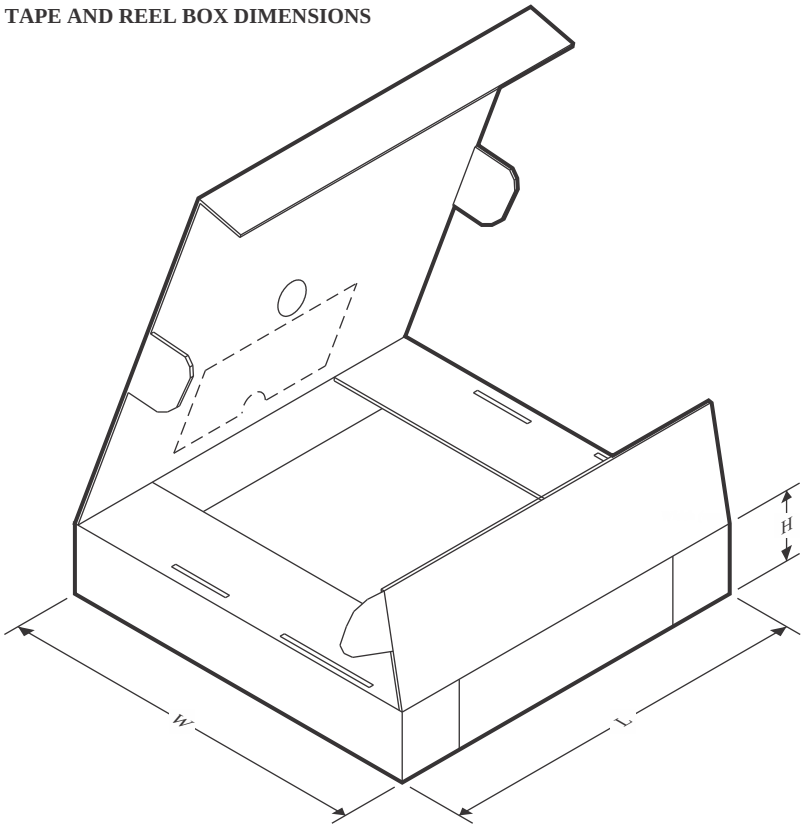
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDS104DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN65LVDS104PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN65LVDS105DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN65LVDS105PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

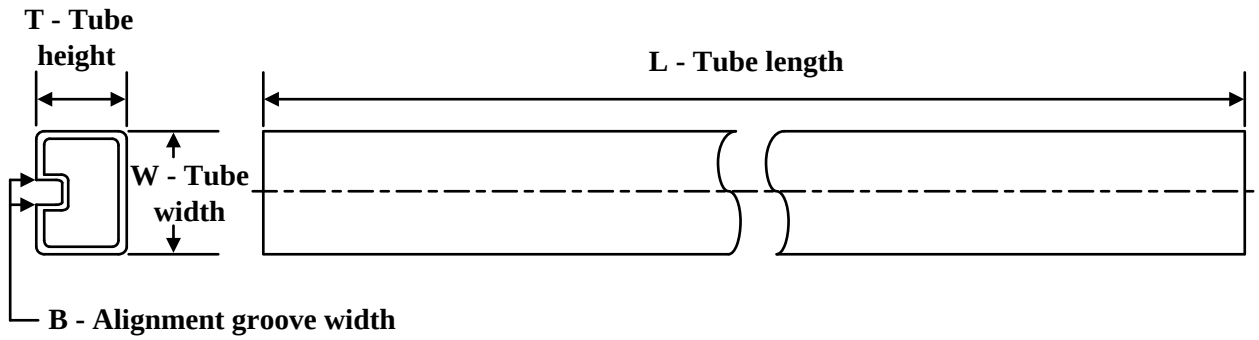
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVDS104DR	SOIC	D	16	2500	350.0	350.0	43.0
SN65LVDS104PWR	TSSOP	PW	16	2000	353.0	353.0	32.0
SN65LVDS105DR	SOIC	D	16	2500	350.0	350.0	43.0
SN65LVDS105PWR	TSSOP	PW	16	2000	353.0	353.0	32.0

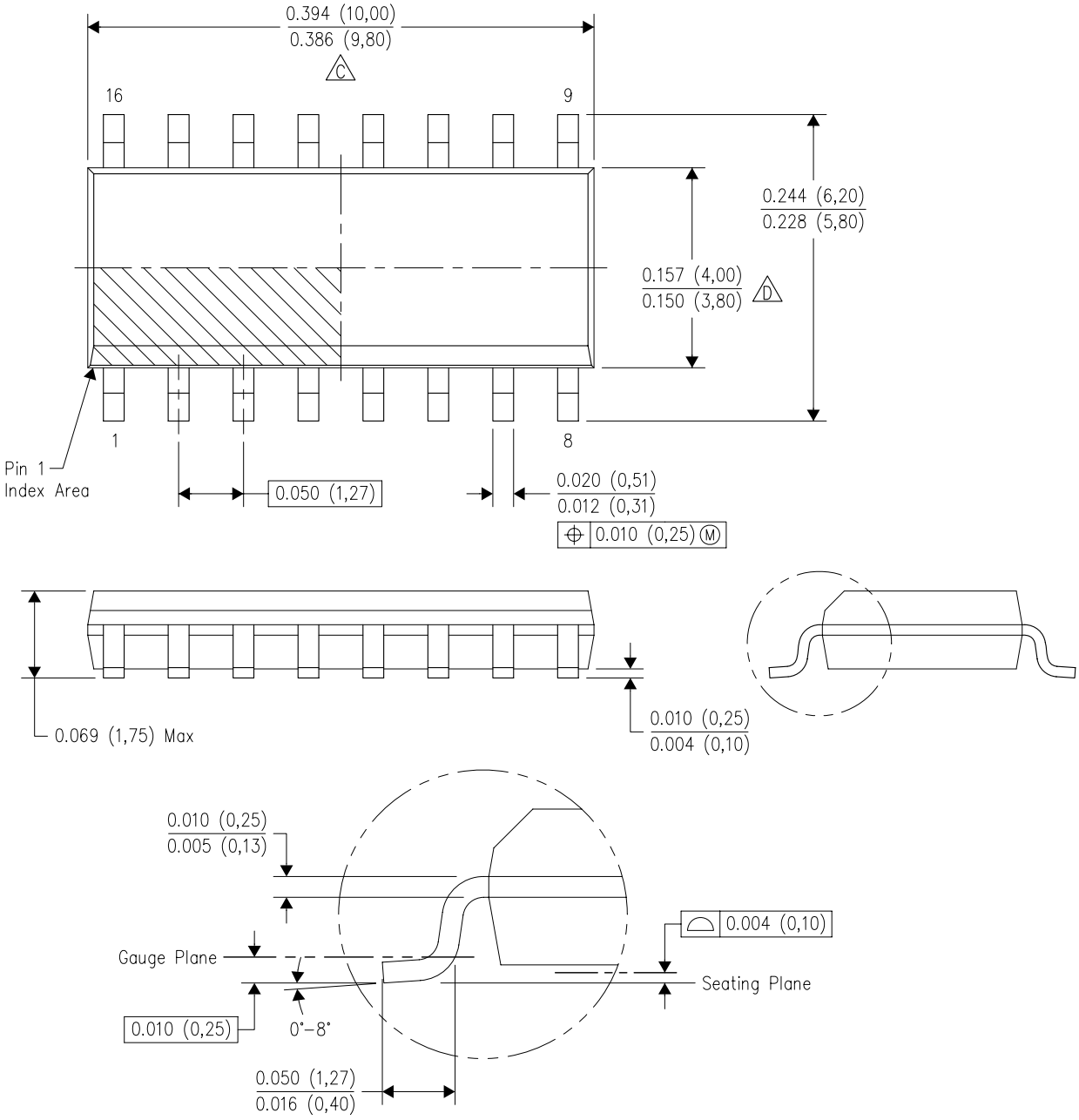
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65LVDS104D	D	SOIC	16	40	505.46	6.76	3810	4
SN65LVDS104D.B	D	SOIC	16	40	505.46	6.76	3810	4
SN65LVDS104DG4	D	SOIC	16	40	505.46	6.76	3810	4
SN65LVDS104PW	PW	TSSOP	16	90	530	10.2	3600	3.5
SN65LVDS104PW.B	PW	TSSOP	16	90	530	10.2	3600	3.5
SN65LVDS104PWG4	PW	TSSOP	16	90	530	10.2	3600	3.5
SN65LVDS105D	D	SOIC	16	40	505.46	6.76	3810	4
SN65LVDS105D.B	D	SOIC	16	40	505.46	6.76	3810	4
SN65LVDS105PW	PW	TSSOP	16	90	530	10.2	3600	3.5
SN65LVDS105PW.B	PW	TSSOP	16	90	530	10.2	3600	3.5

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



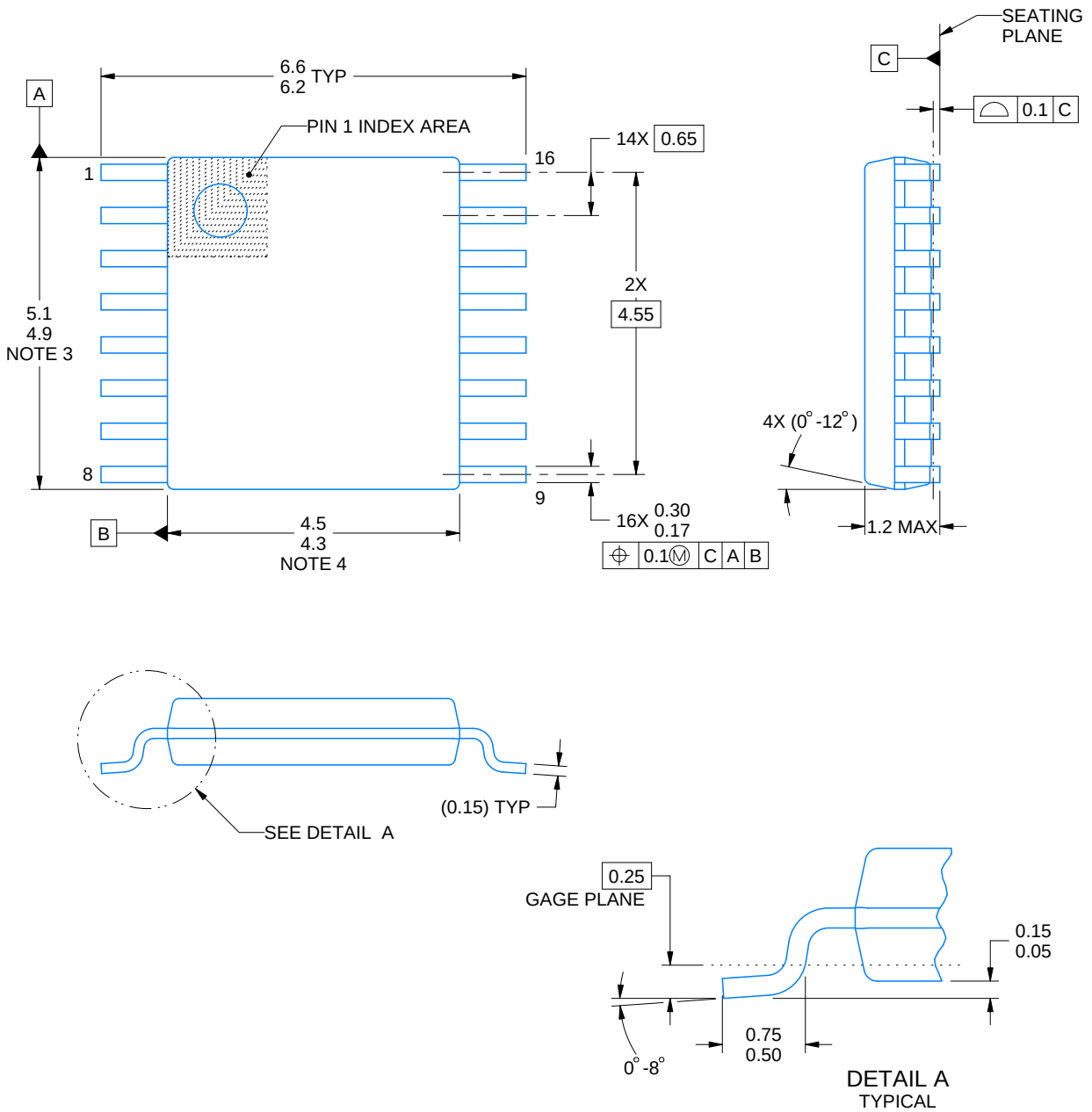
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

PACKAGE OUTLINE

PW0016A

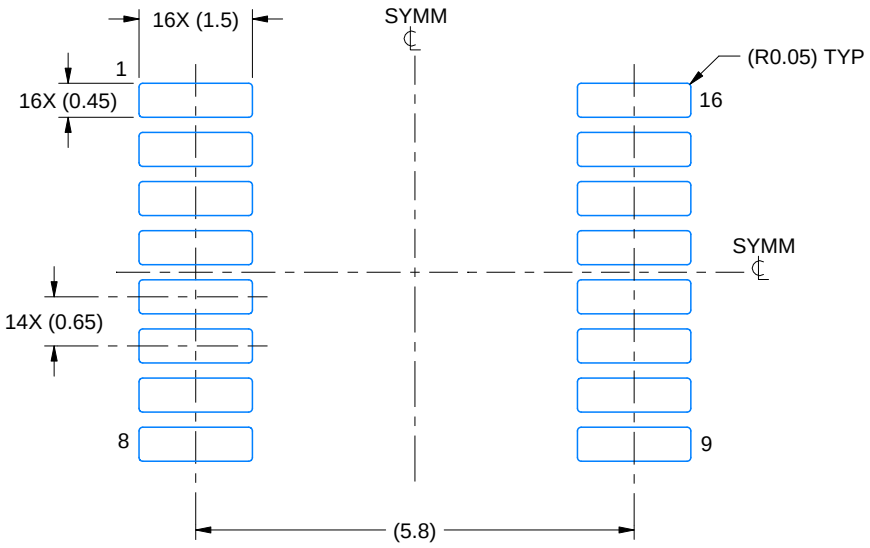
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

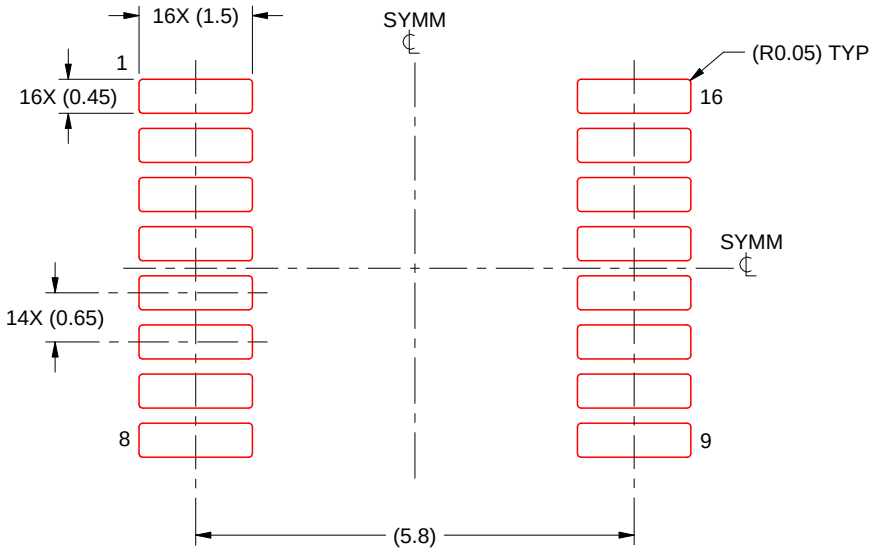


SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025