SN65LVDS93A FlatLink™ Transmitter

1 Features

- Industrial Temperature Range –40°C to 85°C
- LVDS Display Serdes Interfaces Directly to LCD Display Panels With Integrated LVDS
- Package Options: 4.5-mm × 7-mm BGA, and 8.1-mm × 14-mm TSSOP
- 1.8 V up to 3.3-V Tolerant Data Inputs to Connect Directly to Low-Power, Low-Voltage Application and Graphic Processors
- Transfer Rate up to 135 Mpps (Mega Pixels Per Second); Pixel Clock Frequency Range 10 MHz to 135 MHz
- Suited for Display Resolutions Ranging From HVGA up to HD With Low EMI
- Operates From a Single 3.3-V Supply and 170 mW (Typical) at 75 MHz
- 28 Data Channels Plus Clock In Low-Voltage TTL to 4 Data Channels Plus Clock Out Low-Voltage Differential
- Consumes Less Than 1 mW When Disabled
- Selectable Rising or Falling Clock Edge Triggered Inputs
- ESD: 5-kV HBM
- Supports Spread Spectrum Clocking (SSC)
- Compatible With all OMAP™2x, OMAP3x, and DaVinci™ Application Processors

2 Applications

- LCD Display Panel Drivers
- UMPC and Netbook PCs
- Digital Picture Frames

3 Description

The SN65LVDS93A LVDS SerDes (serializer/deserializer) transmitter contains four 7-bit parallel load serial-out shift registers, a 7 × clock synthesizer, and five low-voltage differential signaling (LVDS) drivers in a single integrated circuit. These functions allow synchronous transmission of 28 bits of single-ended LVTTL data over five balanced-pair conductors for receipt by a compatible receiver, such as the SN65LVDS94 (SLLS928).

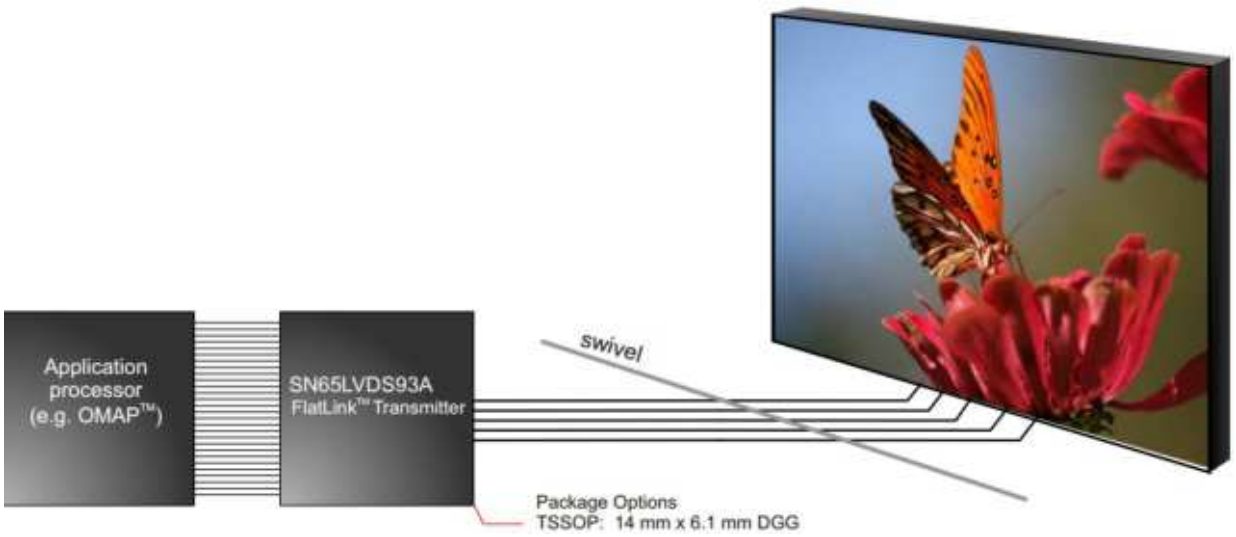
When transmitting, data bits D0 through D27 are each loaded into registers upon the edge of the input clock signal (CLKIN). The rising or falling edge of the clock can be selected through the clock select (CLKSEL) pin. The frequency of CLKIN is multiplied seven times and then used to serially unload the data registers in 7-bit slices. The four serial streams and a phase-locked clock (CLKOUT) are then output to LVDS output drivers. The frequency of CLKOUT is the same as the input clock, CLKIN.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN65LVDS93A	TSSOP (56)	14.00 mm × 6.10 mm
	BGA MICROSTAR JUNIOR (56)	7.00 mm × 4.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

RGB Video System Using Discrete LVDS TX



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Description (continued) ... 3
6 Pin Configuration and Functions ... 3
7 Specifications ... 6
7.1 Absolute Maximum Ratings ... 6
7.2 ESD Ratings ... 6
7.3 Recommended Operating Conditions ... 7
7.4 Thermal Information ... 7
7.5 Electrical Characteristics ... 7
7.6 Timing Requirements ... 8
7.7 Switching Characteristics ... 9
7.8 Typical Characteristics ... 11
8 Parameter Measurement Information ... 12
9 Detailed Description ... 16
9.1 Overview ... 16
9.2 Functional Block Diagram ... 16
9.3 Feature Description ... 17
9.4 Device Functional Modes ... 18
10 Application and Implementation ... 19
10.1 Application Information ... 19
10.2 Typical Application ... 20
11 Power Supply Recommendations ... 27
12 Layout ... 27
12.1 Layout Guidelines ... 27
12.2 Layout Example ... 29
13 Device and Documentation Support ... 31
13.1 Documentation Support ... 31
13.2 Trademarks ... 31
13.3 Electrostatic Discharge Caution ... 31
13.4 Glossary ... 31
14 Mechanical, Packaging, and Orderable Information ... 31

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (August 2011) to Revision B **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Original (August 2009) to Revision A **Page**

- Deleted all maximum values from I_{CC} - Supply current (average) ... 8
- Changed t_{en} - Enable Time, unit value From: 6 ns To: 6 µs ... 9

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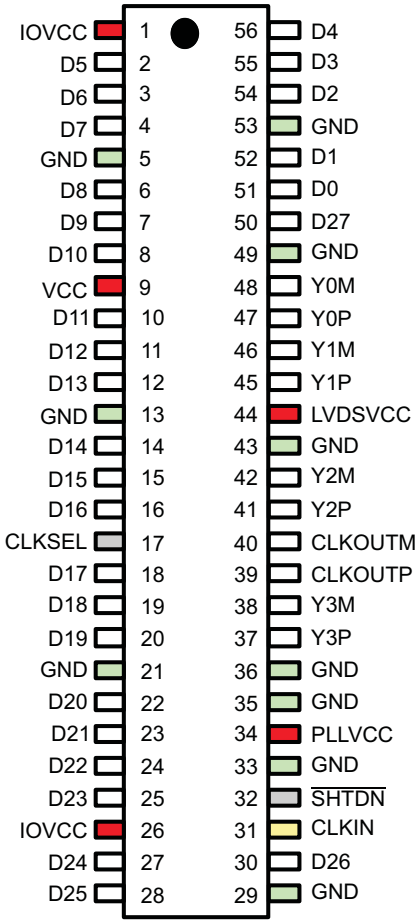
5 Description (continued)

The SN65LVDS93A device requires no external components and little or no control. The data bus appears the same at the input to the transmitter and output of the receiver with the data transmission transparent to the users. The only user intervention is selecting a clock rising edge by inputting a high level to CLKSEL or a falling edge with a low-level input and the possible use of the shutdown/clear (SHTDN) signal. SHTDN is an active-low input to inhibit the clock and shut off the LVDS output drivers for lower power consumption. A low level on this signal clears all internal registers at a low level.

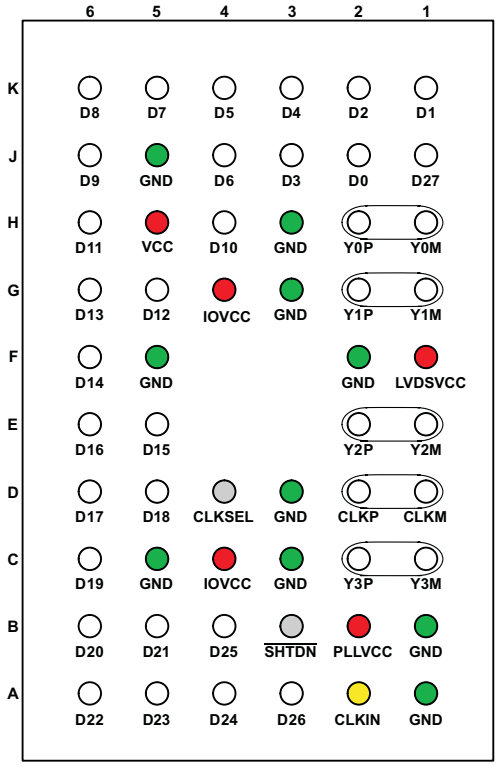
The SN65LVDS93A is characterized for operation over ambient air temperatures of –40°C to 85°C.

6 Pin Configuration and Functions

DGG Package
56-Pin TSSOP
(Top View)



ZQL Package
56-Ball BGA MICROSTAR
(Top View)



Pin Functions - TSSOP

PIN		I/O	DESCRIPTION
NAME	NO.		
CLKSEL	17	I	Selects between rising edge input clock trigger (CLKSEL = V_{IH}) and falling edge input clock trigger (CLKSEL = V_{IL}).
CLKIN	31	I	Input pixel clock; rising or falling clock polarity is selectable by Control input CLKSEL.
CLKOUTM	40	O	Differential LVDS pixel clock output. Output is high-impedance when $\overline{SHTDN}$ is pulled low (de-asserted).
CLKOUTP	39	O	
D0	51	I	Data inputs; supports 1.8-V to 3.3-V input voltage selectable by VDD supply. To connect a graphic source successfully to a display, the bit assignment of D[27:0] is critical (and not necessarily intuitive). Note: if application only requires 18-bit color, connect unused inputs D5, D10, D11, D16, D17, D23, and D27 to GND
D1	52		
D2	54		
D3	55		
D4	56		
D5	2		
D6	3		
D7	4		
D8	6		
D9	7		
D10	8		
D11	10		
D12	11		
D13	12		
D14	14		
D15	15		
D16	16		
D17	18		
D18	19		
D19	20		
D20	22		
D21	23		
D22	24		
D23	25		
D24	27		
D25	28		
D26	30		
D27	50		
GND	5, 13, 21, 29, 33, 35, 36, 43, 49, 53	Power Supply(1)	Supply Ground for VCC, IOVCC, LVDSVCC, and PLLVCC.
IOVCC	1, 26		I/O supply reference voltage (1.8 V up to 3.3 V matching the GPU data output signal swing)
LVDSVCC	44		3.3-V LVDS output analog supply
PLLVCC	34		3.3-V PLL analog supply
$\overline{SHTDN}$	32	I	Device shut down; pull low (de-assert) to shut down the device (low power, resets all registers) and high (assert) for normal operation.
VCC	9	Power Supply(1)	3.3-V digital supply voltage

(1) For a multilayer pcb, TI recommends keeping one common GND layer underneath the device and connecting all ground terminals directly to this plane.

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Pin Functions - TSSOP (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
Y0M	48	O	Differential LVDS data outputs. Outputs are high-impedance when $\overline{\text{SHTDN}}$ is pulled low (de-asserted)
Y1M	46		
Y2M	42		
Y0P	47		
Y1P	45		
Y2P	41		
Y3M	38	O	Differential LVDS Data outputs. Output is high-impedance when $\overline{\text{SHTDN}}$ is pulled low (de-asserted). Note: if the application only requires 18-bit color, this output can be left open.
Y3P	37		

Pin Functions - BGA MICROSTAR

BALL		I/O	DESCRIPTION
NAME	NO.		
CLKIN	A2	CMOS IN with pulldn	Input pixel clock; rising or falling clock polarity is selectable by Control input CLKSEL.
CLKM	D1	LVDS Out	Differential LVDS pixel clock output. Output is high-impedance when $\overline{\text{SHTDN}}$ is pulled low (de-asserted).
CLKP	D2		
CLKSEL	D4	CMOS IN with pulldn	Selects between rising edge input clock trigger (CLKSEL = V_{IH}) and falling edge input clock trigger (CLKSEL = V_{IL}).
D0	J2	CMOS IN with pulldn	Data inputs; supports 1.8-V to 3.3-V input voltage selectable by VDD supply. To connect a graphic source successfully to a display, the bit assignment of D[27:0] is critical (and not necessarily intuitive). Note: if application only requires 18-bit color, connect unused inputs D5, D10, D11, D16, D17, D23, and D27 to GND.
D1	K1		
D2	K2		
D3	J3		
D4	K3		
D5	K4		
D6	J4		
D7	K5		
D8	K6		
D9	J6		
D10	H4		
D11	H6		
D12	G5		
D13	G6		
D14	F6		
D15	E5		
D16	E6		
D17	D6		
D18	D5		
D19	C6		
D20	B6		
D21	B5		
D22	A6		
D23	A5		
D24	A4		
D25	B4		
D26	A3		
D27	J1		

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Pin Functions - BGA MICROSTAR (continued)

BALL		I/O	DESCRIPTION
NAME	NO.		
GND	A1, B1, C3, C5, F2, F5, J5, D3, G3, H3	Power Supply (1)	Supply Ground for VCC, IOVCC, LVDSVCC, and PLLVCC.
IOVCC	C4, G4		I/O supply reference voltage (1.8 V up to 3.3 V matching the GPU data output signal swing)
LVDSVCC	F1		3.3-V LVDS output analog supply
PLLVCC	B2		3.3-V PLL analog supply
$\overline{SHTDN}$	B3	CMOS IN with pulldn	Device shut down; pull low (de-assert) to shut down the device (low power, resets all registers) and high (assert) for normal operation.
VCC	H5	Power Supply (1)	3.3-V digital supply voltage
Y0M	H1	LVDS Out	Differential LVDS data outputs. Outputs are high-impedance when $\overline{SHTDN}$ is pulled low (de-asserted)
Y1M	G1		
Y2M	E1		
Y0P	H2		
Y1P	G2		
Y2P	E2		
Y3M	C1	LVDS Out	Differential LVDS Data outputs. Output is high-impedance when $\overline{SHTDN}$ is pulled low (de-asserted). Note: if the application only requires 18-bit color, this output can be left open.
Y3P	C2		
--	E3, E4, F3, F4	–	Not connected

(1) For a multilayer pcb, it is recommended to keep one common GND layer underneath the device and connect all ground terminals directly to this plane.

7 Specifications

7.1 Absolute Maximum Ratings (1)

	MIN	MAX	UNIT
Supply voltage, VCC, IOVCC, LVDSVCC, PLLVCC (2)	–0.5	4	V
Voltage at any output terminal	–0.5	VCC + 0.5	V
Voltage at any input terminal	–0.5	IOVCC + 0.5	V
Continuous power dissipation	See *Thermal Information*		
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the GND terminals.

7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±5000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
Supply voltage, VCC		3	3.3	3.6	V
LVDS output supply voltage, LVDSVCC		3	3.3	3.6	
PLL analog supply voltage, PLLVCC		3	3.3	3.6	
IO input reference supply voltage, IOVCC		1.62	1.8 / 2.5 / 3.3	3.6	
Power supply noise on any VCC terminal				0.1	
High-level input voltage, V_{IH}	IOVCC = 1.8 V	IOVCC/2 + 0.3 V			V
	IOVCC = 2.5 V	IOVCC/2 + 0.4 V			
	IOVCC = 3.3 V	IOVCC/2 + 0.5 V			
Low-level input voltage, V_{IL}	IOVCC = 1.8 V			IOVCC/2 – 0.3 V	V
	IOVCC = 2.5 V			IOVCC/2 – 0.4 V	
	IOVCC = 3.3 V			IOVCC/2 – 0.5 V	
Differential load impedance, Z_L		90		132	Ω
Operating free-air temperature, T_A		–45		85	°C

7.4 Thermal Information

THERMAL METRIC(1)		SN65LVDS93A		UNIT
		ZQL (BGA MICROSTAR)	DGG (TSSOP)	
		56 PINS	56 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	67.1	62.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	25.2	18.4	
$R_{\theta JB}$	Junction-to-board thermal resistance	31.0	31.1	
ψ_{JT}	Junction-to-top characterization parameter	0.8	0.8	
ψ_{JB}	Junction-to-board characterization parameter	30.3	30.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_T	Input voltage threshold	R_L = 100 Ω, See Figure 7		IOVCC/2		V
$\lvert V_{OD}\rvert$	Differential steady-state output voltage magnitude		250		450	mV
$\Delta\lvert V_{OD}\rvert$	Change in the steady-state differential output voltage magnitude between opposite binary states			1	35	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 7 $t_{R/F}$ (Dx, CLKin) = 1 ns	1.125		1.375	V
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage				35	mV
I_{IH}	High-level input current	V_{IH} = IOVCC			25	µA
I_{IL}	Low-level input current	V_{IL} = 0 V			±10	µA
I_{OS}	Short-circuit output current	V_{OY} = 0 V			±24	mA
		V_{OD} = 0 V			±12	mA
I_{OZ}	High-impedance state output current	V_O = 0 V to VCC			±20	µA
R_{pdn}	Input pulldown integrated resistor on all inputs (Dx, CLKSEL, $\overline{SHTDN}$, CLKIN)	IOVCC = 1.8 V		200		kΩ
		IOVCC = 3.3 V		100		
I_Q	Quiescent current	Disabled, all inputs at GND; $\overline{SHTDN}$ = V_{IL}		2	100	µA

(1) All typical values are at VCC = 3.3 V, T_A = 25°C.

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Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
I_{CC}	Supply current (average)	$\overline{SHTDN}$ = V_{IH}, R_L = 100 Ω (5 places), grayscale pattern (Figure 8) VCC = 3.3 V, f_{CLK} = 75 MHz				
		$I_{(VCC)}$ + $I_{(PLLVCC)}$ + $I_{(LVDSVCC)}$		51.9		mA
		$I_{(IOVCC)}$ with IOVCC = 3.3 V		0.4		
		$I_{(IOVCC)}$ with IOVCC = 1.8 V		0.1		
		$\overline{SHTDN}$ = V_{IH}, R_L = 100 Ω (5 places), 50% transition density pattern (Figure 8), VCC = 3. 3 V, f_{CLK} = 75 MHz				
		$I_{(VCC)}$ + $I_{(PLLVCC)}$ + $I_{(LVDSVCC)}$		53.3		mA
		$I_{(IOVCC)}$ with IOVCC = 3.3 V		0.6		
		$I_{(IOVCC)}$ with IOVCC = 1.8 V		0.2		
		$\overline{SHTDN}$ = V_{IH}, R_L = 100 Ω (5 places), worst-case pattern (Figure 9), VCC = 3.6 V, f_{CLK} = 75 MHz				
		$I_{(VCC)}$ + $I_{(PLLVCC)}$ + $I_{(LVDSVCC)}$		63.7		mA
		$I_{(IOVCC)}$ with IOVCC = 3.3 V		1.3		
		$I_{(IOVCC)}$ with IOVCC = 1.8 V		0.5		
		$\overline{SHTDN}$ = V_{IH}, R_L = 100 Ω (5 places), worst-case pattern (Figure 9), f_{CLK} = 100 MHz				
		$I_{(VCC)}$ + $I_{(PLLVCC)}$ + $I_{(LVDSVCC)}$		81.6		mA
		$I_{(IOVCC)}$ with IOVCC = 3.6 V		1.6		
		$I_{(IOVCC)}$ with IOVCC = 1.8 V		0.6		
		$\overline{SHTDN}$ = V_{IH}, R_L = 100 Ω (5 places), worst-case pattern (Figure 9), f_{CLK} = 135 MHz				
		$I_{(VCC)}$ + $I_{(PLLVCC)}$ + $I_{(LVDSVCC)}$		102.2		mA
		$I_{(IOVCC)}$ with IOVCC = 3.6 V		2.1		
		$I_{(IOVCC)}$ with IOVCC = 1.8 V		0.8		
C_I	Input capacitance			2		pF

7.6 Timing Requirements

		MIN	MAX	UNIT
Input clock period, t_c		7.4	100	ns
Input clock modulation	w/ modulation frequency 30 kHz		8%	
	w/ modulation frequency 50 kHz		6%	
High-level input clock pulse width duration, t_w		0.4 t_c	0.6 t_c	ns
Input signal transition time, t_t			3	ns
Data set up time, D0 through D27 before CLKIN (See Figure 6)		2		ns
Data hold time, D0 through D27 after CLKIN		0.8		ns

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7.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_0	Delay time, CLKOUT↑ after Yn valid (serial bit position 0, equal D1, D9, D20, D5)	See Figure 10, t_C = 10 ns, |Input clock jitter| < 25 ps (2)	–0.1	0	0.1	ns
t_1	Delay time, CLKOUT↑ after Yn valid (serial bit position 1, equal D0, D8, D19, D27)		$^1/_7\ t_c - 0.1$		$^1/_7\ t_c + 0.1$	ns
t_2	Delay time, CLKOUT↑ after Yn valid (serial bit position 2, equal D7, D18, D26. D23)		$^2/_7\ t_c - 0.1$		$^2/_7\ t_c + 0.1$	ns
t_3	Delay time, CLKOUT↑ after Yn valid (serial bit position 3; equal D6, D15, D25, D17)		$^3/_7\ t_c - 0.1$		$^3/_7\ t_c + 0.1$	ns
t_4	Delay time, CLKOUT↑ after Yn valid (serial bit position 4, equal D4, D14, D24, D16)		$^4/_7\ t_c - 0.1$		$^4/_7\ t_c + 0.1$	ns
t_5	Delay time, CLKOUT↑ after Yn valid (serial bit position 5, equal D3, D13, D22, D11)		$^5/_7\ t_c - 0.1$		$^5/_7\ t_c + 0.1$	ns
t_6	Delay time, CLKOUT↑ after Yn valid (serial bit position 6, equal D2, D12, D21, D10)		$^6/_7\ t_c - 0.1$		$^6/_7\ t_c + 0.1$	ns
$t_{c(o)}$	Output clock period			t_c		ns
$\Delta t_{c(o)}$	Output clock cycle-to-cycle jitter (3)	t_C = 10 ns; clean reference clock, see Figure 11		±26		ps
		t_C = 10 ns with 0.05UI added noise modulated at 3 MHz, see Figure 11		±44		
		t_C = 7.4 ns; clean reference clock, see Figure 11		±35		
		t_C = 7.4 ns with 0.05UI added noise modulated at 3 MHz, see Figure 11		±42		
t_w	High-level output clock pulse duration			$^4/_7\ t_c$		ns
$t_{r/f}$	Differential output voltage transition time (t_r or t_f)	See Figure 7		225	500	ps
t_{en}	Enable time, $\overline{SHTDN}$↑ to phase lock (Yn valid)	$f_{(clk)}$ = 135 MHz, See Figure 12		6		µs
t_{dis}	Disable time, $\overline{SHTDN}$↓ to off-state (CLKOUT high-impedance)	$f_{(clk)}$ = 135 MHz, See Figure 13		7		ns

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(2) |Input clock jitter| is the magnitude of the change in the input clock period.
(3) The output clock cycle-to-cycle jitter is the largest recorded change in the output clock period from one cycle to the next cycle observed over 15,000 cycles.Tektronix TDSJIT3 Jitter Analysis software was used to derive the maximum and minimum jitter value.

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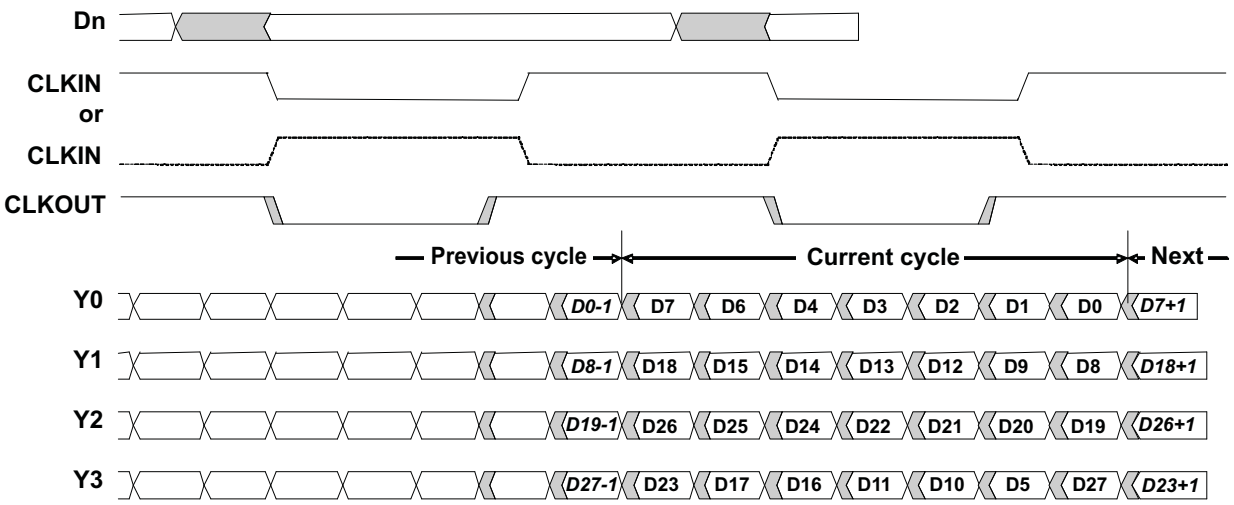
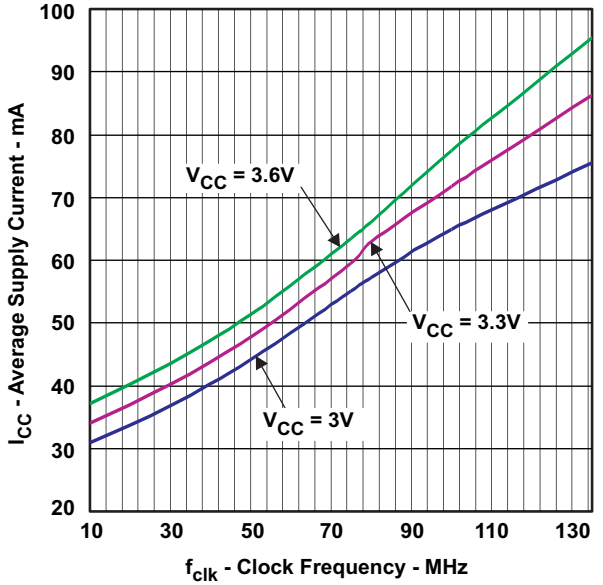


Figure 1. Typical SN65LVDS93A Load and Shift Sequences

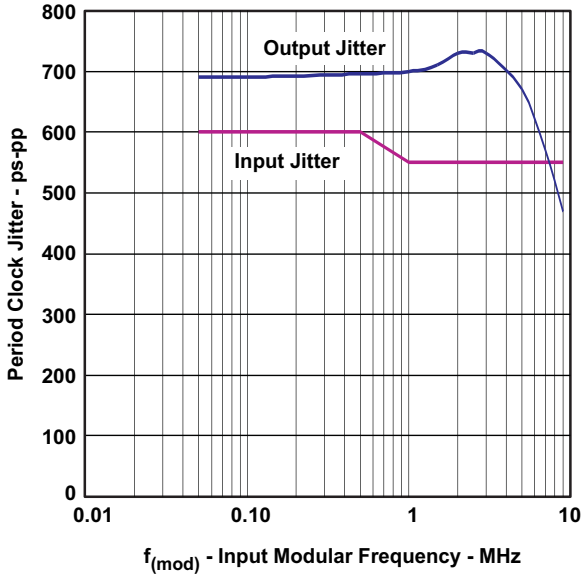
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7.8 Typical Characteristics



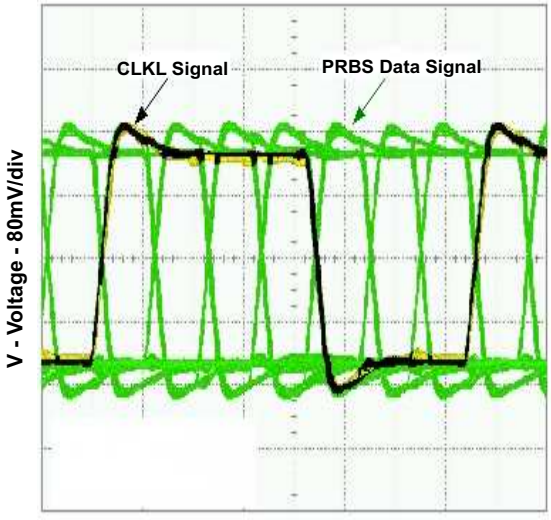
Total device current (using grayscale pattern) over pixel clock frequency

Figure 2. Average Grayscale ICC vs Clock Frequency



CLK frequency during text = 100 MHz

Figure 3. Output Clock Jitter vs Input Clock Jitter



Clock signal = 135 MHz

Figure 4. Typical PRBS Output Signal Over One Clock Period

8 Parameter Measurement Information

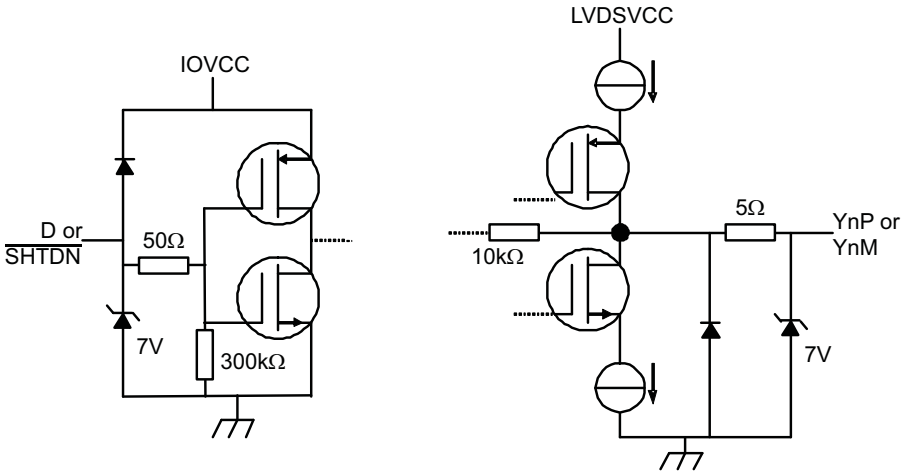
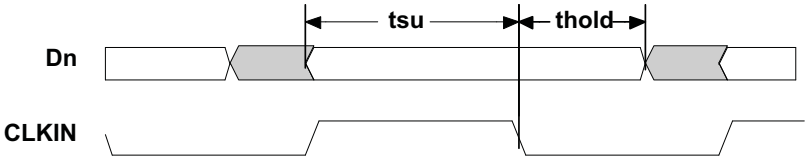


Figure 5. Equivalent Input and Output Schematic Diagrams



All input timing is defined at IOVDD / 2 on an input signal with a 10% to 90% rise or fall time of less than 3 ns. CLKSEL = 0V.

Figure 6. Setup and Hold Time Definition

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Parameter Measurement Information (continued)

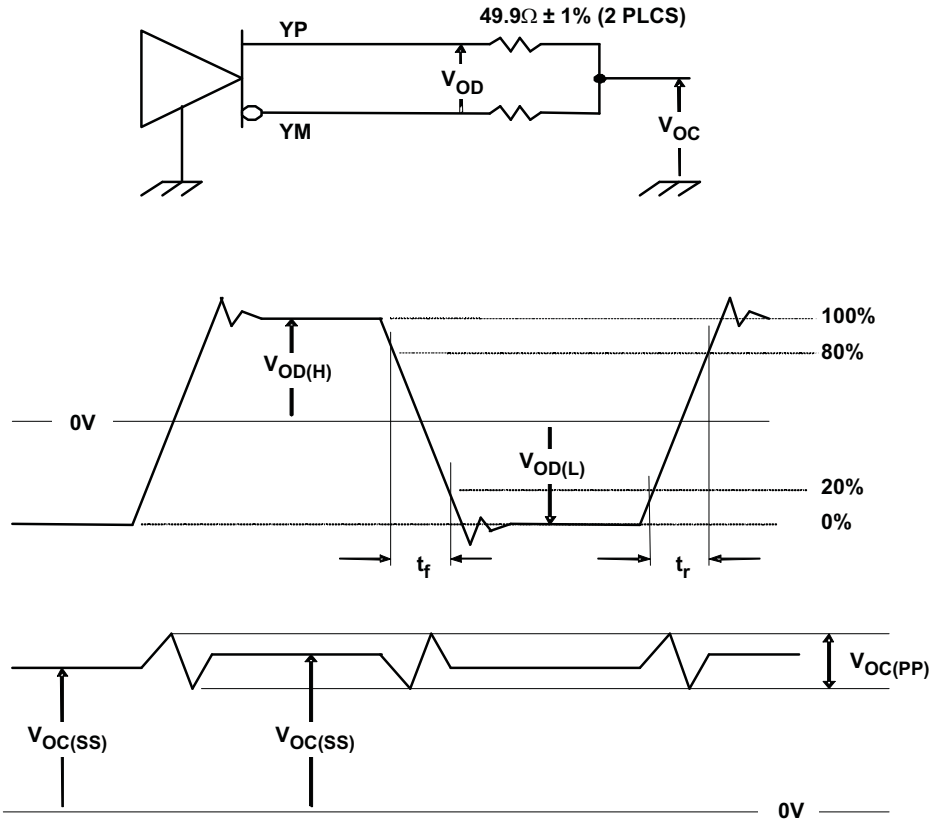
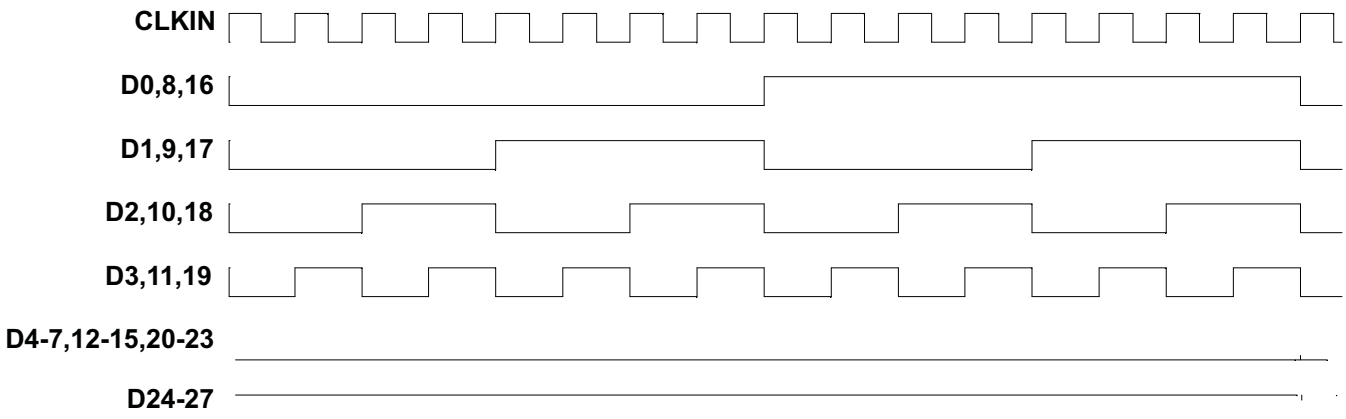


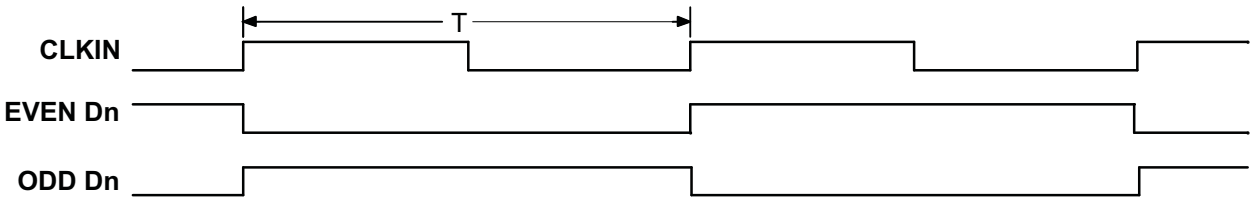
Figure 7. Test Load and Voltage Definitions for LVDS Outputs



The 16 grayscale test pattern test device power consumption for a typical display pattern.

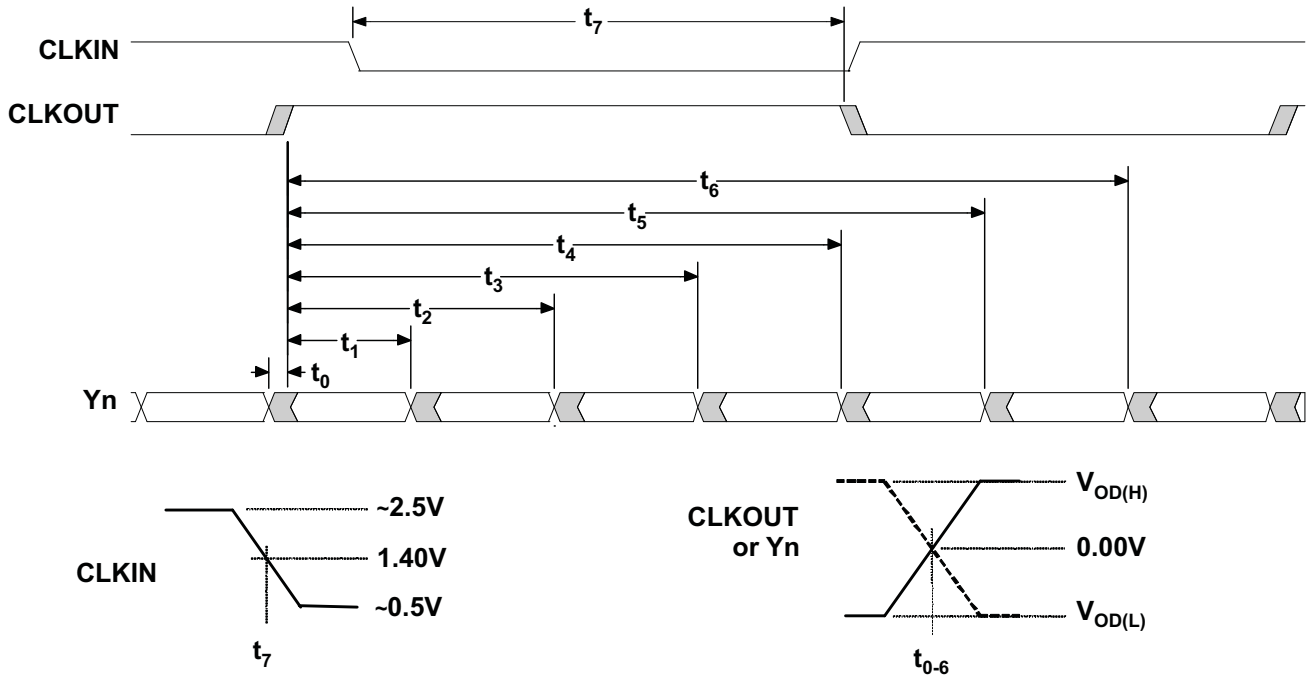
Figure 8. 16 Grayscale Test Pattern

Parameter Measurement Information (continued)



The worst-case test pattern produces nearly the maximum switching frequency for all of the LVDS outputs.

Figure 9. Worst-Case Power Test Pattern

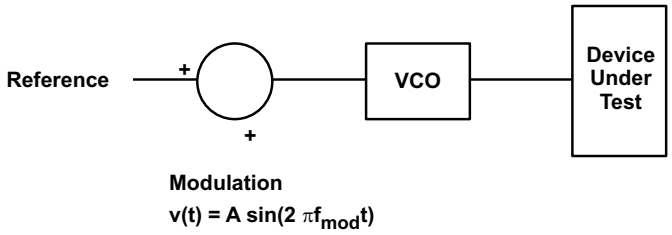


CLKOUT is shown with CLKSEL at high-level.
CLKIN polarity depends on CLKSEL input level.

Figure 10. SN65LVDS93A Timing Definitions

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Parameter Measurement Information (continued)



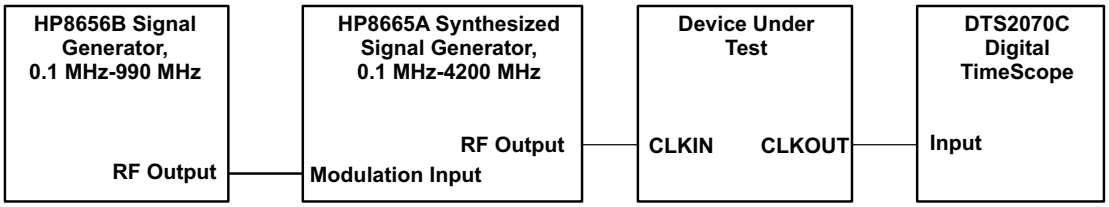


Figure 11. Output Clock Jitter Test Set Up

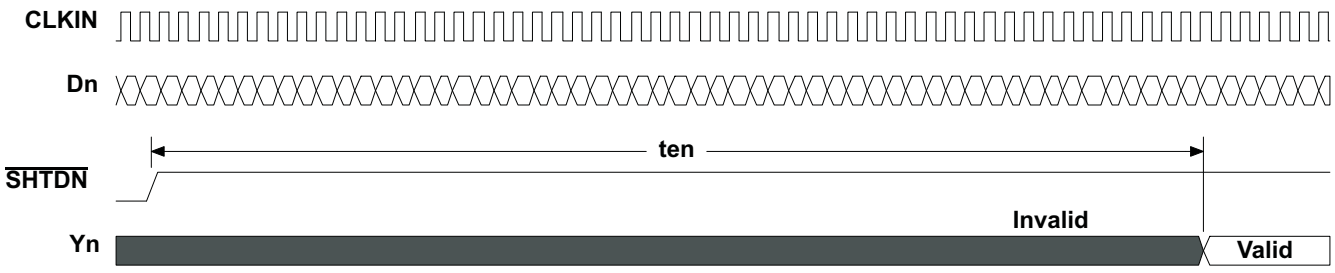


Figure 12. Enable Time Waveforms

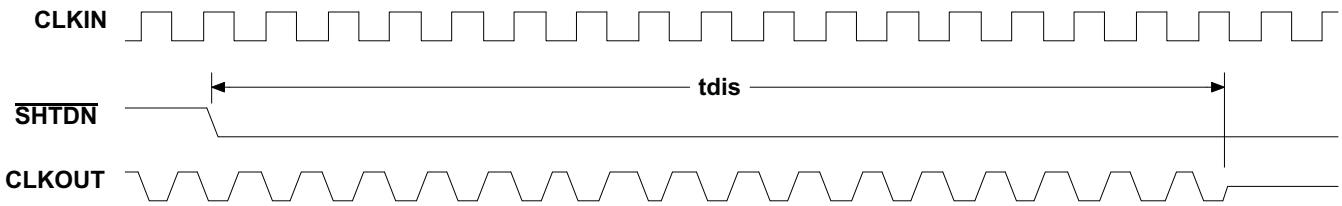


Figure 13. Disable Time Waveforms

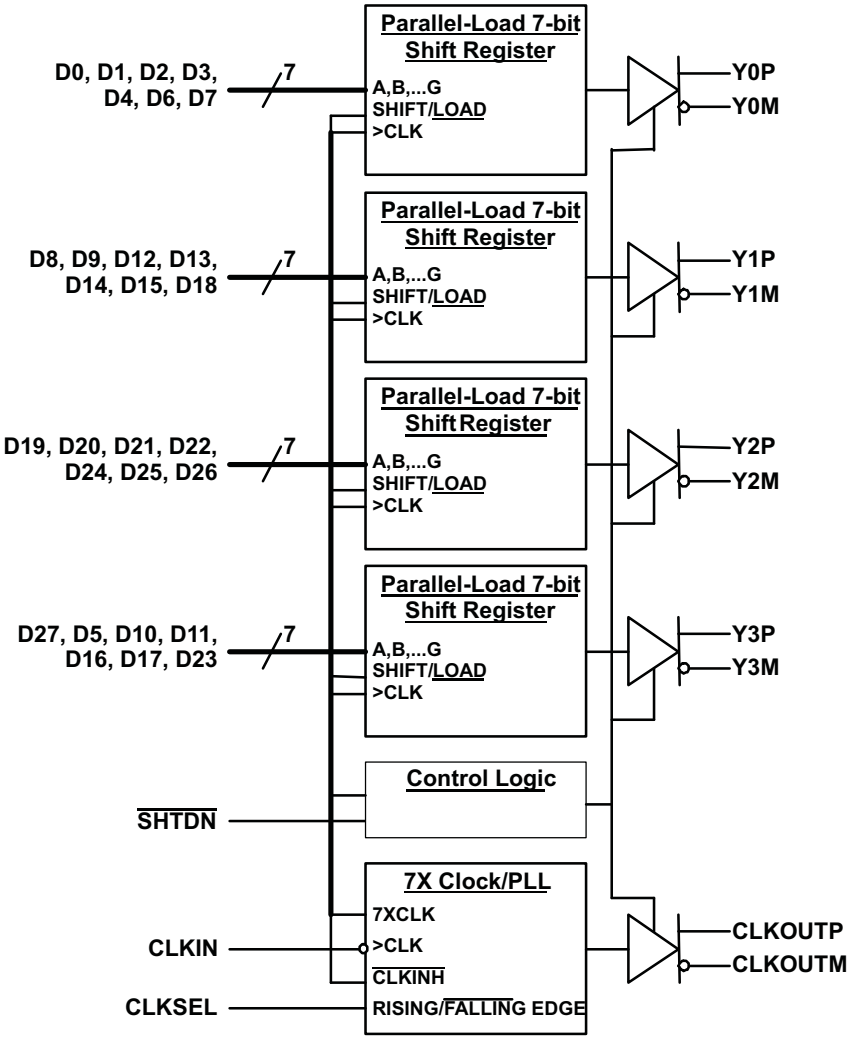
9 Detailed Description

9.1 Overview

FlatLink™ is an LVDS SerDes data transmission system. The SN65LVDS93A takes in three (or four) data words each containing seven single-ended data bits, and converts this to an LVDS serial output. Each serial output runs at seven times that of the parallel data rate. The deserializer (receiver) device operates in the reverse manner. The three (or four) LVDS serial inputs are transformed back to the original 7-bit parallel single-ended data. FlatLink devices are available in 21:3 or 28:4 SerDes ratios.

- The 21-bit devices are designed for 6-bit RGB video for a total of 18 bits in addition to 3 extra bits for horizontal synchronization, vertical synchronization, and data enable.
- The 28-bit devices are intended for 8-bit RGB video applications. Again, the extra 4 bits are for horizontal synchronization, vertical synchronization, data enable, and the remaining is the reserved bit. These 28-bit devices can also be used in 6-bit and 4-bit RGB applications as shown in the subsequent system diagrams.

9.2 Functional Block Diagram



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9.3 Feature Description

9.3.1 TTL Input Data

The data inputs to the transmitter come from the graphics processor and consist of up to 24 bits of video information, a horizontal synchronization bit, a vertical synchronization bit, an enable bit, and a spare bit. The data can be loaded into the registers upon either the rising or falling edge of the input clock selectable by the CLKSEL pin. Data inputs are 1.8 V to 3.3 V tolerant for the SN65LVDS93A and can connect directly to low-power, low-voltage application and graphic processors. The bit mapping is listed in Table 1.

Table 1. Pixel Bit Ordering

	RED	GREEN	BLUE
LSB	R0	G0	B0
	R1	G1	B1
	R2	G2	B2
4-bit MSB	R3	G3	B3
	R4	G4	B4
6-bit MSB	R5	G5	B5
	R6	G6	B6
8-bit MSB	R7	G7	B7

9.3.2 LVDS Output Data

The pixel data assignment is listed in Table 2 for 24-bit, 18-bit, and 12-bit color hosts.

Table 2. Pixel Data Assignment

SERIAL CHANNEL	DATA BITS	8-BIT			6-BIT	4-BIT	
		FORMAT-1	FORMAT-2	FORMAT-3		NON-LINEAR STEP SIZE	LINEAR STEP SIZE
Y0	D0	R0	R2	R2	R0	R2	VCC
	D1	R1	R3	R3	R1	R3	GND
	D2	R2	R4	R4	R2	R0	R0
	D3	R3	R5	R5	R3	R1	R1
	D4	R4	R6	R6	R4	R2	R2
	D6	R5	R7	R7	R5	R3	R3
	D7	G0	G2	G2	G0	G2	VCC
Y1	D8	G1	G3	G3	G1	G3	GND
	D9	G2	G4	G4	G2	G0	G0
	D12	G3	G5	G5	G3	G1	G1
	D13	G4	G6	G6	G4	G2	G2
	D14	G5	G7	G7	G5	G3	G3
	D15	B0	B2	B2	B0	B2	VCC
	D18	B1	B3	B3	B1	B3	GND
Y2	D19	B2	B4	B4	B2	B0	B0
	D20	B3	B5	B5	B3	B1	B1
	D21	B4	B6	B6	B4	B2	B2
	D22	B5	B7	B7	B5	B3	B3
	D24	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
	D25	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
	D26	ENABLE	ENABLE	ENABLE	ENABLE	ENABLE	ENABLE

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Table 2. Pixel Data Assignment (continued)

SERIAL CHANNEL	DATA BITS	8-BIT			6-BIT	4-BIT	
		FORMAT-1	FORMAT-2	FORMAT-3		NON-LINEAR STEP SIZE	LINEAR STEP SIZE
Y3	D27	R6	R0	GND	GND	GND	GND
	D5	R7	R1	GND	GND	GND	GND
	D10	G6	G0	GND	GND	GND	GND
	D11	G7	G1	GND	GND	GND	GND
	D16	B6	B0	GND	GND	GND	GND
	D17	B7	B1	GND	GND	GND	GND
	D23	RSVD	RSVD	GND	GND	GND	GND
CLKOUT	CLKIN	CLK	CLK	CLK	CLK	CLK	CLK

9.4 Device Functional Modes

9.4.1 Input Clock Edge

The transmission of data bits D0 through D27 occurs as each are loaded into registers upon the edge of the CLKIN signal, where the rising or falling edge of the clock may be selected through CLKSEL. The selection of a clock rising edge occurs by inputting a high level to CLKSEL, which is achieved by populating pullup resistor to pull CLKSEL=high. Inputting a low level to select a clock falling edge is achieved by directly connecting CLKSEL to GND.

9.4.2 Low Power Mode

The SN65LVDS93A can be put in low-power consumption mode by active-low input SHTDN#. Connecting pin SHTDN# to GND will inhibit the clock and shut off the LVDS output drivers for lower power consumption. A low-level on this signal clears all internal registers to a low-level. Populate a pullup to VCC on SHTDN# to enable the device for normal operation.

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10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

This section describes the power up sequence, provides information on device connectivity to various GPU and LCD display panels, and offers a PCB routing example.

10.1.1 Power

The SN65LVDS93A does not require a specific power-up sequence.

The device is permitted to power up IOVCC while VCC, VCCPLL, and VCCLVDS remain powered down and connected to GND. The input level of the $\overline{\text{SHTDN}}$ during this time does not matter as only the input stage is powered up while all other device blocks are still powered down.

The device is also permitted to power up all 3.3-V power domains while IOVCC is still powered down to GND. The device will not suffer damage. However, in this case, all the I/Os are detected as logic HIGH, regardless of their true input voltage level. Hence, connecting $\overline{\text{SHTDN}}$ to GND will still be interpreted as a logic HIGH; the LVDS output stage will turn on. The power consumption in this condition is significantly higher than standby mode, but still lower than normal mode.

The user experience can be impacted by the way a system powers up and powers down an LCD screen. The following sequence is recommended:

Power-up sequence (SN65LVDS93A $\overline{\text{SHTDN}}$ input initially low):

1. Ramp up LCD power (maybe 0.5 ms to 10 ms) but keep backlight turned off.
2. Wait for additional 0-200ms to ensure display noise won't occur.
3. Enable video source output; start sending black video data.
4. Toggle LVDS83B shutdown to $\overline{\text{SHTDN}} = V_{IH}$.
5. Send >1 ms of black video data; this allows the LVDS83B to be phase locked, and the display to show black data first.
6. Start sending true image data.
7. Enable backlight.

Power-down sequence (SN65LVDS93A $\overline{\text{SHTDN}}$ input initially high):

1. Disable LCD backlight; wait for the minimum time specified in the LCD data sheet for the backlight to go low.
2. Video source output data switch from active video data to black image data (all visible pixel turn black); drive this for >2 frame times.
3. Set SN65LVDS93A input $\overline{\text{SHTDN}}$ = GND; wait for 250 ns.
4. Disable the video output of the video source.
5. Remove power from the LCD panel for lowest system power.

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10.2 Typical Application

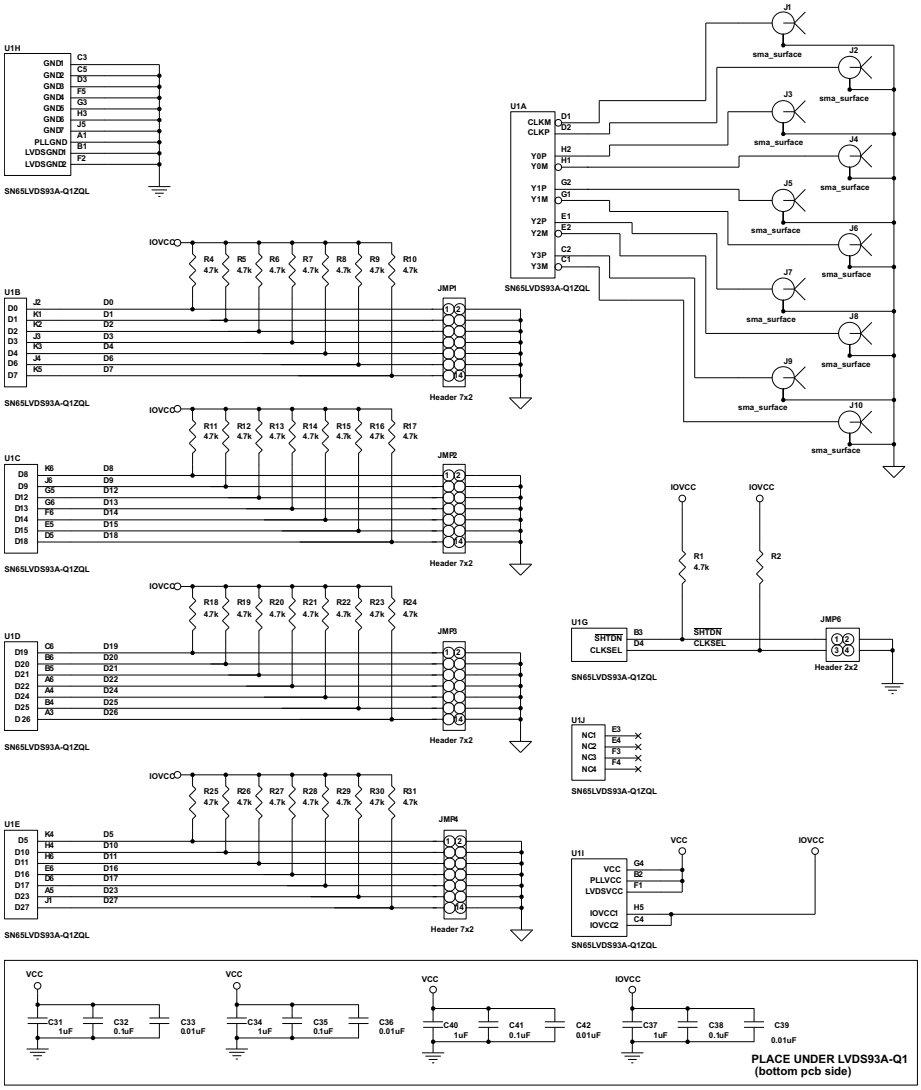


Figure 14. Schematic Example (SN65LVDS93A Evaluation Board)

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Typical Application (continued)

10.2.1 Design Requirements

For this design example, use the parameters listed in Table 3 as the input parameters.

Table 3. Design Parameters

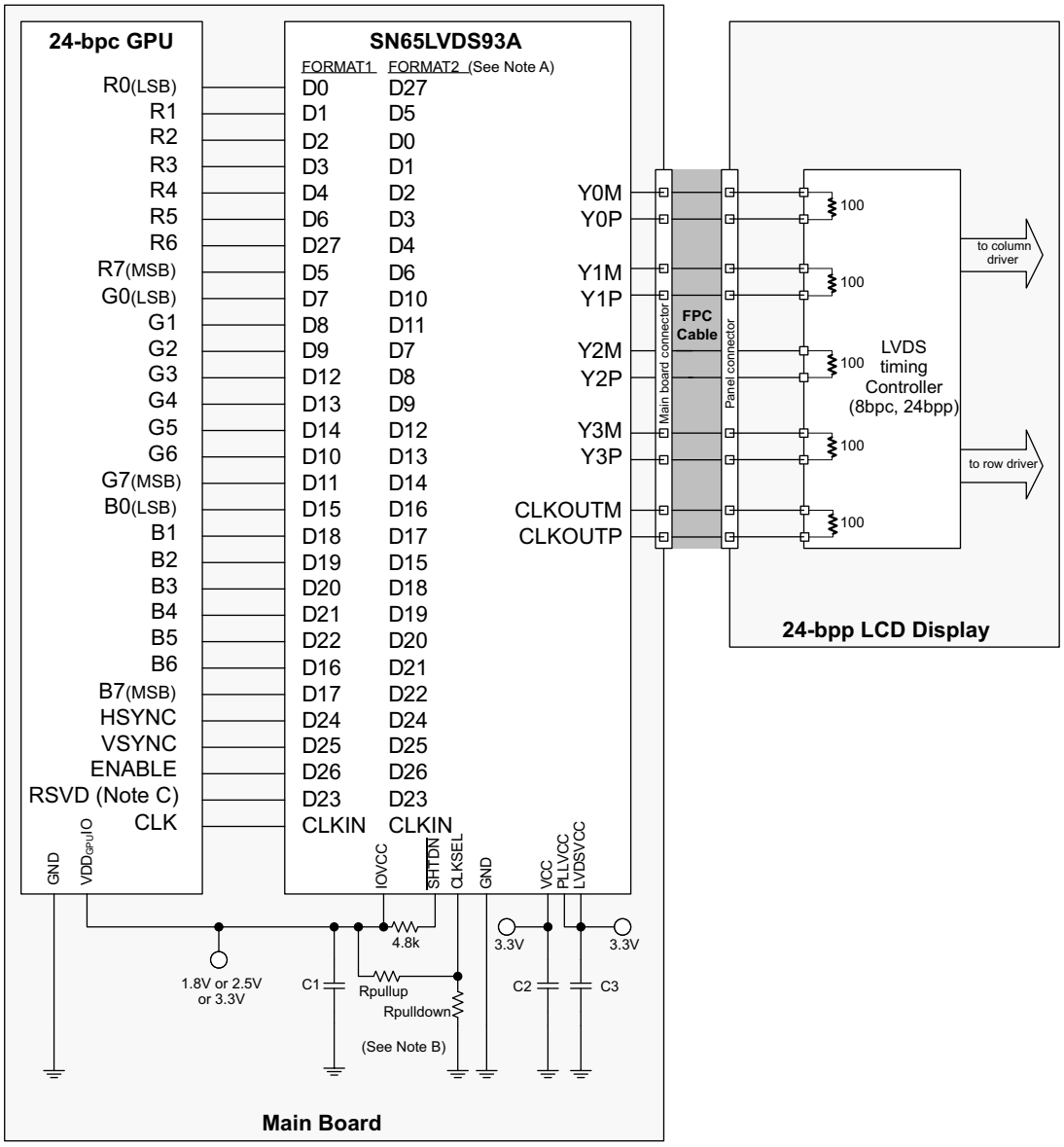
DESIGN PARAMETER	EXAMPLE VALUE
VCC	3.3 V
VCCIO	1.8 V
CLKIN	Falling edge
SHTDN#	High
Format	18-bit GPU to 24-bit LCD

10.2.2 Detailed Design Procedure

10.2.2.1 Signal Connectivity

While there is no formal industry standardized specification for the input interface of LVDS LCD panels, the industry has aligned over the years on a certain data format (bit order). Figure 15 through Figure 18 show how each signal should be connected from the graphic source through the SN65LVDS93A input, output and LVDS LCD panel input. Detailed notes are provided with each figure.

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Note A. **FORMAT**: The majority of 24-bit LCD display panels require the two most significant bits (2 MSB) of each color to be transferred over the 4th serial data output Y3. A few 24-bit LCD display panels require the two LSBs of each color to be transmitted over the Y3 output. The system designer needs to verify which format is expected by checking the LCD display data sheet.

- Format 1: use with displays expecting the 2 MSB to be transmitted over the 4th data channel Y3. This is the dominate data format for LCD panels.
- Format 2: use with displays expecting the 2 LSB to be transmitted over the 4th data channel.

Note B. **Rpullup**: install only to use rising edge triggered clocking.
Rpulldown: install only to use falling edge triggered clocking.

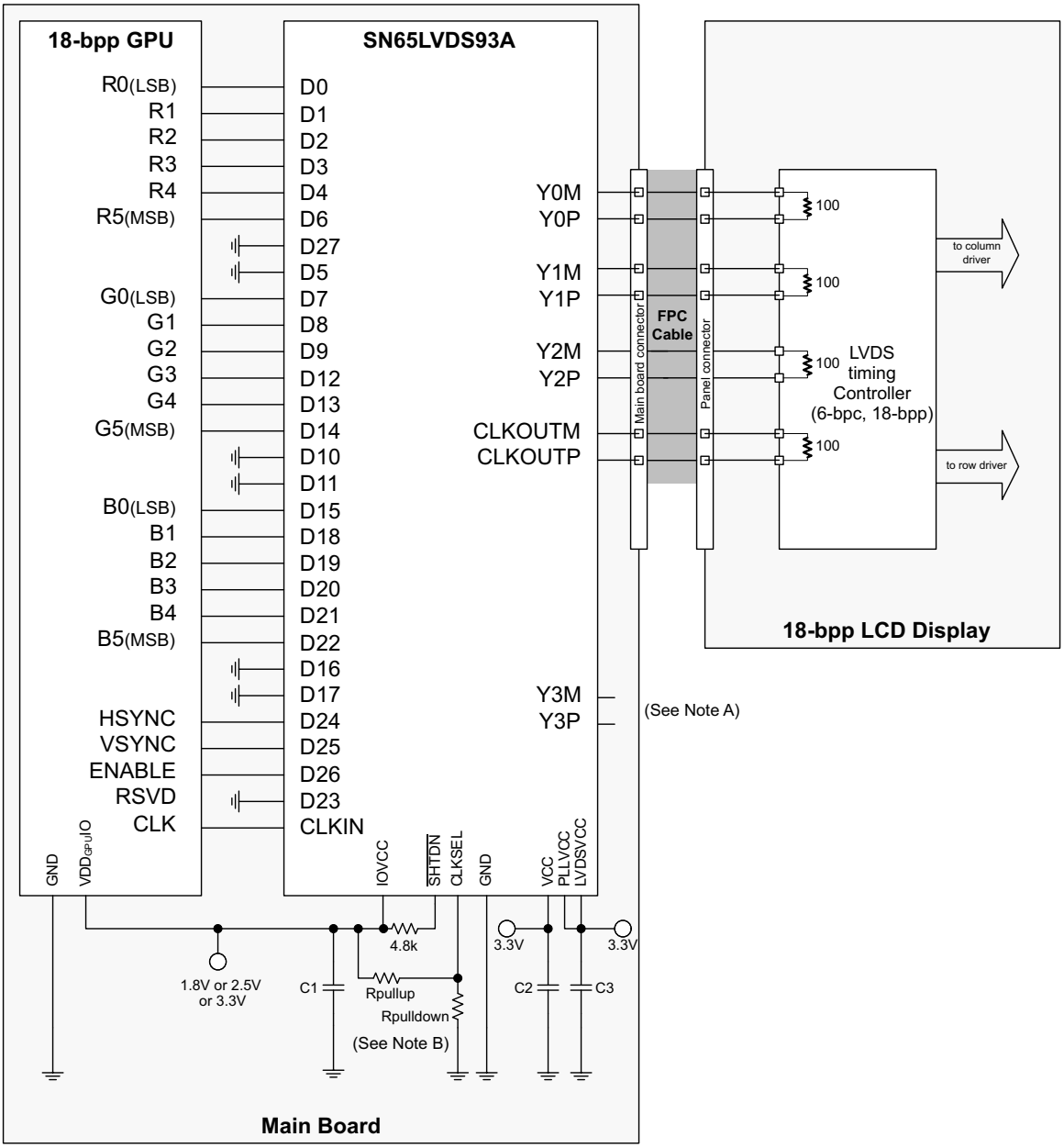
- C1: decoupling capacitor for the VDDIO supply; install at least 1x0.01µF.
- C2: decoupling capacitor for the VDD supply; install at least 1x0.1µF and 1x0.01µF.
- C3: decoupling capacitor for the VDDPLL and VDDLVDS supply; install at least 1x0.1µF and 1x0.01µF.

Note C. If RSVD is not driven to a valid logic level, then an external connection to GND is recommended.

Note D. RSVD must be driven to a valid logic level. All unused SN65LVDS93A inputs must be tied to a valid logic level.

Figure 15. 24-Bit Color Host to 24-Bit LCD Panel Application

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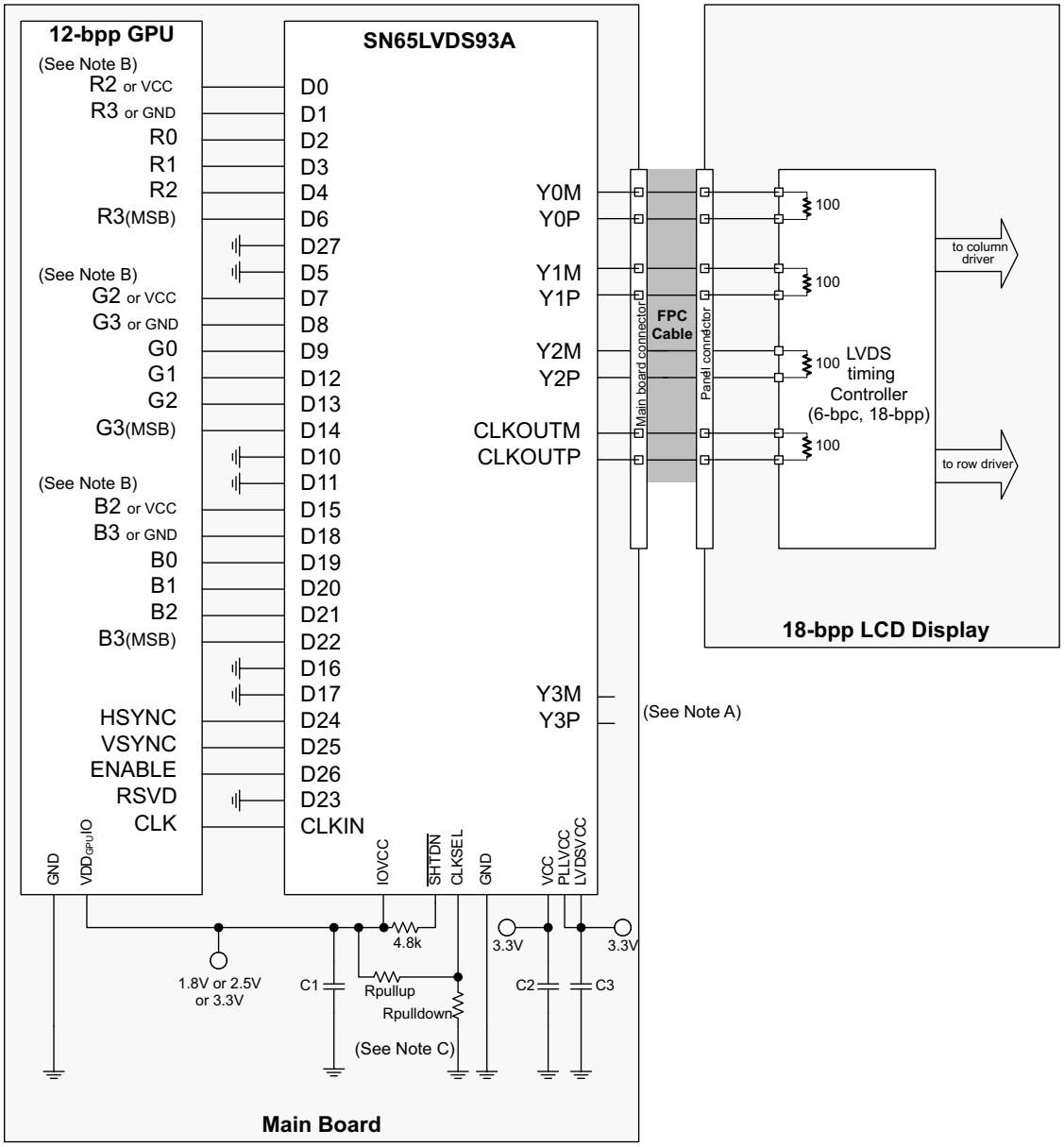
Note A. Leave output Y3 NC.

Note B.**Rpullup**: install only to use rising edge triggered clocking.
Rpulldown: install only to use falling edge triggered clocking.

- C1: decoupling capacitor for the VDDIO supply; install at least 1x0.01µF.
- C2: decoupling capacitor for the VDD supply; install at least 1x0.1µF and 1x0.01µF.
- C3: decoupling capacitor for the VDDPLL and VDDLVDS supply; install at least 1x0.1µF and 1x0.01µF.

Figure 16. 18-Bit Color Host to 18-Bit Color LCD Panel Display Application

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Note A. Leave output Y3 N.C.

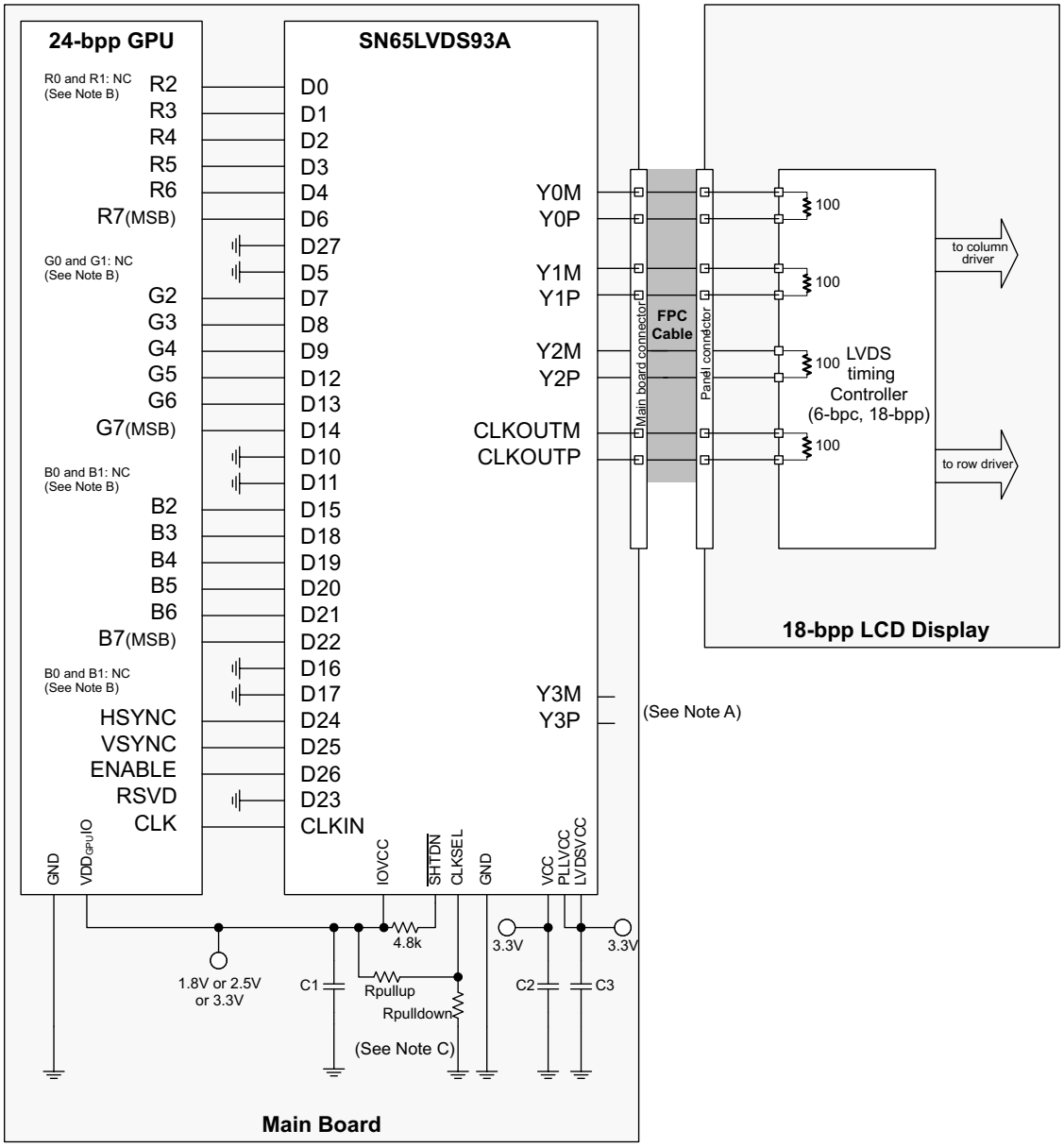
Note B. **R3, G3, B3**: this MSB of each color also connects to the 5th bit of each color for increased dynamic range of the entire color space at the expense of nonlinear step sizes between each step. For linear steps with less dynamic range, connect D1, D8, and D18 to GND.
R2, G2, B2: these outputs also connects to the LSB of each color for increased, dynamic range of the entire color space at the expense of nonlinear step sizes between each step. For linear steps with less dynamic range, connect D0, D7, and D15 to VCC.

Note C.**Rpullup**: install only to use rising edge triggered clocking.
Rpulldown: install only to use falling edge triggered clocking.

- C1: decoupling capacitor for the VDDIO supply; install at least 1x0.01µF.
- C2: decoupling capacitor for the VDD supply; install at least 1x0.1µF and 1x0.01µF.
- C3: decoupling capacitor for the VDDPLL and VDDLVDS supply; install at least 1x0.1µF and 1x0.01µF.

Figure 17. 12-Bit Color Host to 18-Bit Color LCD Panel Display Application

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Note A. Leave output Y3 NC.

Note B. **R0, R1, G0, G1, B0, B1**: For improved image quality, the GPU should dither the 24-bit output pixel down to18-bit per pixel.

NoteC.**Rpullup**: install only to use rising edge triggered clocking.
Rpulldown: install only to use falling edge triggered clocking.

- C1: decoupling capacitor for the VDDIO supply; install at least 1x0.01µF.
- C2: decoupling capacitor for the VDD supply; install at least 1x0.1µF and 1x0.01µF.
- C3: decoupling capacitor for the VDDPLL and VDDLVDS supply; install at least 1x0.1µF and 1x0.01µF.

Figure 18. 24-Bit Color Host to 18-Bit Color LCD Panel Display Application

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10.2.2.2 PCB Routing

Figure 19 shows a possible breakout of the data input and output signals on two layers of a printed-circuit-board.

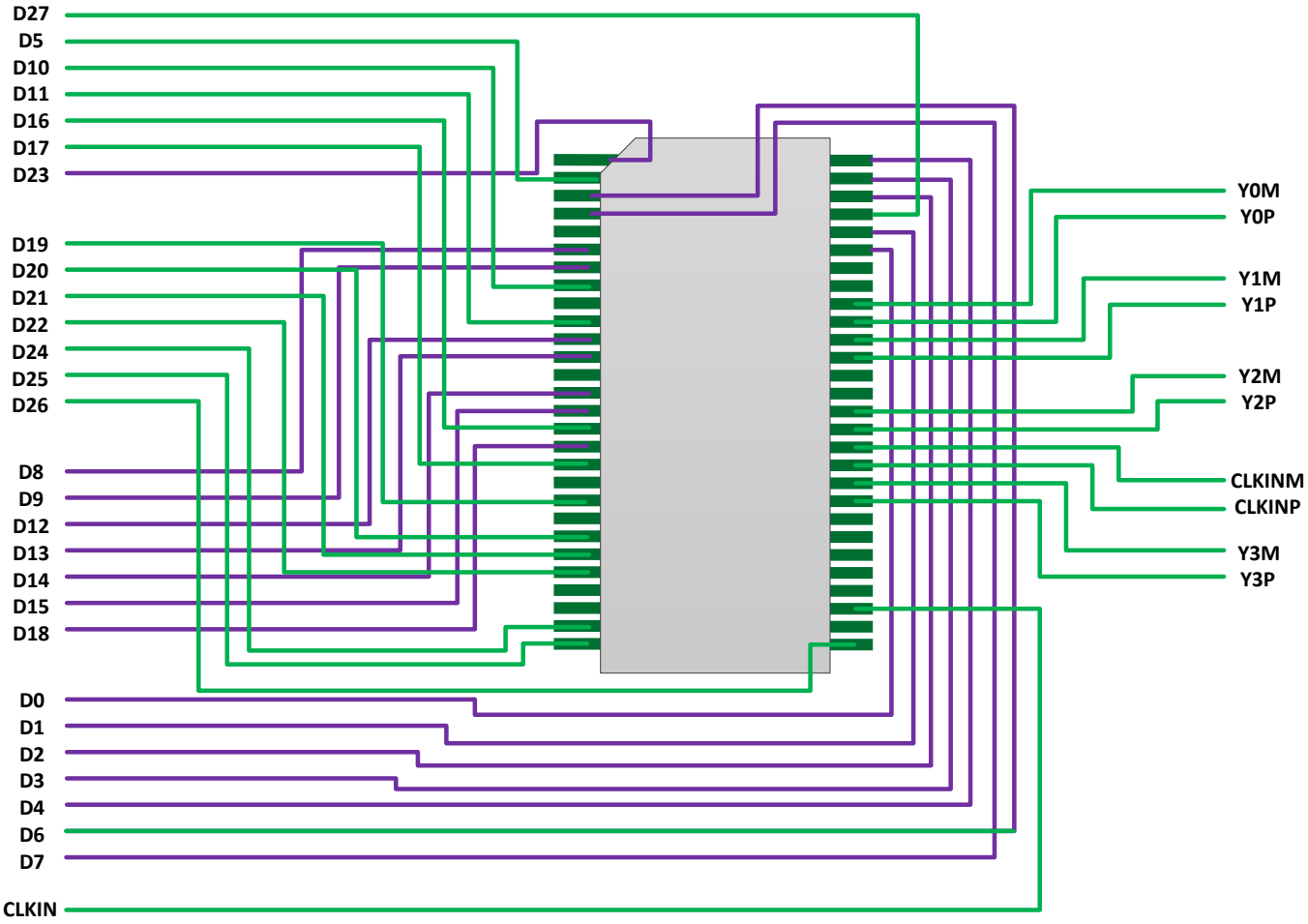


Figure 19. Printed-Circuit-Board Routing Example (See Figure 14 for the Schematic)

10.2.3 Application Curve

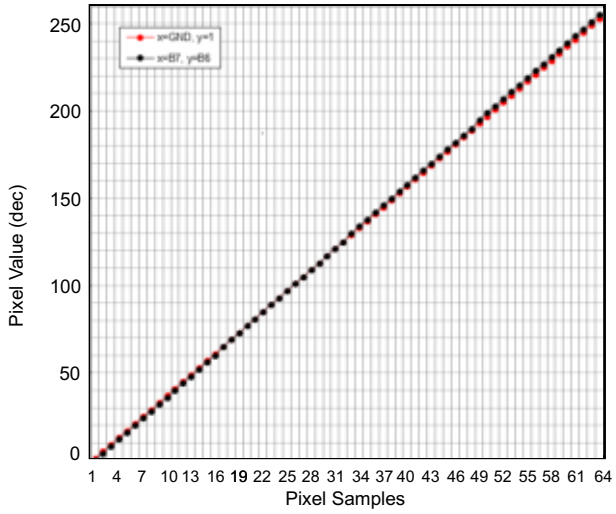


Figure 20. 18b GPU to 24b LCD

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11 Power Supply Recommendations

Power supply PLL, IO, and LVDS pins must be uncoupled from each.

12 Layout

12.1 Layout Guidelines

12.1.1 Board Stackup

There is no fundamental information about how many layers should be used and how the board stackup should look. Again, the easiest way the get good results is to use the design from the EVMs of TI. The magazine *Elektronik Praxis* has published an article with an analysis of different board stackups. These are listed in Table 4. Generally, the use of microstrip traces needs at least two layers, whereas one of them must be a GND plane. Better is the use of a 4-layer PCB, with a GND and a VCC plane and two signal layers. If the circuit is complex and signals must be routed as stripline, because of propagation delay and/or characteristic impedance, a 6-layer stackup should be used.

Table 4. Possible Board Stackup on a Four-Layer PCB

	MODEL 1	MODEL 2	MODEL 3	MODEL 4
Layer 1	SIG	SIG	SIG	GND
Layer 2	SIG	GND	GND	SIG
Layer 3	VCC	VCC	SIG	VCC
Layer 4	GND	SIG	VCC	SIG
Decoupling	Good	Good	Bad	Bad
EMC	Bad	Bad	Bad	Bad
Signal Integrity	Bad	Bad	Good	Bad
Self Disturbance	Satisfaction	Satisfaction	Satisfaction	High

12.1.2 Power and Ground Planes

A complete ground plane in high-speed design is essential. Additionally, a complete power plane is recommended as well. In a complex system, several regulated voltages can be present. The best solution is for every voltage to have its own layer and its own ground plane. But this would result in a huge number of layers just for ground and supply voltages. What are the alternatives? Split the ground planes and the power planes? In a mixed-signal design, for example, using data converters, the manufacturer often recommends splitting the analog ground and the digital ground to avoid noise coupling between the digital part and the sensitive analog part. Take care when using split ground planes because:

- Split ground planes act as slot antennas and radiate.
- A routed trace over a gap creates large loop areas, because the return current cannot flow beside the signal, and the signal can induce noise into the nonrelated reference plane (Figure 21).
- With a proper signal routing, crosstalk also can arise in the return current path due to discontinuities in the ground plane. Always take care of the return current (Figure 22).

For Figure 22, do not route a signal referenced to digital ground over analog ground and vice versa. The return current cannot take the direct way along the signal trace and so a loop area occurs. Furthermore, the signal induces noise, due to crosstalk (dotted red line) into the analog ground plane.

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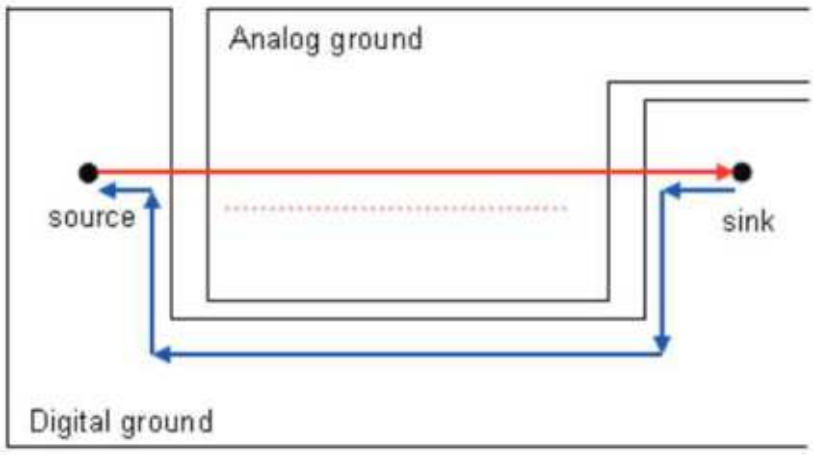


Figure 21. Loop Area and Crosstalk Due to Poor Signal Routing and Ground Splitting

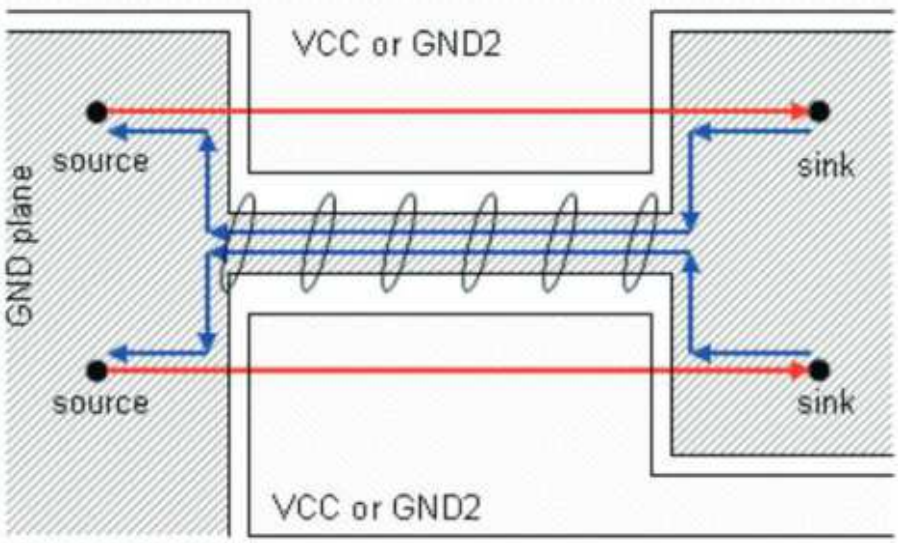


Figure 22. Crosstalk Induced by the Return Current Path

12.1.3 Traces, Vias, and Other PCB Components

A right angle in a trace can cause more radiation. The capacitance increases in the region of the corner, and the characteristic impedance changes. This impedance change causes reflections.

- Avoid right-angle bends in a trace and try to route them at least with two 45° corners. To minimize any impedance change, the best routing would be a round bend (see Figure 23).
- Separate high-speed signals (for example, clock signals) from low-speed signals and digital from analog signals; again, placement is important.
- To minimize crosstalk not only between two signals on one layer but also between adjacent layers, route them with 90° to each other.

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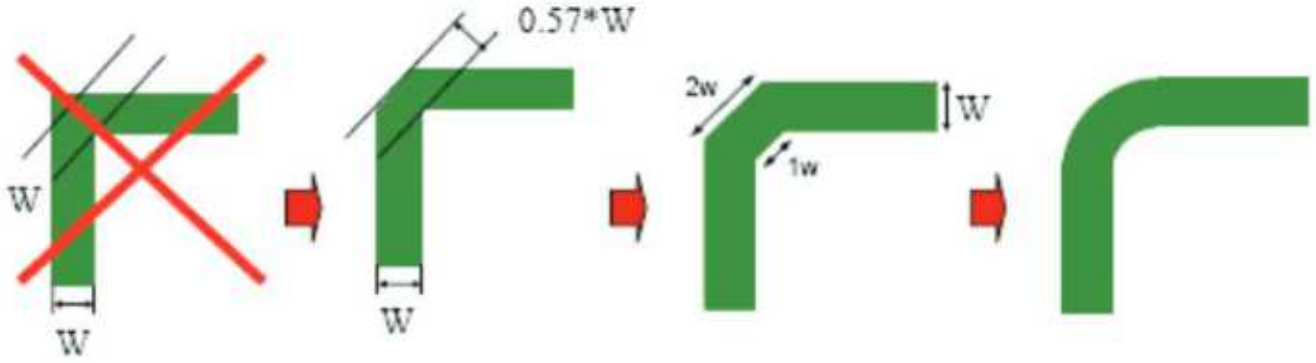


Figure 23. Poor and Good Right-Angle Bends

12.2 Layout Example

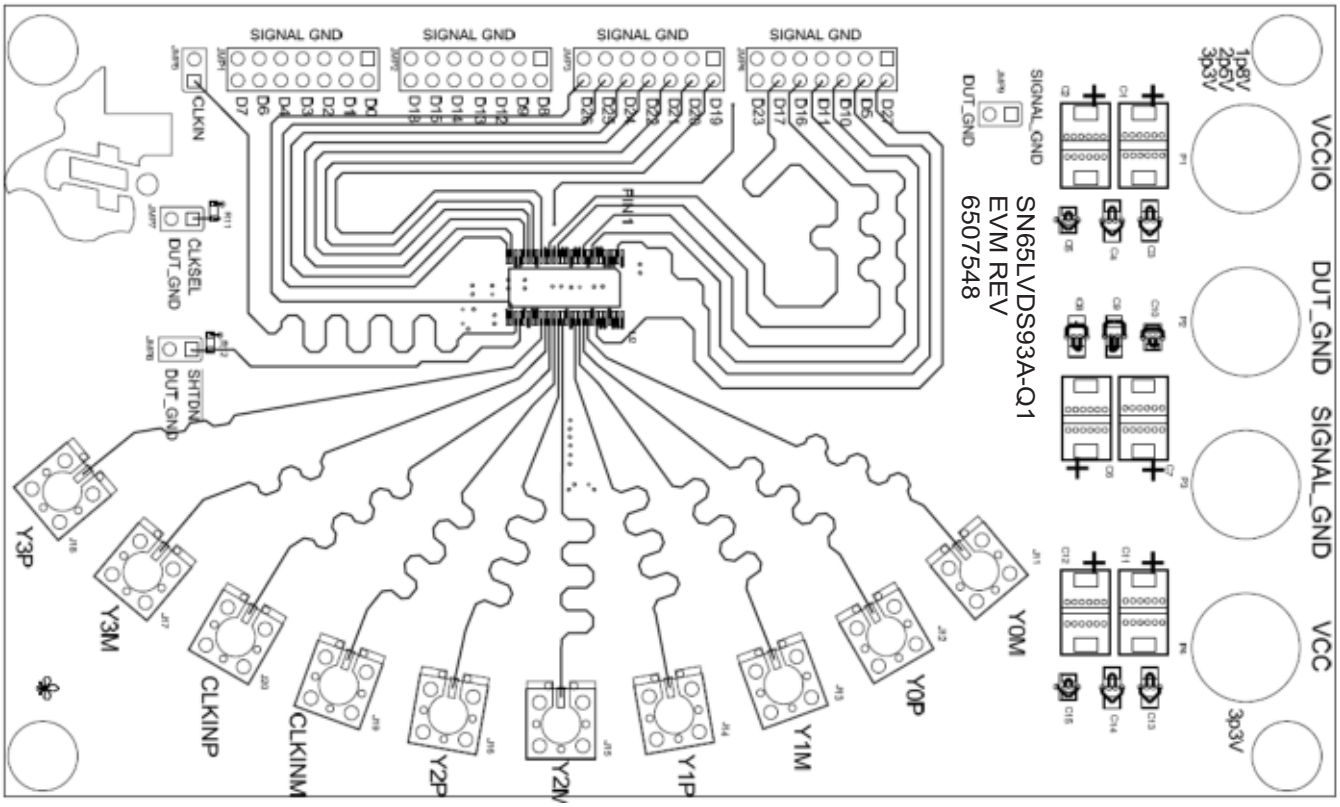


Figure 24. SN65LVDS93A EVM Top Layer – TSSOP Package

Layout Example (continued)

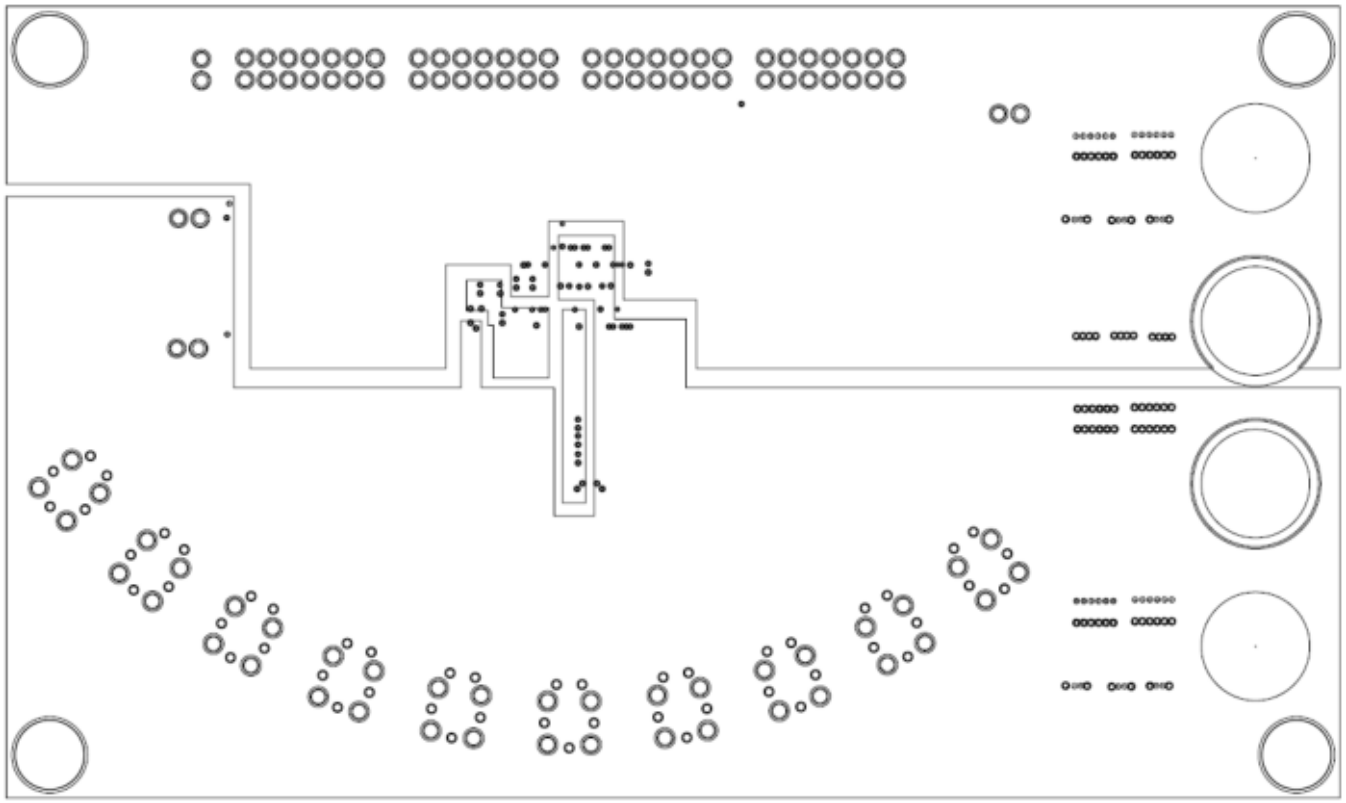


Figure 25. SN65LVDS93A EVM VCC Layer – TSSOP Package

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13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation see the following:

LVDS SerDes Receiver, SLLS928

13.2 Trademarks

OMAP, DaVinci, FlatLink are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65LVDS93ADGG	Active	Production	TSSOP (DGG) | 56	35 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDS93A
SN65LVDS93ADGG.A	Active	Production	TSSOP (DGG) | 56	35 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDS93A
SN65LVDS93ADGGR	Active	Production	TSSOP (DGG) | 56	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDS93A
SN65LVDS93ADGGR.A	Active	Production	TSSOP (DGG) | 56	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDS93A
SN65LVDS93ADGGRG4	Active	Production	TSSOP (DGG) | 56	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDS93A
SN65LVDS93ADGGRG4.A	Active	Production	TSSOP (DGG) | 56	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVDS93A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN65LVDS93A :

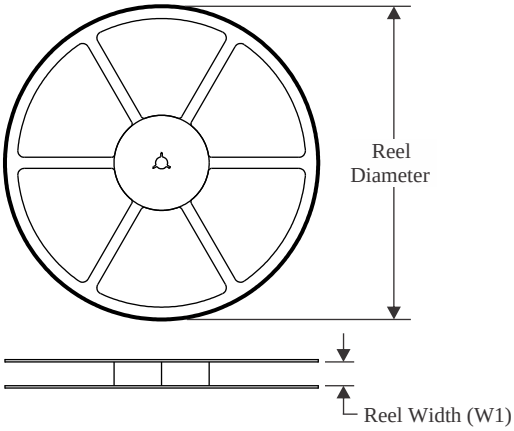
- Automotive : SN65LVDS93A-Q1

NOTE: Qualified Version Definitions:

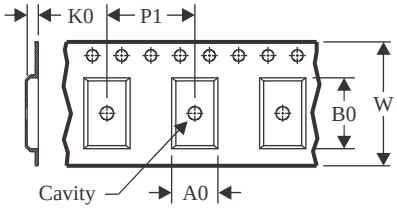
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

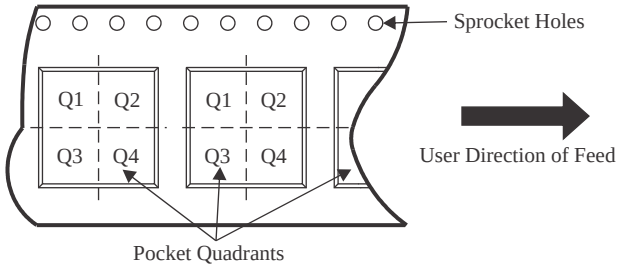


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

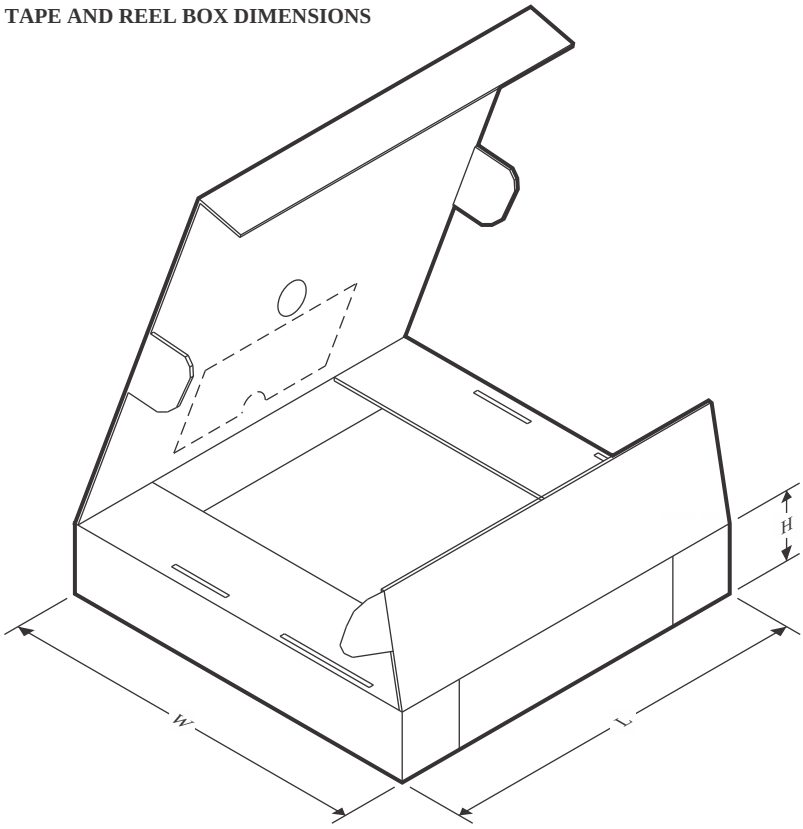
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDS93ADGGR	TSSOP	DGG	56	2000	330.0	24.4	8.9	14.7	1.4	12.0	24.0	Q1
SN65LVDS93ADGGRG4	TSSOP	DGG	56	2000	330.0	24.4	8.9	14.7	1.4	12.0	24.0	Q1

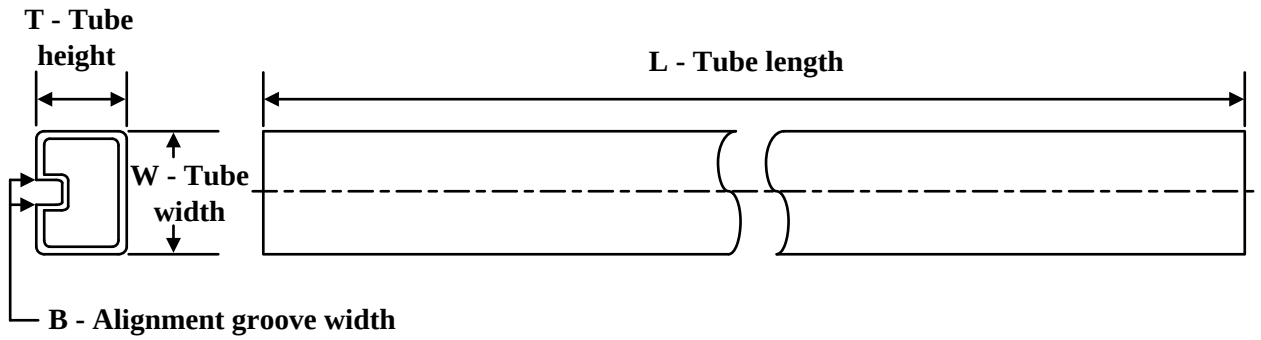
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVDS93ADGGR	TSSOP	DGG	56	2000	356.0	356.0	45.0
SN65LVDS93ADGGRG4	TSSOP	DGG	56	2000	356.0	356.0	45.0

TUBE



*All dimensions are nominal

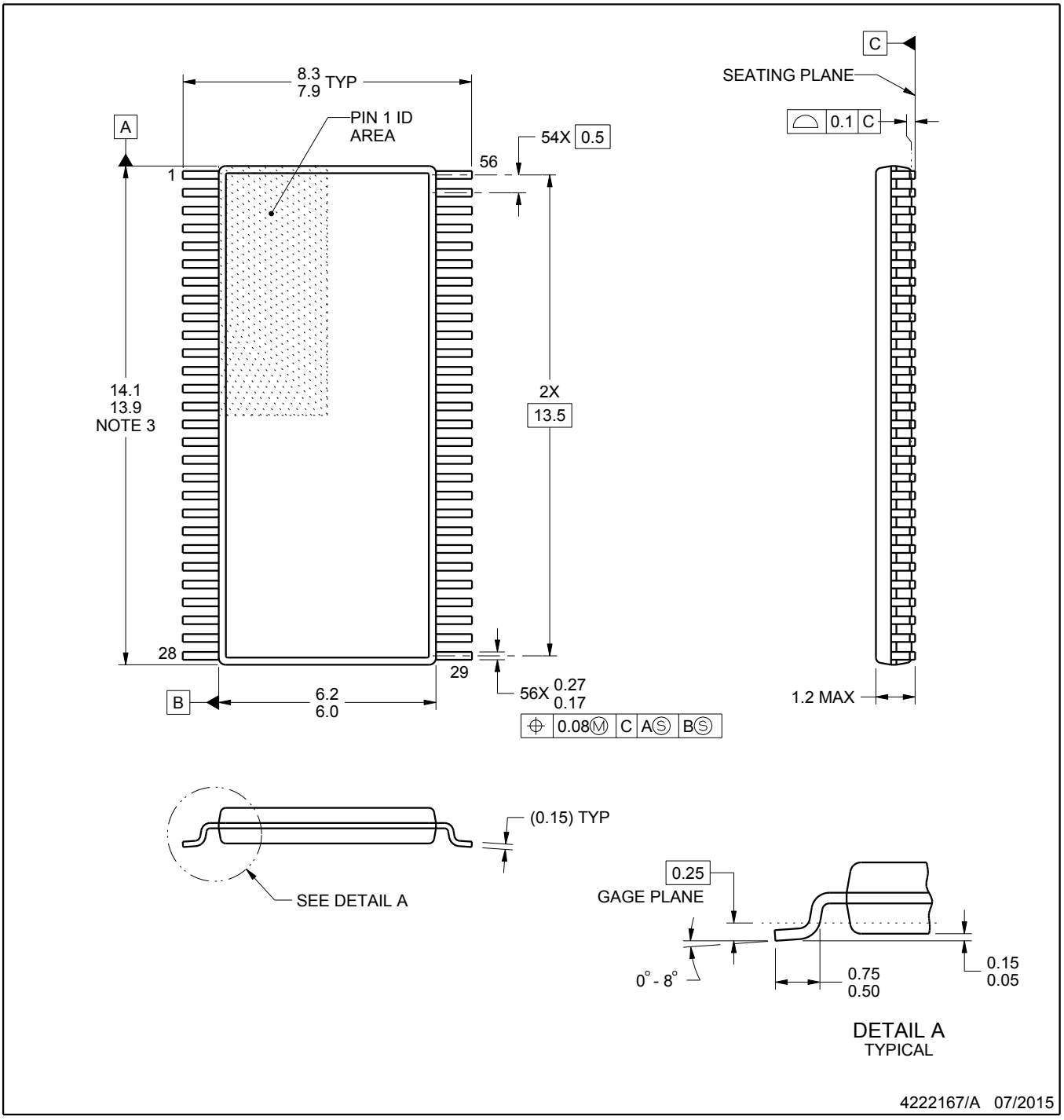
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65LVDS93ADGG	DGG	TSSOP	56	35	530	11.89	3600	4.9
SN65LVDS93ADGG.A	DGG	TSSOP	56	35	530	11.89	3600	4.9

PACKAGE OUTLINE

DGG0056A

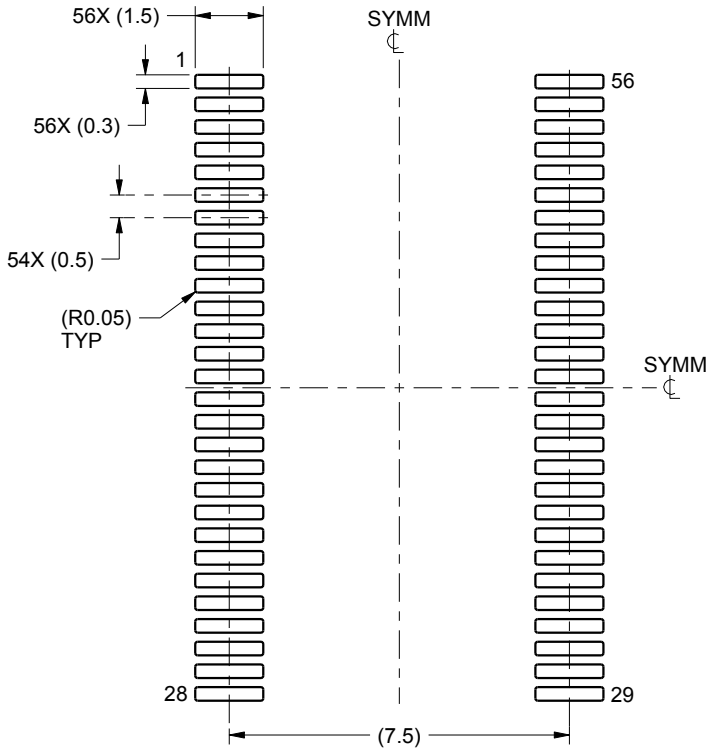
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

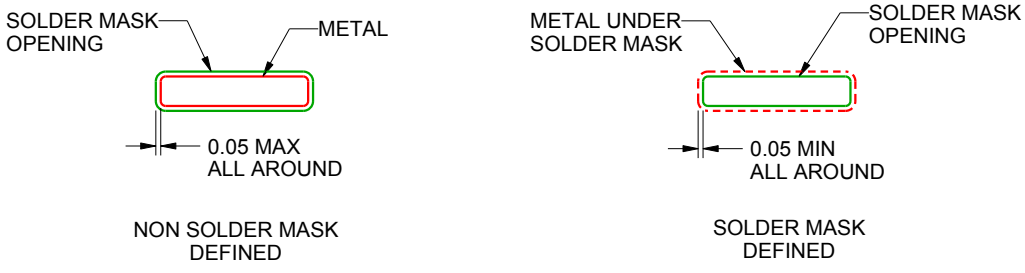


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
SCALE:6X

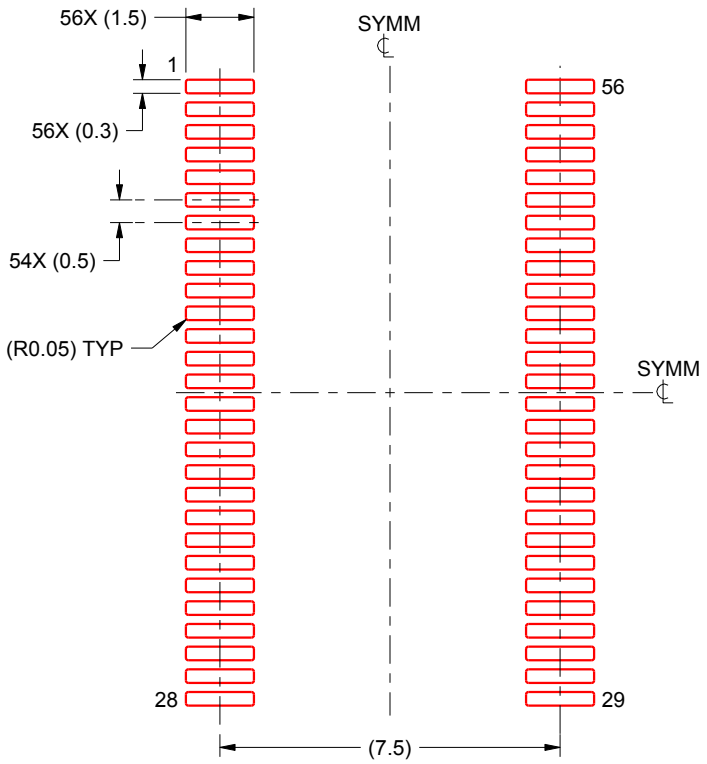


SOLDER MASK DETAILS

4222167/A 07/2015

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4222167/A 07/2015

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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