2.5 V/3.3 V PECL/ECL 1:2 Fanout Buffer

FEATURES

- 1:2 PECL/ECL Fanout Buffer
- Operating Range
  - PECL: V_{CC} = 2.375 V to 3.8V With V_{EE} = 0 V
  - NECL: V_{CC} = 0 V With V_{EE} = –2.375V to –3.8 V
- Open Input Default State
- Support for Clock Frequencies > 3.0 GHz
- 240 ps Typical Propagation Delay
- Deterministic Output Value for Open Input Conditions
- Q Output Will Default Low When Input Open or at V_{EE}
- Built-in Temperature Compensation
- Drop in Compatible to MC10LVEP11, MC100LVEP11
- LVDS Input Compatible

DESCRIPTION

The SN65LVEP11 is a differential 1:2 PECL/ECL fanout buffer. The device includes circuitry to maintain known logic levels when the inputs are in an open condition. Single-ended clock input operation is limited to V_{CC} ≥ 3 V in PECL mode, or V_{EE} ≤ 3 V in NECL mode. The device is housed in an industry-standard SOIC-8 package and is also available in TSSOP-8 package option.

PINOUT ASSIGNMENT

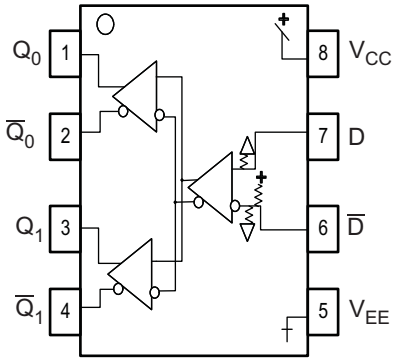


Table 1. PIN DESCRIPTION

PIN	FUNCTION
D, $\overline{D}$	PECL/ECL data inputs
Q_0, $\overline{Q}_0$, Q_1, $\overline{Q}_1$	PECL/ECL outputs
V_{CC}	Positive supply
V_{EE}	Negative supply

ORDERING INFORMATION(1)

PART NUMBER	PART MARKING	PACKAGE	LEAD FINISH
SN65LVEP11D	SN65LVEP11	SOIC	NiPdAu
SN65LVEP11DGK	SN65LVEP11	SOIC-TSSOP	NiPdAu

(1) Leaded device option not initially available; contact TI sales representative for further information.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	CONDITION	VALUE	UNIT
Absolute PECL mode supply voltage VCC	V_{EE} = 0 V	6	V
Absolute NECL mode supply voltage, V_{EE}	V_{CC} = 0 V	–6	V
PECL mode input voltage	V_{EE} = 0 V; $V_I \le V_{CC}$	6	V
NECL mode input voltage	V_{CC} = 0 V; $V_I \ge V_{EE}$	–6	V
Output current	Continuous	50	mA
	Surge	100	mA
Operating temperature range		–40 to 85	°C
Storage temperature range		–65 to 150	°C

POWER DISSIPATION RATINGS

PACKAGE	CIRCUIT BOARD MODEL	POWER RATING T_A < 25°C (mW)	THERMAL RESISTANCE, JUNCTION TO AMBIENT NO AIRFLOW	DERATING FACTOR T_A > 25°C (mW/°C)	POWER RATING T_A = 85°C (mW)
SOIC	Low-K	719	139	7	288
	High-K	840	119	8	336
SOIC-TSSOP	Low-K	469	213	5	188
	High-K	527	189	5	211

THERMAL CHARACTERISTICS

PARAMETER		PACKAGE	VALUE	UNIT
θ_{JB}	Junction-to Board Thermal Resistance	SOIC	79	°C/W
		SOIC-TSSOP	120	
θ_{JC}	Junction-to Case Thermal Resistance	SOIC	98	°C/W
		SOIC-TSSOP	74	

KEY ATTRIBUTES

CHARACTERISTICS	VALUE
Internal input pull down resistor	75 kΩ
Internal input pull up resistor	37.5 kΩ
Moisture sensitivity level	Level 1
Flammability rating (Oxygen Index: 28 to 34)	UL 94 V-0 at 0.125 in
ESD-HBM	4 kV
ESD-machine model	200 V
ESD-charged device model	2 kV
Meets or exceeds JEDEC Spec EIA/JESD78 latchup test	

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PECL DC CHARACTERISTICS(1) (V_{CC} = 2.5 V; V_{EE} = 0.0 V)(2)

PARAMETER		–40°C			25°C			85°C			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	Power supply current		28	45		31	45		35	45	mA
V_{OH}	Output HIGH voltage(3)	1355		1605	1355	1425	1605	1335		1605	mV
V_{OL}	Output LOW voltage(3)	555		900	555	759	900	555		900	mV
V_{IH}	Input high voltage (Single-Ended)	1335		1620	1335		1620	1335		1620	mV
V_{IL}	Input low voltage (Single-Ended)	555		900	555		900	555		900	mV
V_{IHCMR}	Input HIGH voltage common mode range (Differential)(4)	1.2		2.5	1.2		2.5	1.2		2.5	V
I_{IH}	Input HIGH current			150			150			150	µA
I_{IL}	Input LOW current (D)	0.5			0.5			0.5			µA
	nput LOW current (–D)	–150			–150			–150			

(1) The device will meet the specifications after the thermal balance has been established when mounted in a socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.
(2) Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.125 V to – 1.3 V.
(3) All loading with 50 Ω to V_{CC} –2 V.
(4) $V_{IHCMR\ min}$ varies 1:1 with V_{EE}, $V_{IHCMR\ max}$ varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. Single ended input clock pin operation is limited to V_{CC} ≥ 3.0 V in PECL mode.

PECL DC CHARACTERISTICS(1) (V_{CC} = 3.3 V; V_{EE} = 0.0 V)(2)

PARAMETER		–40°C			25°C			85°C			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	Power supply current		28	45		32	45		36	45	mA
V_{OH}	Output HIGH voltage(3)	2155		2405	2155	2221	2405	2155		2405	mV
V_{OL}	Output LOW voltage(3)	1355		1700	1355	1543	1700	1355		1700	mV
V_{IH}	Input high voltage (Single-Ended)(4)	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input low voltage (Single-Ended)(4)	1355		1700	1355		1700	1355		1700	mV
V_{IHCMR}	Input HIGH voltage common mode range (Differential)(5)	1.2		3.3	1.2		3.3	1.2		3.3	V
I_{IH}	Input HIGH current			150			150			150	µA
I_{IL}	Input LOW current (D)	0.5			0.5			0.5			µA
	nput LOW current (–D)	–150			–150			–150			

(1) The device will meet the specifications after the thermal balance has been established when mounted in a socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are specified only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously
(2) Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.925 V to –0.5 V.
(3) All loading with 50 Ω to V_{CC} – 2 V.
(4) Single Ended input clock pin operation is limited to VCC ≥ 3 V in PECL mode.
(5) $V_{IHCMR\ min}$ varies 1:1 with V_{EE}, $V_{IHCMR\ max}$ varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

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NECL DC CHARACTERISTICS[1] (V_{CC} = 0.0 V; V_{EE} = –3.8V to –2.375 V)[2]

PARAMETER		–40°C			25°C			85°C			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I_{CC}	Power supply current		28	45		32	45		36	45	mA
V_{OH}	Output HIGH voltage[3]	–1145		–895	–1145	–1065	–895	–1145		–895	mV
V_{OL}	Output LOW voltage[3]	–1945		–1600	–1945	–1777	–1600	–1945		–1600	mV
V_{IH}	Input high voltage (Single-Ended)[4]	–1165		–880	–1165		–880	–1165		–880	mV
V_{IL}	Input low voltage (Single-Ended)[4]	–1945		–1600	–1945		–1600	–1945		–1600	mV
V_{IHCMR}	Input HIGH voltage common mode range (Differential)[5]	V_{EE}+1.2	V_{EE}+1.2	0.0	V_{EE}+1.2	V_{EE}+1.2	0.0	V_{EE}+1.2	V_{EE}+1.2	0.0	V
I_{IH}	Input HIGH current			150			150			150	µA
I_{IL}	Input LOW current (D)	0.5			0.5			0.5			µA
	nput LOW current (–D)	–150			–150			–150			

(1) The device will meet the specifications after thermal balance has been established when mounted in a socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously
(2) Input and output parameters vary 1:1 with V_{CC}.
(3) All loading with 50 Ω to V_{CC} – 2 V.
(4) Single Ended input clock pin operation is limited to VCC ≤ –3 V in NECL mode.
(5) $V_{IHCMR\ min}$ varies 1:1 with V_{EE}, $V_{IHCMR\ max}$ varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

AC CHARACTERISTICS[1] (V_{CC} = 2.375 V to 3.8 V; V_{EE} = 0.0 V or V_{CC} = 0.0 V; V_{EE} = –3.8 V to –2.375 V[2]

PARAMETER		–40°C			25°C			85°C			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
f_{MAX}	Max switching frequency[3] (see Figure 6)		3.8			3.5			3.1		GHz
t_{PLH}/t_{PHL}	Propagation delay to output differential (CLK, Q, –Q)	200		300	200		300	200		300	ps
t_{SKEW}	Device skew (Q, –Q)		8			8	15		8	15	ps
	Device to Device Skew (Q, –Q) [4]			25			25			25	
t_{JITTER}	Random clock jitter (RMS) ≤ 1.0 GHz			0.3			0.3			0.3	ps
	Random Clock Jitter (RMS) ≤ 1.5 GHz			0.2			0.2			0.2	
	Random Clock Jitter (RMS) ≤ 2.0 GHz			0.2			0.2			0.2	
	Random Clock Jitter (RMS) ≤ 2.5 GHz			0.2			0.2			0.2	
	Random Clock Jitter (RMS) ≤ 3.0 GHz			0.2			0.2			0.2	
V_{PP}	Input swing Differential Config.	150	800	1200	150		1200	150		1200	mV
t_r/t_f	Output rise/fall times Q, –Q (20%–80%)	100		200	100		200	100		200	ps

(1) The device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.
(2) Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50 Ω to V_{CC} –2 V.
(3) The maximum switching frequency measured at the output amplitude of 300 mVpp.
(4) Skew is measured between outputs under identical transitions

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Typical Termination for Output Driver

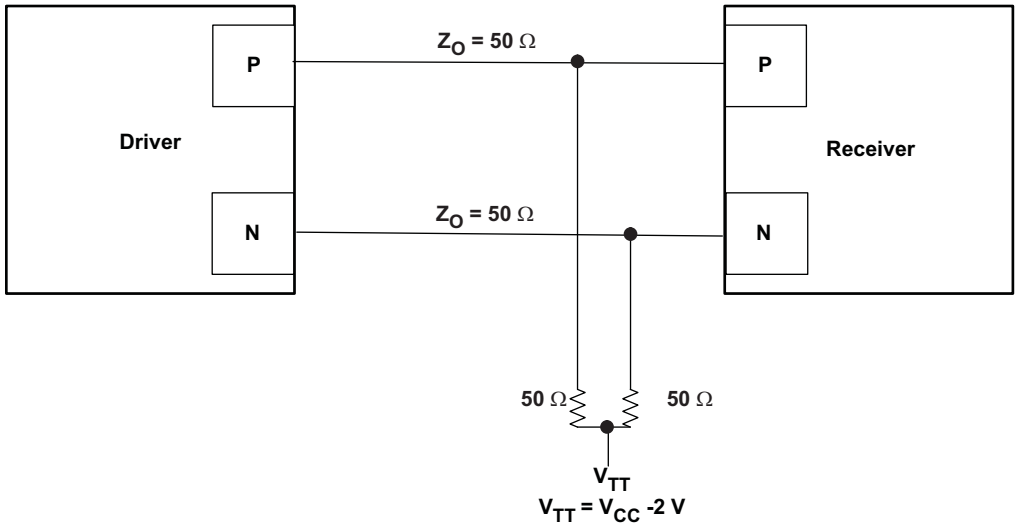


Figure 1. Typical Termination for Output Driver

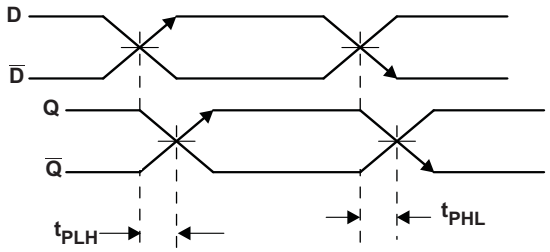


Figure 2. Propagation Delay

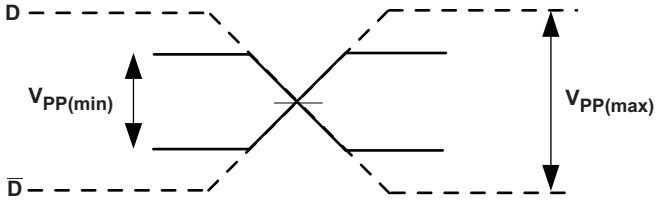


Figure 3. Input Voltage Swing

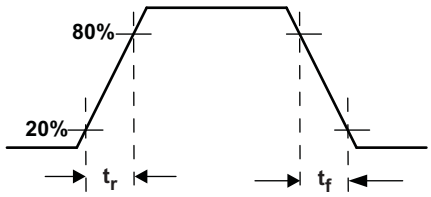


Figure 4. Output Rise and Fall Times

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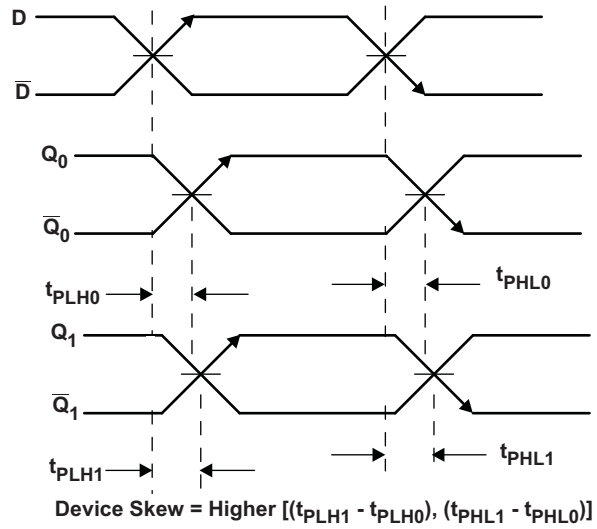


Figure 5. Device Skew

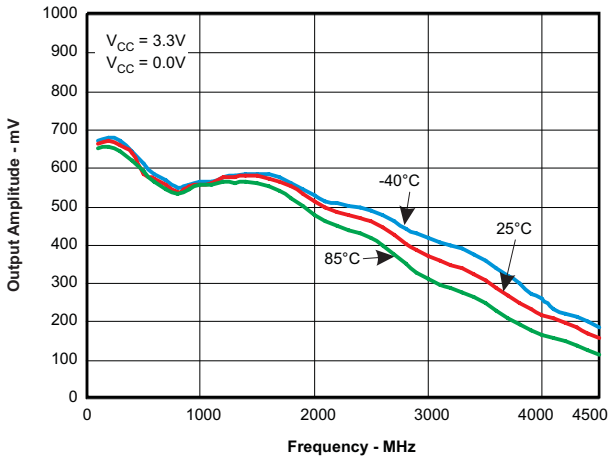


Figure 6. Output Amplitude vs Frequency

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65LVEP11D	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVEP11
SN65LVEP11D.B	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVEP11
SN65LVEP11DGK	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	Call TI | Nipdau	Level-1-260C-UNLIM	-40 to 85	SIJI
SN65LVEP11DGK.B	Active	Production	VSSOP (DGK) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SIJI
SN65LVEP11DGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SIJI
SN65LVEP11DGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SIJI
SN65LVEP11DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVEP11
SN65LVEP11DR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVEP11

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

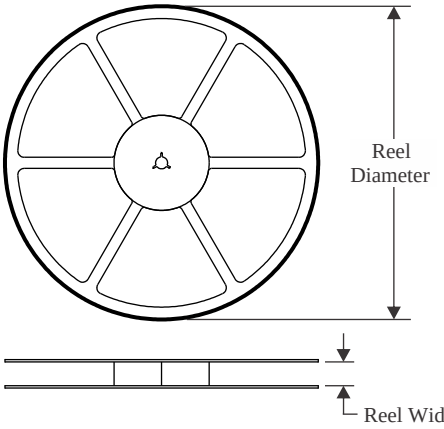
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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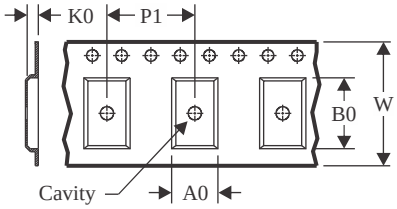
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

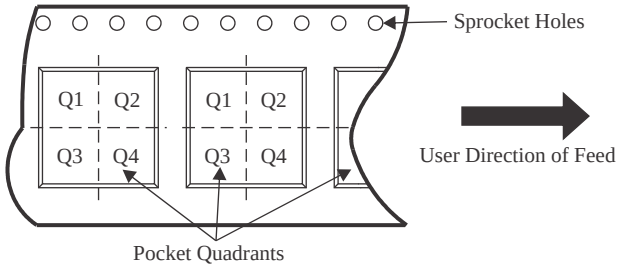


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

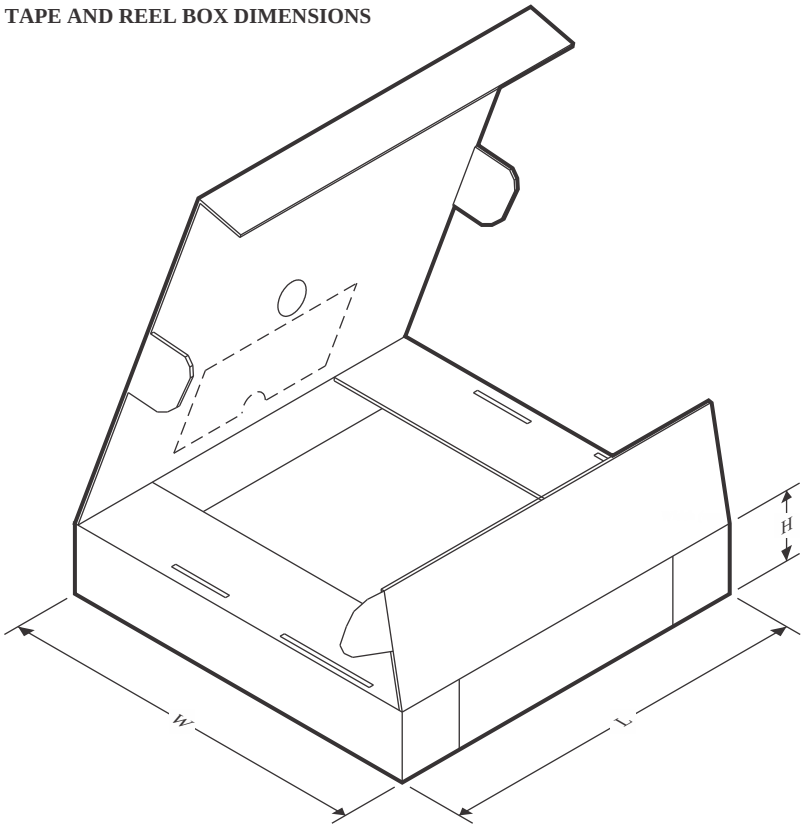
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVEP11DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65LVEP11DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

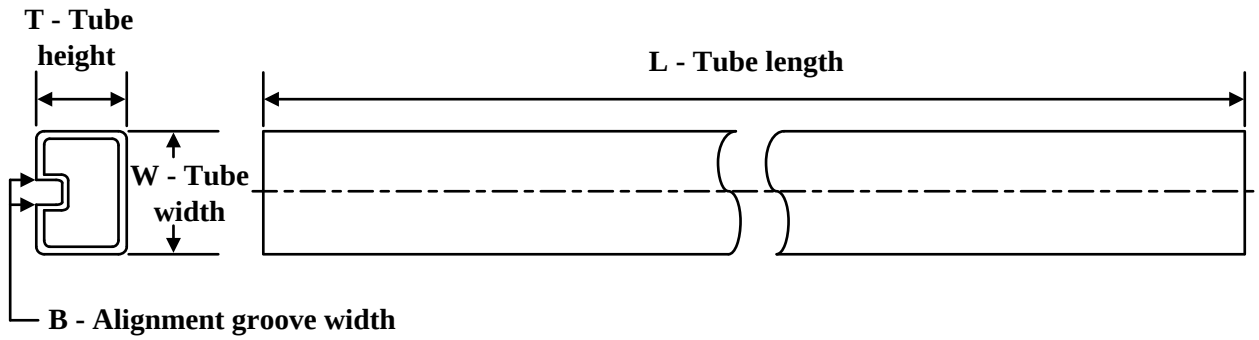
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVEP11DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
SN65LVEP11DR	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

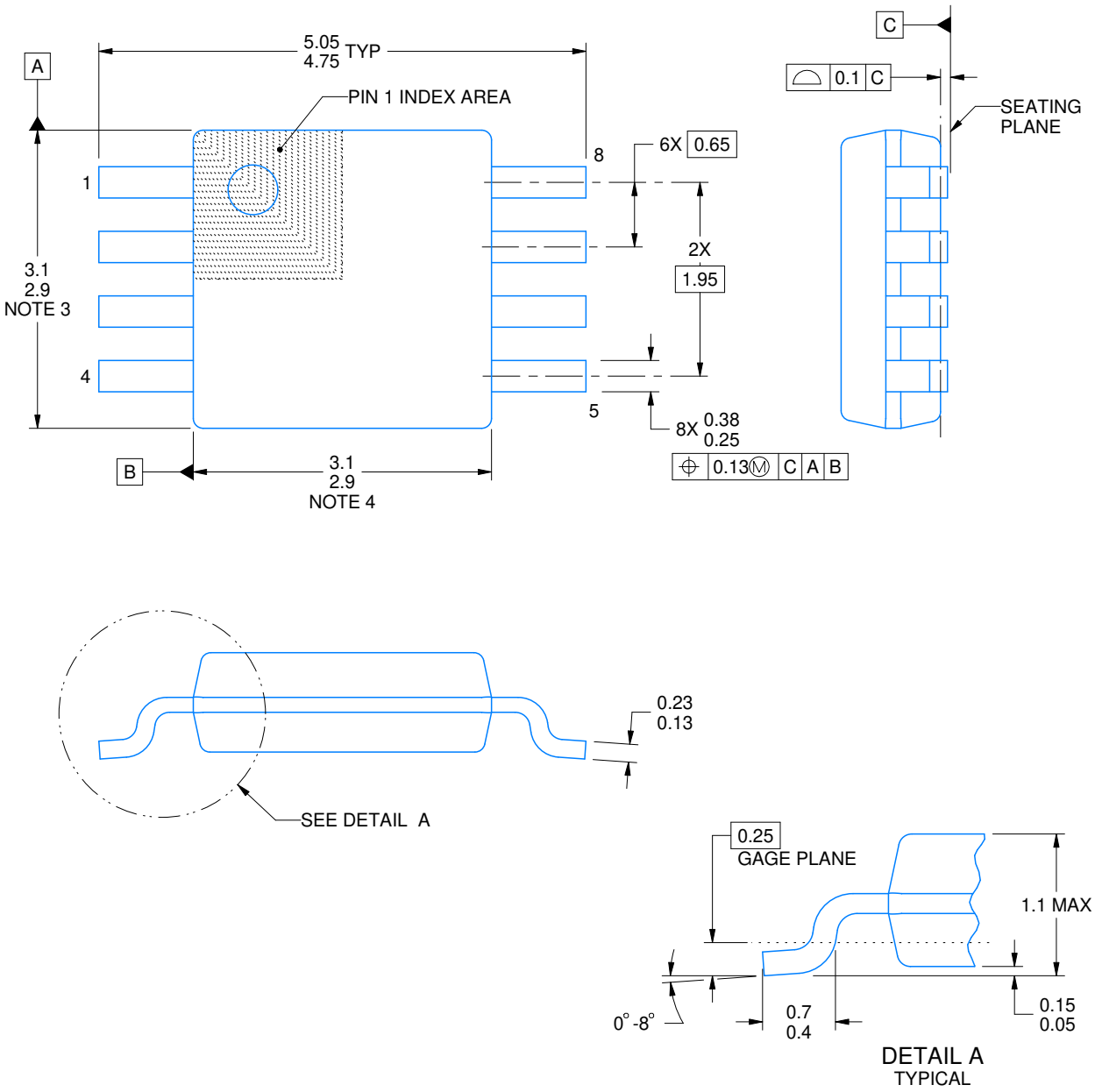
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65LVEP11D	D	SOIC	8	75	506.6	8	3940	4.32
SN65LVEP11D.B	D	SOIC	8	75	506.6	8	3940	4.32
SN65LVEP11DGK	DGK	VSSOP	8	80	330.2	6.6	3005	1.88
SN65LVEP11DGK.B	DGK	VSSOP	8	80	330.2	6.6	3005	1.88

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

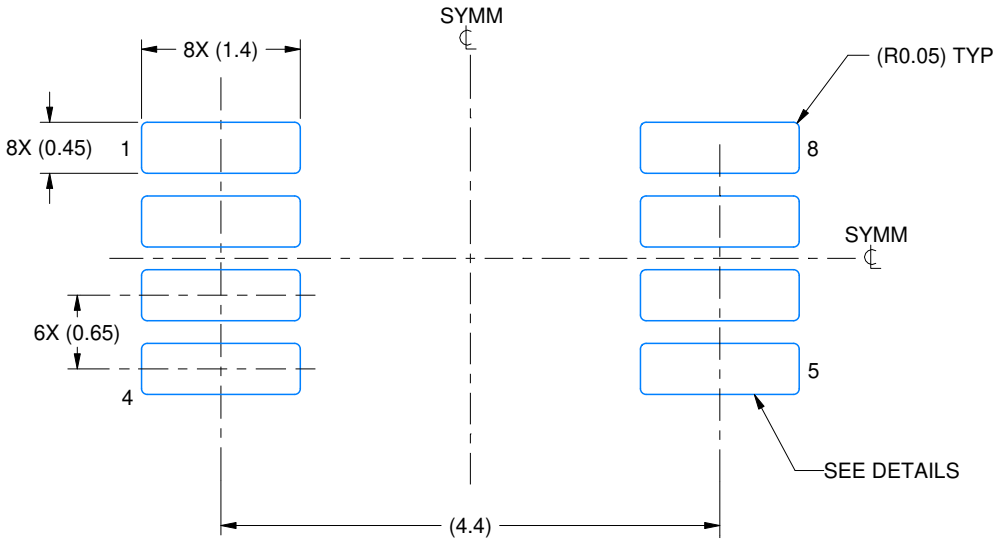


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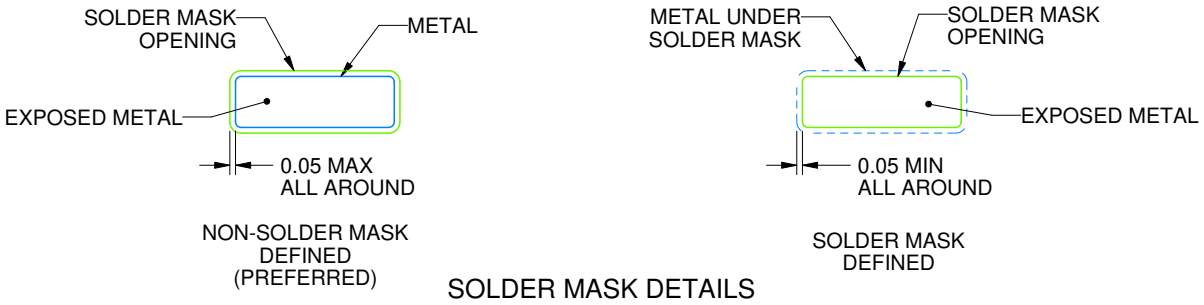
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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

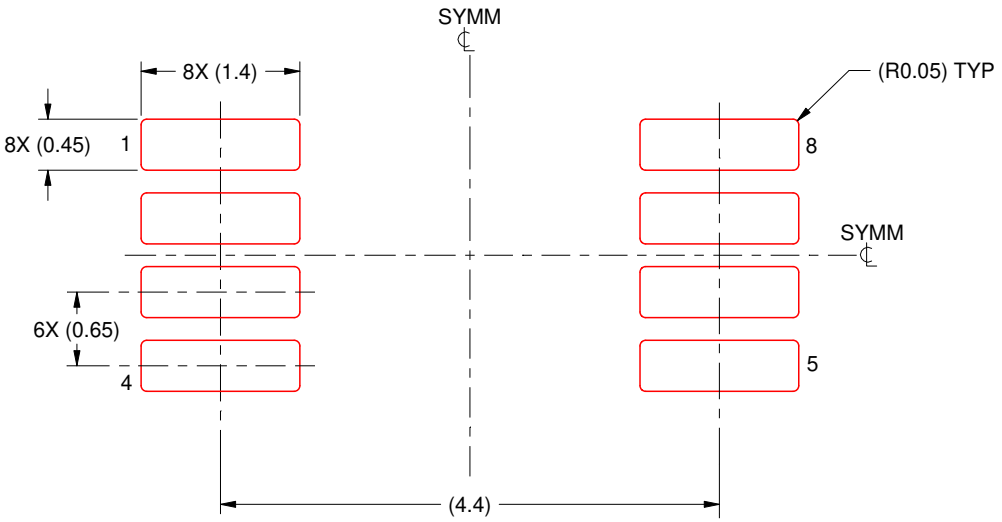


SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

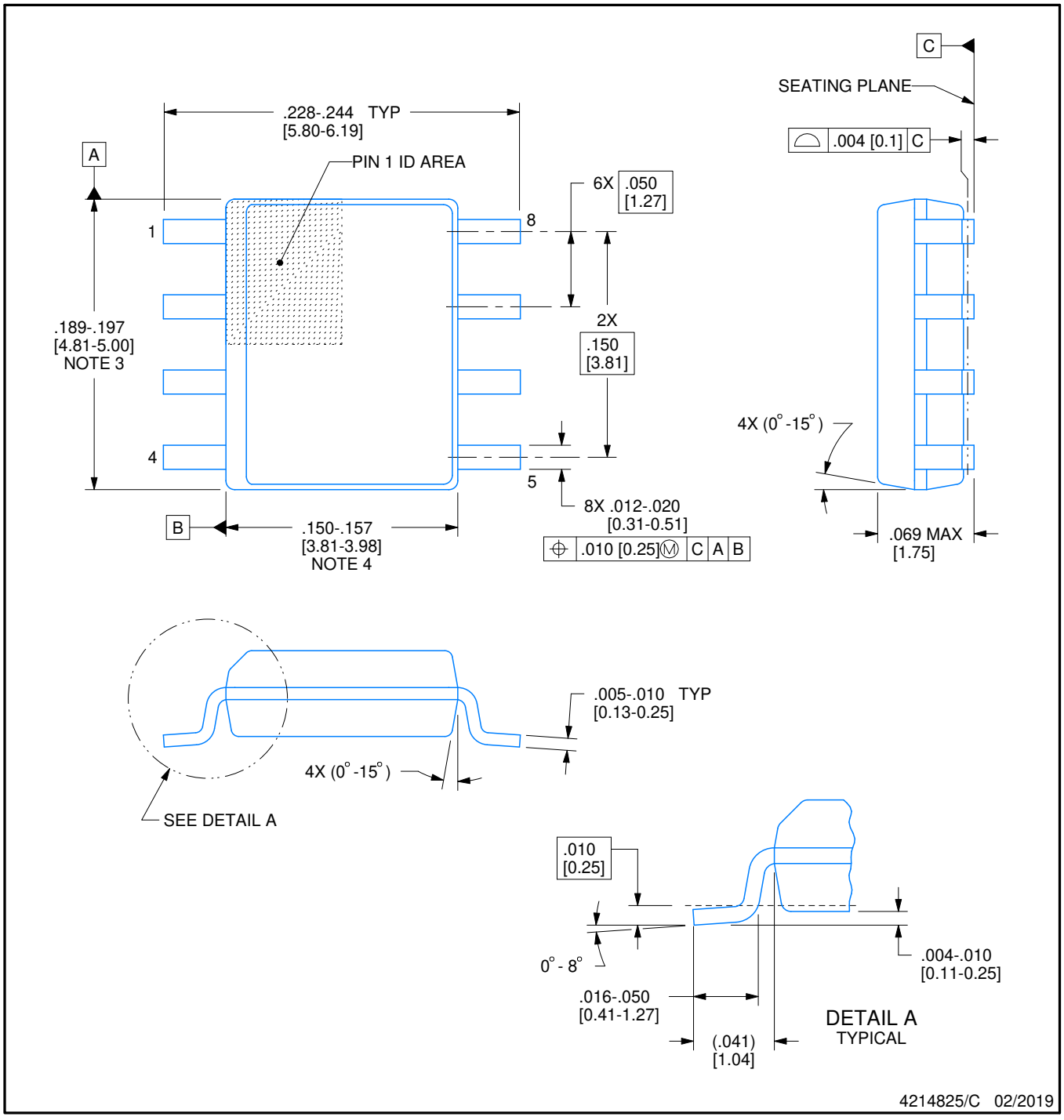


PACKAGE OUTLINE

D0008A

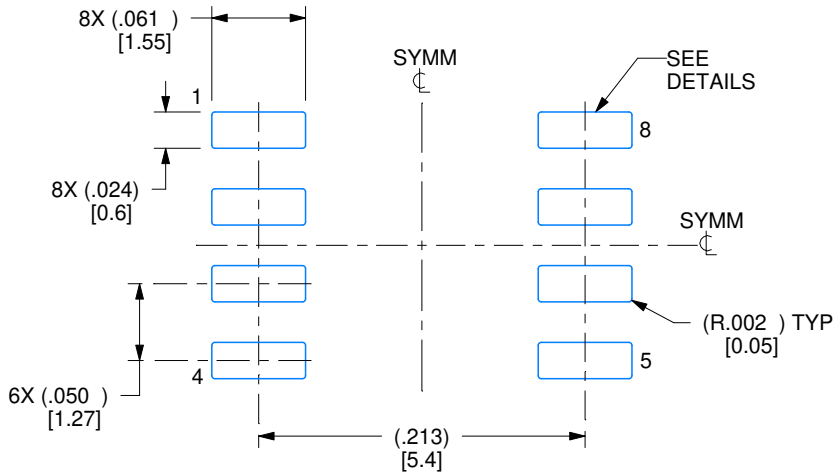
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

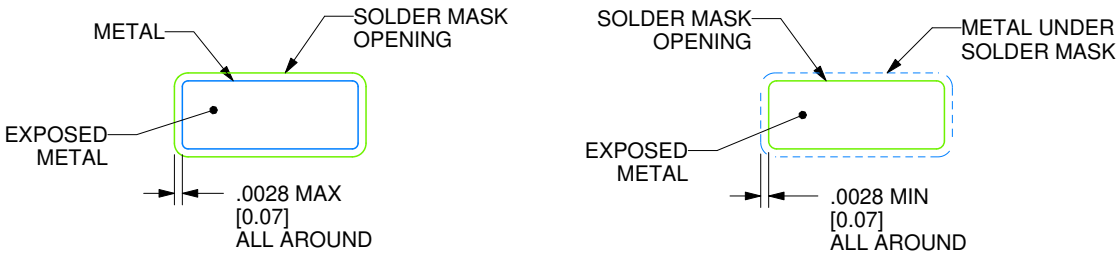


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

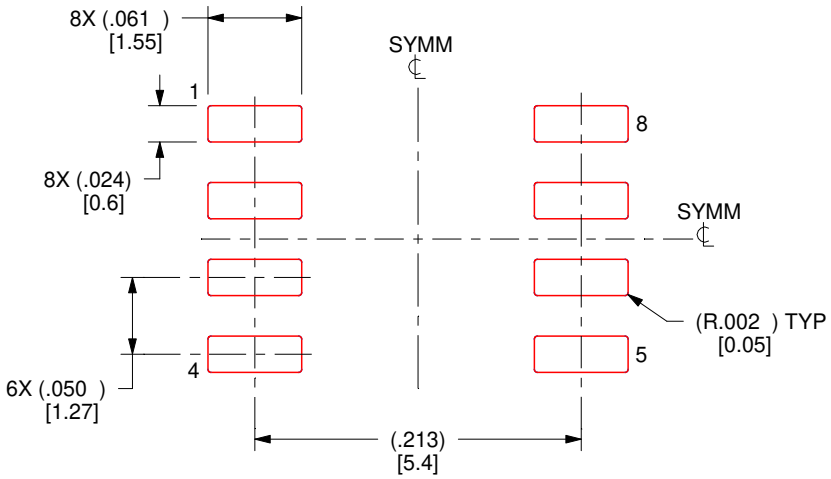
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025