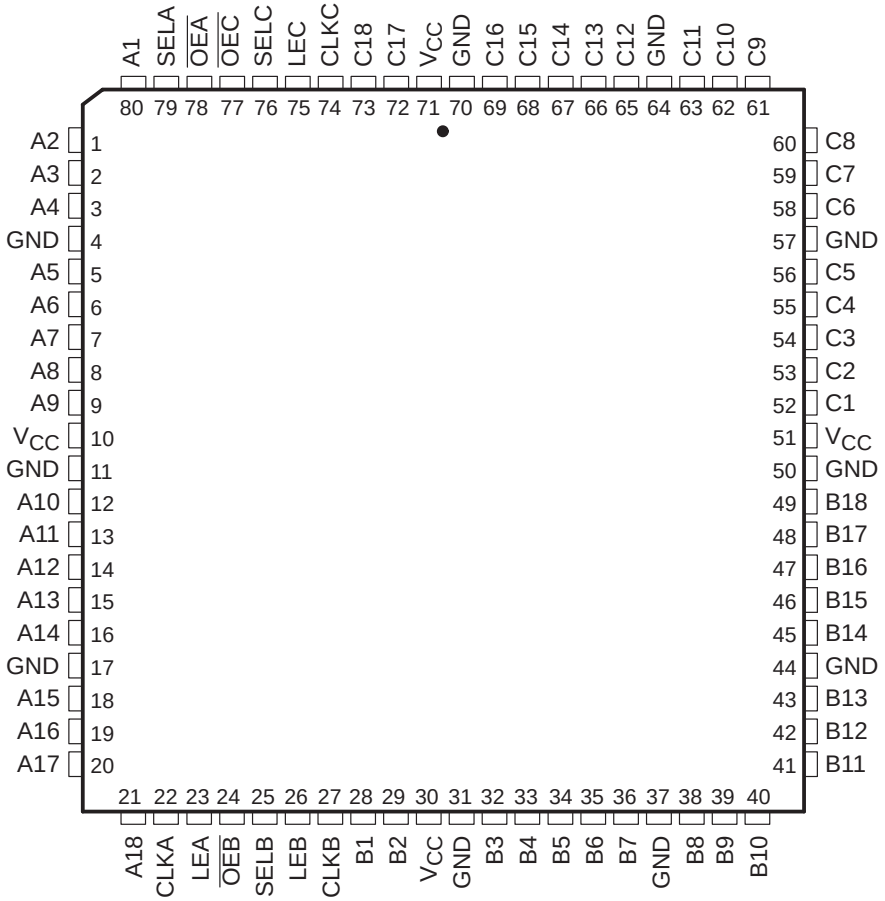
SCBS180E – JUNE 1992 – REVISED MAY 1997

- **Members of the Texas Instruments *Widebus+*™ Family**
- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- ***UBE*™ (Universal Bus Exchanger) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 5 V, T_A = 25°C**
- **High-Impedance State During Power Up and Power Down**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **High-Drive Outputs (–32-mA I_{OH}, 64-mA I_{OL})**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include 80-Pin Plastic Thin Quad Flat (PN) Package With 12 × 12-mm Body Using 0.5-mm Lead Pitch and 84-Pin Ceramic Quad Flat (HT) Package**

SN74ABTH32318 . . . PN PACKAGE
(TOP VIEW)



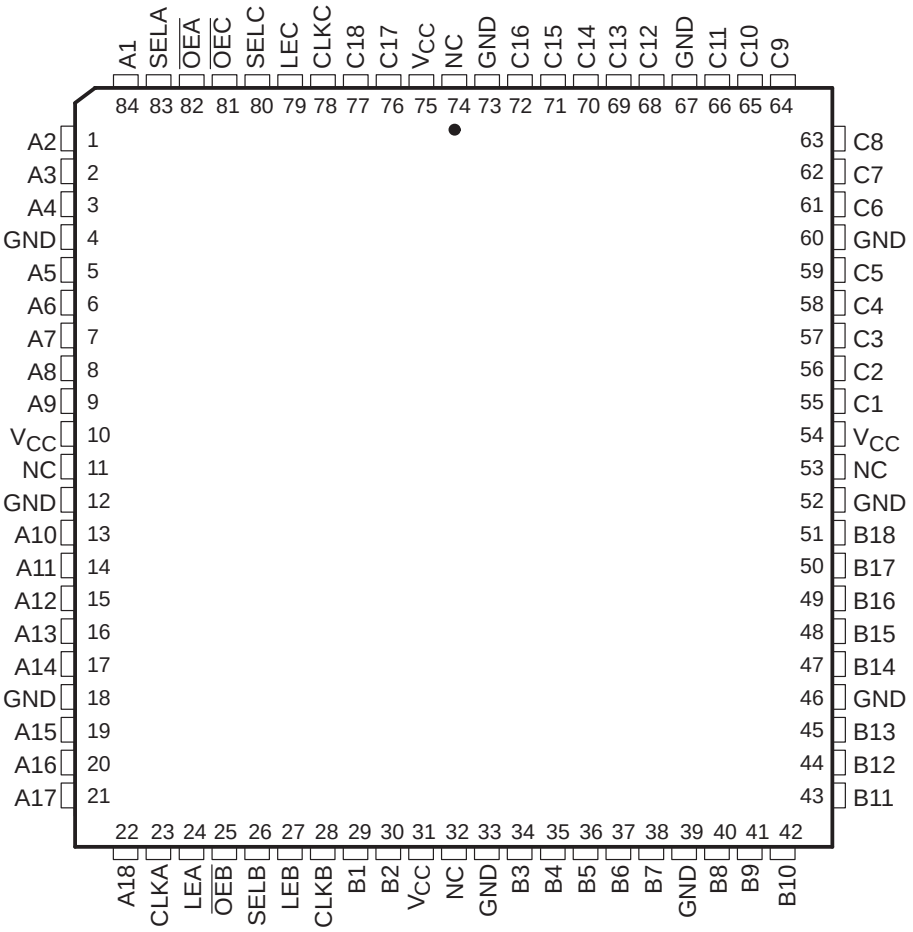
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SN54ABTH32318 . . . HT PACKAGE
(TOP VIEW)



NC – No internal connection

description

The ’ABTH32318 consist of three 18-bit registered input/output (I/O) ports. These registers combine D-type latches and flip-flops to allow data flow in transparent, latch, and clock modes. Data from one input port can be exchanged to one or more of the other ports. Because of the universal storage element, multiple combinations of real-time and stored data can be exchanged among the three ports.

Data flow in each direction is controlled by the output-enable ($\overline{OEA}$, $\overline{OEB}$, and $\overline{OEC}$), select-control (SELA, SELB, and SELC), latch-enable (LEA, LEB, and LEC), and clock (CLKA, CLKB, and CLKC) inputs. The A data register operates in the transparent mode when LEA is high. When LEA is low, data is latched if CLKA is held at a high or low logic level. If LEA is low, data is stored on the low-to-high transition of CLKA. Output data selection is accomplished by the select-control pins. All three ports have active-low output enables, so when the output-enable input is low, the outputs are active; when the output-enable input is high, the outputs are in the high-impedance state.

When V_{CC} is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

description (continued)

The SN54ABTH32318 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABTH32318 is characterized for operation from –40°C to 85°C.

Function Tables

STORAGE†

INPUTS			OUTPUT
CLKA	LEA	A	
↑	L	L	L
↑	L	H	H
H	L	X	Q_0‡
L	L	X	Q_0‡
X	H	L	L
X	H	H	H

† A-port register shown. B and C ports are similar but use CLKB, CLKC, LEB, and LEC.

‡ Output level before the indicated steady-state input conditions were established

A-PORT OUTPUT

INPUTS		OUTPUT A
$\overline{OEA}$	SELA	
H	X	Z
L	H	Output of C register
L	L	Output of B register

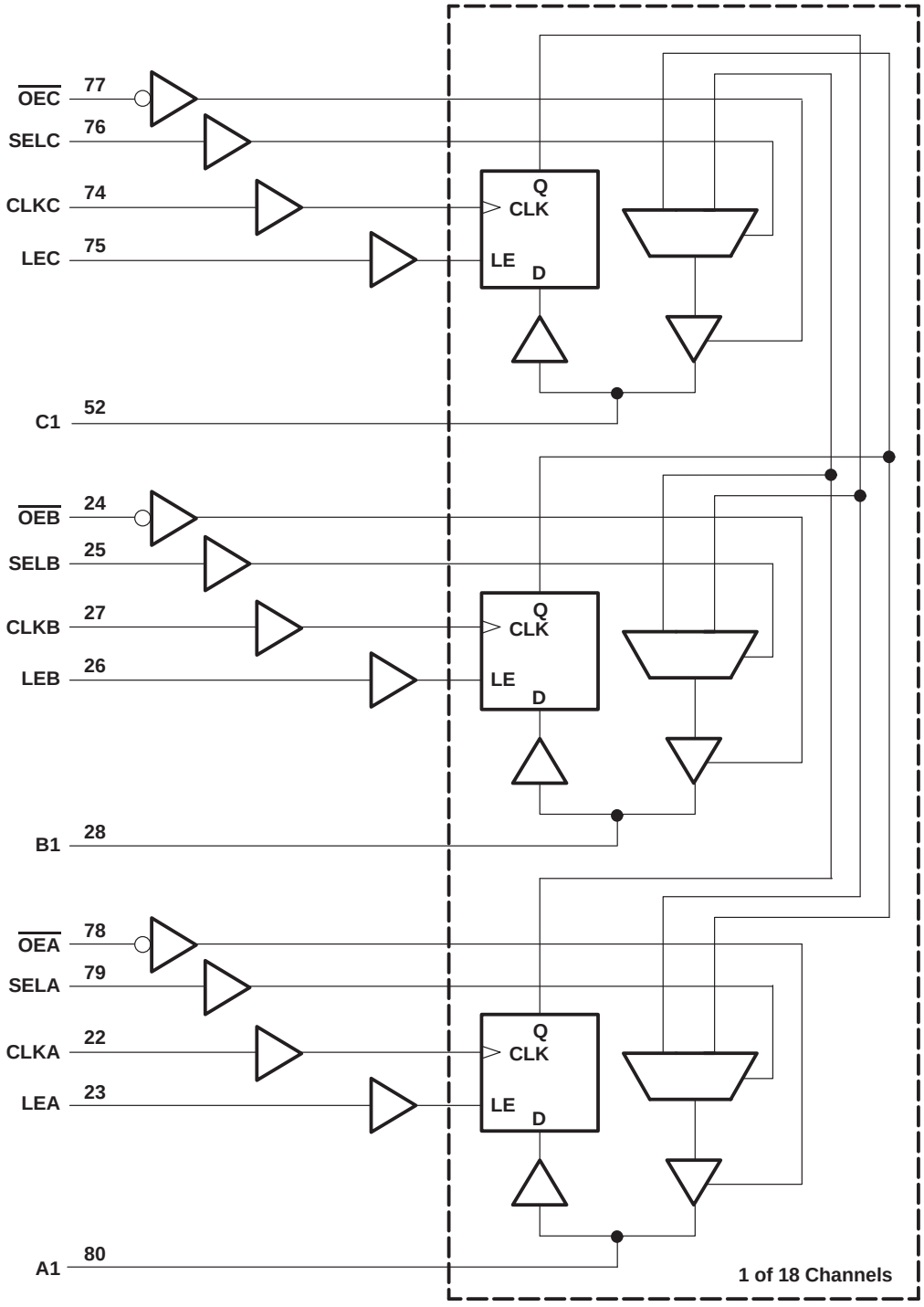
B-PORT OUTPUT

INPUTS		OUTPUT B
$\overline{OEB}$	SELB	
H	X	Z
L	H	Output of A register
L	L	Output of C register

C-PORT OUTPUT

INPUTS		OUTPUT C
$\overline{OEC}$	SELC	
H	X	Z
L	H	Output of B register
L	L	Output of A register

logic diagram (positive logic)



Pin numbers shown are for the PN package.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O . . . . . –0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABTH32318 . . . . . 96 mA
SN74ABTH32318 . . . . . 128 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . –18 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . –50 mA
Package thermal impedance, θ_{JA} (see Note 2): PN package . . . . . 62°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

recommended operating conditions (see Note 3)

			SN54ABTH32318		SN74ABTH32318		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current			–24		–32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		200		μs/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

PRODUCT PREVIEW

NOTE 3: Unused control pins must be held high or low to prevent them from floating.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ABTH32318			SN74ABTH32318			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–1.2			–1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = –3 mA	2.5			2.5			V
		V_{CC} = 5 V,	I_{OH} = –3 mA	3			3			
		V_{CC} = 4.5 V	I_{OH} = –24 mA	2						
			I_{OH} = –32 mA				2			
V_{OL}		V_{CC} = 4.5 V	I_{OL} = 48 mA			0.55			0.55	V
			I_{OL} = 64 mA			0.55			0.55	
V_{hys}					100			100		mV
I_I	Control inputs	V_{CC} = 0 to 5.5 V,	V_I = V_{CC} or GND			±1			±1	µA
	A, B, or C ports	V_{CC} = 2.1 V to 5.5 V,	V_I = V_{CC} or GND			±20			±20	
$I_{I(hold)}$	A, B, or C ports	V_{CC} = 4.5 V	V_I = 0.8 V	100			100			µA
			V_I = 2 V	–100			–100			
I_{OZPU}‡		V_{CC} = 0 to 2.1 V, V_O = 0.5 V to 2.7 V, $\overline{OE}$ = X				±50			±50	µA
I_{OZPD}‡		V_{CC} = 2.1 V to 0, V_O = 0.5 V to 2.7 V, $\overline{OE}$ = X				±50			±50	µA
I_{off}		V_{CC} = 0,	V_I or V_O ≤ 4.5 V			±100			±100	µA
I_{CEX}		V_{CC} = 5.5 V, V_O = 5.5 V	Outputs high			50			50	µA
I_O§		V_{CC} = 5.5 V,	V_O = 2.5 V	–50	–100	–180	–50	–100	–180	mA
I_{CC}		V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			2			2	mA
			Outputs low			45			45	
			Outputs disabled			1			1	
ΔI_{CC}¶		V_{CC} = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND				0.5			0.5	mA
C_i	Control inputs	V_I = 2.5 V or 0.5 V			3			3		pF
C_{io}	A, B, or C ports	V_O = 2.5 V or 0.5 V			11.5			11.5		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ This parameter is specified by characterization.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			SN54ABTH32318		SN74ABTH32318		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency			150		150	MHz
t_w	Pulse duration	LE high	3.3		3.3		ns
		CLK high or low	3.3		3.3		
t_{su}	Setup time	A, B, or C before CLK↑	2.4		2.4		ns
		A, B, or C before LE↓	2.1		2.1		
t_h	Hold time	A, B, or C after CLK↑	1.4		1.4		ns
		A, B, or C after LE↓	2.1		2.1		

PRODUCT PREVIEW

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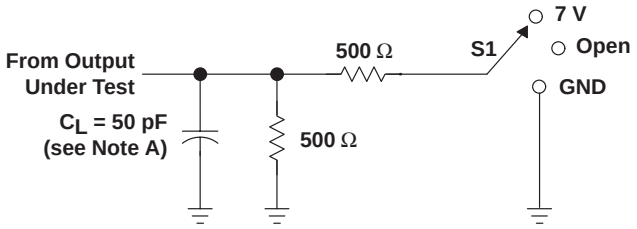
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABTH32318		SN74ABTH32318		UNIT
			MIN	MAX	MIN	MAX	
f_{max}			150		150		MHz
t_{PLH}	A, B, or C	C, B, or A	1.4	6.5	1.4	6.1	ns
t_{PHL}			1.1	6.8	1.1	6.6	
t_{PLH}	SEL	A, B, or C	1.4	6.7	1.4	6.5	ns
t_{PHL}			1.8	6.8	1.8	6.5	
t_{PLH}	LE	A, B, or C	2.6	8	2.6	7.5	ns
t_{PHL}			2.6	7.4	2.6	6.9	
t_{PLH}	CLK	A, B, or C	2.5	8	2.5	7.4	ns
t_{PHL}			2.5	7.2	2.5	6.7	
t_{PZH}	$\overline{OE}$	A, B, or C	1.4	6.9	1.4	6.8	ns
t_{PZL}			2.4	7.2	2.4	7.1	
t_{PHZ}	$\overline{OE}$	A, B, or C	1	6.4	1	6.2	ns
t_{PLZ}			2	6.4	2	6	

PRODUCT PREVIEW

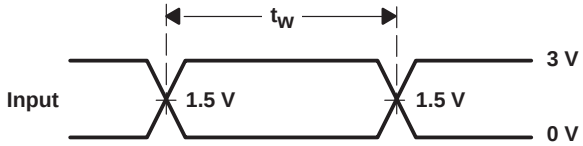
PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

PARAMETER MEASUREMENT INFORMATION

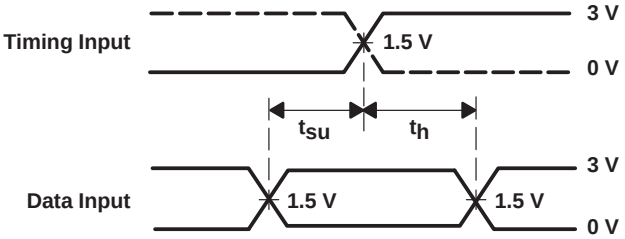


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

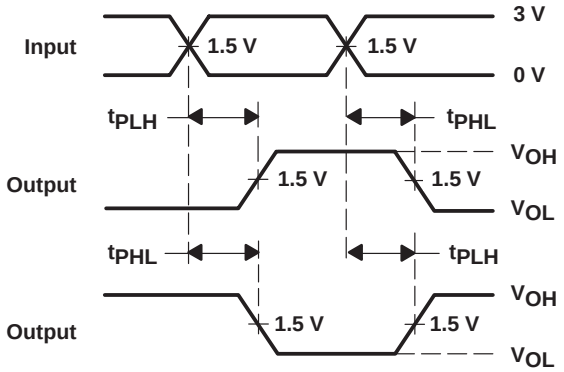
LOAD CIRCUIT



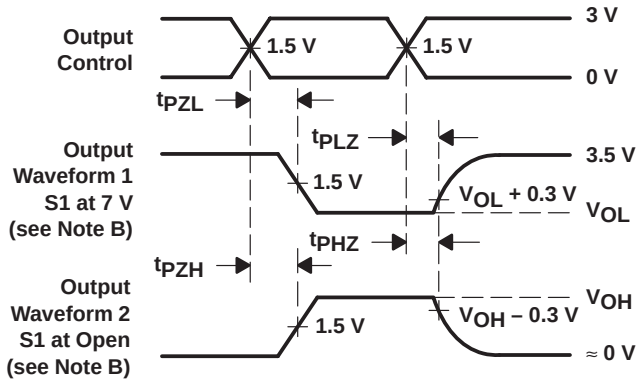
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74ABTH32318PN	Active	Production	LQFP (PN) | 80	119 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	ABTH32318
SN74ABTH32318PN.B	Active	Production	LQFP (PN) | 80	119 | JEDEC TRAY (10+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	ABTH32318

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

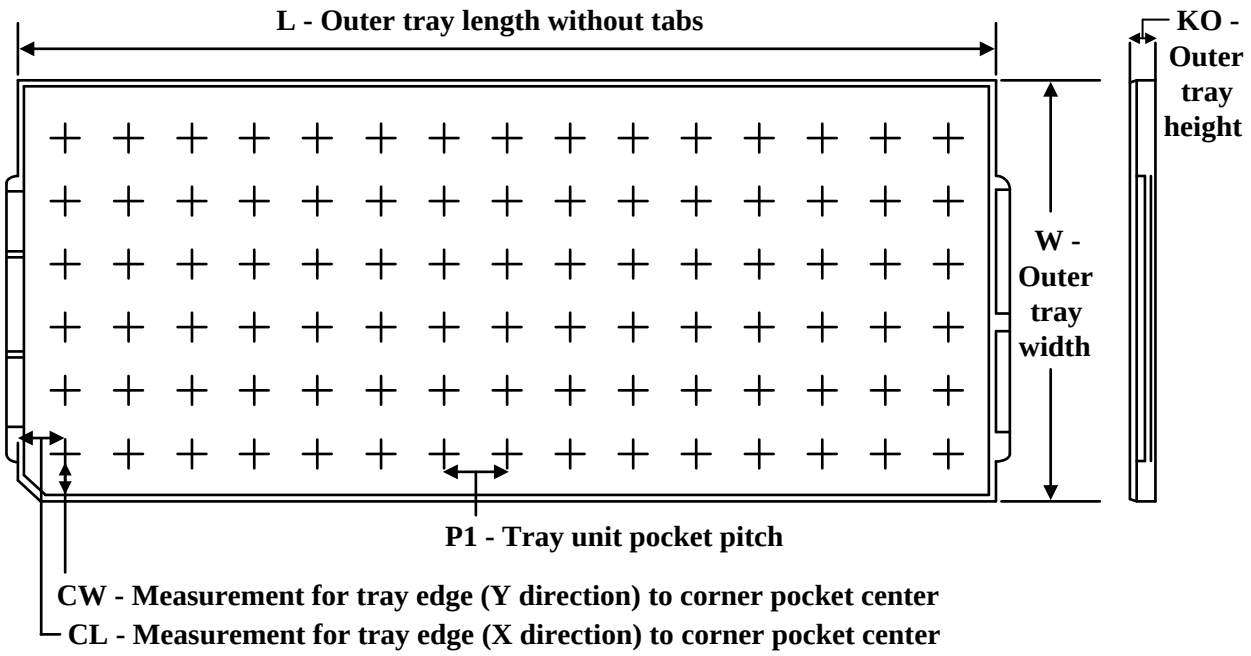
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

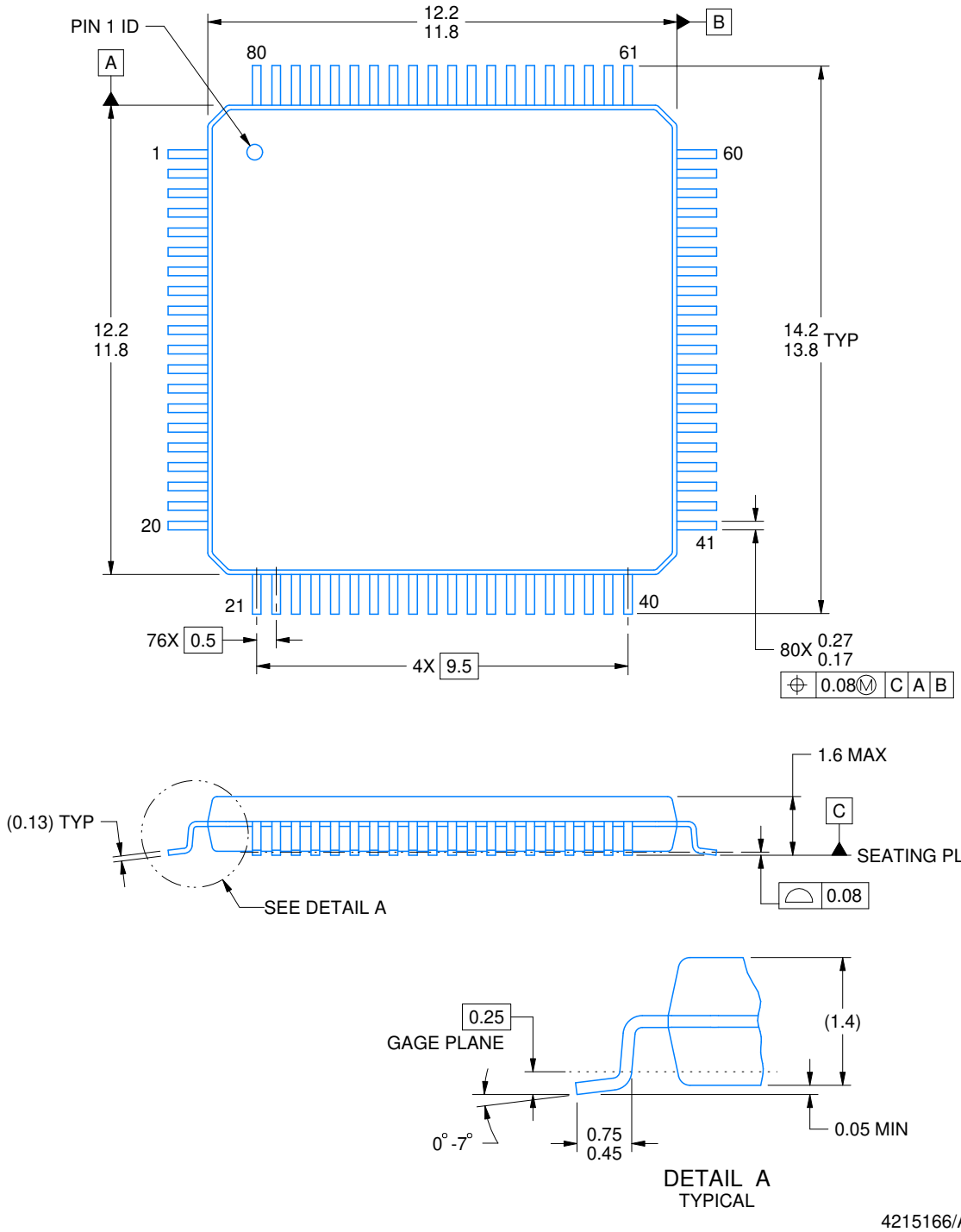
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
SN74ABTH32318PN	PN	LQFP	80	119	7 x 17	150	315	135.9	7620	17.9	14.3	13.95
SN74ABTH32318PN.B	PN	LQFP	80	119	7 x 17	150	315	135.9	7620	17.9	14.3	13.95

PACKAGE OUTLINE

PN0080A

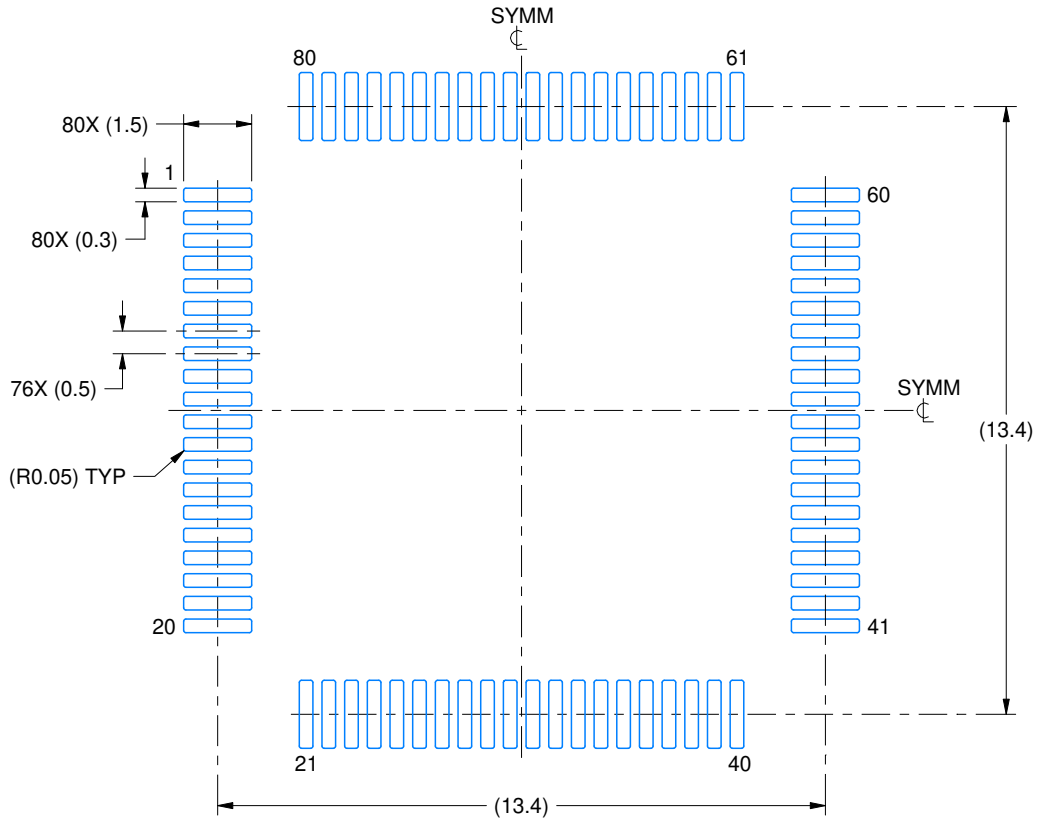
LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X

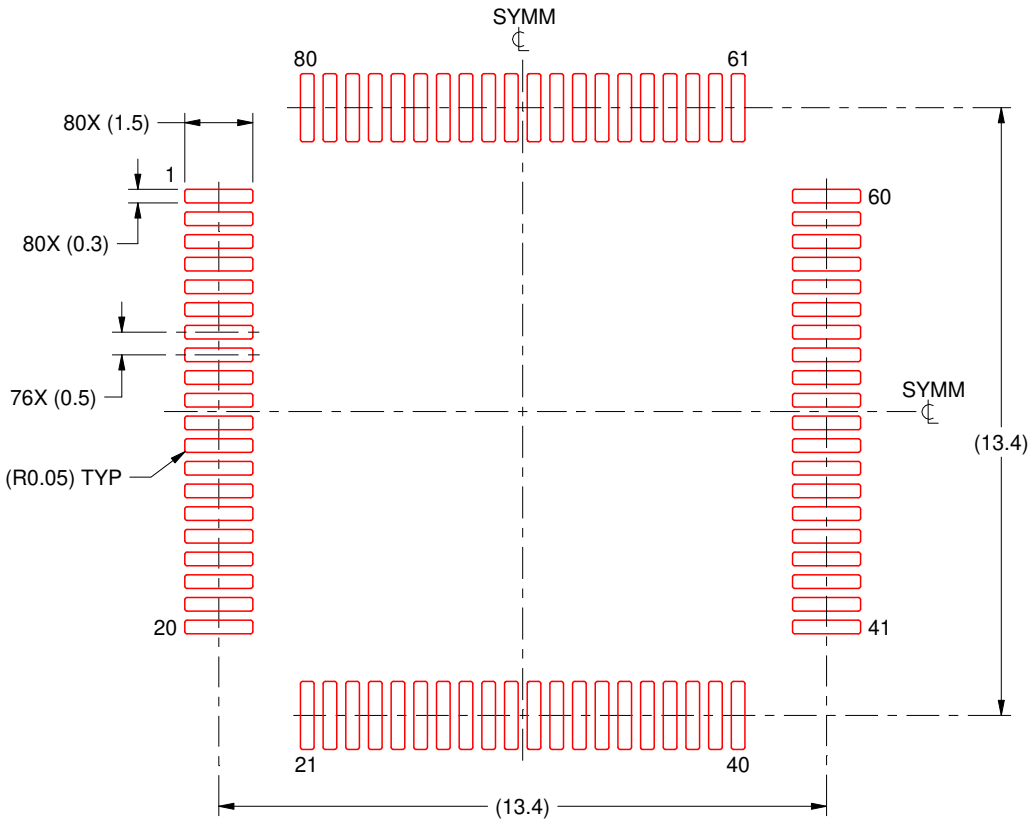


SOLDER MASK DETAILS

4215166/A 08/2022

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:6X

4215166/A 08/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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