# SNx4ACT14 Hex Schmitt-Trigger Inverter

## 1 Features

- $V_{CC}$ operation of 4.5V to 5.5V
- Inputs accept voltages to 5.5V
- Max $t_{pd}$ of 11ns at 5V
- Inputs are TTL-voltage compatible

## 2 Applications

- Synchronize inverted clock inputs
- Debounce a switch
- Invert a digital signal

## 3 Description

These Schmitt-trigger devices contain six independent inverters.

**Device Information**

| PART NUMBER | PACKAGE(1) | PACKAGE SIZE(2) | BODY SIZE(3) |
|---|---|---|---|
| SN54ACT14 | J (CDIP, 14) | 19.56mm × 7.9mm | 19.56mm × 6.67mm |
| | W (CFP, 14) | 9.21mm × 9.02mm | 9.21mm × 6.3mm |
| | FK (LCCC, 20) | 8.89mm × 8.89mm | 8.89mm × 8.89mm |
| SNx4ACT14 | BQA (WQFN, 14) | 3mm × 2.5mm | 3mm × 2.5mm |
| | D (SOIC, 14) | 8.65mm × 6mm | 8.65mm × 3.9mm |
| | DB (SSOP, 14) | 6.2mm x 7.8mm | 6.2mm x 5.3mm |
| | N (PDIP, 14) | 19.3mm × 9.4mm | 19.3mm × 6.35mm |
| | NS (SOP, 14) | 10.2mm x 7.8mm | 10.3mm x 5.3mm |
| | PW (TSSOP, 14) | 5mm × 6.4mm | 5mm × 4.4mm |

(1) For more information, see Section 11
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.




**Logic Diagram (Positive Logic)**

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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## 4 Pin Configuration and Functions

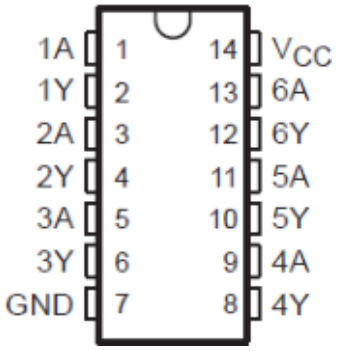



**Figure 4-1. SN54ACT14 J or W Package and SN74ACT14 D, DB, N, NS, or PW Package (Top View)**

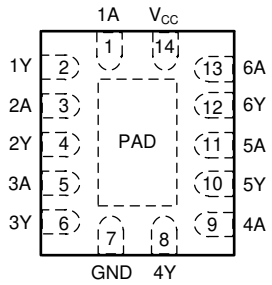
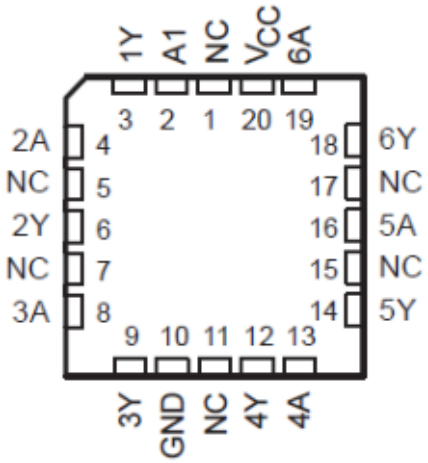



**Figure 4-2. SN74ACT14 BQA Package, 14-Pin WQFN (Top View)**




NC − No internal connection

**Figure 4-3. SN54ACT14 FK Package (Top View)**

**Table 4-1. Pin Function**

| PIN | | I/O[1] | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| 1A | 1 | Input | Channel 1, Input A |
| 1Y | 2 | Output | Channel 1, Output Y |
| 2A | 3 | Input | Channel 2, Input A |
| 2Y | 4 | Output | Channel 2, Output Y |
| 3A | 5 | Input | Channel 3, Input A |
| 3Y | 6 | Output | Channel 3, Output Y |
| GND | 7 | — | Ground |
| 4Y | 8 | Output | Channel 4, Output Y |
| 4A | 9 | Input | Channel 4, Input A |
| 5Y | 10 | Output | Channel 5, Output Y |
| 5A | 11 | Input | Channel 5, Input A |
| 6Y | 12 | Output | Channel 6, Output Y |
| 6A | 13 | Input | Channel 6, Input A |

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**Table 4-1. Pin Function (continued)**

| PIN | | I/O[1] | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| $V_{CC}$ | 14 | — | Positive Supply |
| Thermal pad | | — | Connect the GND pin to the exposed thermal pad for correct operation. Connect the thermal pad to any internal PCB ground plane using multiple vias for good thermal performance. |

(1) I = input, O = output, P = power, FB = feedback, GND = ground, N/A = not applicable


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# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | | –0.5 | 7 | V |
| $V_I$ | Input voltage range(1) | | –0.5 | $V_{CC}$ + 0.5 | V |
| $V_O$ | Output voltage range(1) | | –0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | $V_I$ < 0 or $V_I$ > $V_{CC}$ | | ±20 | mA |
| $I_{OK}$ | Output clamp current | $V_O$ < 0 or $V_O$ > $V_{CC}$ | | ±20 | mA |
| $I_O$ | Continuous output current | $V_O$ = 0 to $V_{CC}$ | | ±50 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±200 | mA |
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |

(1) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | ±1500 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 Recommended Operating Conditions

| | | SN54ACT14 | | SN74ACT14 | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $V_I$ | Input voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $V_O$ | Output voltage | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | | –24 | | –24 | mA |
| $I_{OL}$ | Low-level output current | | 24 | | 24 | mA |
| $T_A$ | Operating free-air temperature | –55 | 125 | –40 | 85 | °C |

## 5.4 Thermal Information

| THERMAL METRIC(1) | | SN74ACT14 | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | BQA (WQFN) | D (SOIC) | DB (SSOP) | N (PDIP) | NS (SOP) | PW (TSSOP) | |
| | | 14 PINS | | | | | | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 85.4 | 89.9 | 96 | 80 | 76 | 148 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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## 5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54ACT14 | | SN74ACT14 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{T+}$ Positive-going threshold | | 4.5 V | 1.2 | 1.5 | 1.9 | 1.2 | 1.9 | 1.2 | 1.9 | V |
| | | 5.5 V | 1.4 | 1.7 | 2.1 | 1.4 | 2.1 | 1.4 | 2.1 | |
| $V_{T-}$ Negative-going threshold | | 4.5 V | 0.5 | 0.9 | 1.2 | 0.5 | 1.2 | 0.5 | 1.2 | V |
| | | 5.5 V | 0.6 | 1 | 1.4 | 0.6 | 1.4 | 0.6 | 1.4 | |
| $\Delta V_T$ Hysteresis ($V_{T+} - V_{T-}$) | | 4.5 V | 0.4 | 0.6 | 1.4 | 0.4 | 1.4 | 0.4 | 1.4 | V |
| | | 5.5 V | 0.4 | 0.6 | 1.5 | 0.4 | 1.5 | 0.4 | 1.5 | |
| $V_{OH}$ | $I_{OH}$ = –50 µA | 4.5 V | 4.4 | 4.49 | | 4.4 | | 4.4 | | V |
| | | 5.5 V | 5.4 | 5.49 | | 5.4 | | 5.4 | | |
| | $I_{OH}$ = –24 mA | 4.5 V | 3.86 | | | 3.7 | | 3.76 | | |
| | | 5.5 V | 4.86 | | | 4.7 | | 4.76 | | |
| | $I_{OH}$ = –50 mA(1) | 5.5 V | | | | 3.85 | | | | |
| | $I_{OH}$ = –75 mA(1) | 5.5 V | | | | | | 3.85 | | |
| $V_{OL}$ | $I_{OL}$ = 50 µA | 4.5 V | | 0.001 | 0.1 | | 0.1 | | 0.1 | V |
| | | 5.5 V | | 0.001 | 0.1 | | 0.1 | | 0.1 | |
| | $I_{OL}$ = 24 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| | | 5.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| | $I_{OL}$ = 50 mA(1) | 5.5 V | | | | | 1.65 | | | |
| | $I_{OL}$ = 75 mA(1) | 5.5 V | | | | | | | 1.65 | |
| $I_I$ | $V_I = V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | | ±1 | µA |
| $I_{CC}$ | $V_I = V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 2 | | 40 | | 20 | µA |
| $\Delta I_{CC}$ (2) | One input at 3.4 V, Other inputs at GND or $V_{CC}$ | 5.5 V | | 0.6 | | | 1.6 | | 1.5 | mA |
| $C_i$ | $V_I = V_{CC}$ or GND | 5 V | | 4.5 | | | | | | pF |

(1) Not more than one output should be tested at a time, and the duration of the test should not exceed 2 ms.
(2) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or $V_{CC}$.

## 5.6 Switching Characteristics

over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $T_A$ = 25°C | | SN54ACT14 | | SN74ACT14 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A | Y | 1.5 | 11.5 | 1 | 14 | 1 | 12.5 | ns |
| $t_{PHL}$ | | | 1.5 | 10 | 1 | 13 | 1 | 11 | |

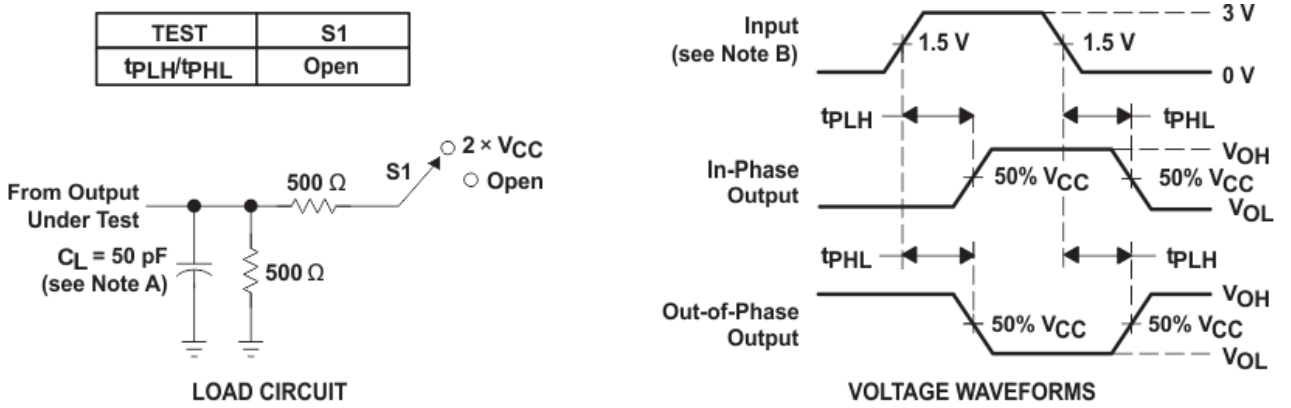
## 5.7 Operating Characteristics

$V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | $C_L$ = 50 pF, | f = 1 MHz | 20 | pF |


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## 6 Parameter Measurement Information




NOTES: A. $C_L$ includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
C. The outputs are measured one at a time, with one input transition per measurement.

**Figure 6-1. Load Circuit and Voltage Waveforms**

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# 7 Detailed Description

## 7.1 Overview

These 'ACT14 devices perform the Boolean function Y = $\overline{A}$. Because of the Schmitt action, they have different input threshold levels for positive-going ($V_{T+}$) and for negative-going ($V_{T-}$) signals.

These circuits are temperature compensated and can be triggered from the slowest of input ramps and still give clean, jitter-free output signals. They also have a greater noise margin than conventional inverters.

## 7.2 Functional Block Diagram




## 7.3 Feature Description

- $V_{CC}$ is optimized at 5 V
- Allows up voltage translation from 3.3 V to 5 V
  - Inputs accept $V_{IH}$ levels of 2 V
- Slow edge rates minimize output ringing
- Inputs are TTL-Voltage compatible

### *7.3.1 Balanced CMOS Push-Pull Outputs*

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important to limit the output power of the device to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs must be left disconnected.

### *7.3.2 Clamp Diode Structure*

As shown in Figure 7-1, the inputs and outputs to this device have both positive and negative clamping diodes.

**CAUTION**

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

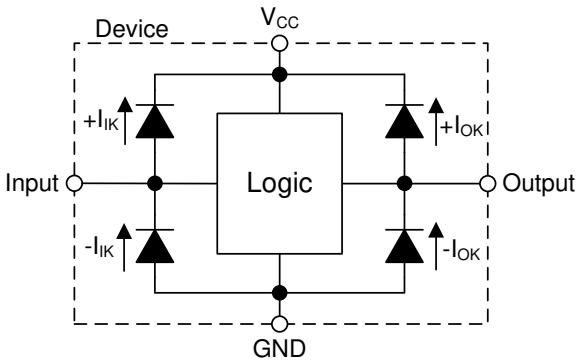



**Figure 7-1. Electrical Placement of Clamping Diodes for Each Input and Output**


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## 7.4 Device Functional Modes

**Table 7-1. Function Table**

| INPUT | OUTPUT |
|---|---|
| A | Y |
| H | L |
| L | H |

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# 8 Application Information Disclaimer

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 8.1 Application Information

The SNx4ACT14 device is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs are tolerant to 5.5 V at any valid $V_{CC}$. This feature makes it Ideal for translating down to the $V_{CC}$ level. Switching Characteristics Comparison shows the reduction in ringing compared to higher drive parts such as AC.

## 8.2 Typical Application

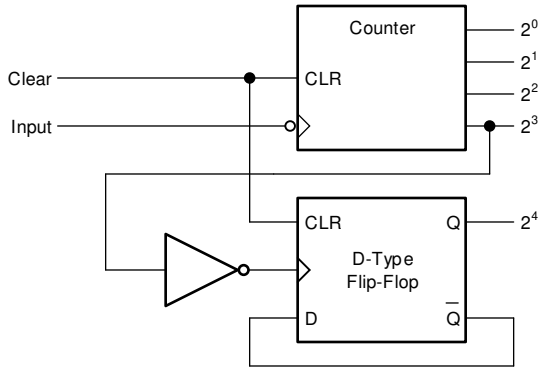



**Figure 8-1. Typical application schematic**

### *8.2.1 Design Requirements*

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

### *8.2.2 Detailed Design Procedure*

1. Recommended Input Conditions
   - For rise time and fall time specifications, see Δt/ΔV in the *Section 5.3* table.
   - For specified High and low levels, see $V_{IH}$ and $V_{IL}$ in the *Section 5.3* table.
   - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid $V_{CC}$.
2. Recommend Output Conditions
   - Load currents should not exceed 35 mA per output and 70 mA total for the part.
   - Outputs should not be pulled above $V_{CC}$.


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### 8.2.3 Application Curves

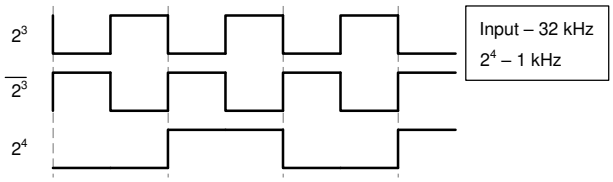



**Figure 8-2. Typical application timing diagram**

## 8.3 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *Section 5.3* table.

Each $V_{CC}$ pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 µF is recommended. If there are multiple $V_{CC}$ pins, 0.01 µF or 0.022 µF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

## 8.4 Layout

### 8.4.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Example Diagram are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or $V_{CC}$, whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

#### 8.4.1.1 Layout Example

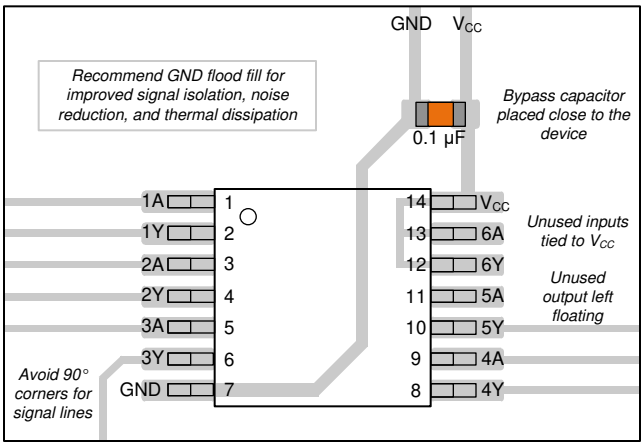



**Figure 8-3. Example Layout for the SN74ACT14**

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# 9 Device and Documentation Support

## 9.1 Documentation Support

### 9.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 9-1. Related Links**

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| SN54ACT14 | Click here | Click here | Click here | Click here | Click here |
| SN74ACT14 | Click here | Click here | Click here | Click here | Click here |

## 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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## 9.4 Trademarks

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## 9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 9.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

# 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision J (August 2024) to Revision K (November 2024)** — **Page**

- Added BQA package to *Device Information* table, *Pin Configuration and Functions* section, and *Thermal Information* table ..... 1
- Added J, W, and FK packages to *Device Information* table ..... 1

**Changes from Revision I (January 2023) to Revision J (August 2024)** — **Page**

- Added package size to *Device Information* table ..... 1
- Updated RθJA values: D = 86 to 89.9, PW = 113 to 148, all values in °C/W ..... 5
- Updated *Layout Example* ..... 11


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## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| 5962-9218301M2A | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9218301M2A SNJ54ACT 14FK |
| 5962-9218301MCA | NRND | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9218301MCA SNJ54ACT14J |
| 5962-9218301MDA | Active | Production | CFP (W) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9218301MDA SNJ54ACT14W |
| SN74ACT14BQAR | Active | Production | WQFN (BQA) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AD14 |
| SN74ACT14BQAR.A | Active | Production | WQFN (BQA) \| 14 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AD14 |
| SN74ACT14D | Obsolete | Production | SOIC (D) \| 14 | - | - | Call TI | Call TI | -40 to 85 | ACT14 |
| SN74ACT14DBR | Active | Production | SSOP (DB) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AD14 |
| SN74ACT14DBR.A | Active | Production | SSOP (DB) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AD14 |
| SN74ACT14DR | Active | Production | SOIC (D) \| 14 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ACT14 |
| SN74ACT14DR.A | Active | Production | SOIC (D) \| 14 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ACT14 |
| SN74ACT14N | NRND | Production | PDIP (N) \| 14 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 85 | SN74ACT14N |
| SN74ACT14N.A | NRND | Production | PDIP (N) \| 14 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 85 | SN74ACT14N |
| SN74ACT14NSR | NRND | Production | SOP (NS) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ACT14 |
| SN74ACT14NSR.A | NRND | Production | SOP (NS) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ACT14 |
| SN74ACT14NSRG4 | NRND | Production | SOP (NS) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ACT14 |
| SN74ACT14PW | Obsolete | Production | TSSOP (PW) \| 14 | - | - | Call TI | Call TI | -40 to 85 | AD14 |
| SN74ACT14PWR | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 85 | AD14 |
| SN74ACT14PWR.A | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AD14 |
| SN74ACT14PWR1G4 | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AD14 |
| SN74ACT14PWR1G4.A | Active | Production | TSSOP (PW) \| 14 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AD14 |
| SNJ54ACT14FK | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9218301M2A SNJ54ACT 14FK |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| SNJ54ACT14FK.A | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9218301M2A SNJ54ACT 14FK |
| SNJ54ACT14J | NRND | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9218301MCA SNJ54ACT14J |
| SNJ54ACT14J.A | NRND | Production | CDIP (J) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9218301MCA SNJ54ACT14J |
| SNJ54ACT14W | Active | Production | CFP (W) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9218301MDA SNJ54ACT14W |
| SNJ54ACT14W.A | Active | Production | CFP (W) \| 14 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9218301MDA SNJ54ACT14W |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54ACT14, SN74ACT14 :**

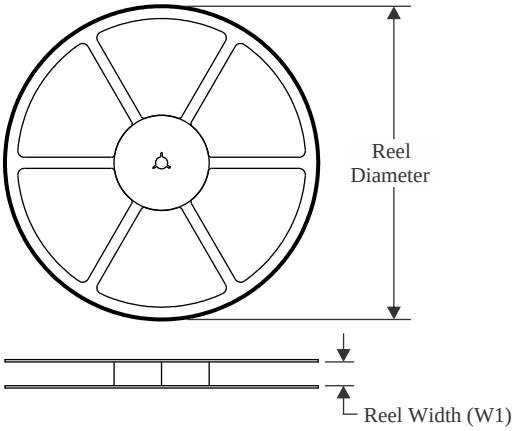
- Catalog : SN74ACT14
- Automotive : SN74ACT14-Q1, SN74ACT14-Q1
- Military : SN54ACT14

NOTE: Qualified Version Definitions:

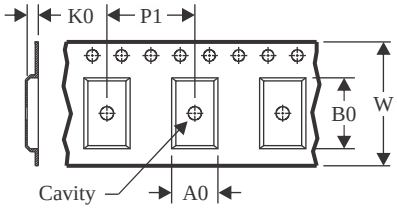
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

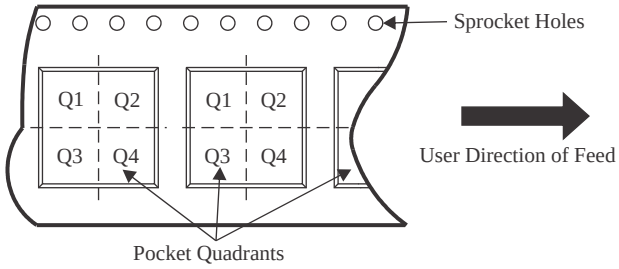



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

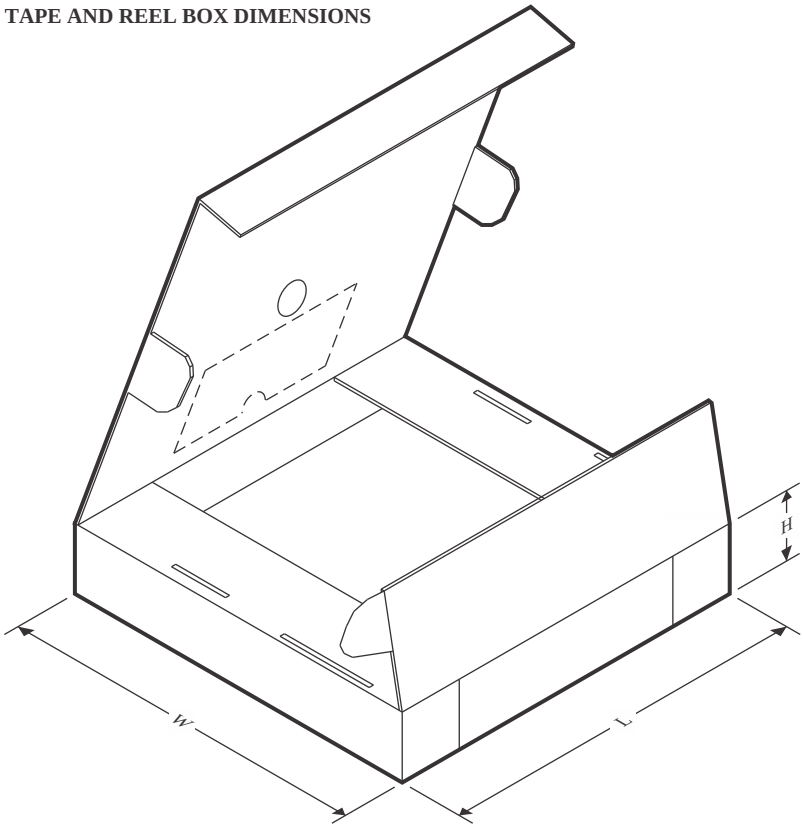
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74ACT14BQAR | WQFN | BQA | 14 | 3000 | 180.0 | 12.4 | 2.8 | 3.3 | 1.1 | 4.0 | 12.0 | Q1 |
| SN74ACT14DBR | SSOP | DB | 14 | 2000 | 330.0 | 16.4 | 8.35 | 6.6 | 2.4 | 12.0 | 16.0 | Q1 |
| SN74ACT14DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74ACT14DR | SOIC | D | 14 | 2500 | 330.0 | 12.4 | 3.75 | 3.75 | 1.15 | 8.0 | 12.0 | Q1 |
| SN74ACT14NSR | SOP | NS | 14 | 2000 | 330.0 | 16.4 | 8.1 | 10.4 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74ACT14PWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74ACT14PWR1G4 | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

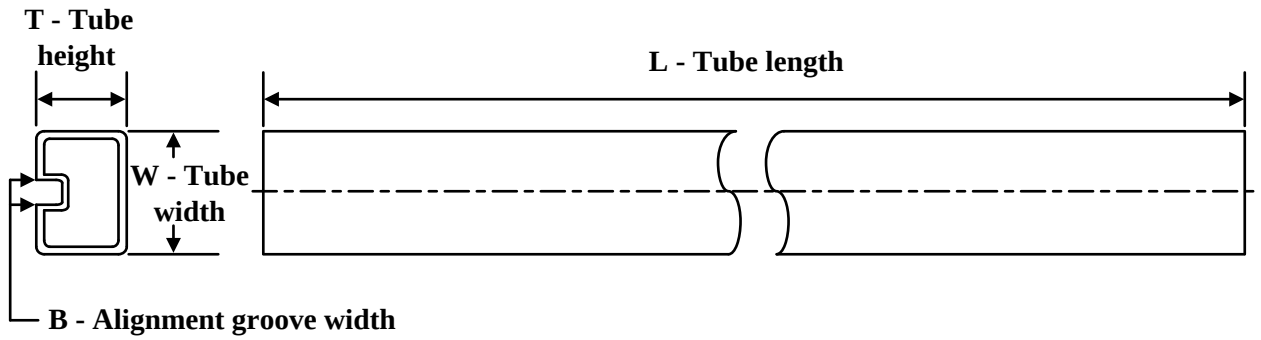
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74ACT14BQAR | WQFN | BQA | 14 | 3000 | 210.0 | 185.0 | 35.0 |
| SN74ACT14DBR | SSOP | DB | 14 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74ACT14DR | SOIC | D | 14 | 2500 | 353.0 | 353.0 | 32.0 |
| SN74ACT14DR | SOIC | D | 14 | 2500 | 340.5 | 336.1 | 32.0 |
| SN74ACT14NSR | SOP | NS | 14 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74ACT14PWR | TSSOP | PW | 14 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74ACT14PWR1G4 | TSSOP | PW | 14 | 2000 | 353.0 | 353.0 | 32.0 |

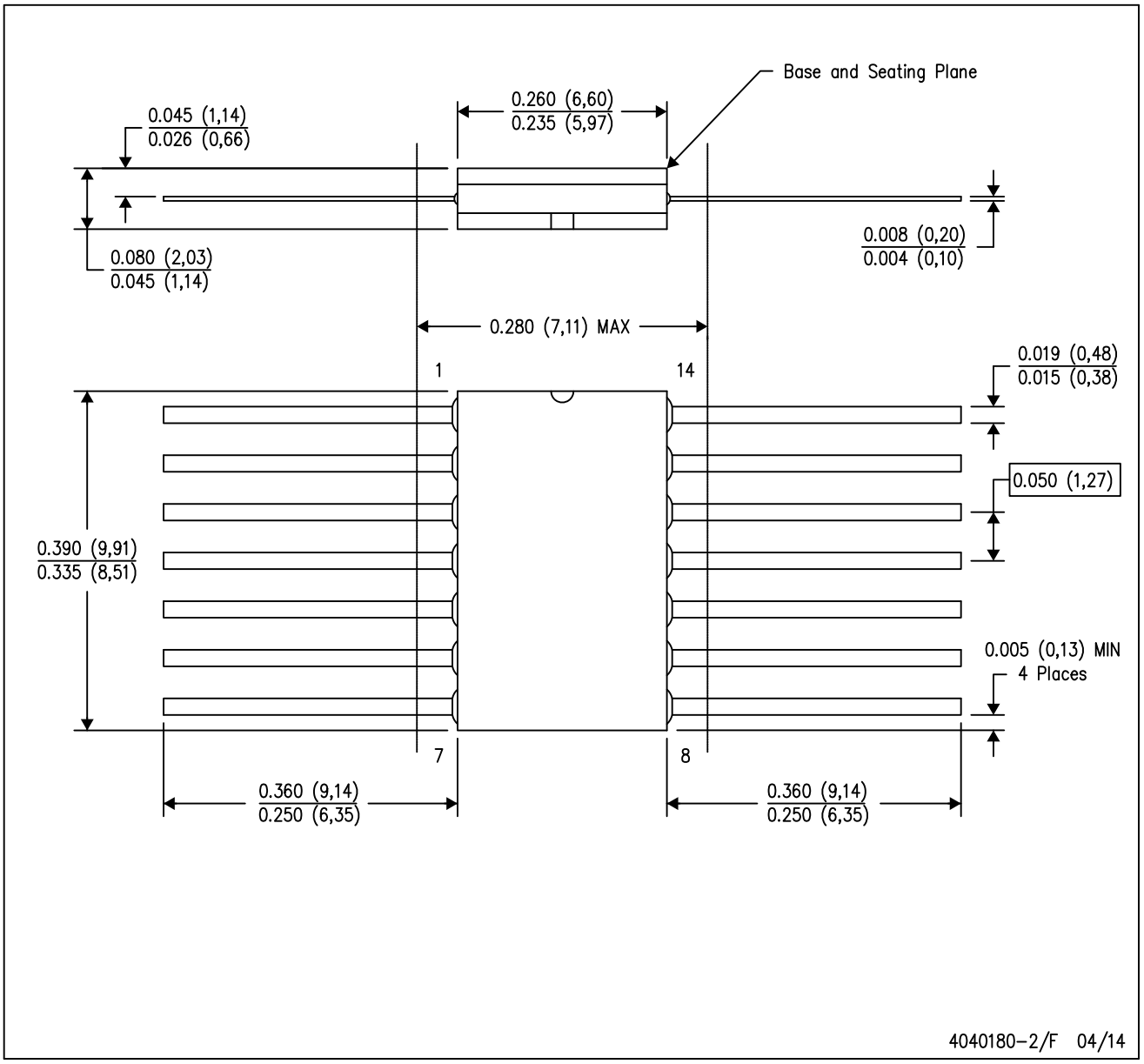
## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| 5962-9218301M2A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| 5962-9218301MDA | W | CFP | 14 | 25 | 506.98 | 26.16 | 6220 | NA |
| SN74ACT14N | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74ACT14N | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74ACT14N.A | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74ACT14N.A | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SNJ54ACT14FK | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SNJ54ACT14FK.A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SNJ54ACT14W | W | CFP | 14 | 25 | 506.98 | 26.16 | 6220 | NA |
| SNJ54ACT14W.A | W | CFP | 14 | 25 | 506.98 | 26.16 | 6220 | NA |

W (R–GDFP–F14) CERAMIC DUAL FLATPACK




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14

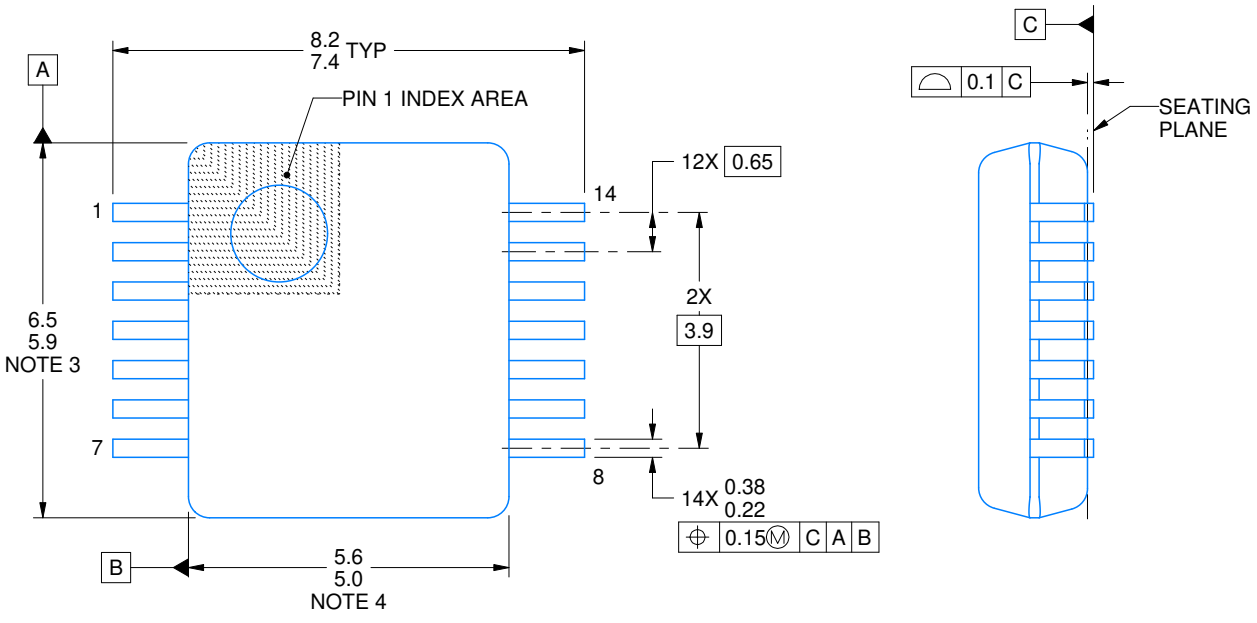
# DB0014A

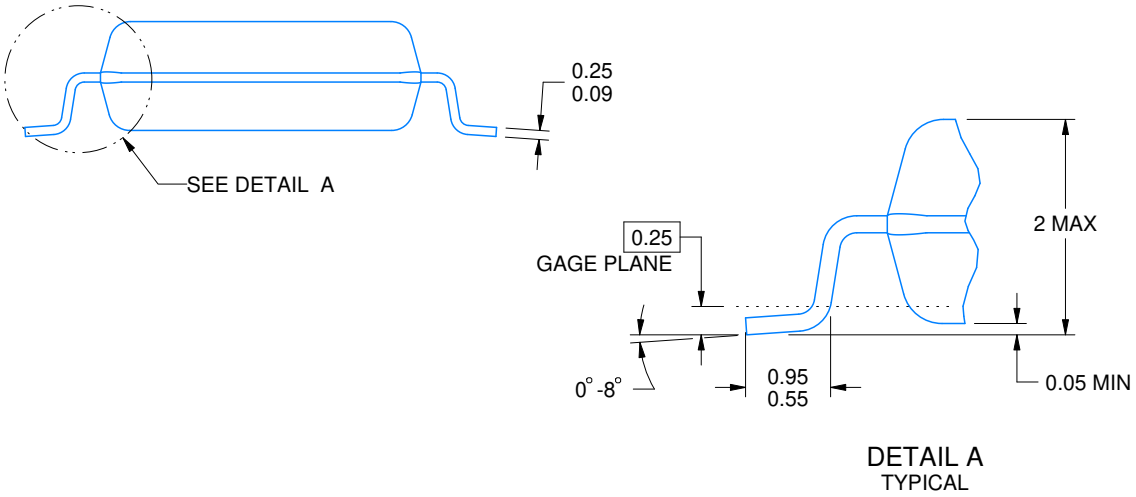


# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



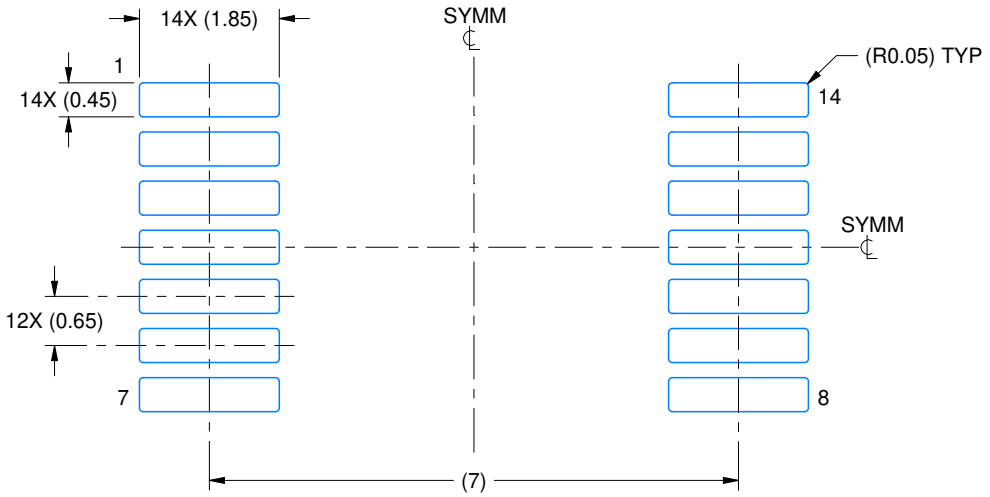




DETAIL A
TYPICAL

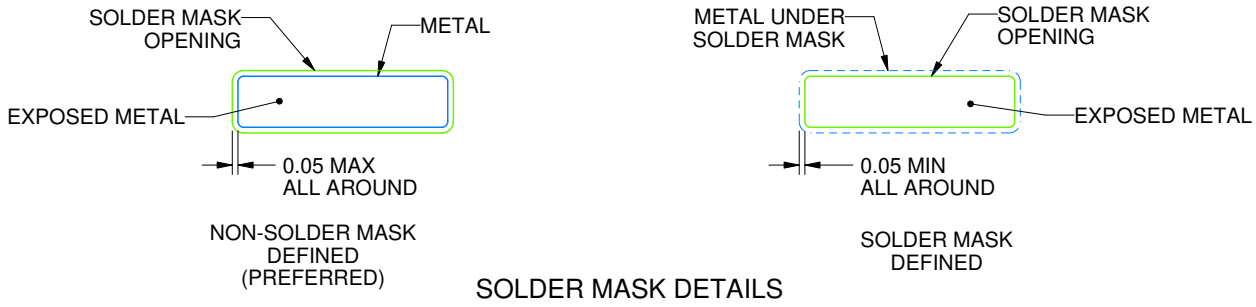
4220762/A 05/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X




SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

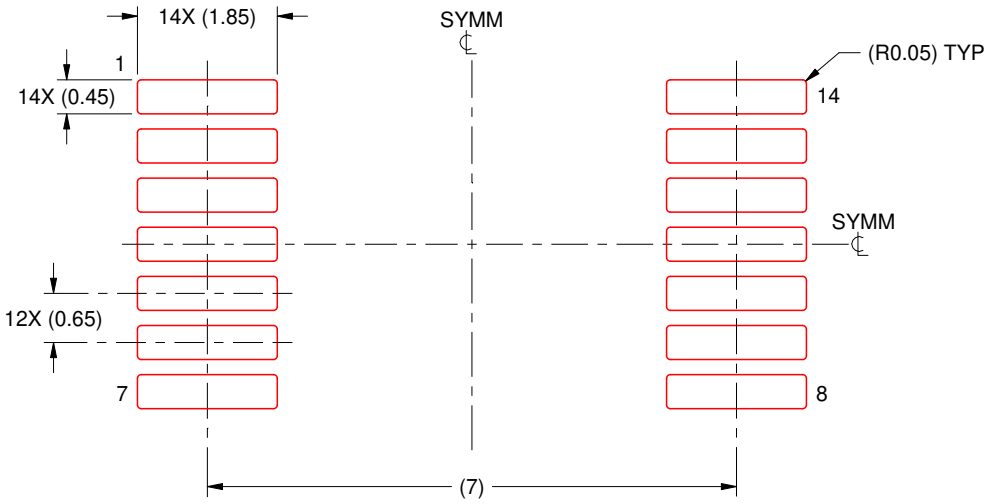
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## DB0014A

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

# GENERIC PACKAGE VIEW

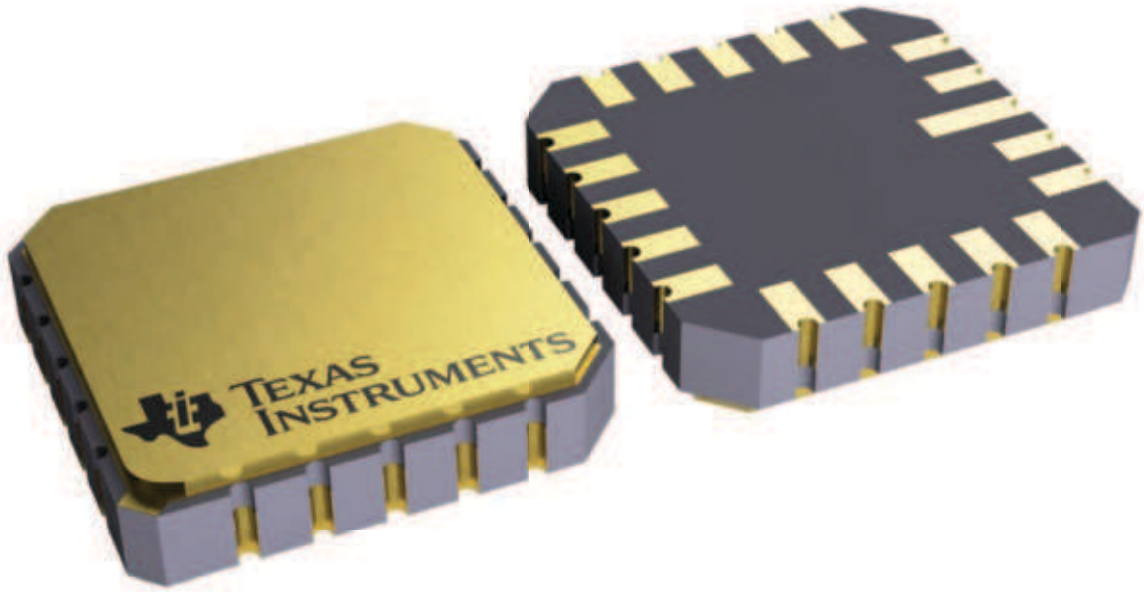
## FK 20

## LCCC - 2.03 mm max height

**8.89 x 8.89, 1.27 mm pitch**

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



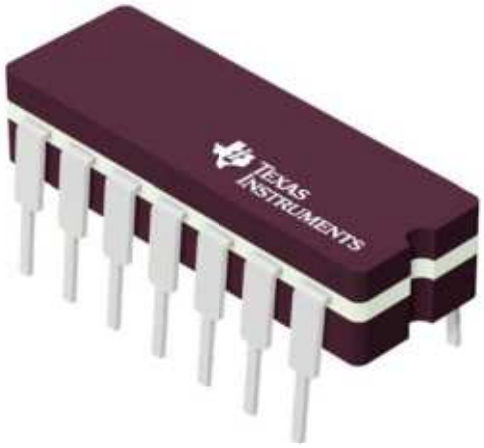

4229370\VA\

# GENERIC PACKAGE VIEW

## J 14

## CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

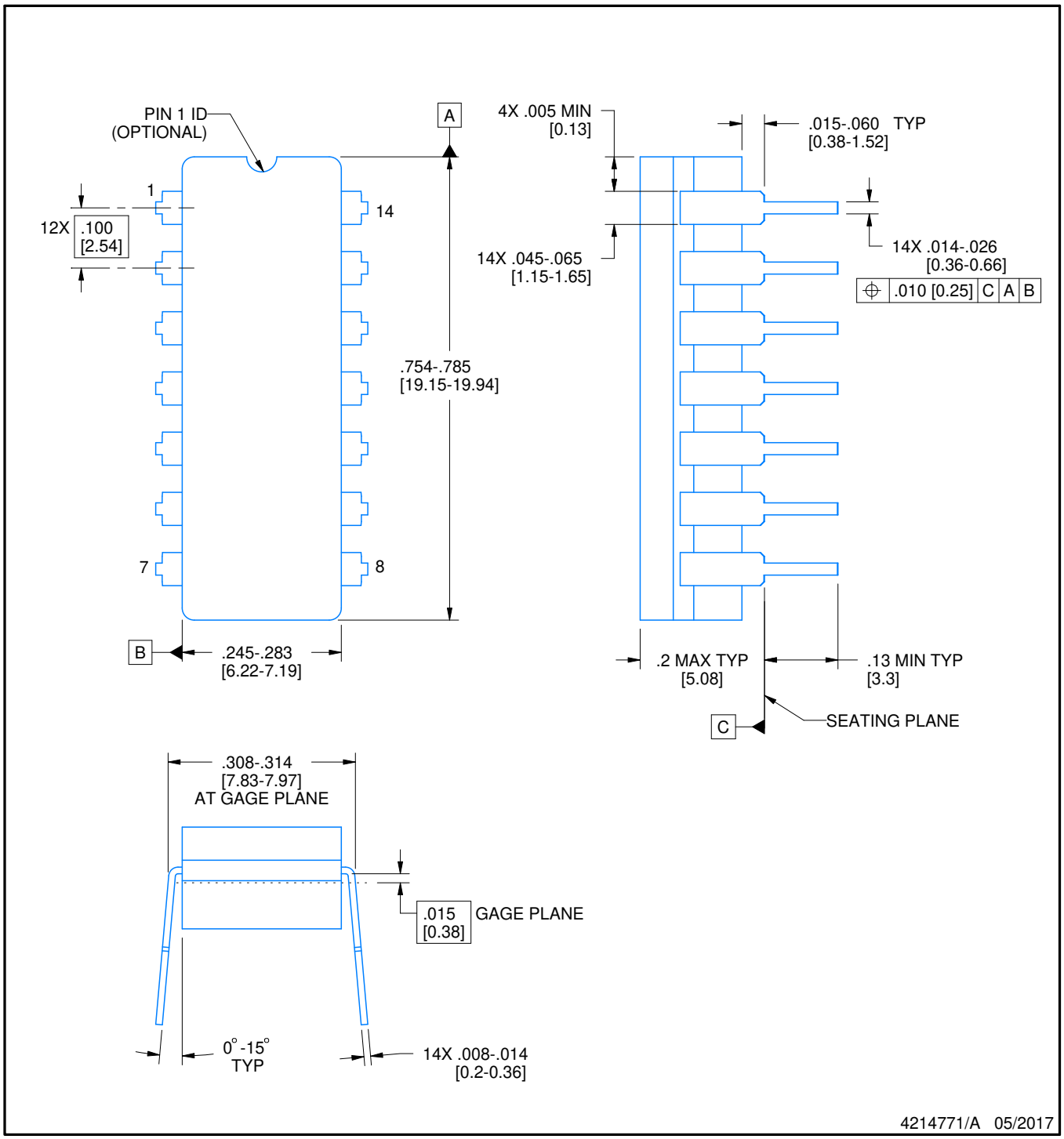


# PACKAGE OUTLINE

## J0014A

## CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE




NOTES:

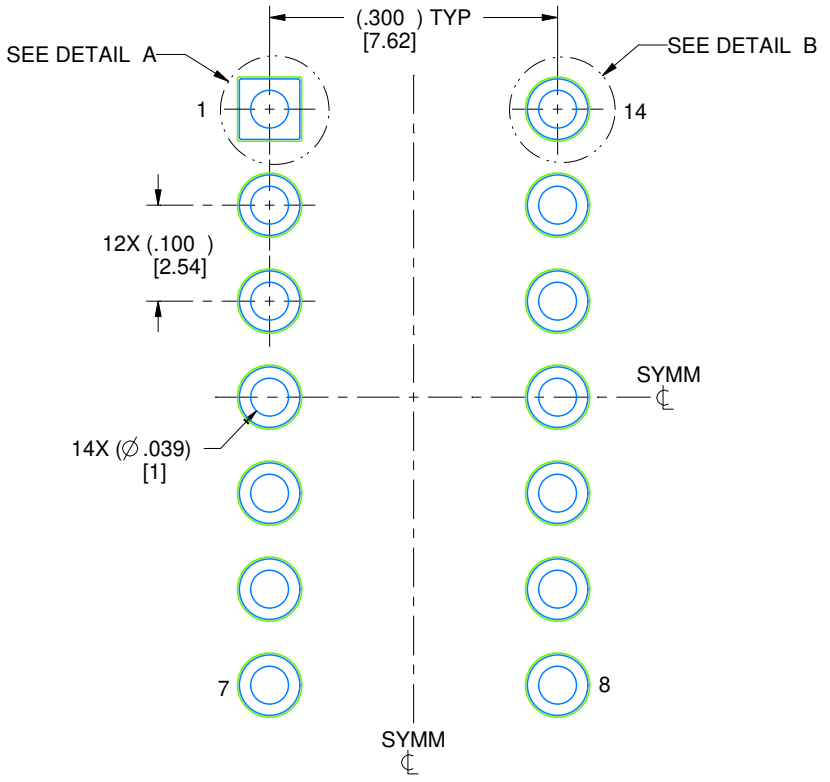
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

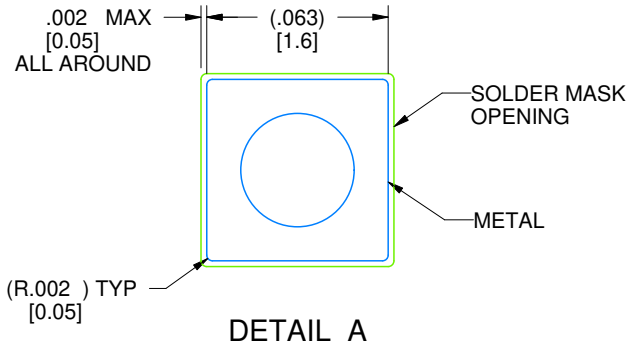
## J0014A

## CDIP - 5.08 mm max height

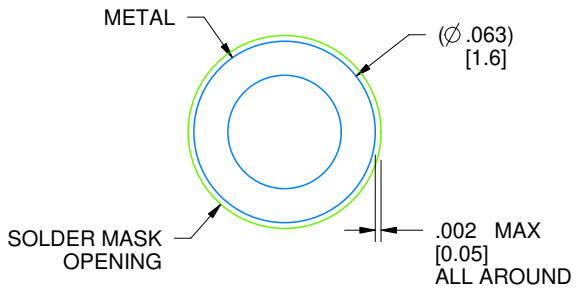
CERAMIC DUAL IN LINE PACKAGE




LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X




DETAIL A
SCALE: 15X



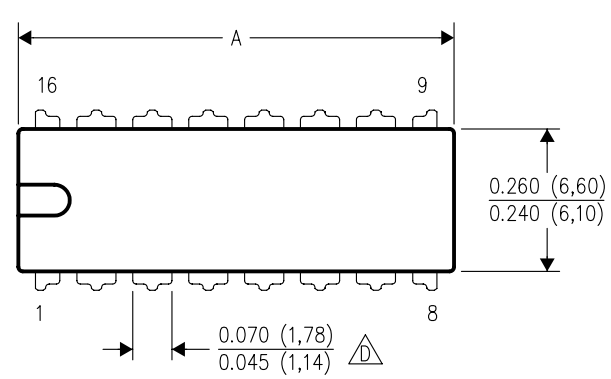

DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

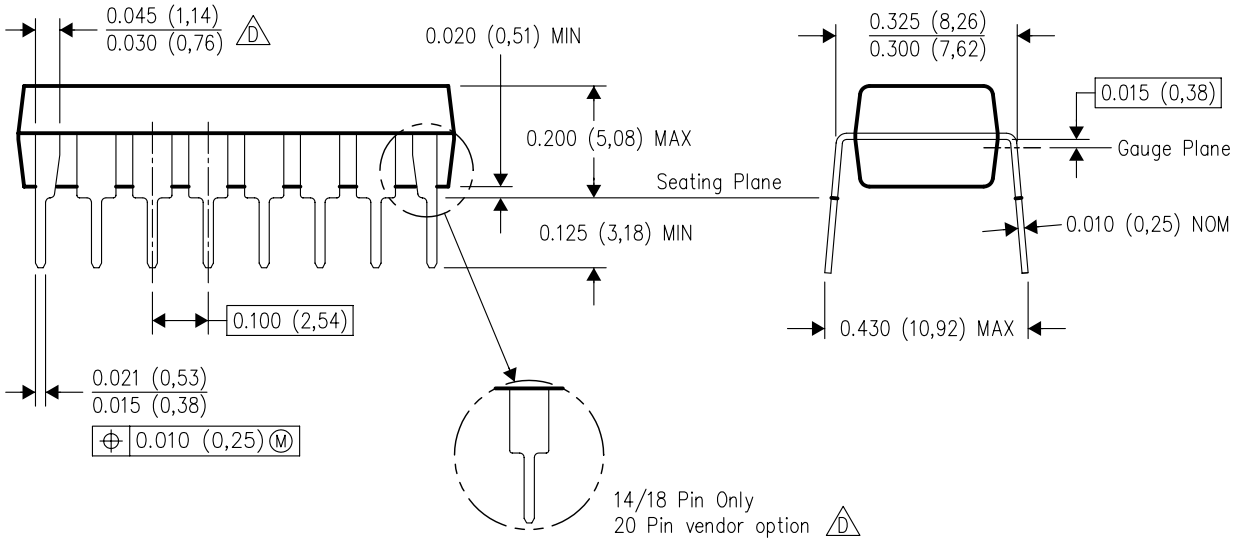
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

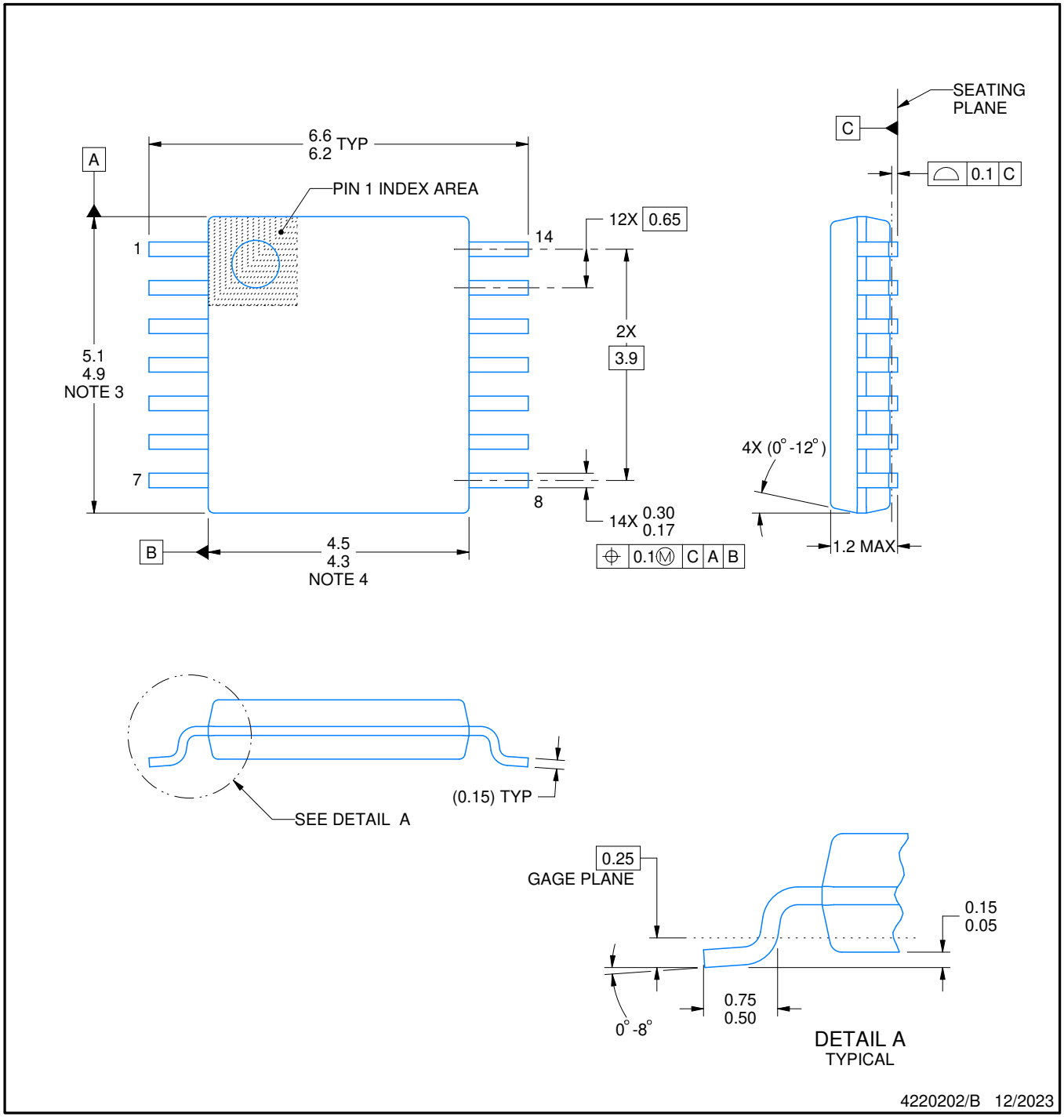
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

# PACKAGE OUTLINE

## PW0014A

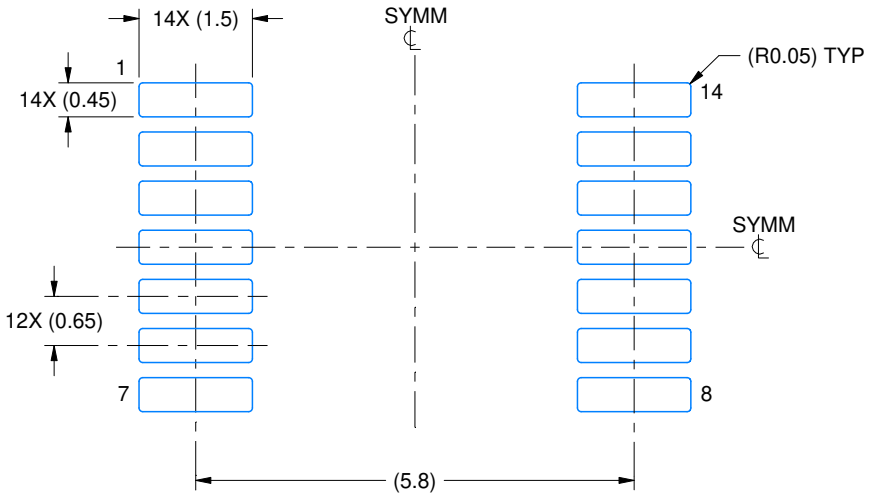
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE




NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X




NON-SOLDER MASK DEFINED (PREFERRED)

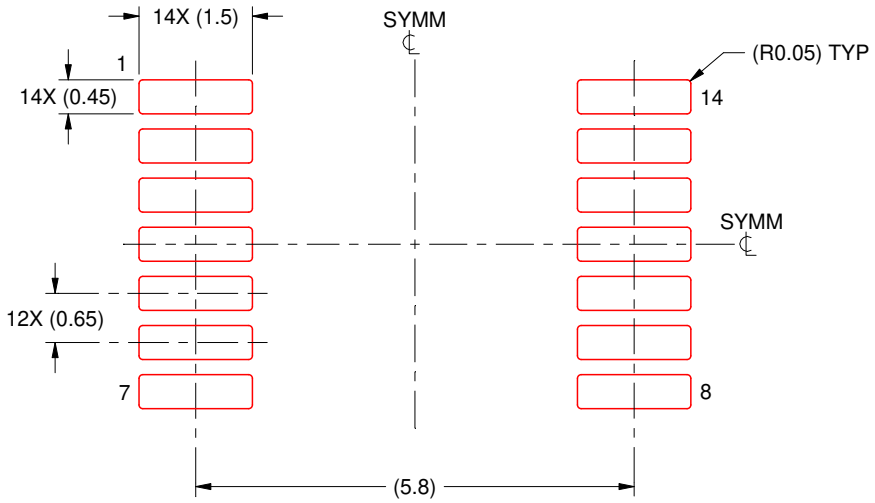
SOLDER MASK DETAILS

SOLDER MASK DEFINED

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

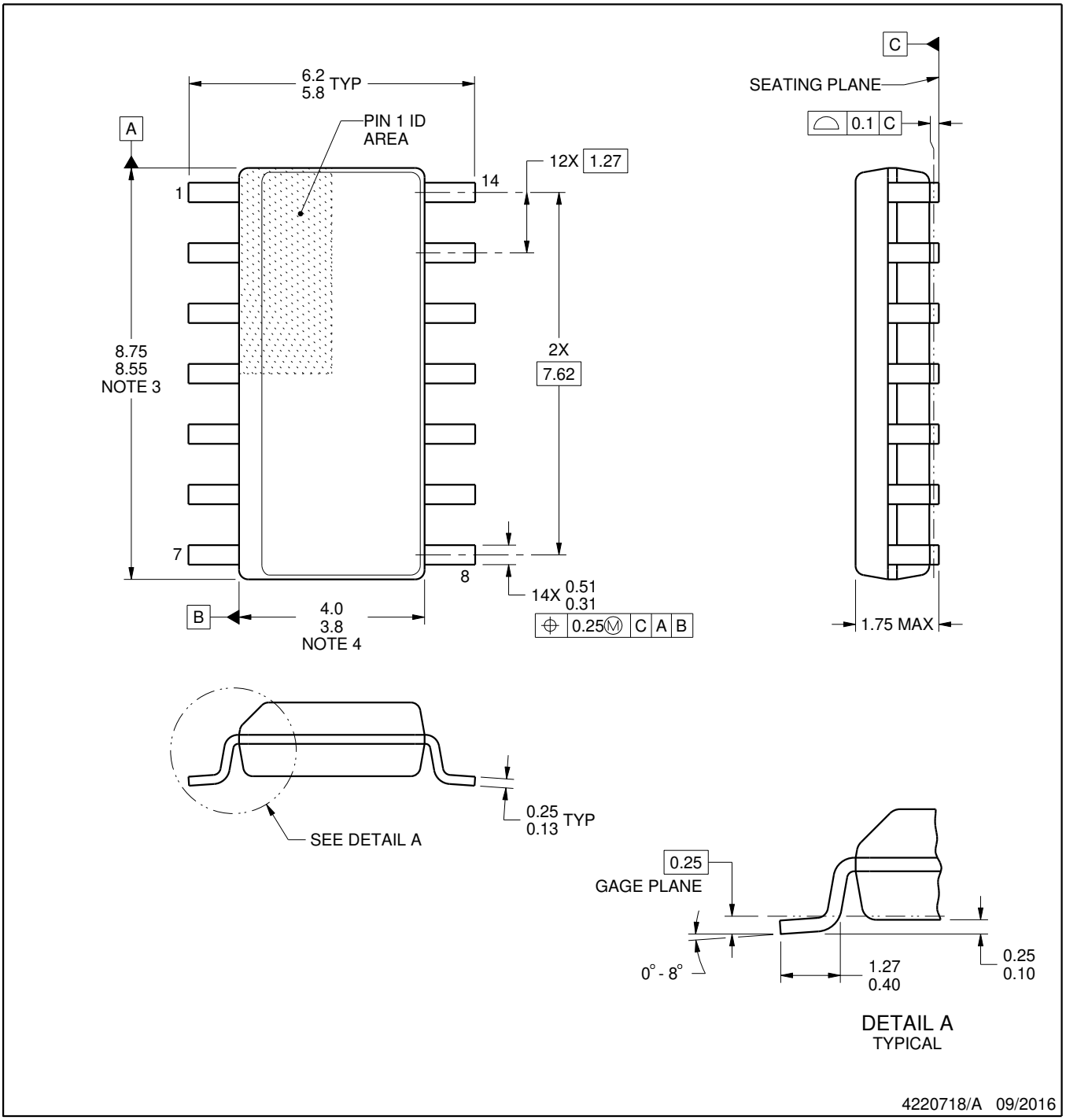


# PACKAGE OUTLINE

## D0014A

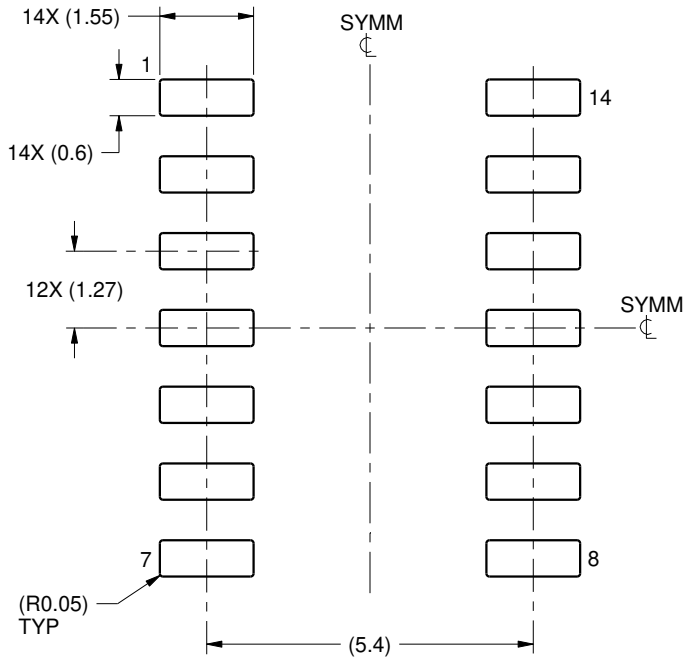
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

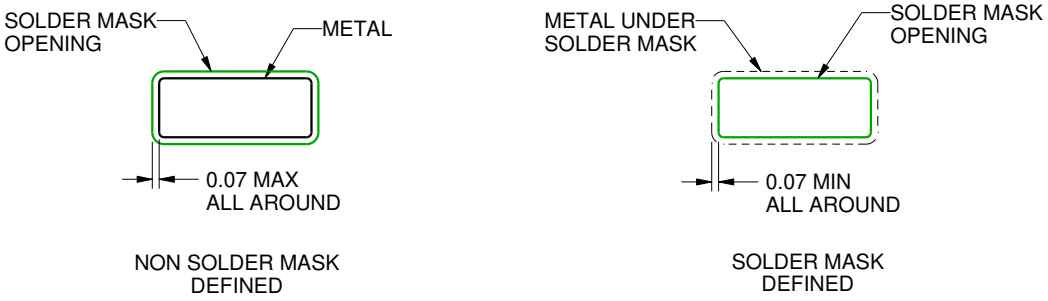



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.




LAND PATTERN EXAMPLE
SCALE:8X




SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

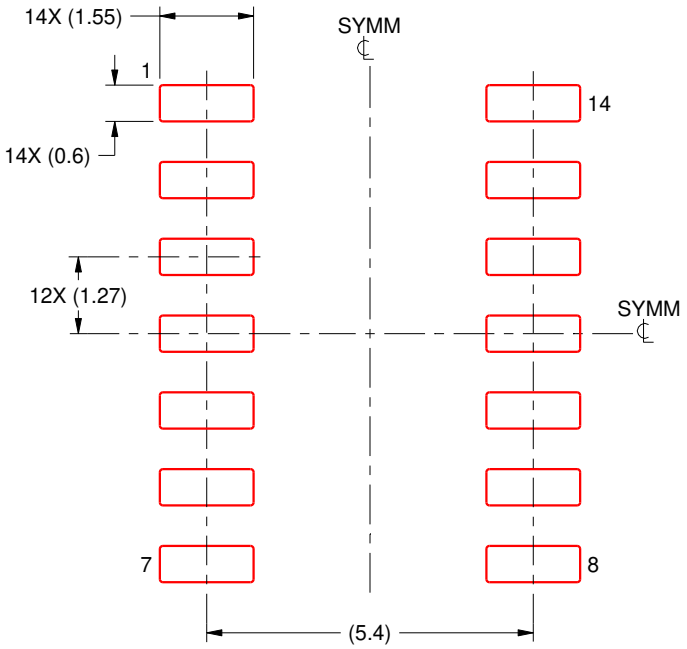
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0014A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# GENERIC PACKAGE VIEW

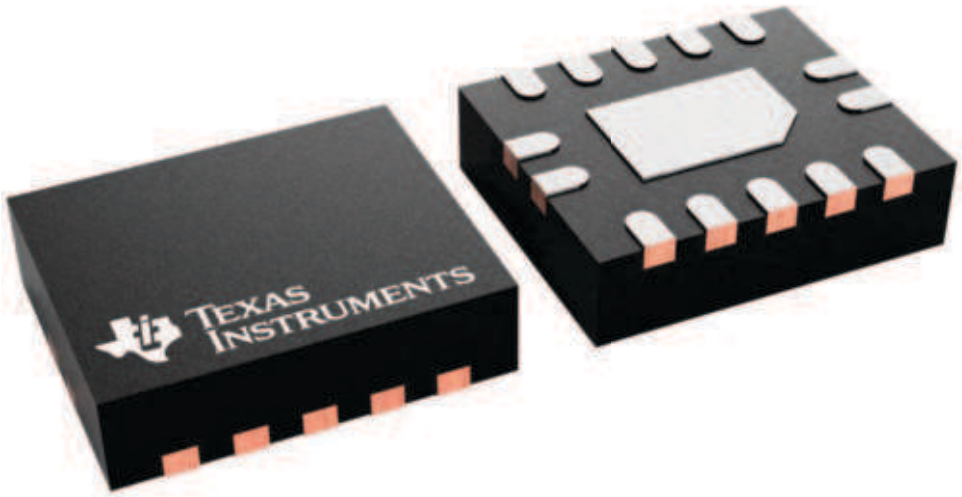
## BQA 14

## WQFN - 0.8 mm max height

**2.5 x 3, 0.5 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



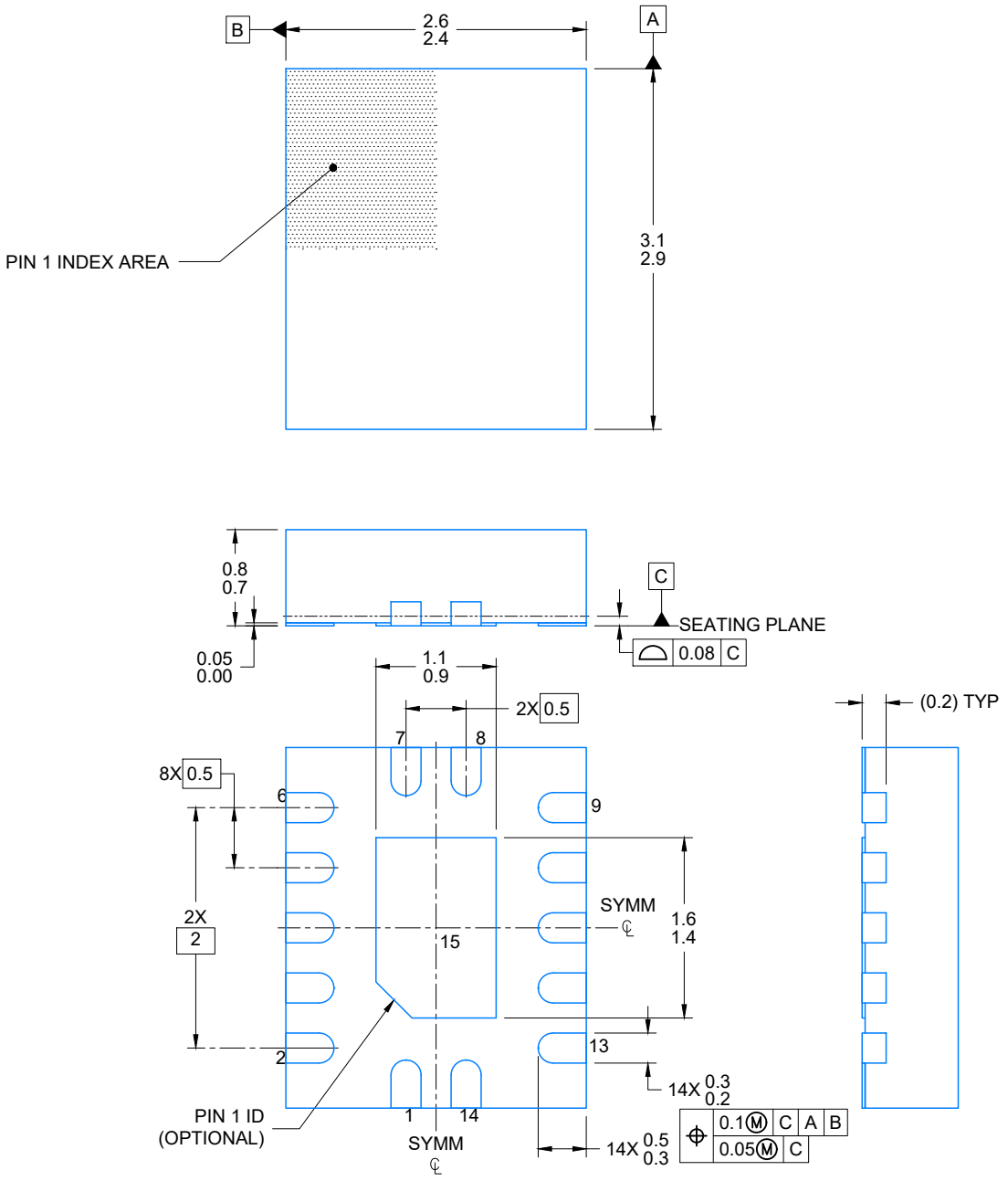

4227145/A

# PACKAGE OUTLINE

## BQA0014A

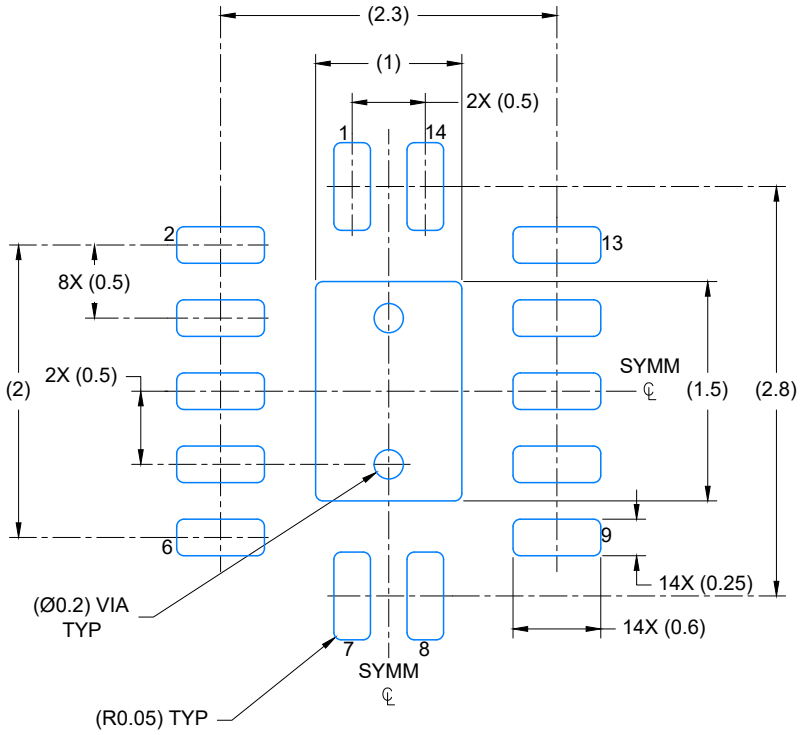
### WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD

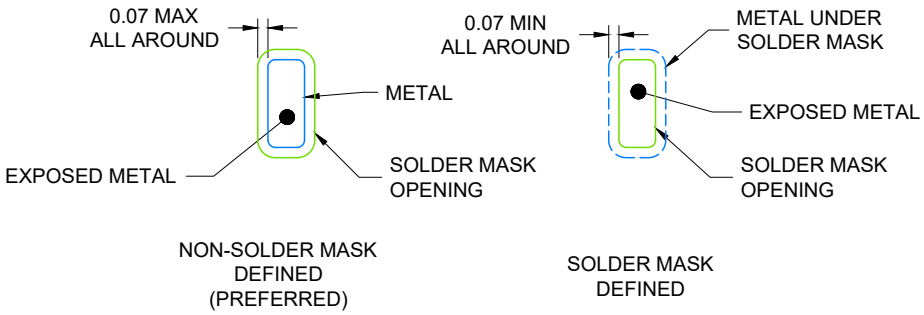



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



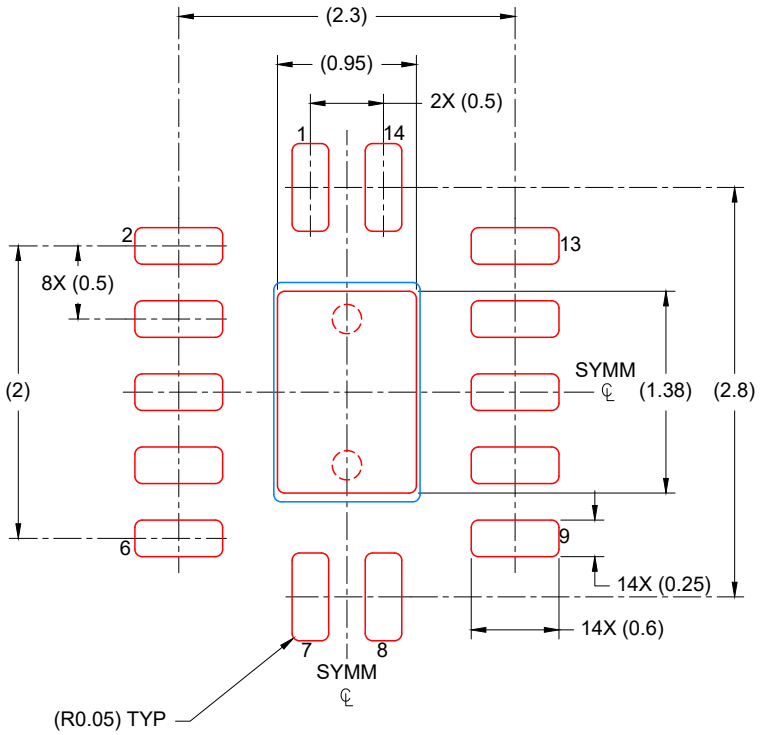

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X




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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
88% PRINTED COVERAGE BY AREA
SCALE: 20X

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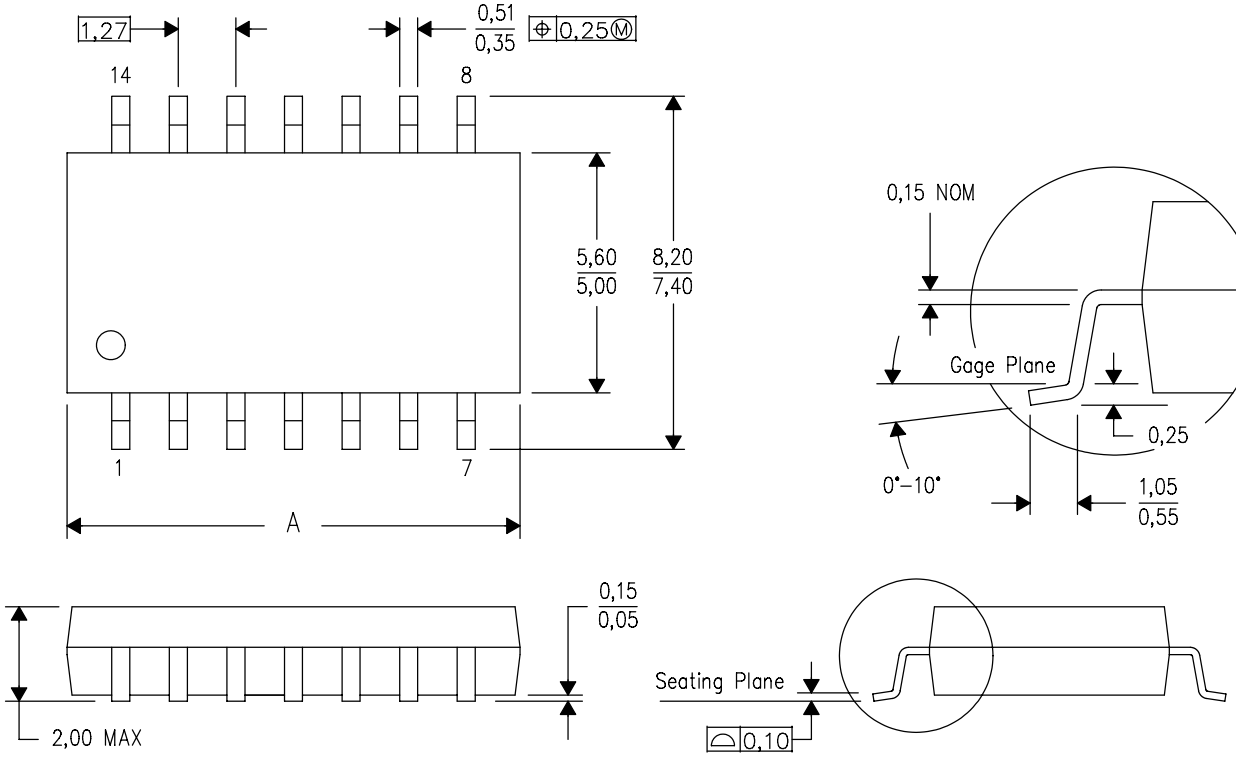
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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