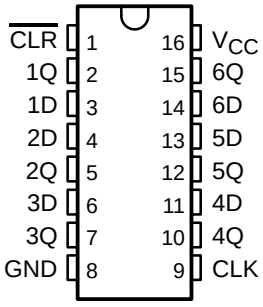
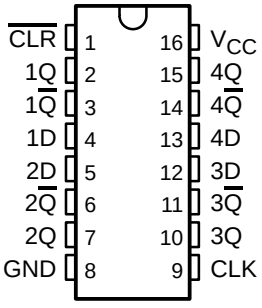
- **'ALS174 and 'AS174 Contain Six Flip-Flops With Single-Rail Outputs**
- **'ALS175 and 'AS175B Contain Four Flip-Flops With Double-Rail Outputs**
- **Buffered Clock and Direct-Clear Inputs**
- **Applications Include:**
  - **Buffer/Storage Registers**
  - **Shift Registers**
  - **Pattern Generators**
- **Fully Buffered Outputs for Maximum Isolation From External Disturbances ('AS Only)**

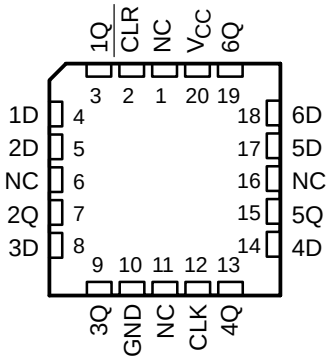
**SN54ALS174 . . . J OR W PACKAGE**
**SN54AS174 . . . J PACKAGE**
**SN74ALS174, SN74AS174 . . . D , N, OR NS PACKAGE**
**(TOP VIEW)**



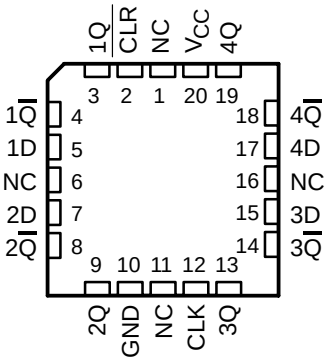

**SN54ALS175 . . . J OR W PACKAGE**
**SN54AS175B . . . J PACKAGE**
**SN74ALS175, SN74AS175B . . . D, N, OR NS PACKAGE**
**(TOP VIEW)**




**SN54ALS174, SN54AS174 . . . FK PACKAGE**
**(TOP VIEW)**




**SN54ALS175 . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

These positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct-clear ($\overline{CLR}$) input. The 'ALS175 and 'AS175B feature complementary outputs from each flip-flop.

Information at the data (D) inputs meeting the setup-time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock (CLK) input is at either the high or low level, the D-input signal has no effect at the output.

These circuits are fully compatible for use with most TTL circuits.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.**

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**On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.**

## ORDERING INFORMATION

| $T_A$ | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| 0°C to 70°C | PDIP – N | Tube | SN74ALS174N | SN74ALS174N |
| | | | SN74AS174N | SN74AS174N |
| | | | SN74ALS175N | SN74ALS175N |
| | | | SN74AS175BN | SN74AS175BN |
| | SOIC – D | Tube | SN74ALS174D | ALS174 |
| | | Tape and reel | SN74ALS174DR | |
| | | Tube | SN74AS174D | AS174 |
| | | Tape and reel | SN74AS174DR | |
| | | Tube | SN74ALS175D | ALS175 |
| | | Tape and reel | SN74ALS175DR | |
| | | Tube | SN74AS175BD | AS175B |
| | | Tape and reel | SN74AS175BDR | |
| | SOP – NS | Tape and reel | SN74ALS174NSR | ALS174 |
| | | | SN74AS174NSR | 74AS174 |
| | | | SN74ALS175NSR | ALS175 |
| | | | SN74AS175BNSR | 74AS175B |
| –55°C to 125°C | CDIP – J | Tube | SNJ54ALS174J | SNJ54ALS174J |
| | | | SNJ54AS174J | SNJ54AS174J |
| | | | SNJ54ALS175J | SNJ54ALS175J |
| | | | SNJ54AS175BJ | SNJ54AS175BJ |
| | CFP – W | Tube | SNJ54ALS174W | SNJ54ALS174W |
| | | | SNJ54ALS175W | SNJ54ALS175W |
| | LCCC – FK | Tube | SNJ54ALS174FK | SNJ54ALS174FK |
| | | | SNJ54AS174FK‡ | SNJ54AS174FK |
| | | | SNJ54ALS175FK | SNJ54ALS175FK |

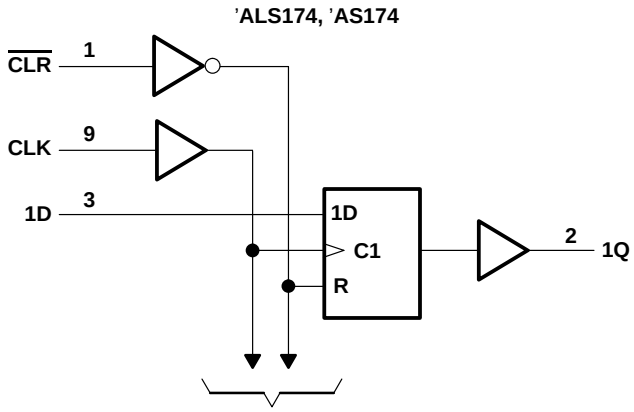
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
‡ This orderable is not recommended for new designs.

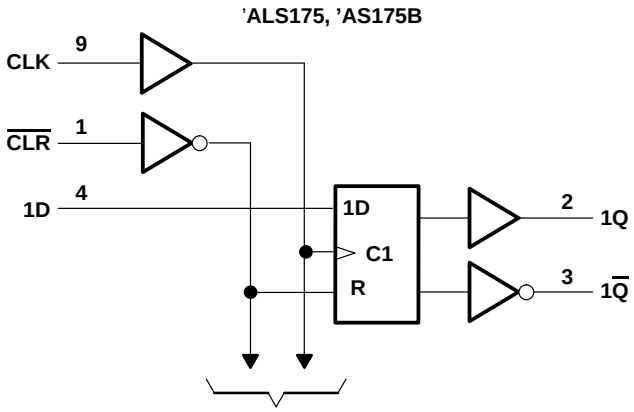
**FUNCTION TABLE**
**(each flip-flop)**

| INPUTS | | | OUTPUTS | |
|---|---|---|---|---|
| $\overline{CLR}$ | CLK | D | Q | $\overline{Q}$§ |
| L | X | X | L | H |
| H | ↑ | H | H | L |
| H | ↑ | L | L | H |
| H | L | X | $Q_0$ | $\overline{Q}_0$ |

§ 'ALS175 and 'AS175B only

## logic diagrams (positive logic)




Pin numbers shown are for the D, J, N, NS, and W packages.

## absolute maximum ratings over operating free-air temperature range, SN54/74ALS174, SN54/74ALS175 (unless otherwise noted)†

Supply voltage, $V_{CC}$ . . . . . 7 V
Input voltage, $V_I$ . . . . . 7 V
Package thermal impedance, $\theta_{JA}$ (see Note 1): D package . . . . . 73°C/W
N package . . . . . 67°C/W
NS package . . . . . 64°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 2)

| | | SN54ALS174 SN54ALS175 | | | SN74ALS174 SN74ALS175 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| $I_{OH}$ | High-level output current | | | –0.4 | | | –0.4 | mA |
| $I_{OL}$ | Low-level output current | | | 4 | | | 8 | mA |
| $T_A$ | Operating free-air temperature | –55 | | 125 | 0 | | 70 | °C |

NOTE 2: All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | SN54ALS174 SN54ALS175 | | | SN74ALS174 SN74ALS175 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = –18 mA | | | –1.5 | | | –1.5 | V |
| $V_{OH}$ | | $V_{CC}$ = 4.5 V to 5.5 V, | $I_{OH}$ = –0.4 mA | $V_{CC}$–2 | | | $V_{CC}$–2 | | | V |
| $V_{OL}$ | | $V_{CC}$ = 4.5 V | $I_{OL}$ = 4 mA | | 0.25 | 0.4 | | 0.25 | 0.4 | V |
| | | | $I_{OL}$ = 8 mA | | | | | 0.35 | 0.5 | |
| $I_I$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | | | 20 | µA |
| $I_{IL}$ | All others | $V_{CC}$ = 5.5 V, | $V_I$ = 0.4 V | | | –0.1 | | | –0.1 | mA |
| | CLK | | | | | –0.15 | | | | |
| $I_O$‡ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.25 V | –20 | | –112 | –30 | | –112 | mA |
| $I_{CC}$ | ’ALS174 | $V_{CC}$ = 5.5 V, | See Note 3 | | 11 | 19 | | 11 | 19 | mA |
| | ’ALS175 | | | | 8 | 14 | | 9 | 14 | |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, $I_{OS}$.
NOTE 3: $I_{CC}$ is measured with D inputs and $\overline{CLR}$ grounded, and CLK at 4.5 V.

## timing requirements over recommended operating free-air temperature range (unless otherwise noted)

| | | | SN54ALS174 SN54ALS175 | | SN74ALS174 SN74ALS175 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | | | 40 | | 50 | MHz |
| $t_w$ | Pulse duration | $\overline{CLR}$ low | 15 | | 10 | | ns |
| | | CLK high | 12.5 | | 10 | | |
| | | CLK low | 12.5 | | 10 | | |
| $t_{su}$ | Setup time before CLK↑ | Data | 15 | | 10 | | ns |
| | | $\overline{CLR}$ inactive | 8 | | 6 | | |
| $t_h$ | Hold time, data after CLK↑ | | 0 | | 0 | | ns |

## switching characteristics (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX§ | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | SN54ALS174 SN54ALS175 | | SN74ALS174 SN74ALS175 | | |
| | | | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | 40 | | 50 | | MHz |
| $t_{PLH}$ | $\overline{CLR}$ | Any Q (or $\overline{Q}$, ’ALS175) | 3 | 20 | 5 | 18 | ns |
| $t_{PHL}$ | | | 5 | 30 | 8 | 23 | |
| $t_{PLH}$ | CLK | Any Q (or $\overline{Q}$, ’ALS175) | 3 | 20 | 3 | 15 | ns |
| $t_{PHL}$ | | | 5 | 24 | 5 | 17 | |

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

### absolute maximum ratings over operating free-air temperature range, SN54/74AS174, SN54/74AS175B (unless otherwise noted)†

Supply voltage, $V_{CC}$ . . . . . 7 V
Input voltage, $V_I$ . . . . . 7 V
Package thermal impedance, $\theta_{JA}$ (see Note 1): D package . . . . . 73°C/W
N package . . . . . 67°C/W
NS package . . . . . 64°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

### recommended operating conditions (see Note 2)

| | | SN54AS174 SN54AS175B | | | SN74AS174 SN74AS175B | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| $I_{OH}$ | High-level output current | | | –2 | | | –2 | mA |
| $I_{OL}$ | Low-level output current | | | 20 | | | 20 | mA |
| $T_A$ | Operating free-air temperature | –55 | | 125 | 0 | | 70 | °C |

NOTE 2: All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | SN54AS174 SN54AS175B | | | SN74AS174 SN74AS175B | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = –18 mA | | | –1.2 | | | –1.2 | V |
| $V_{OH}$ | | $V_{CC}$ = 4.5 V to 5.5 V, | $I_{OH}$ = –2 mA | $V_{CC}$–2 | | | $V_{CC}$–2 | | | V |
| $V_{OL}$ | | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 20 mA | | 0.35 | 0.5 | | 0.35 | 0.5 | V |
| $I_I$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | | | 20 | µA |
| $I_{IL}$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 0.4 V | | | –0.5 | | | –0.5 | mA |
| $I_O$§ | | $V_{CC}$ = 5.5 V, | $V_O$ = 2.25 V | –30 | | –112 | –30 | | –112 | mA |
| $I_{CC}$ | 'AS174 | $V_{CC}$ = 5.5 V, | See Note 4 | | 30 | 45 | | 30 | 45 | mA |
| | 'AS175B | | | | 22.5 | 34 | | 22.5 | 34 | |

‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

§ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, $I_{OS}$.

NOTE 4: $I_{CC}$ is measured with D inputs, $\overline{CLR}$, and CLK grounded.

### timing requirements over recommended operating free-air temperature range (unless otherwise noted)

| | | | | SN54AS174 SN54AS175B | | SN74AS174 SN74AS175B | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | |
| $f_{clock}$* | Clock frequency | | | | 100 | | 100 | MHz |
| $t_w$* | Pulse duration | $\overline{CLR}$ low | | 5.5 | | 5 | | ns |
| | | CLK high | | 4 | | 4 | | |
| | | CLK low | 'AS174 | 6 | | 6 | | |
| | | CLK low | 'AS175B | 5 | | 5 | | |
| $t_{su}$* | Setup time before CLK↑ | Data | 'AS174 | 4 | | 4 | | ns |
| | | | 'AS175B | 3 | | 3 | | |
| | | $\overline{CLR}$ inactive | | 6 | | 6 | | |
| $t_h$* | Hold time, data after CLK↑ | | | 1 | | 1 | | ns |

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data, but is not production tested.

### switching characteristics (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX† | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | SN54AS174 | | SN74AS174 | | |
| | | | MIN | MAX | MIN | MAX | |
| $f_{max}$* | | | 100 | | 100 | | MHz |
| $t_{PHL}$ | $\overline{CLR}$ | Any Q | 5 | 15 | 5 | 14 | ns |
| $t_{PLH}$ | CLK | Any Q | 3.5 | 9.5 | 3.5 | 8 | ns |
| $t_{PHL}$ | | | 4.5 | 11.5 | 4.5 | 10 | |

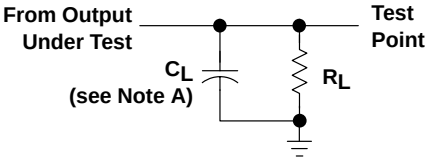
* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data, but is not production tested.
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

### switching characteristics (see Figure 1)

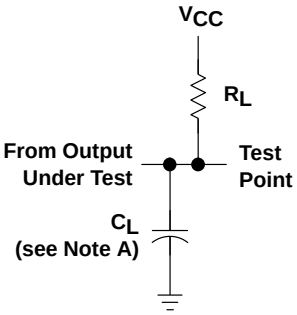
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 4.5 V to 5.5 V, $C_L$ = 50 pF, $R_L$ = 500 Ω, $T_A$ = MIN to MAX† | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | SN54AS175B | | SN74AS175B | | |
| | | | MIN | MAX | MIN | MAX | |
| $f_{max}$* | | | 100 | | 100 | | MHz |
| $t_{PLH}$ | $\overline{CLR}$ | Any Q or $\overline{Q}$ | 4 | 10 | 4 | 9 | ns |
| $t_{PHL}$ | | | 4.5 | 15 | 4.5 | 13 | |
| $t_{PLH}$ | CLK | Any Q or $\overline{Q}$ | 3 | 8.5 | 3 | 7.5 | ns |
| $t_{PHL}$ | | | 3 | 11 | 3 | 10 | |

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data, but is not production tested.
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

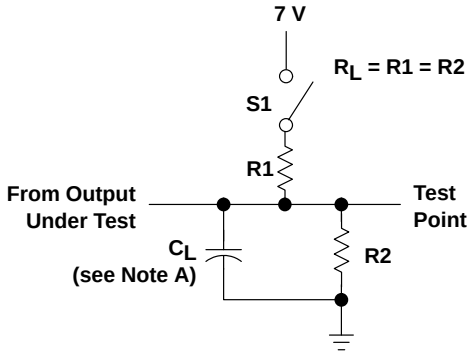
## PARAMETER MEASUREMENT INFORMATION
## SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



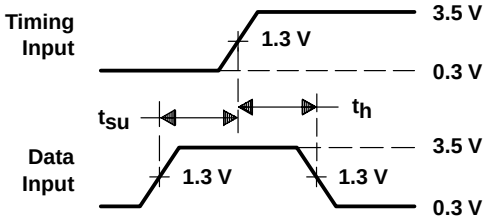

LOAD CIRCUIT FOR
BI-STATE
TOTEM-POLE OUTPUTS



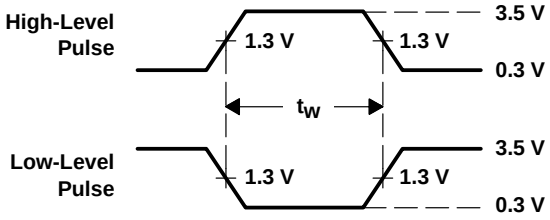

LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS



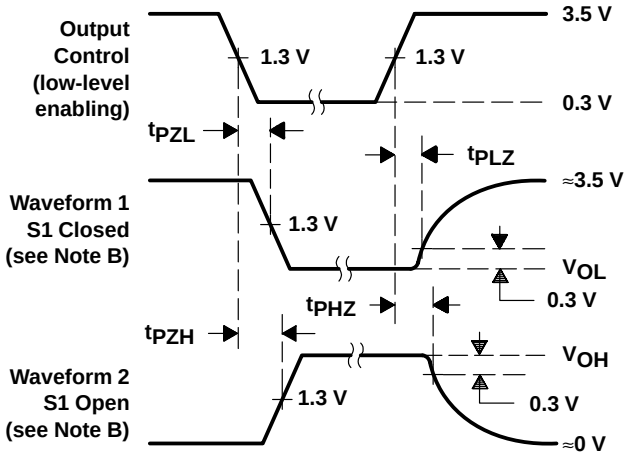

LOAD CIRCUIT
FOR 3-STATE OUTPUTS



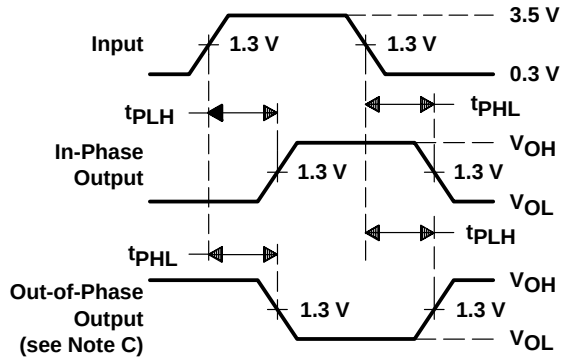

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PULSE DURATIONS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
D. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
E. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuits and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| 5962-9553701QEA | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9553701QE A SNJ54AS175BJ |
| 83019012A | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 83019012A SNJ54ALS 174FK |
| 8301901EA | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 8301901EA SNJ54ALS174J |
| 8301901FA | Active | Production | CFP (W) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 8301901FA SNJ54ALS174W |
| 8301902EA | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 8301902EA SNJ54ALS175J |
| JM38510/37201B2A | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 37201B2A |
| JM38510/37201B2A.A | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 37201B2A |
| JM38510/37201BEA | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 37201BEA |
| JM38510/37201BEA.A | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 37201BEA |
| JM38510/37202B2A | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 37202B2A |
| JM38510/37202B2A.A | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 37202B2A |
| JM38510/37202BEA | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 37202BEA |
| JM38510/37202BEA.A | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 37202BEA |
| M38510/37201B2A | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 37201B2A |
| M38510/37201BEA | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 37201BEA |
| M38510/37202B2A | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 37202B2A |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| M38510/37202BEA | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | JM38510/ 37202BEA |
| SN54ALS174J | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SN54ALS174J |
| SN54ALS174J.A | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SN54ALS174J |
| SN54ALS175J | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SN54ALS175J |
| SN54ALS175J.A | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SN54ALS175J |
| SN74ALS174D | Obsolete | Production | SOIC (D) \| 16 | - | - | Call TI | Call TI | 0 to 70 | ALS174 |
| SN74ALS174DR | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS174 |
| SN74ALS174DR.A | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS174 |
| SN74ALS174N | Active | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN74ALS174N |
| SN74ALS174N.A | Active | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN74ALS174N |
| SN74ALS174NSR | Active | Production | SOP (NS) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS174 |
| SN74ALS174NSR.A | Active | Production | SOP (NS) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS174 |
| SN74ALS175D | Obsolete | Production | SOIC (D) \| 16 | - | - | Call TI | Call TI | 0 to 70 | ALS175 |
| SN74ALS175DR | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS175 |
| SN74ALS175DR.A | Active | Production | SOIC (D) \| 16 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS175 |
| SN74ALS175N | Active | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN74ALS175N |
| SN74ALS175N.A | Active | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN74ALS175N |
| SN74ALS175NSR | Active | Production | SOP (NS) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS175 |
| SN74ALS175NSR.A | Active | Production | SOP (NS) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | ALS175 |
| SN74AS174D | Active | Production | SOIC (D) \| 16 | 40 \| TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | AS174 |
| SN74AS174D.A | Active | Production | SOIC (D) \| 16 | 40 \| TUBE | Yes | NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | AS174 |
| SN74AS174N | Active | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN74AS174N |
| SN74AS174N.A | Active | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN74AS174N |
| SN74AS174NSR | Active | Production | SOP (NS) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74AS174 |
| SN74AS174NSR.A | Active | Production | SOP (NS) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74AS174 |
| SN74AS175BD | Active | Production | SOIC (D) \| 16 | 40 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | AS175B |
| SN74AS175BD.A | Active | Production | SOIC (D) \| 16 | 40 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | AS175B |
| SN74AS175BN | Active | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN74AS175BN |
| SN74AS175BN.A | Active | Production | PDIP (N) \| 16 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN74AS175BN |
| SN74AS175BNSR | Active | Production | SOP (NS) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74AS175B |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| SN74AS175BNSR.A | Active | Production | SOP (NS) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74AS175B |
| SNJ54ALS174FK | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 83019012A SNJ54ALS 174FK |
| SNJ54ALS174FK.A | Active | Production | LCCC (FK) \| 20 | 55 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 83019012A SNJ54ALS 174FK |
| SNJ54ALS174J | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 8301901EA SNJ54ALS174J |
| SNJ54ALS174J.A | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 8301901EA SNJ54ALS174J |
| SNJ54ALS174W | Active | Production | CFP (W) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 8301901FA SNJ54ALS174W |
| SNJ54ALS174W.A | Active | Production | CFP (W) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 8301901FA SNJ54ALS174W |
| SNJ54ALS175J | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 8301902EA SNJ54ALS175J |
| SNJ54ALS175J.A | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 8301902EA SNJ54ALS175J |
| SNJ54AS174J | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SNJ54AS174J |
| SNJ54AS174J.A | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | SNJ54AS174J |
| SNJ54AS175BJ | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9553701QE A SNJ54AS175BJ |
| SNJ54AS175BJ.A | Active | Production | CDIP (J) \| 16 | 25 \| TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-9553701QE A SNJ54AS175BJ |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

**(4) Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**(5) MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54ALS174, SN54ALS175, SN54AS174, SN54AS175B, SN74ALS174, SN74ALS175, SN74AS174, SN74AS175B :**

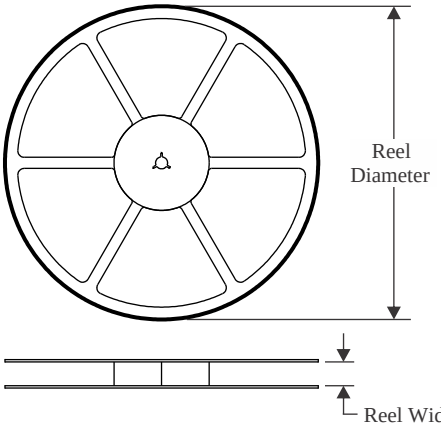
- Catalog : SN74ALS174, SN74ALS175, SN74AS174, SN74AS175B
- Military : SN54ALS174, SN54ALS175, SN54AS174, SN54AS175B

NOTE: Qualified Version Definitions:

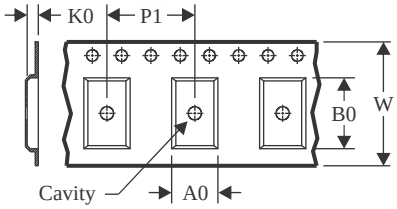
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

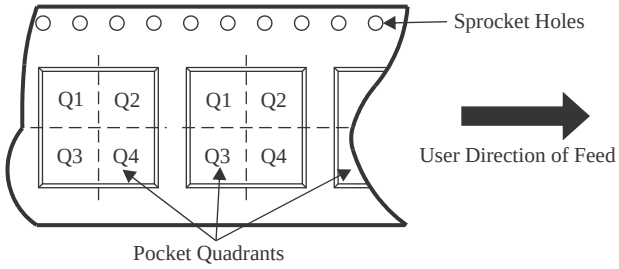



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

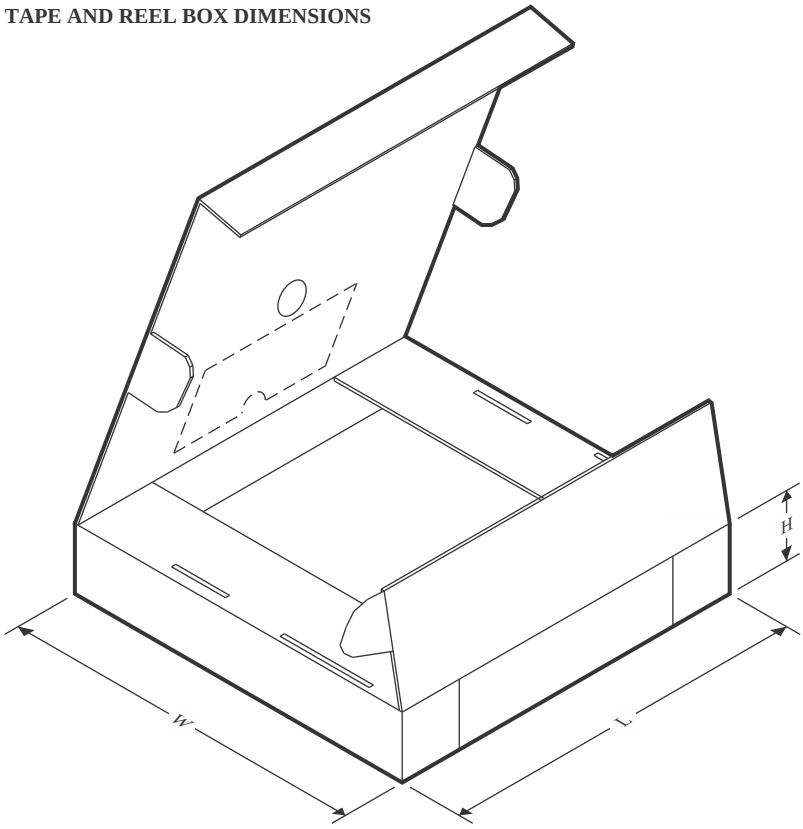
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74ALS174DR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74ALS174NSR | SOP | NS | 16 | 2000 | 330.0 | 16.4 | 8.1 | 10.4 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74ALS175DR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74ALS175NSR | SOP | NS | 16 | 2000 | 330.0 | 16.4 | 8.1 | 10.4 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74AS174NSR | SOP | NS | 16 | 2000 | 330.0 | 16.4 | 8.1 | 10.4 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74AS175BNSR | SOP | NS | 16 | 2000 | 330.0 | 16.4 | 8.1 | 10.4 | 2.5 | 12.0 | 16.0 | Q1 |

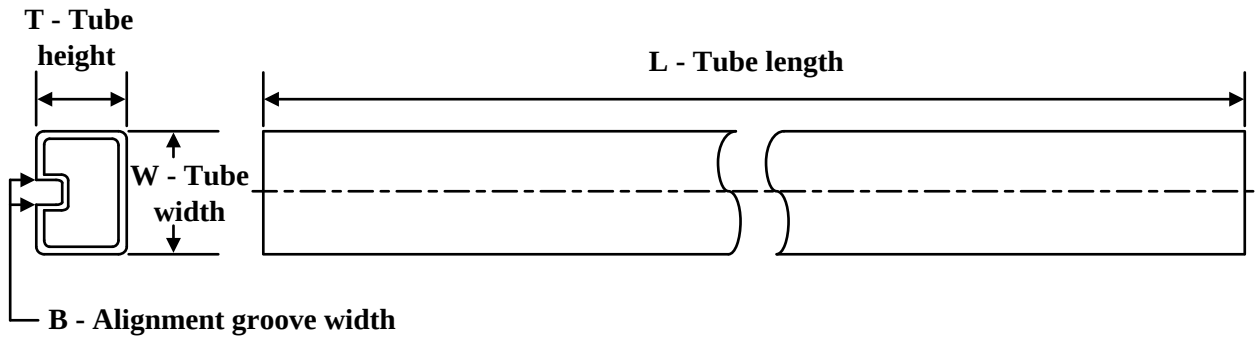
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74ALS174DR | SOIC | D | 16 | 2500 | 353.0 | 353.0 | 32.0 |
| SN74ALS174NSR | SOP | NS | 16 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74ALS175DR | SOIC | D | 16 | 2500 | 353.0 | 353.0 | 32.0 |
| SN74ALS175NSR | SOP | NS | 16 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74AS174NSR | SOP | NS | 16 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74AS175BNSR | SOP | NS | 16 | 2000 | 353.0 | 353.0 | 32.0 |

## TUBE

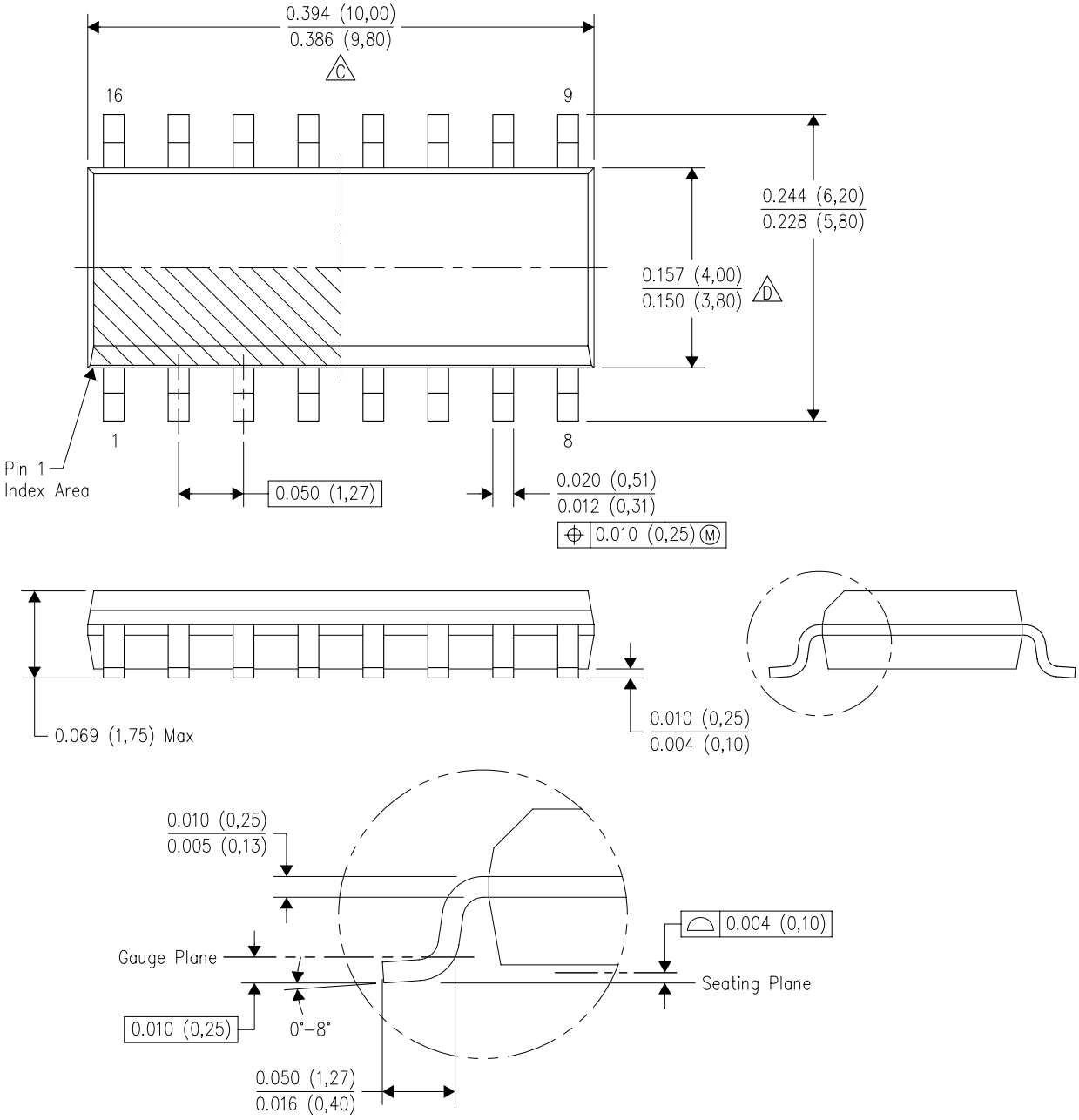



*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| 83019012A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| 8301901FA | W | CFP | 16 | 25 | 506.98 | 26.16 | 6220 | NA |
| JM38510/37201B2A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| JM38510/37201B2A.A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| JM38510/37202B2A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| JM38510/37202B2A.A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| M38510/37201B2A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| M38510/37202B2A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SN74ALS174N | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74ALS174N | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74ALS174N.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74ALS174N.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74ALS175N | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74ALS175N | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74ALS175N.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74ALS175N.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74AS174D | D | SOIC | 16 | 40 | 507 | 8 | 3940 | 4.32 |
| SN74AS174D.A | D | SOIC | 16 | 40 | 507 | 8 | 3940 | 4.32 |
| SN74AS174N | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74AS174N | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74AS174N.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74AS174N.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74AS175BD | D | SOIC | 16 | 40 | 507 | 8 | 3940 | 4.32 |
| SN74AS175BD.A | D | SOIC | 16 | 40 | 507 | 8 | 3940 | 4.32 |
| SN74AS175BN | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74AS175BN | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74AS175BN.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74AS175BN.A | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SNJ54ALS174FK | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |

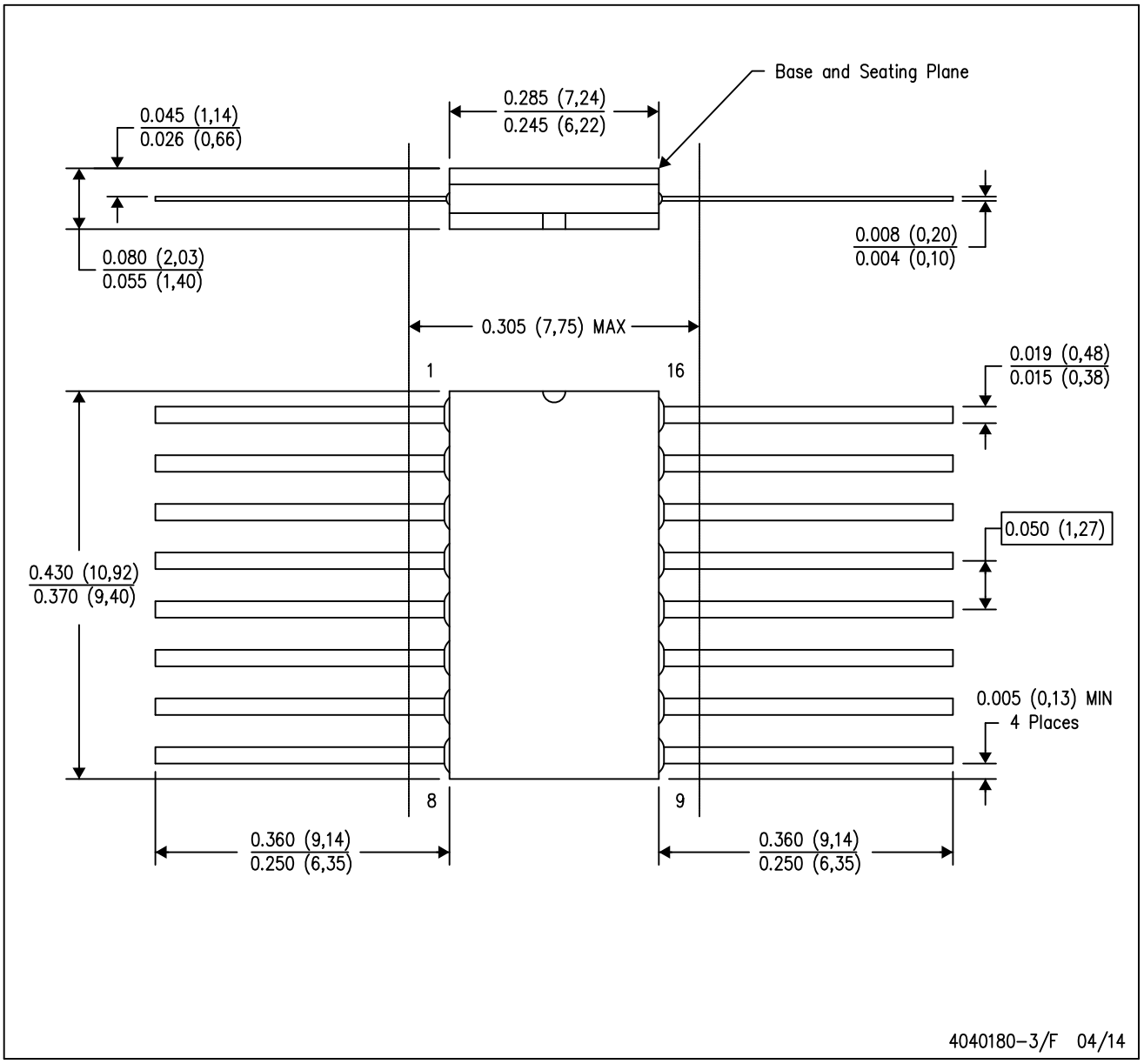
| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| SNJ54ALS174FK.A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SNJ54ALS174W | W | CFP | 16 | 25 | 506.98 | 26.16 | 6220 | NA |
| SNJ54ALS174W.A | W | CFP | 16 | 25 | 506.98 | 26.16 | 6220 | NA |

D (R–PDSO–G16) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

W (R–GDFP–F16) CERAMIC DUAL FLATPACK




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP2–F16

# GENERIC PACKAGE VIEW

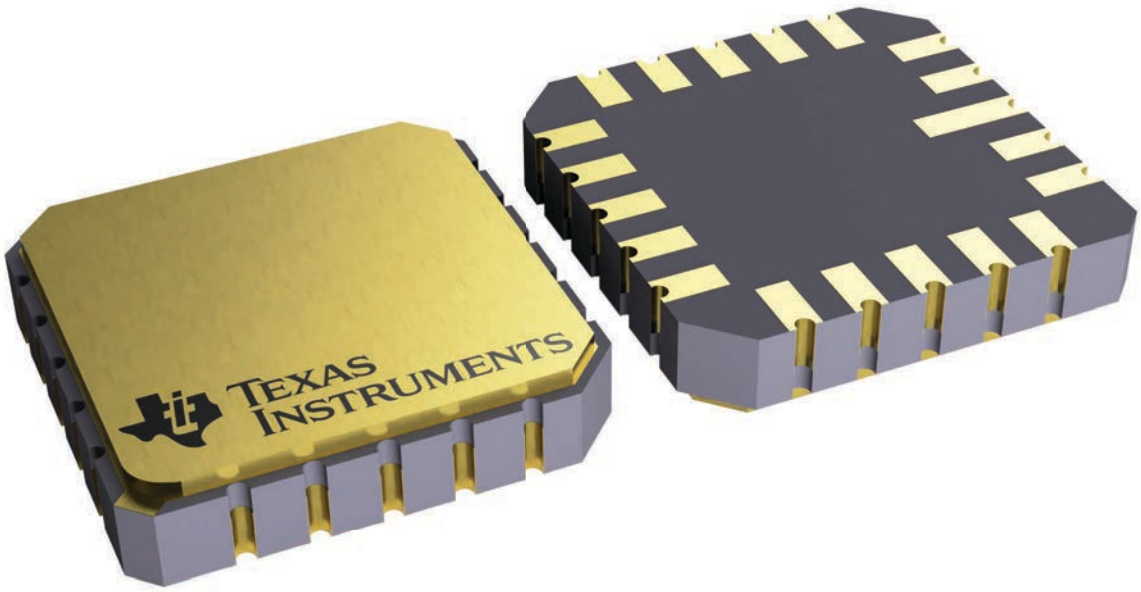
## FK 20

## LCCC - 2.03 mm max height

**8.89 x 8.89, 1.27 mm pitch**

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

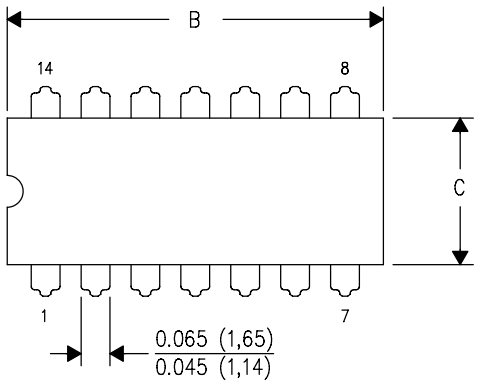



4229370VA\

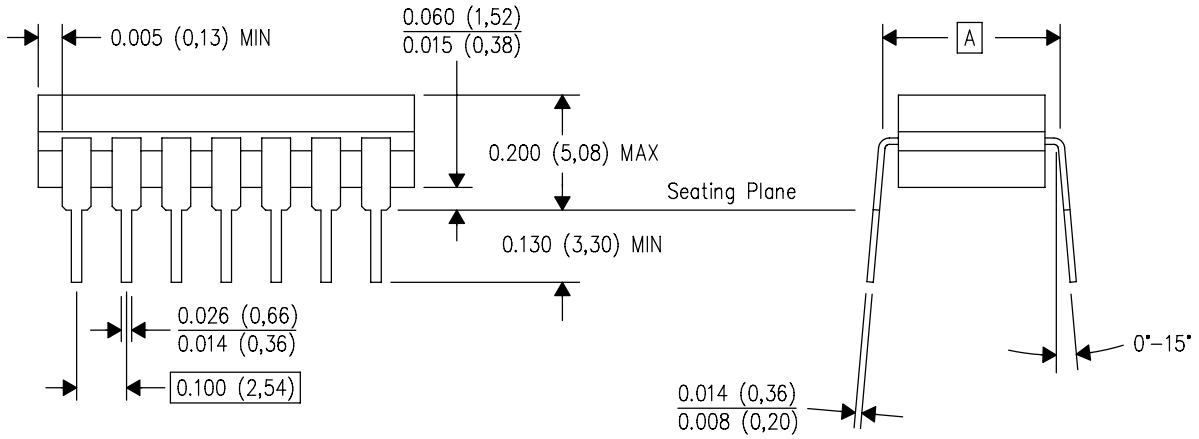
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



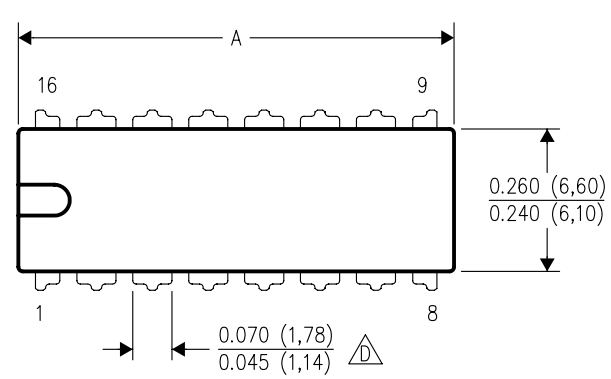

4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

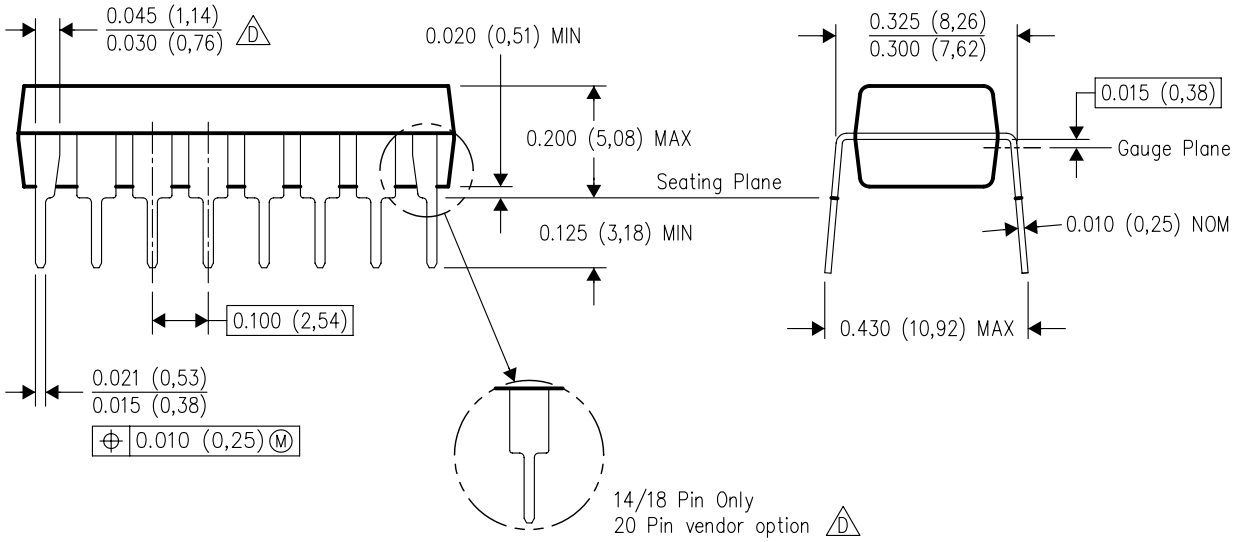
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

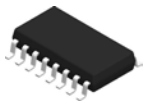



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

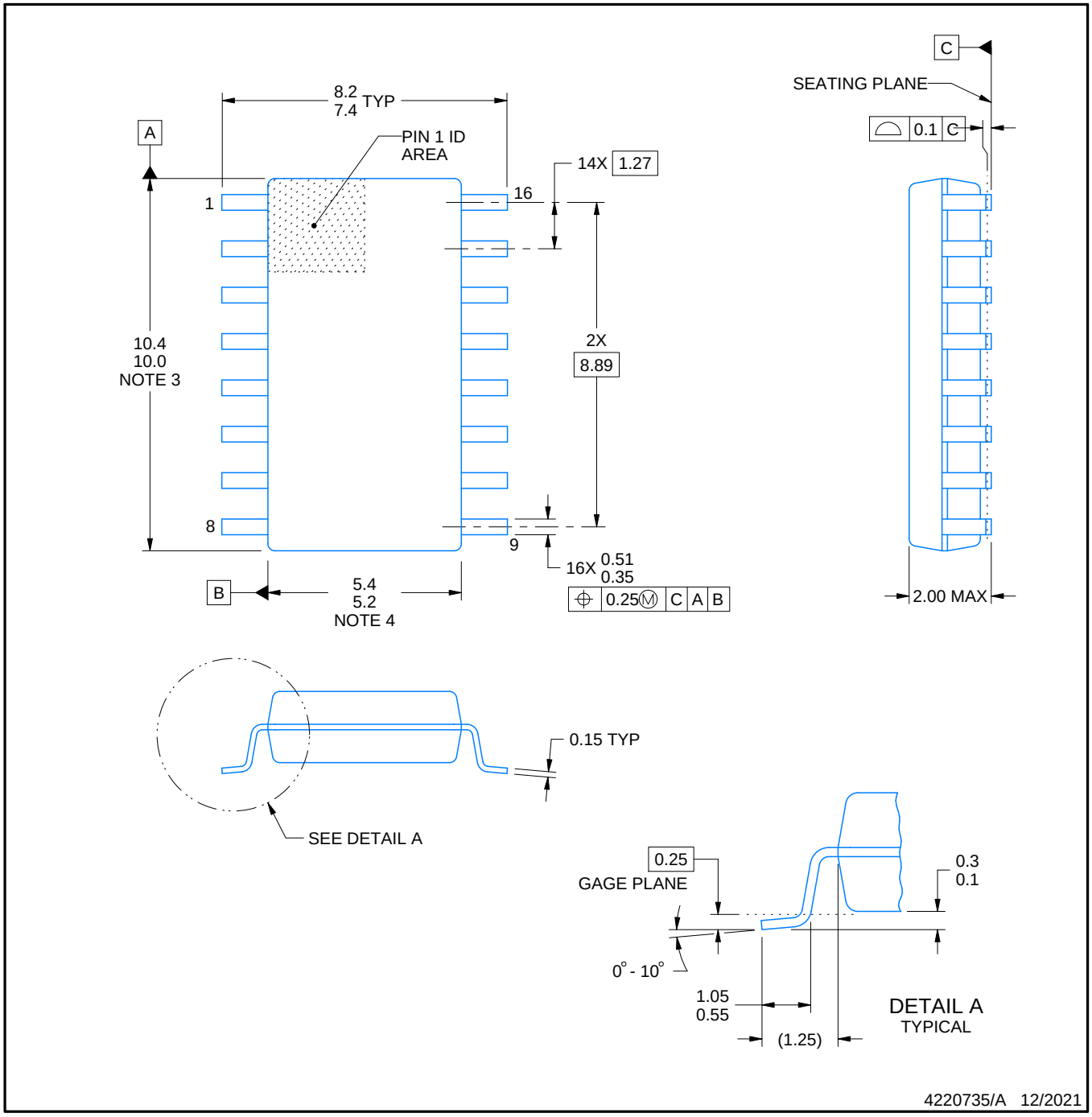


# PACKAGE OUTLINE

## NS0016A

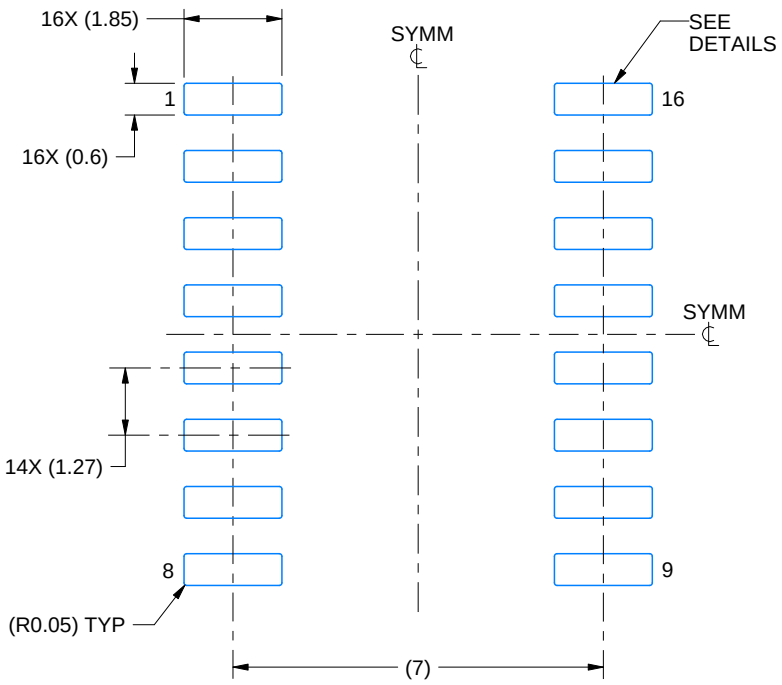
## SOP - 2.00 mm max height

SOP

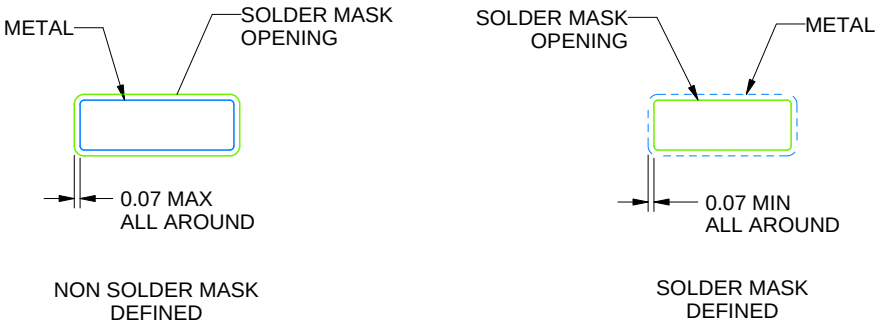



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.




LAND PATTERN EXAMPLE
SCALE:7X




NON SOLDER MASK
DEFINED

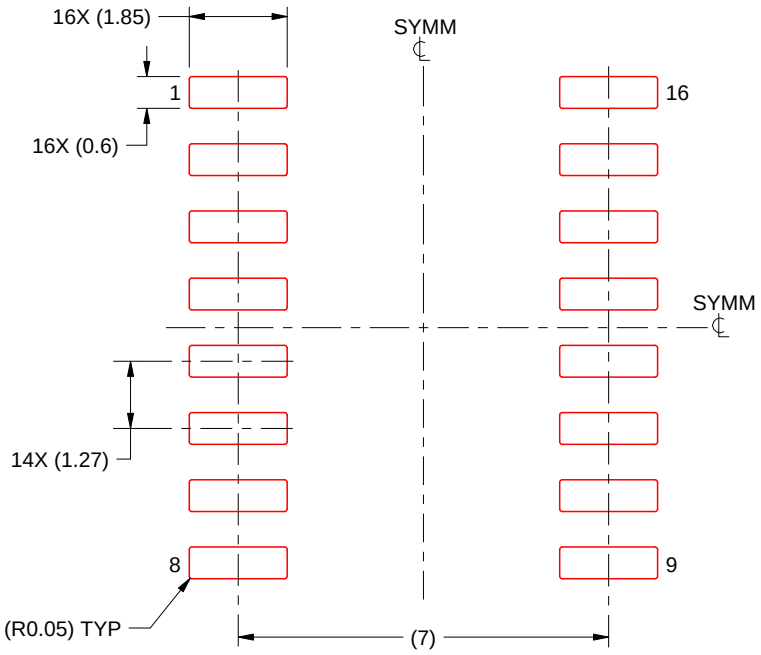
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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