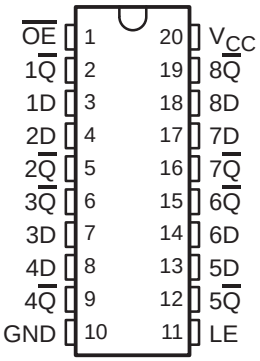
- **Eight Latches in a Single Package**
- **3-State Bus-Driving Inverting Outputs**
- **Full Parallel Access for Loading**
- **Buffered Control Inputs**
- **pnp Inputs Reduce dc Loading on Data Lines**
- **Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic (N) 300-mil DIPs**

DW OR N PACKAGE
(TOP VIEW)



description

These 8-bit D-type transparent latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

While latch-enable (LE) input is high, the $\overline{Q}$ outputs follow the complements of the data (D) inputs. When LE is taken low, the $\overline{Q}$ outputs are latched at the inverses of the levels set up at the D inputs. The SN74ALS533A and SN74AS533A are functionally equivalent to the SN74ALS373A and SN74AS373, except for having inverted outputs.

A buffered output-enable ($\overline{OE}$) input places the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

The SN74ALS533A and SN74AS533A are characterized for operation from 0°C to 70°C.

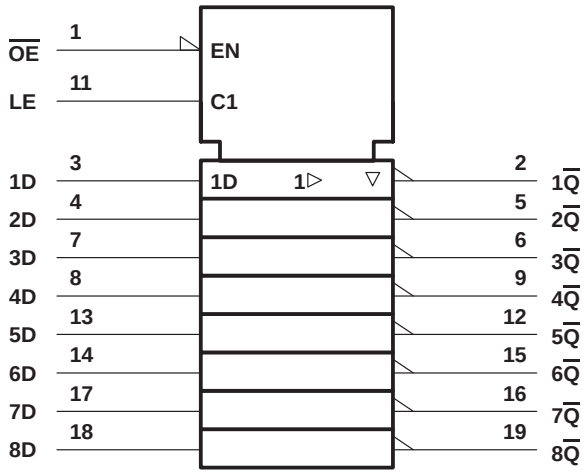
FUNCTION TABLE
(each latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

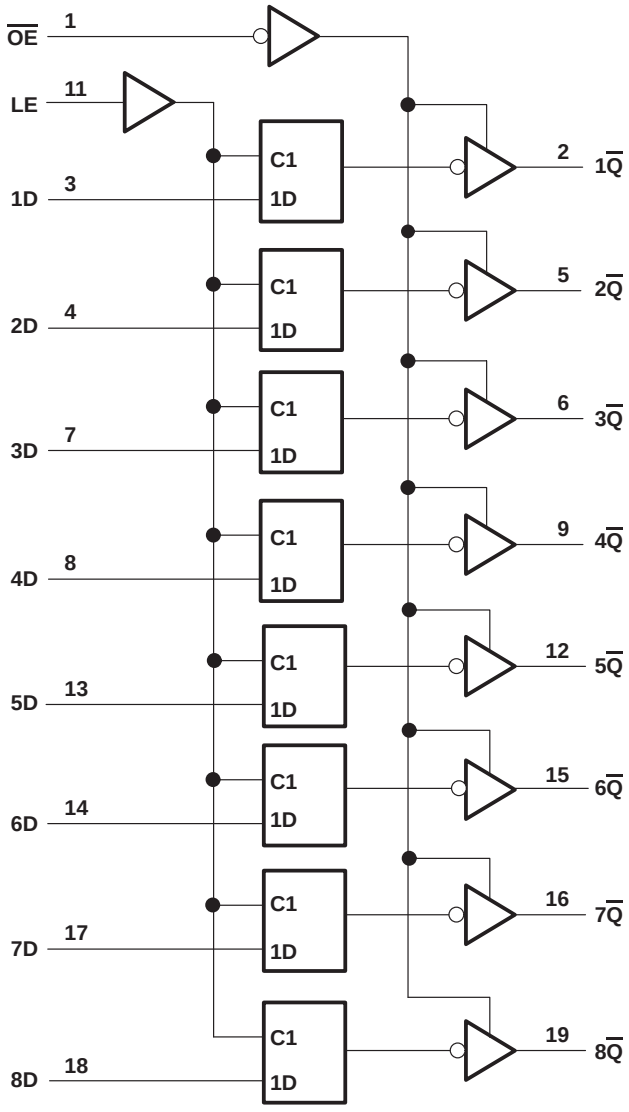
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, V_I . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range, T_A: SN74ALS533A . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN74ALS533A			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			–2.6	mA
I_{OL}	Low-level output current			24	mA
t_w	Pulse duration, LE high	15			ns
t_{su}	Setup time, data before LE↓	15			ns
t_h	Hold time, data after LE↓	7			ns
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN74ALS533A			UNIT
			MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA			–1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = –0.4 mA	V_{CC} –2			V
	V_{CC} = 4.5 V,	I_{OH} = –2.6 mA	2.4	3.2		
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 12 mA		0.25	0.4	V
		I_{OL} = 24 mA		0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20	µA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			–20	µA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			–0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	–30		–112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		10	17	mA
		Outputs low		17	26	
		Outputs disabled		18.5	28	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†		UNIT
			SN74ALS533A		
			MIN	MAX	
t_{PLH}	D	$\overline{Q}$	4	19	ns
t_{PHL}			4	13	
t_{PLH}	LE	Any $\overline{Q}$	5	23	ns
t_{PHL}			4	18	
t_{PZH}	$\overline{OE}$	Any $\overline{Q}$	1	17	ns
t_{PZL}			4	18	
t_{PHZ}	$\overline{OE}$	Any $\overline{Q}$	2	10	ns
t_{PLZ}			2	16	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, V_I . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range, T_A: SN74AS533A . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN74AS533A			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			–15	mA
I_{OL}	Low-level output current			48	mA
t_w	Pulse duration, LE high	2			ns
t_{su}	Setup time, data before LE↓	2			ns
t_h	Hold time, data after LE↓	3			ns
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN74AS533A			UNIT
			MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA			–1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = –2 mA	V_{CC} –2			V
	V_{CC} = 4.5 V,	I_{OH} = –15 mA	2.4	3.3		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.34	0.5	V
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50	µA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			–50	µA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V		–0.02	–0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	–30		–112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		62	100	mA
		Outputs low		64	100	
		Outputs disabled		71	110	

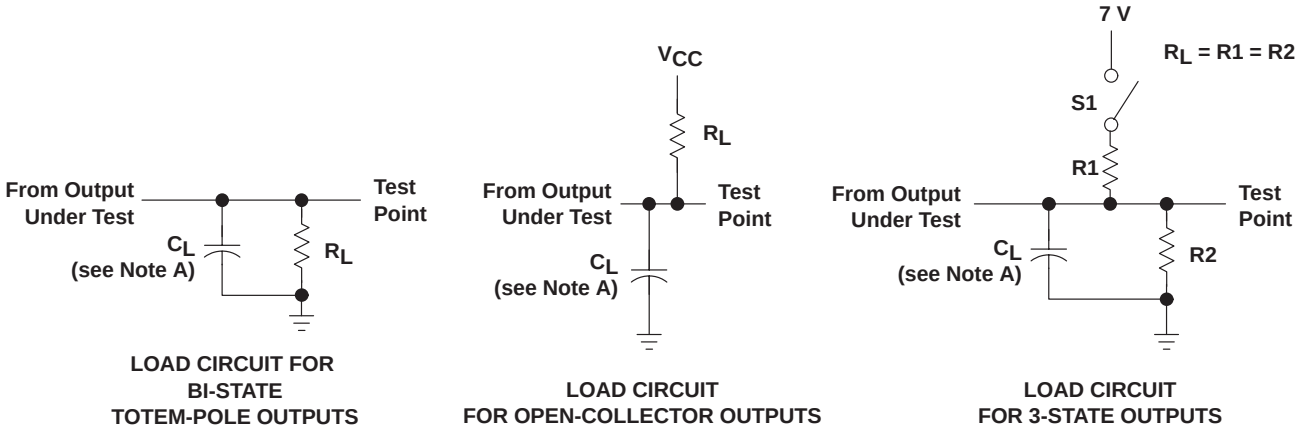
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX§		UNIT
			SN74AS533A		
			MIN	MAX	
t_{PLH}	D	$\overline{Q}$	4	7.5	ns
t_{PHL}			4	7	
t_{PLH}	LE	Any $\overline{Q}$	5	9	ns
t_{PHL}			4	8	
t_{PZH}	$\overline{OE}$	Any $\overline{Q}$	2	6.5	ns
t_{PZL}			4	9.5	
t_{PHZ}	$\overline{OE}$	Any $\overline{Q}$	2	6.5	ns
t_{PLZ}			3	7	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

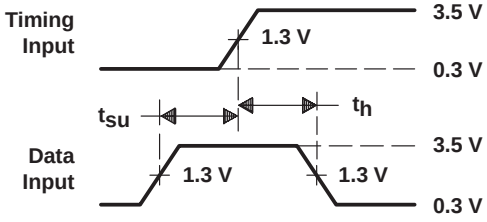
PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



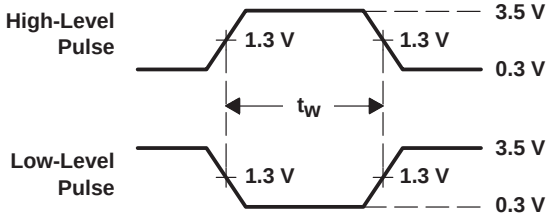
LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS

LOAD CIRCUIT FOR OPEN-COLLECTOR OUTPUTS

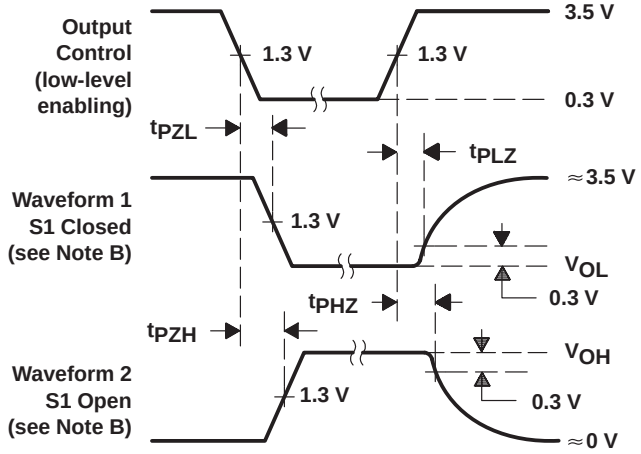
LOAD CIRCUIT FOR 3-STATE OUTPUTS



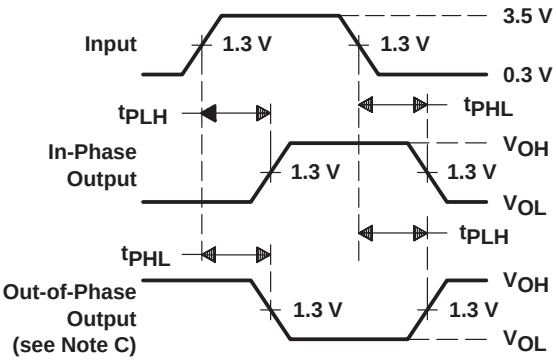
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
D. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

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