OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

SDAS065B − DECEMBER 1982 − REVISED JANUARY 1995

- **3-State Buffer-Type Inverting Outputs Drive Bus Lines Directly**
- **Bus-Structured Pinout**
- **Buffered Control Inputs**
- **SN74ALS577A Has Synchronous Clear**
- **Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), Standard Plastic (N, NT) and Ceramic (J) 300-mil DIPs, and Ceramic Flat (W) Packages**

description

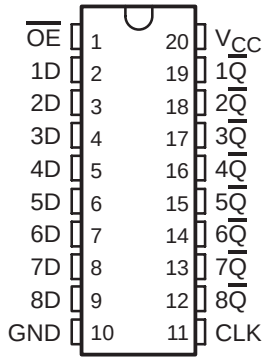
These octal D-type edge-triggered flip-flops feature 3-state outputs designed specifically for bus driving. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

These flip-flops enter data on the low-to-high transition of the clock (CLK) input.

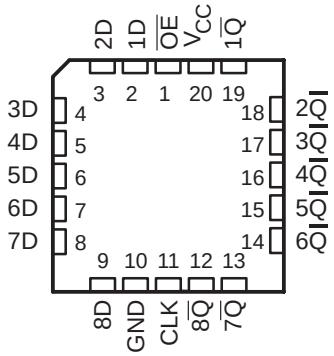
The output-enable ($\overline{OE}$) input does not affect internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are disabled.

The SN54ALS576B and SN54AS576 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS576B, SN74ALS577A, and SN74AS576 are characterized for operation from 0°C to 70°C.

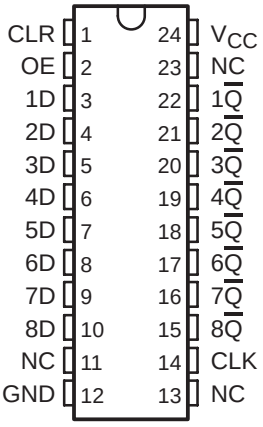
SN54ALS576B, SN54AS576 . . . J OR W PACKAGE
SN74ALS576B, SN74AS576 . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS576B, SN54AS576 . . . FK PACKAGE
(TOP VIEW)



SN74ALS577A . . . DW OR NT PACKAGE
(TOP VIEW)



NC − No internal connection

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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Function Tables

′ALS576B, ′AS576 (each flip-flop)

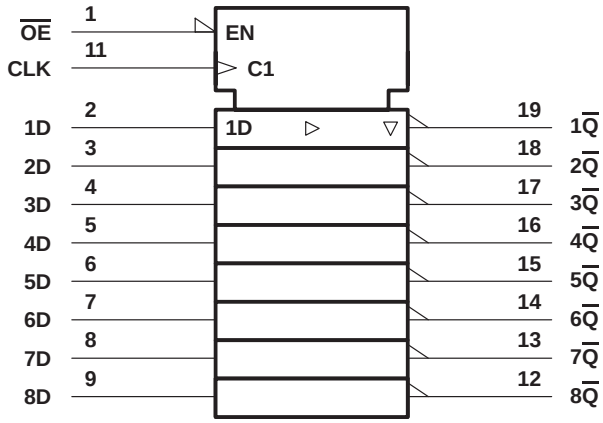
INPUTS			OUTPUT
$\overline{OE}$	CLK	D	$\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

SN74ALS577A (each flip-flop)

INPUTS				OUTPUT
$\overline{OE}$	$\overline{CLR}$	CLK	D	$\overline{Q}$
L	L	↑	X	H
L	H	↑	H	L
L	H	↑	L	H
L	H	L	X	$\overline{Q}_0$
H	X	X	X	Z

logic symbols†

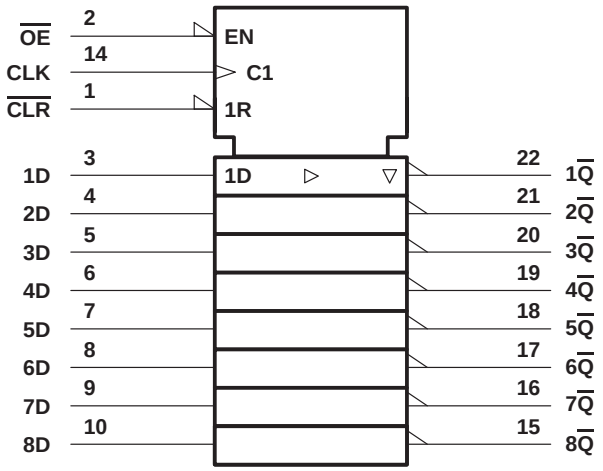
′ALS576B, ′AS576



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown for the ′ALS576B and ′AS576 are for the DW, J, N, and W packages.

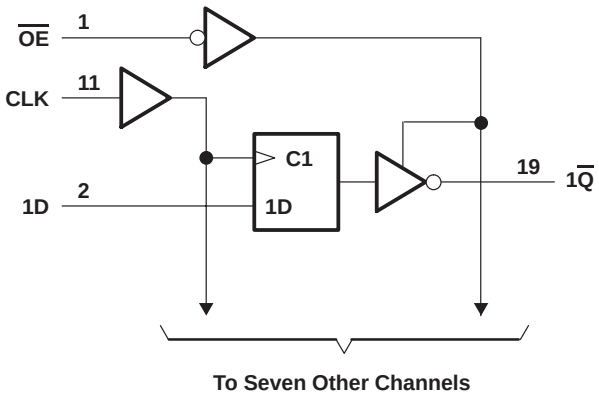
SN74ALS577A



Pin numbers shown for the SN74ALS577A are for the DW and NT packages.

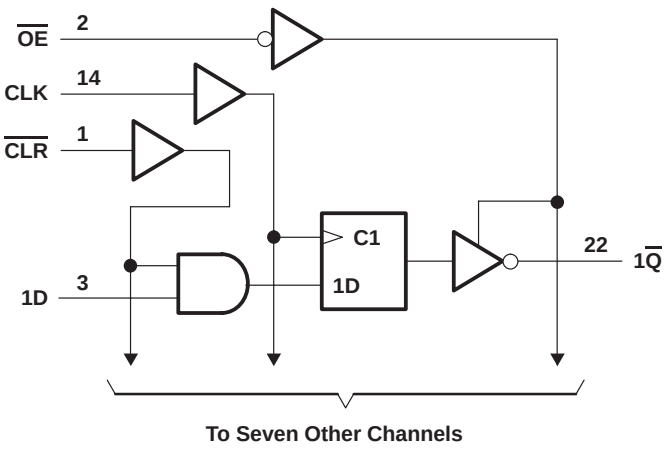
logic diagrams (positive logic)

′ALS576B, ′AS576



Pin numbers shown are for the DW, J, N, and W packages.

SN74ALS577A



Pin numbers shown are for the DW and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, V_I . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range, T_A: SN54ALS576B . . . . . −55°C to 125°C
SN74ALS576B, SN74ALS577A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54ALS576B			SN74ALS576B SN74ALS577A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current				−1			−2.6	mA
I_{OL}	Low-level output current				12			24	mA
f_{clock}	Clock frequency	′ALS576B	0		22	0		30	MHz
		SN74ALS577A				0		30	
t_w	Pulse duration	′ALS576B, CLK high or low	25			16.5			ns
		SN74ALS577A, CLK high or low				16.5			
t_{su}	Setup time before CLK↑	Data	15			15			ns
		SN74ALS577A $\overline{CLR}$				15			
t_h	Hold time after CLK↑	Data	4			0			ns
		SN74ALS577A $\overline{CLR}$				0			
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS576B			SN74ALS576B SN74ALS577A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} −2			V_{CC} −2			V
	V_{CC} = 4.5 V	I_{OH} = −1 mA	2.4	3.3					
		I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	µA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	µA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−20		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		10	18		10	18	mA
		Outputs low		15	24		15	24	
		Outputs disabled		16	30		16	30	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX§						UNIT
			SN54ALS576B		SN74ALS576B		SN74ALS577A		
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			22		30		30		MHz
t_{PLH}	CLK	Any $\overline{Q}$	4	24	3	14	4	14	ns
t_{PHL}			4	20	4	14	4	14	
t_{PZH}	$\overline{OE}$	Any $\overline{Q}$	4	24	3	18	4	18	ns
t_{PZL}			3	23	4	18	4	18	
t_{PHZ}	$\overline{OE}$	Any $\overline{Q}$	2	14	1	10	2	10	ns
t_{PLZ}			3	29	2	15	3	15	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, V_I . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range, T_A: SN54AS576 . . . . . −55°C to 125°C
SN74AS576 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			SN54AS576			SN74AS576			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−12			−15	mA
I_{OL}	Low-level output current				32			48	mA
f_{clock}*	Clock frequency		0		100	0		125	MHz
t_w*	Pulse duration	CLK high	5			4			ns
		CLK low	4			2			
t_{su}*	Setup time, data before CLK↑		3			2			ns
t_h*	Hold time, data after CLK↑		3			2			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS576			SN74AS576			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC} −2			V_{CC} −2			V
		V_{CC} = 4.5 V	I_{OH} = −12 mA	2.4	3.2					
			I_{OH} = −15 mA				2.4	3.3		
V_{OL}		V_{CC} = 4.5 V	I_{OL} = 32 mA		0.29	0.5				V
			I_{OL} = 48 mA					0.33	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	µA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	µA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
I_{IL}	D	V_{CC} = 5.5 V,	V_I = 0.4 V			−3			−2	mA
	All others					−0.5			−0.5	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	Outputs high		77	125		77	125	mA
			Outputs low		84	135		84	135	
			Outputs disabled		84	135		84	135	

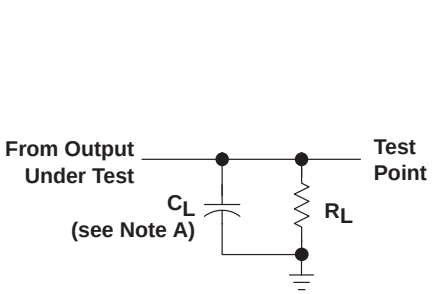
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 1)

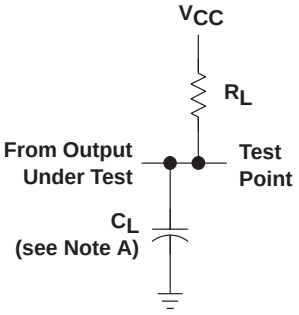
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX§				UNIT
			SN54AS576		SN74AS576		
			MIN	MAX	MIN	MAX	
f_{max}*			100		125		MHz
t_{PLH}	CLK	Any $\overline{Q}$	3	11	3	8	ns
t_{PHL}			4	11	4	9	
t_{PZH}	$\overline{OE}$	Any $\overline{Q}$	2	7	2	6	ns
t_{PZL}			3	11	3	10	
t_{PHZ}	$\overline{OE}$	Any $\overline{Q}$	2	7	2	6	ns
t_{PLZ}			2	7	2	6	

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.
§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

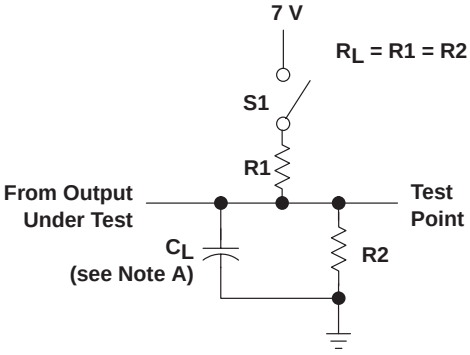
PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



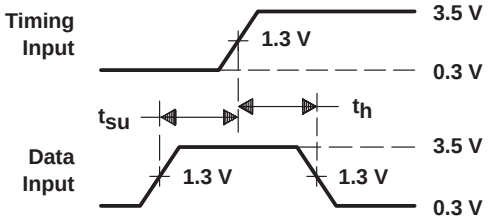
LOAD CIRCUIT FOR
BI-STATE
TOTEM-POLE OUTPUTS



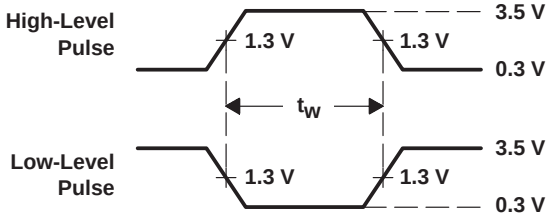
LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS



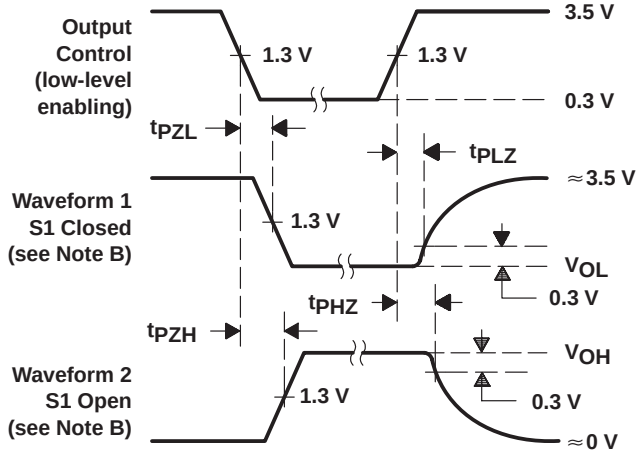
LOAD CIRCUIT
FOR 3-STATE OUTPUTS



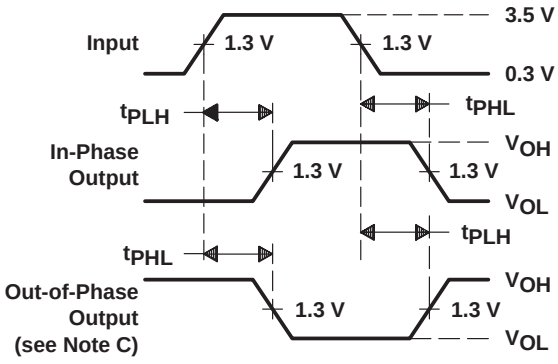
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
D. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
84001022A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	84001022A SNJ54ALS 576BFK
8400102RA	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8400102RA SNJ54ALS576BJ
SN74ALS576BDW	Obsolete	Production	SOIC (DW) | 20	-	-	Call TI	Call TI	0 to 70	ALS576B
SN74ALS576BDWR	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS576B
SN74ALS576BDWR.A	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS576B
SN74ALS576BN	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS576BN
SN74ALS576BN.A	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS576BN
SN74ALS576BNSR	Active	Production	SOP (NS) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS576B
SN74ALS576BNSR.A	Active	Production	SOP (NS) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS576B
SN74ALS577ADWR	Active	Production	SOIC (DW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS577A
SN74ALS577ADWR.A	Active	Production	SOIC (DW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS577A
SN74AS576N	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74AS576N
SN74AS576N.A	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74AS576N
SNJ54ALS576BFK	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	84001022A SNJ54ALS 576BFK
SNJ54ALS576BFK.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	84001022A SNJ54ALS 576BFK
SNJ54ALS576BJ	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8400102RA SNJ54ALS576BJ
SNJ54ALS576BJ.A	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8400102RA SNJ54ALS576BJ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN54ALS576B, SN74ALS576B :

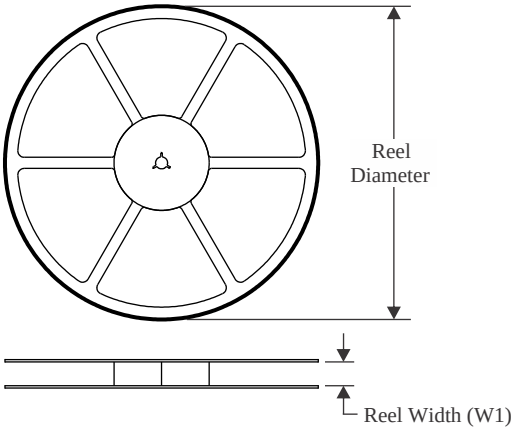
- Catalog : SN74ALS576B
- Military : SN54ALS576B

NOTE: Qualified Version Definitions:

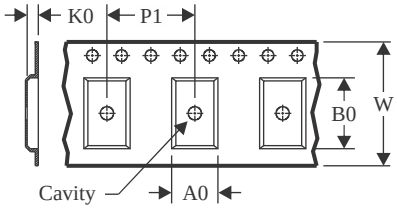
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

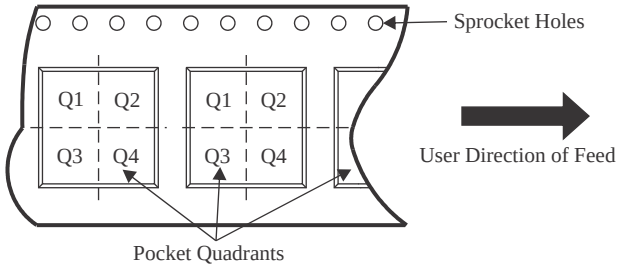


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

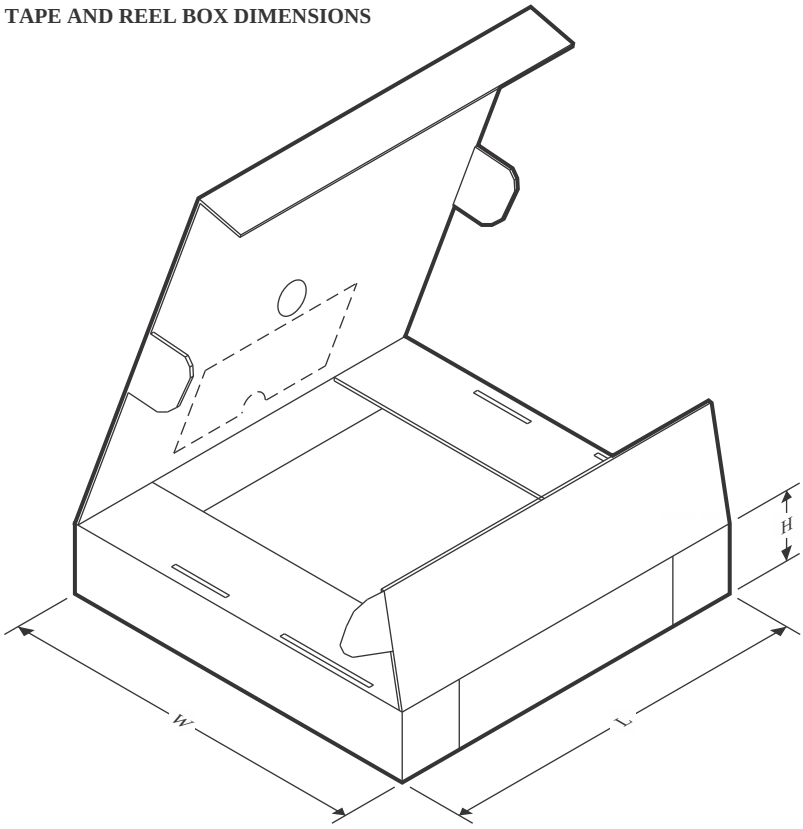
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS576BDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74ALS576BNSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74ALS577ADWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

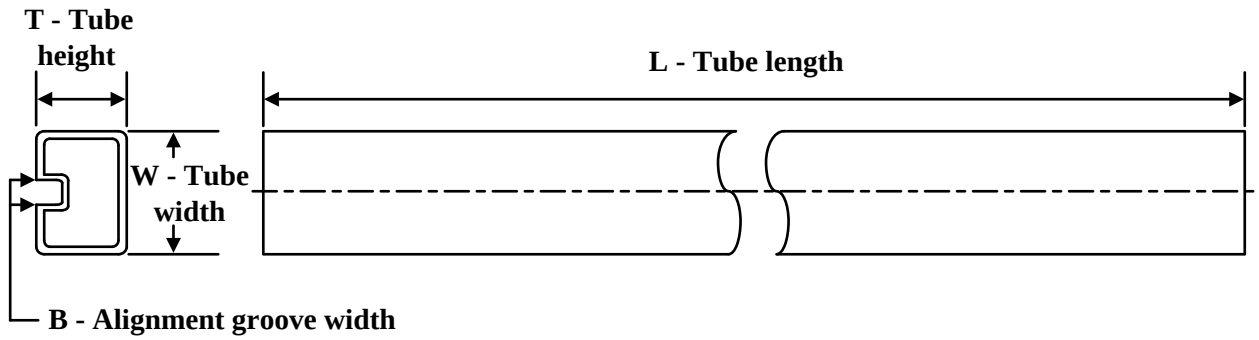
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS576BDWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74ALS576BNSR	SOP	NS	20	2000	356.0	356.0	45.0
SN74ALS577ADWR	SOIC	DW	24	2000	350.0	350.0	43.0

TUBE



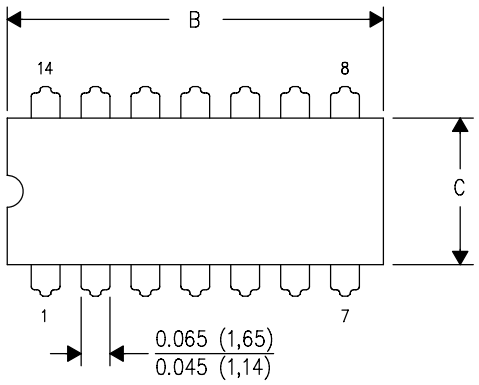
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
84001022A	FK	LCCC	20	55	506.98	12.06	2030	NA
SN74ALS576BN	N	PDIP	20	20	506	13.97	11230	4.32
SN74ALS576BN.A	N	PDIP	20	20	506	13.97	11230	4.32
SN74AS576N	N	PDIP	20	20	506	13.97	11230	4.32
SN74AS576N.A	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54ALS576BFK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54ALS576BFK.A	FK	LCCC	20	55	506.98	12.06	2030	NA

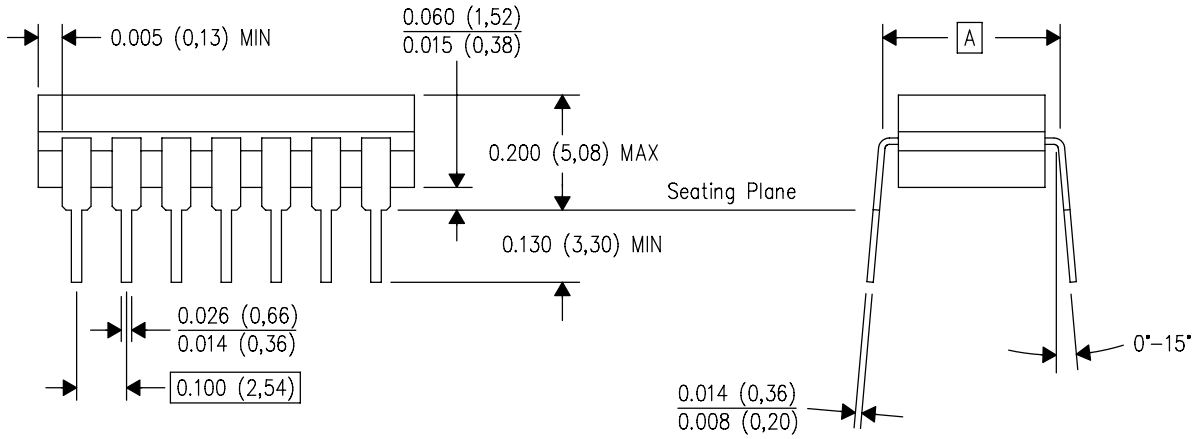
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



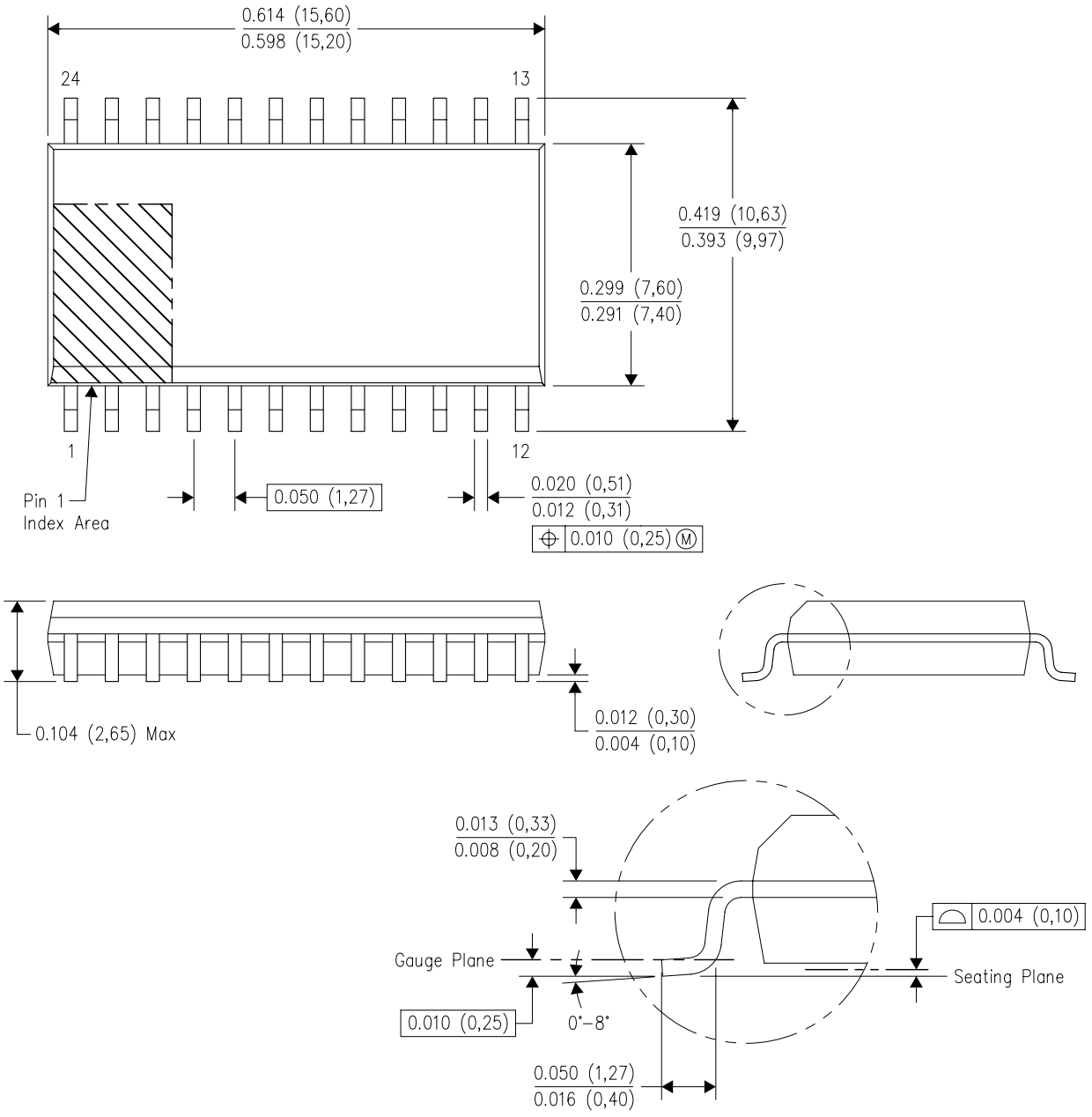
DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

GENERIC PACKAGE VIEW

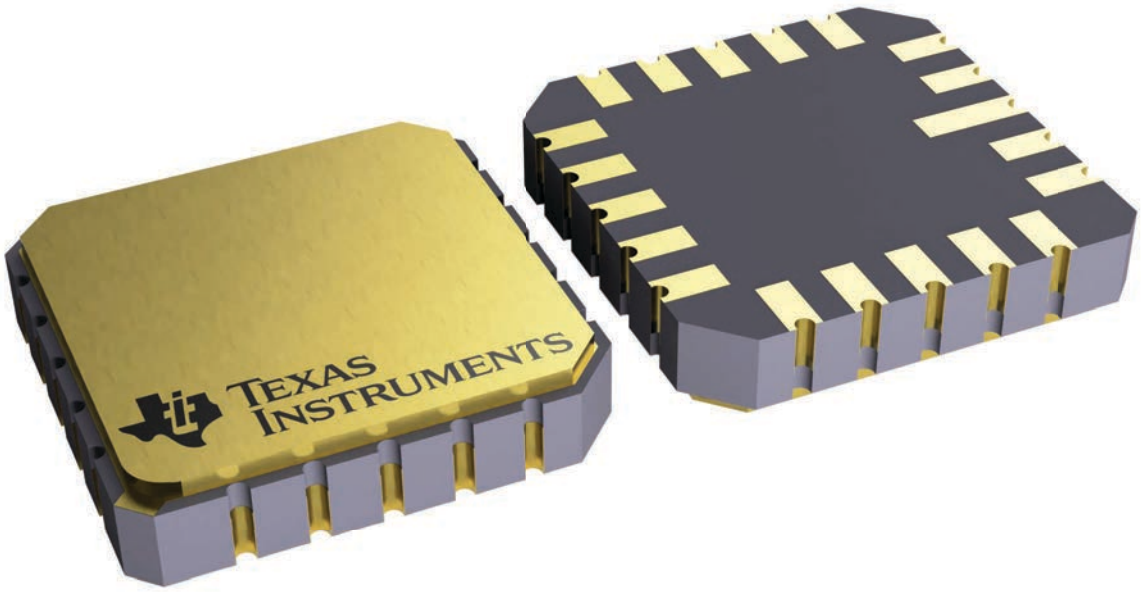
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

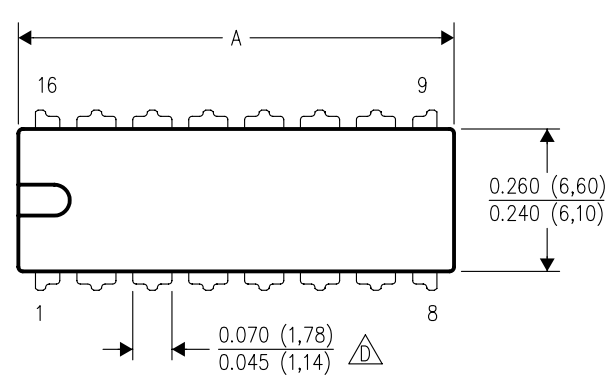


4229370VA\

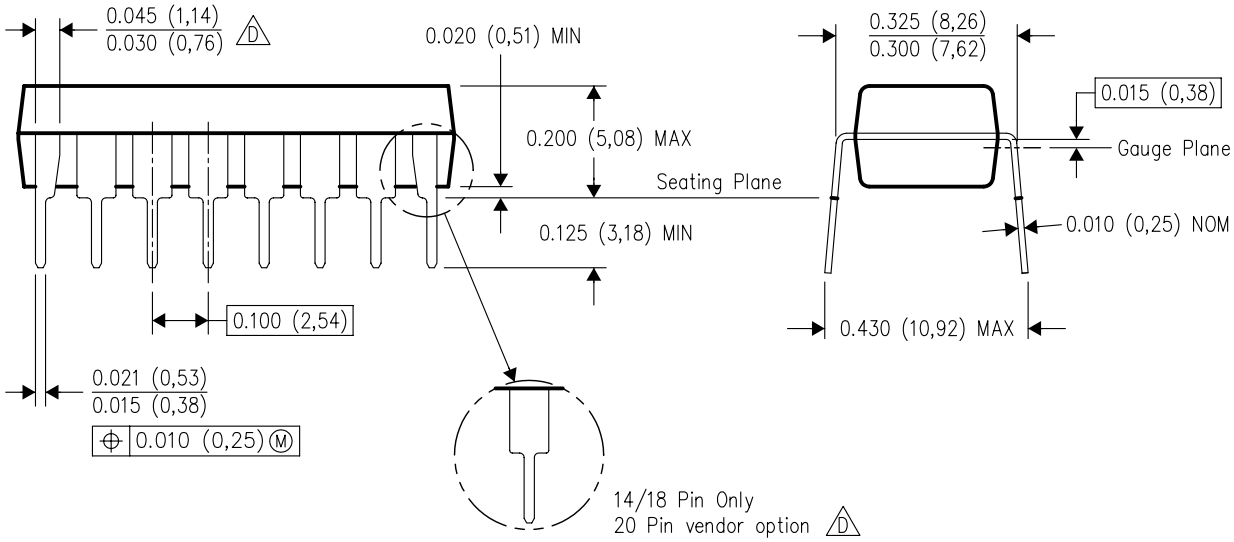
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

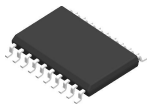


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

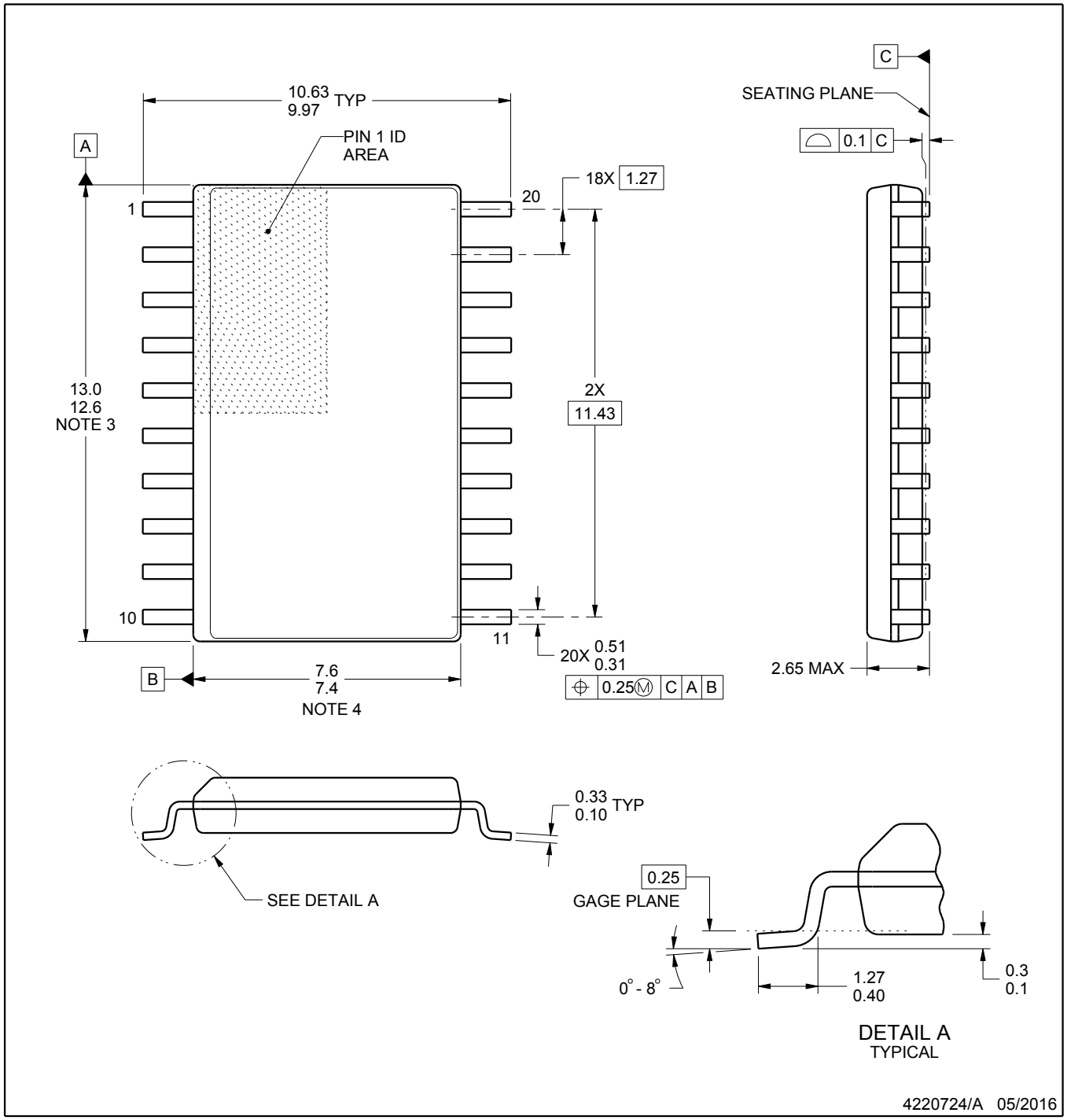


PACKAGE OUTLINE

DW0020A

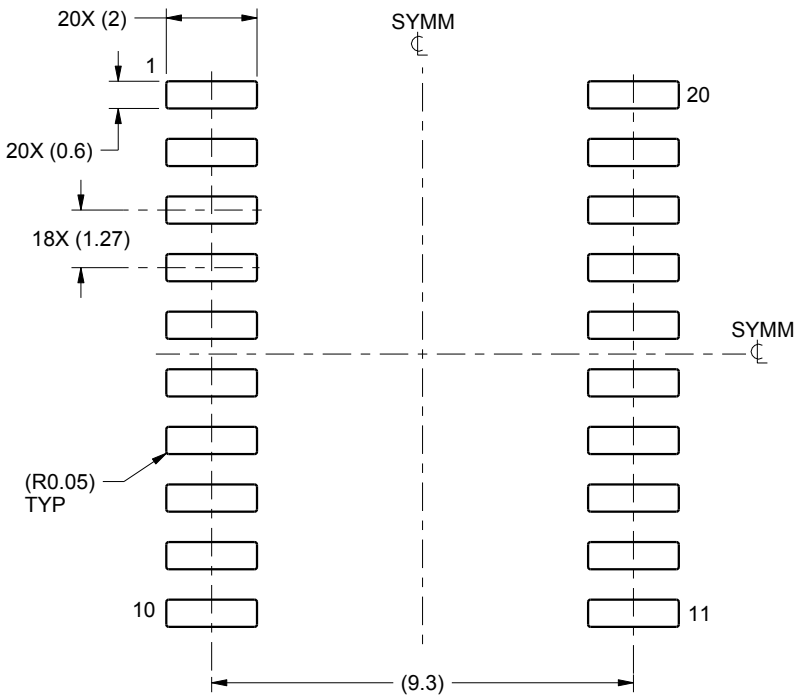
SOIC - 2.65 mm max height

SOIC

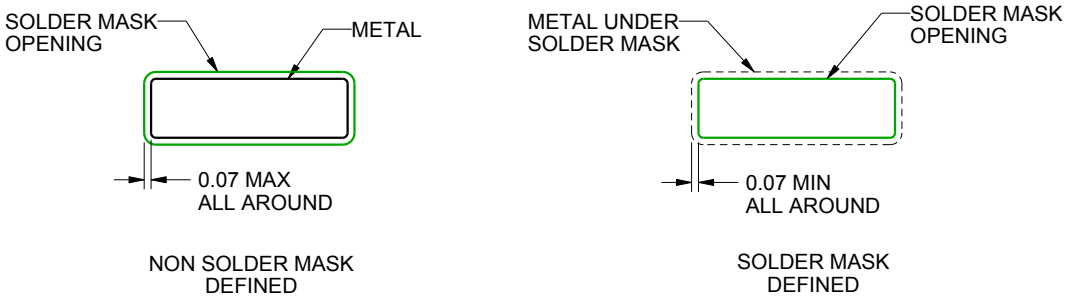


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

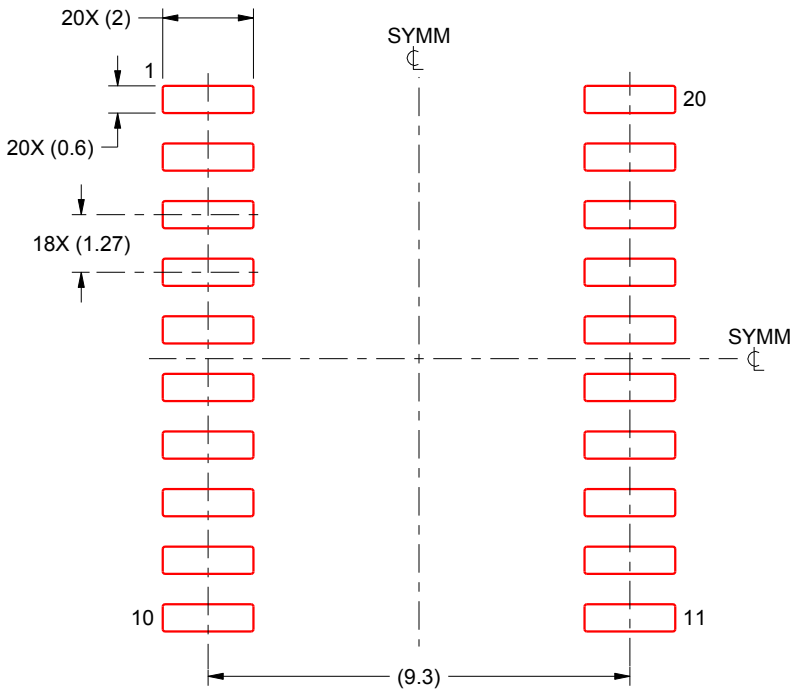


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

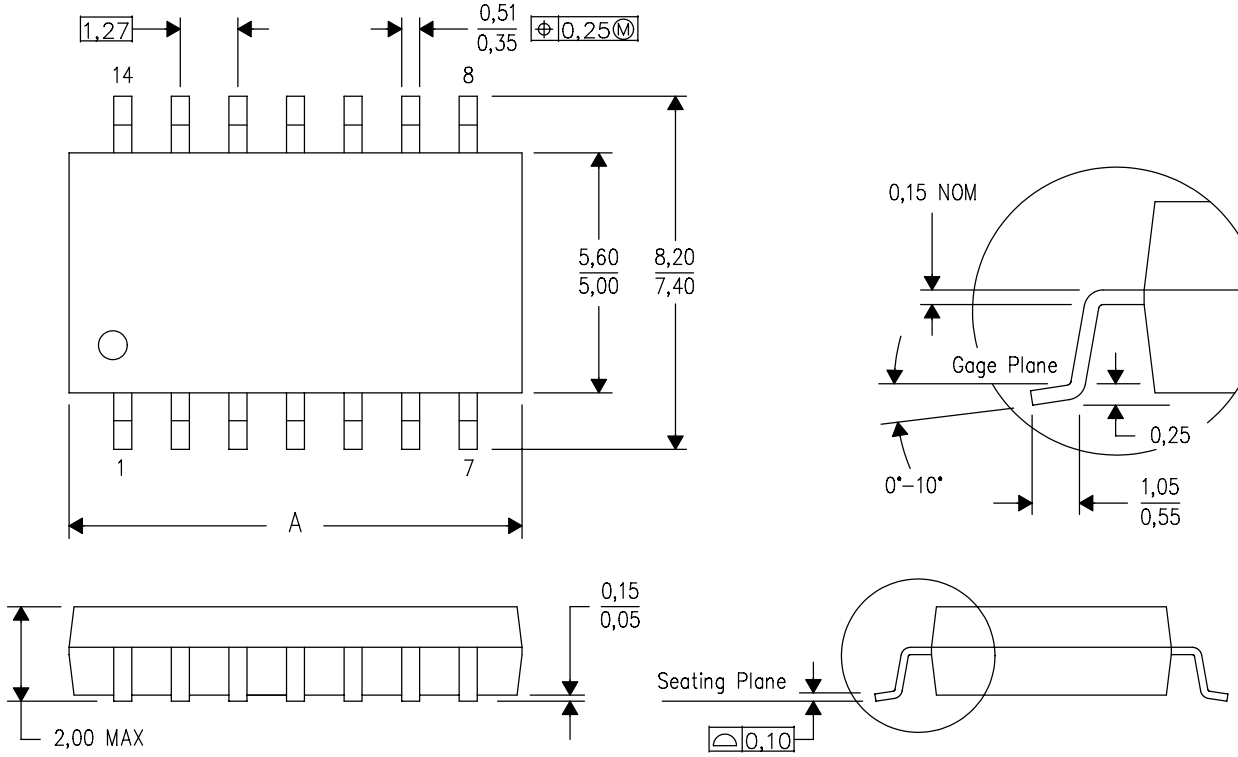
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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